Getting Started with the Xilinx Spartan-6 FPGA SP601 Evaluation Kit

UG523 (v1.5) March 17, 2011

XPM 0402769-02

DISCLAIMER

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials, or to advise you of any corrections or update. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of the Limited Warranties which can be viewed at http://www.xilinx.com/warranty.htm; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in Critical Applications: http://www.xilinx.com/warranty.htm#critapps.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/09	1.0	Internal Xilinx release for beta testing.
08/12/09	1.1	FCS version for limited kit distribution; document not published to web.
08/17/09	1.2	Initial Xilinx release to web.
08/12/10	1.3	Removed detailed installation procedure.
10/12/10	1.4	Updated Figure 1-1. Simplified download instructions under “Installing Software,” page 29.
03/17/11	1.5	Updated Legal “DISCLAIMER”. Removed references to USB flash drive in “What's Inside the Box,” page 5. Replaced references to USB flash drive with references to a ZIP file in “Installing Base System Reference Design Application GUI,” page 16. and in “Running the Base System Reference design” on page page 21.

Table of Contents

Getting Started with the Spartan-6 FPGA SP601 Evaluation Kit

Introduction

The Spartan®-6 FPGA SP601 Evaluation Kit enables hardware and software developers to create or evaluate designs targeting the XC6SLX16-CS324 Spartan-6 FPGA. The Spartan-6 FPGA Family offers an optimal balance of cost, power, performance, and development tool support for creating innovative products targeting consumer, automotive, surveillance, wireless, and other cost-sensitive markets.

The SP601 Evaluation Kit includes an on-board FMC (FPGA Mezzanine Card) daughter card connector as well as many common features used in system design, including capabilities using DDR2 memory, FLASH, Ethernet, general purpose I/O, and UART.

This Getting Started Guide will walk you through the steps to setup the SP601 hardware. It will show you how to run a Diagnostic Demo, designed to exercise a number of basic board features. You will be introduced to a Base System Reference Design, where you were able to see a more complex design exercising key features of the Spartan-6 FPGA. Finally, if you have not already installed the Xilinx ISE software, you will be directed through the steps to install the software, get updates and generate a license.

SP601 Development Kit Contents

What's Inside the Box

- Spartan-6 FPGA SP601 Evaluation Board
- Universal 5V power supply
- Two (2) USB A/MiniB cables (used for download and debug)
- Ethernet Category 5 cable
- ISE® Design Suite DVD:
  - Licensed for ISE WebPACK™ Design Software
- SP601 documentation:
  - Welcome Letter
  - Getting Started Guide

What's on the Web

- Product Home Page: www.xilinx.com/sp601
- Reference Designs User Guides, and Reference design Source Files
- Schematics, gerber and board BOM
- Additional detailed documentation

Key Features

Spartan-6 FPGA:

- XC6SLX16 in CS324 package

Configuration

- Onboard configuration circuitry
- Quad SPI Flash 8 MB
- 16 MB Parallel (BPI) Flash
- JTAG

Memory

- DDR2 component memory 128 MB
- IIC 1 kB IIC EEPROM

Communication

- 10/100/1000 Tri-Speed Ethernet PHY, Marvell Alaska PHY (88E1111)
- Serial (UART) to USB Bridge
- Expansion connectors
  - FMC-LPC connector (68 single-ended or 34 differential
- user-defined signals)
  - 8 User I/O (Digilent 2x6 header)

Clocking

- 200 MHz oscillator (differential)
- Socket (Single-Ended) populated with 27 MHz Osc
- SMA connectors (differential)

Display

- 4X LEDs

Control

- 4X push buttons, 4X DIP switches

Power Management

- Universal 5 volt power adaptor
- Jumper selectable VCCINT of 1.0V or 1.2V
- Current measurement on 3.3V, 2.5V, 1.8V, and 1.2V supplies

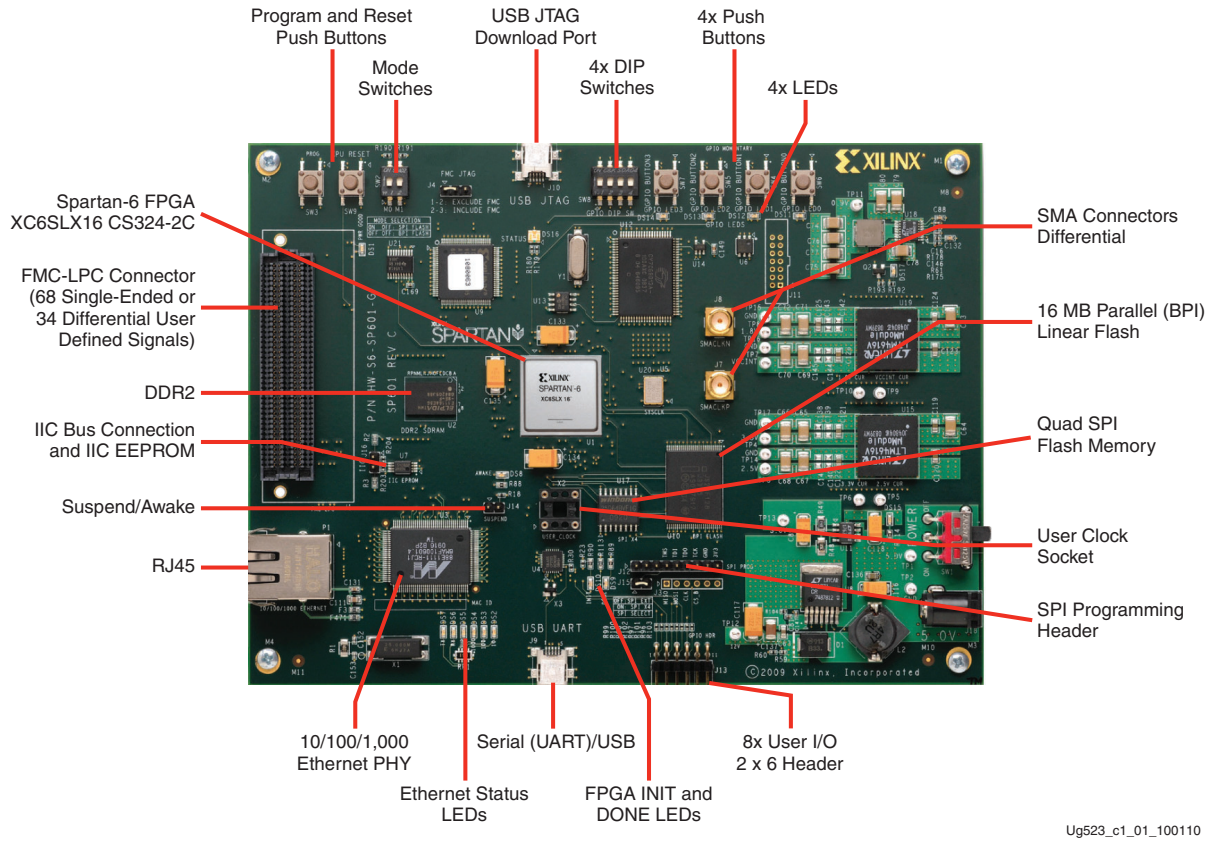


Figure 1-1: **Spartan-6 FPGA SP601 Evaluation Board**

Getting Started with the Diagnostic FLASH Demo

Before installing the software, you can run some of the demonstration designs that are burned in the SPI and BPI FLASH on the SP601 Evaluation Board. This will let you get an overview of the board features. This development kit comes with a number of pre-installed demonstrations and examples, as well as additional reference designs and application notes found on the Xilinx web site. The default Diagnostic Demo found in the BPI FLASH exercises some of the board features including Testing the UART, flashing the LEDs, reading the SWITCHES, Testing the FLASH and DDR2, IIC, and Ethernet.

The numbered boxes shown in Figure 1-2 correspond to the subsequent steps which outline how to connect the cables and power. Figure 1-3 shows the default switch and jumper settings.

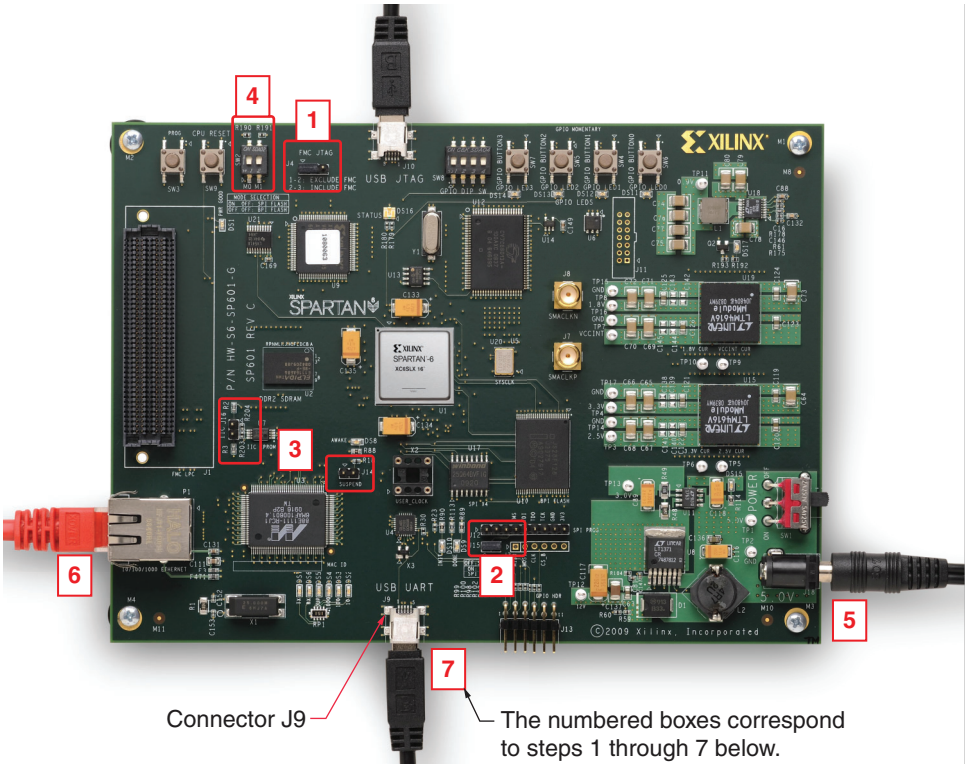


Figure 1-2: **Default Switch and Jumper Settings**

1. Set the JTAG Chain
   Ensure that Jumper J4 is installed on pin 1 and 2. This will cause the JTAG signals to be connected locally to the base board and not routed through the FMC connector.

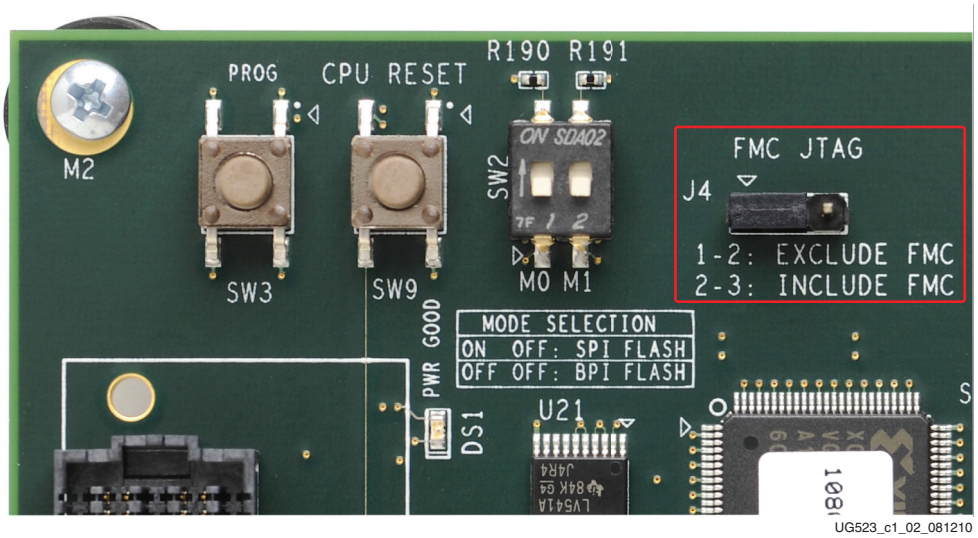


Figure 1-3: **Enlarged View of FMC JTAG Jumper (J4)**

2. Install J15 jumper to allow selection of Local SPI FLASH

   Ensure that a jumper is installed on J15. This will cause the SPI configuration to select the onboard Quad SPI device.

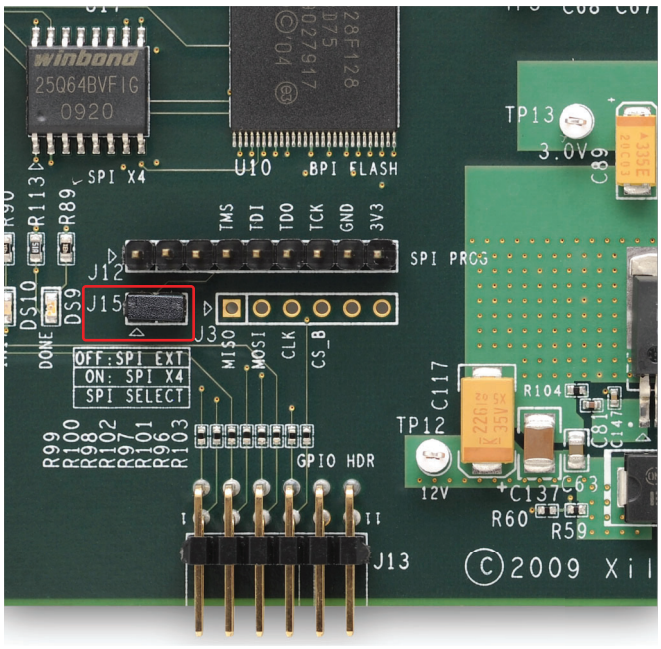


Figure 1-4: **SPI Configuration Target Select**

3. Confirm other jumper installation

   J14 and J16 should not have any jumpers installed.

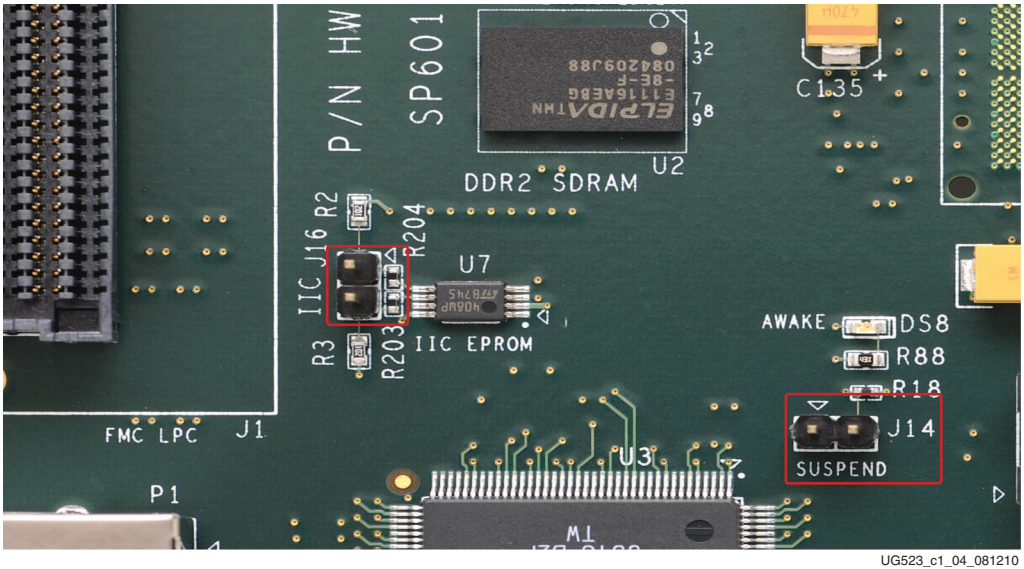


Figure 1-5: **Enlarged View of Jumpers J14 and J16**

4. Select BPI Configuration Mode

   Ensure that the DIP switch SW2 is set to the BPI Configuration Mode, where both M0 and M1 are in the OFF position.

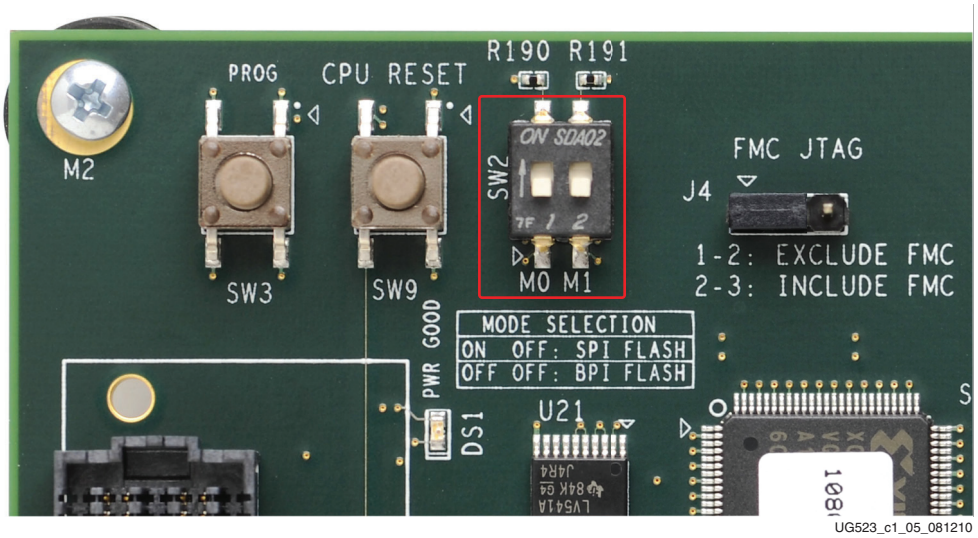


Figure 1-6: **Select Configuration Mode**

5. Connecting 5V Power

Remove the 5 volt power block from the SP 601 box. Plug in the power Adaptor to the local AC power. Plug the 5 volt male power jack into the board female connector on J18 as shown in Figure 1-7.

Turn on the power by switching the SW1 to the "On" position.

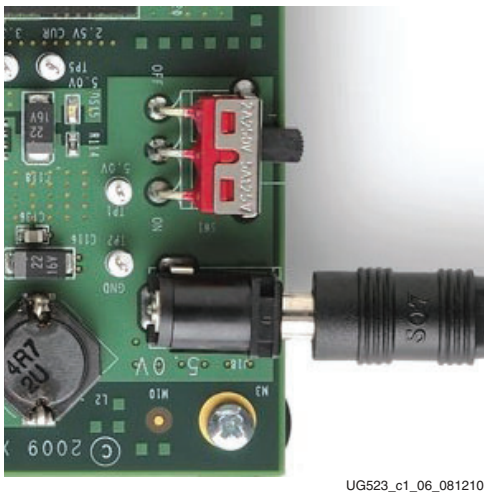


Figure 1-7: **Connecting the 5V Power**

6. Ethernet Cable

Do not connect the Ethernet cable at this time. For the Diagnostic Ethernet Loop-back test to run, you can not have the cable connected.

7. Connecting the UART
   a. Using the USB A/ MiniB Cable provided in the SP601 kit, connect the MiniB USB connected to the J9 USB connector.
   b. Connect the USB A end of the cable to your PC.
   c. The Driver for the Cx210x USB to UART Bridge should be automatically recognized.

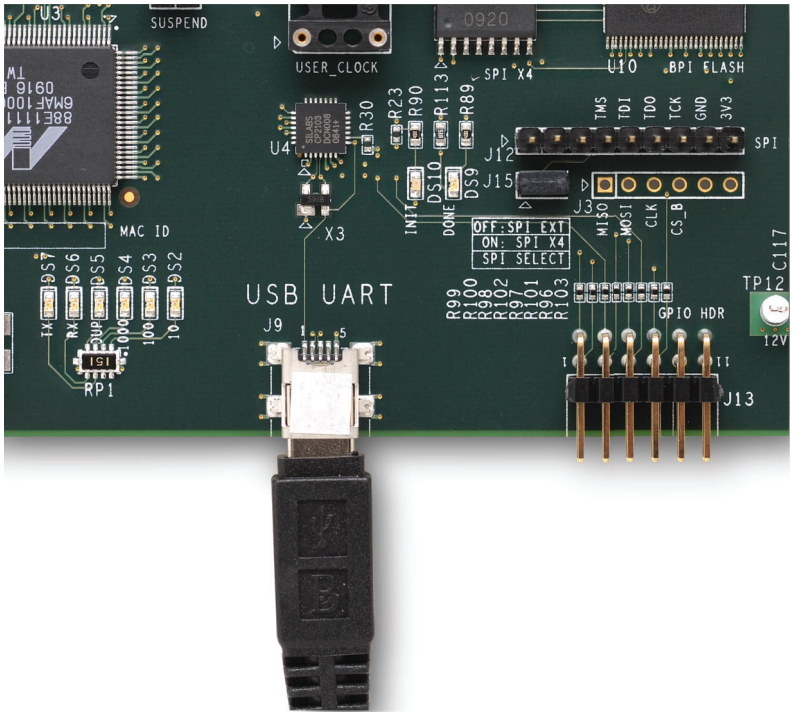
   Note: Note: To troubleshoot, see the SP601 Answer Record Support page found at http://www.xilinx.com/support/answers/33225.htm.

   d. On your PC, open a serial terminal program, then select **Start→Programs→Accessories→Communications→HyperTerminal**.
   e. In the Connection Description window, type **9600** in the Name box, then click **OK**.
   f. In the Connect To window, click **Cancel**.
   g. In the 9600-HyperTerminal window, select **File→Properties**.
   h. Select the Connect To tab.
   i. Select the COM device to which your UART/USB is connected as shown in Figure 1-8. The connection could be made to any of the COM devices listed. You will need to determine which COM port is assigned to that port. (see Figure 1-9).

   Note: To find the assigned COM port, use the Hardware Device Manager and look at the Ports (COM & LPT) to see the CX210x USB 2 UART Bridge Controller Device.

   j. Click **Configure**

The UART/USB connection options are shown in Figure 1-9.



UG523_c1_07_081210

Figure 1-8: **USB/UART Cable Connection**

Figure 1-9: **Open a Terminal Program**

8. In the HyperTerminal Port Settings tab, set the baud rate to **9600**, Data bits to **8**, Parity to **None**, Stop bits to **1**, and Flow control to **None**, then click **OK**.

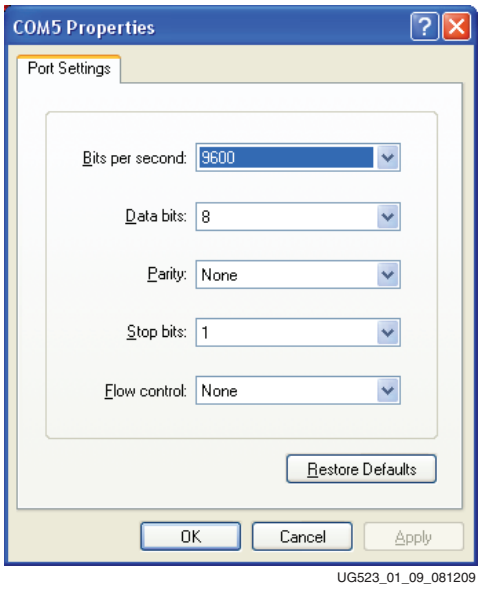
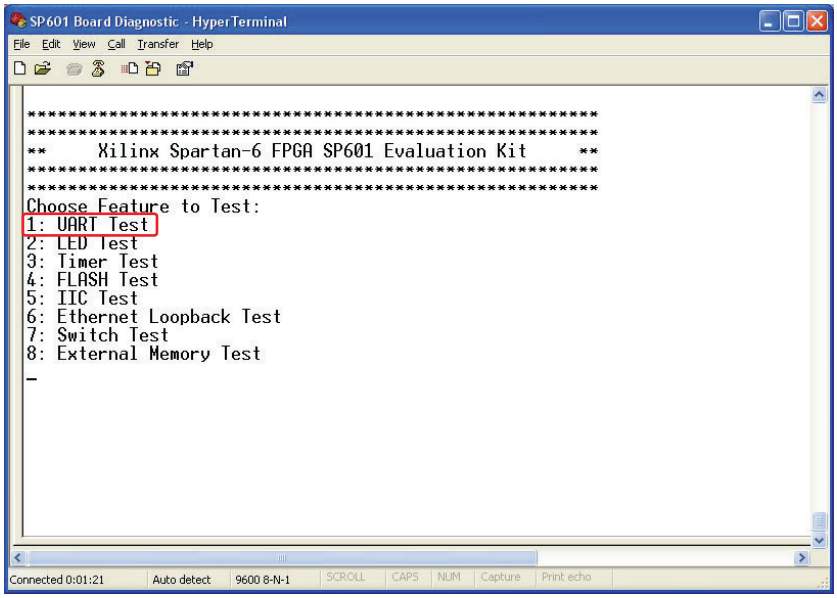


Figure 1-10: **HyperTerminal Port Settings**

9. Be sure to have the SP601 board powered "ON", then press the PROG (SW3) Push Button on the SP601 board to load the Diagnostic Menu. When the SP601 Diagnostic Demo loads from the SPI FLASH, it will print the text to the HyperTerminal Window as shown in Figure 1-11.

   Note: If the Diagnostic Demo Menus does not load when you press the PROG (SW3) button, try clicking the "Disconnect" button and then clicking the "Call" button in the menu bar of the Hyper Terminal.

   Each of the menu option selections will load a simple application that will run a test for the specific feature.

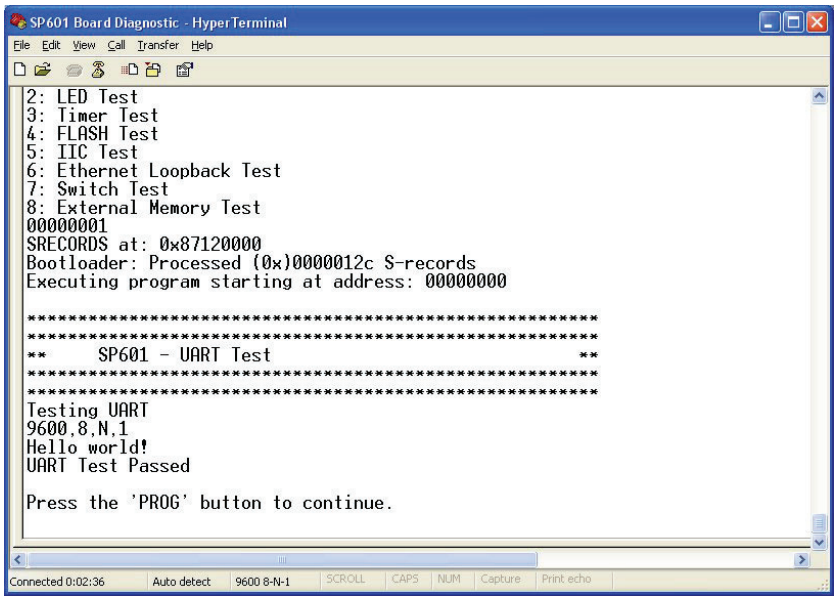


UG523_01_10_081209

Figure 1-11: **SP601 Diagnostic Demo Menu Items**

10. Select Menu option #1 UART Test. This test will exercise the UART.

    After a specific test has been run, press the Prog push button on the SP601 board to reload the bootloaded menu application.



UG523_01_11_081209

Figure 1-12: **Selecting a Diagnostic Test to Run**

You may continue running the different Diagnostic Demo menu options to see the different features working on your board. At this point, you should have been able to see that your board powers and that features like the UART, switches, LEDs, FLASH, Memories and Ethernet are passing their Diagnostic test. If you are having problems, please turn to the "Getting Additional Help and Support" section of this guide.

Getting Started with the Base System Reference Design

The Base System Reference Design targeting the SP601 evaluation board, will filter images that are transferred via Ethernet between the evaluation board and a PC. The images are stored in DDR2 SDRAM using the hard Memory Controller Blocks available in the Spartan-6 FPGA. The stored image is continuously read from SDRAM and filtered. The resulting image is continuously stored back in the DDR2 SDRAM. This filtered image is then retrieved by the Base Reference Design Interface Software and displayed on a PC. Figure 1-13 shows a block diagram of the base reference design that has been implemented in the Spartan-6 LX16 FPGA. The reference design includes common functions for communication, external memory interface, UART, and control.

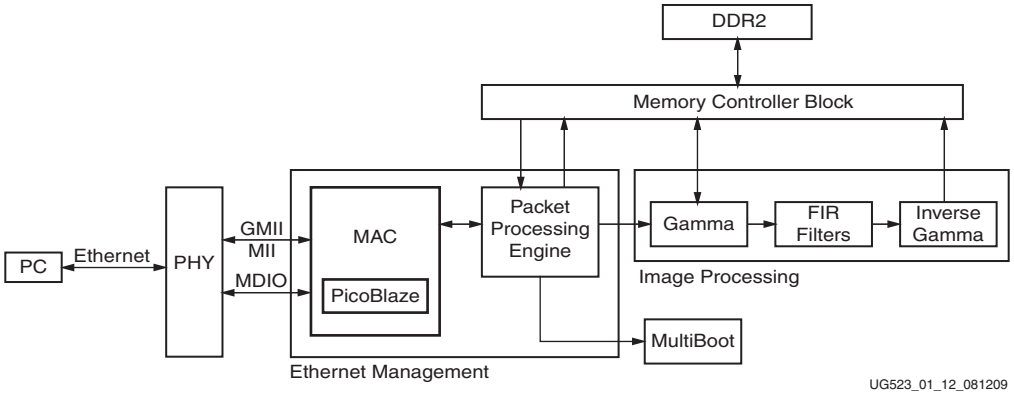


Figure 1-13: **Base System Reference Design**

A Memory Controller Block is used to store both the unfiltered and filtered images in the DDR2 SDRAM. These images are sent from a PC via a series of Ethernet packets. This memory controller is continuously reading, filtering, and storing images back into this memory. The PC also periodically retrieves the filtered images via Ethernet for display.

The Ethernet Management section includes a MAC and a Packet Processing Engine. This section provides a way to control various aspects of the demo, transfer images between the demo board and a PC, and receive status from the demo. A simple MDIO controller is implemented using a Picoblaze™ processor. The purpose of this controller is determine when a Ethernet link is present, and if so, what speed this link is operating at (for example, 1000 Mb/s (GMII) or 100 Mb/s (MII)). The MAC and packet processing logic can run in either mode.

The Image Processing structure consists of a 5x5 pixel 2D FIR filter that is built using DSP48A slices.

A multiboot demonstration exists to switch from between a reference design that implements the 2D filtering in DSP Slices to a similar reference design that implements the 2D filtering in standard FPGA logic.

Setting up the Hardware for the Base System Reference design

In addition to maintaining the settings and cable connections used to run the SP601 Diagnostic Demo, connect the Ethernet cable and USB JTAG cable as shown in Figure 1-14.

1. Connect the USB JTAG
   a. Remove the second USB A/MiniB Cable from the SP601 box
   b. Connect the MiniB USB connector to USB connector marked J10 (USB JTAG)
   c. Connect the USB A end of the cable to your PC. This will be used as a Xilinx download cable port in the SP601 Base System Reference Design later.
2. Connecting the Ethernet Cable
   a. Remove the Ethernet cable from the SP601 box.
   b. Connect one end to the RJ45 connector P1 and the other end to the Ethernet port on your PC. This connection will be used as a crossover from the SP601 board to your PC in the SP601 Base System Reference Design demo.

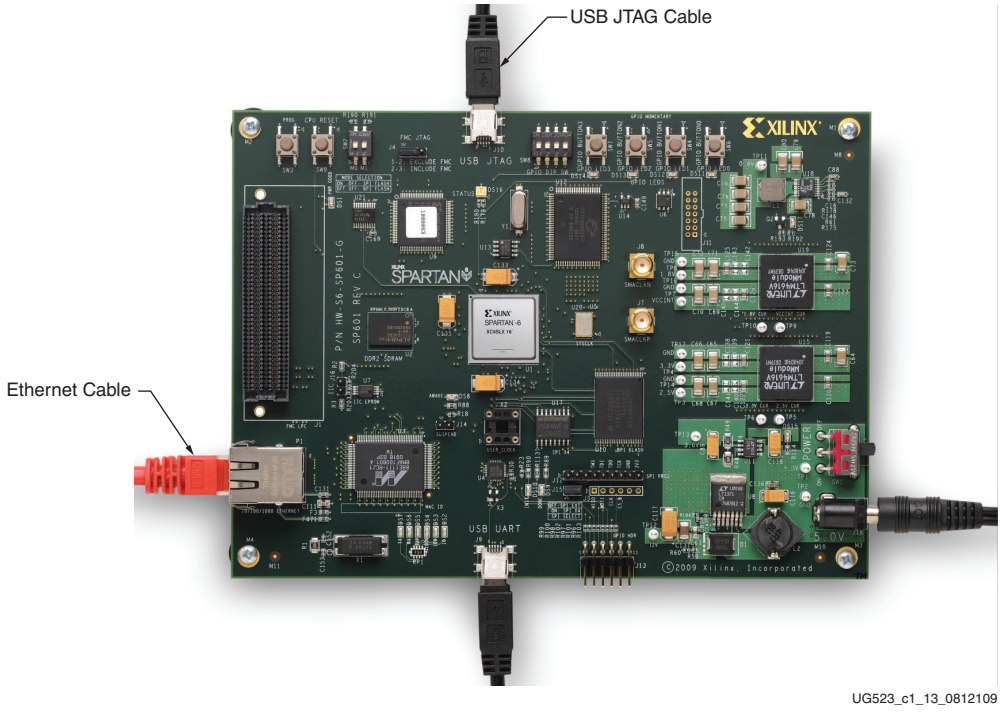


Figure 1-14: **Ethernet and USB JTAG Cable Connection**

3. Select SPI Configuration Mode

   Ensure that the DIP switch SW2 is set to the SPI Configuration Mode, where M0 is set to "ON" and M1 is set to the "OFF" positions.

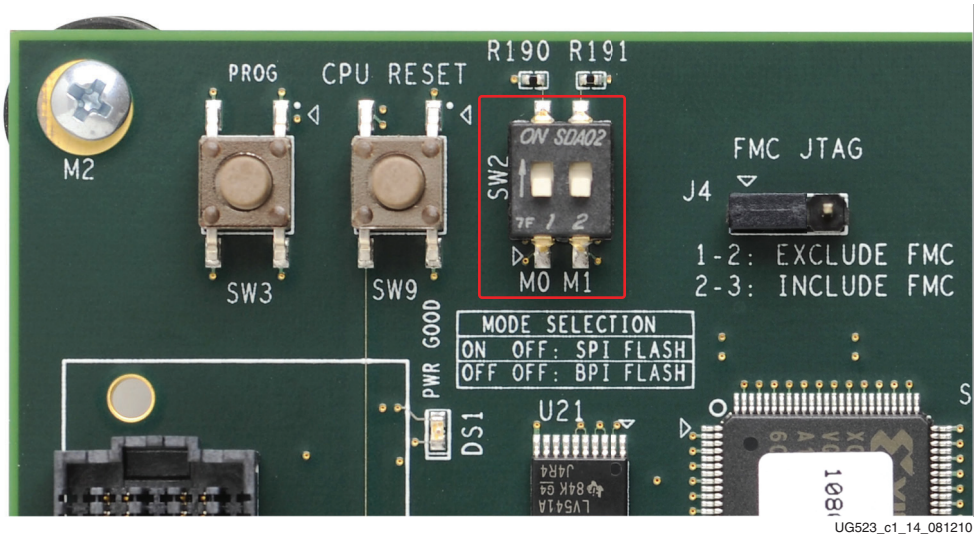


Figure 1-15: **Select Configuration Mode**

Installing Base System Reference Design Application GUI

The Base System Reference Design includes an application GUI that must be installed before running the demonstration. To set up the source files, go to the SP601 Documentation webpage at:

http://www.xilinx.com/products/boards/sp601/reference_designs.htm

and click **SP601_BRD_rdf0003** (ZIP). Unzip the file, and use Windows Explorer to navigate to the local directory. The directory structure is as follows:

```
Base_System_Reference_Design/
  Base_System_Application/
  Base_System_Images/
  Base_System_Source_Project/
  Ready_For_Download/
```

Navigate to the `Base_System_Application` directory and locate the install image `BaseRefDISetup2_0_0.msi`. This application is used to display the graphical information for the Base Reference Design. Double-click the MSI file to install the software.

In the dialog window shown in Figure 1-16. Click **Run**.

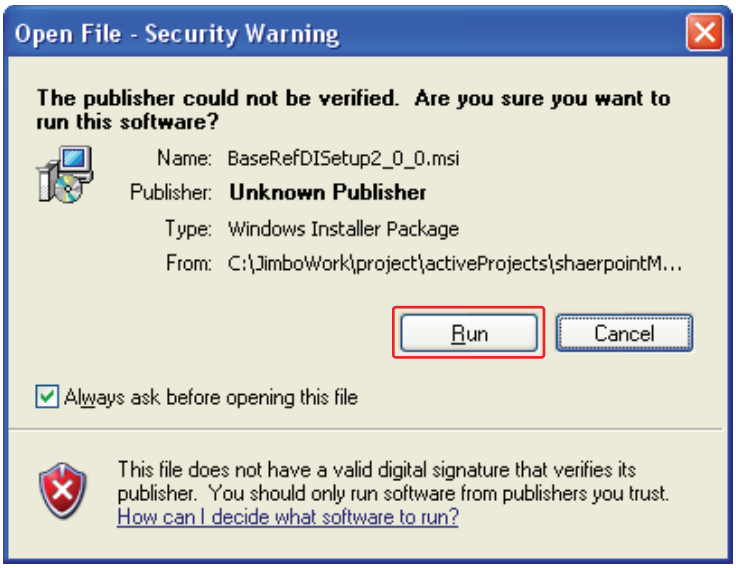


Figure 1-16: **Opening Base System Install**

Please select **Next** or **I agree** in the subsequent installation dialog windows until the installation is complete.

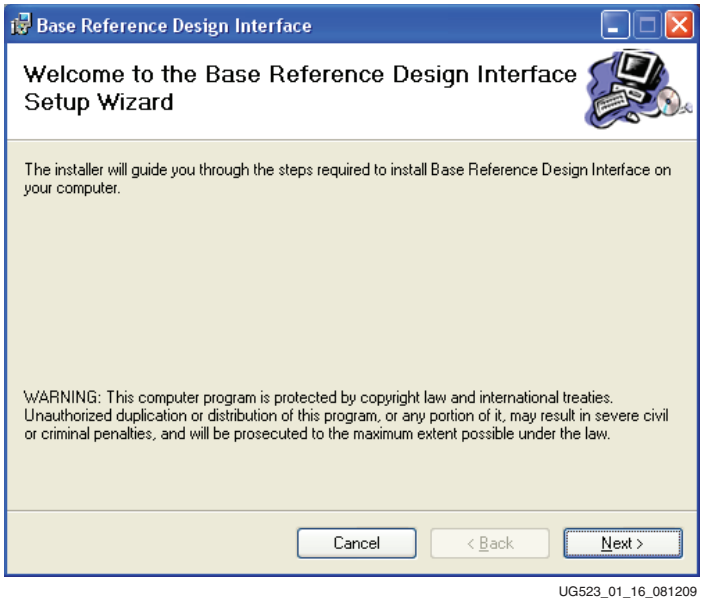


Figure 1-17: **Base System GUI Application Install**

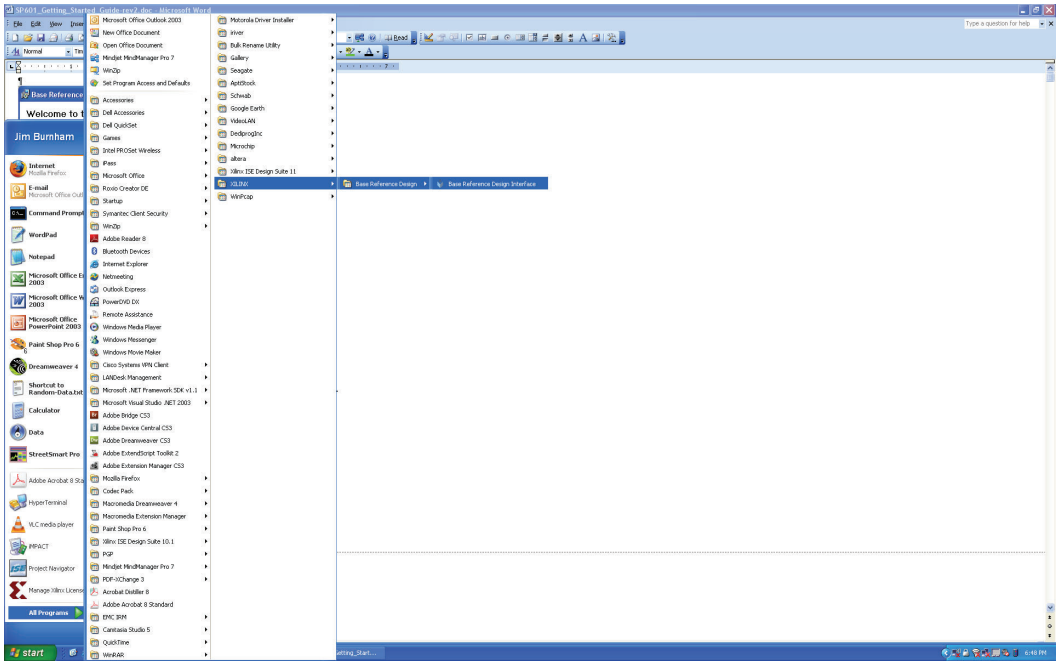
Running the Base System Reference design

Now that you have the SP601 set up and the Base System Reference Design Application software installed, you can run the demo.

You should have the Ethernet cable connected between the SP601 board and your PC Ethernet port. You should make sure that any wireless Ethernet connections are disabled, as this tends to interfere with the application GUI.

Make sure the mode switches on SW2 are set to M0 = “ON” and M1 = “OFF”. This will put the SP601 in SPI configuration mode, which is where the Base Reference Design is stored.

To start the application GUI, please go to your Windows START menu and select “All Programs ' XILINX ' Base Reference Design“ Base Reference Design Interface.



UG523_01_17_081209

Figure 1-18: **Open Base System GUI Application**

The GUI shown in Figure 1-19 will start. At this point, if the SP601 is not already turned on, please turn on the power on SW1.

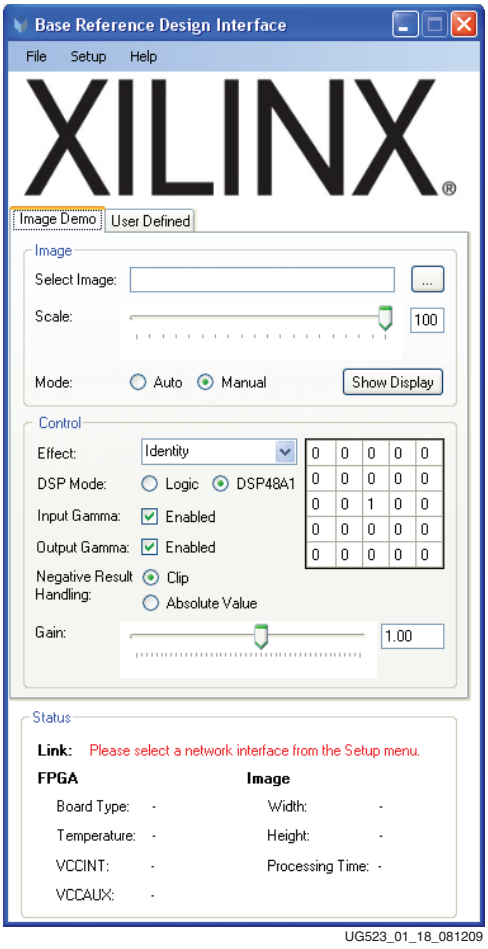


Figure 1-19: **Base System GUI Application**

You will notice in the Status field at the bottom of the GUI, that the **Link** needs to be set. Select the menu item **Setup**, then select a network.

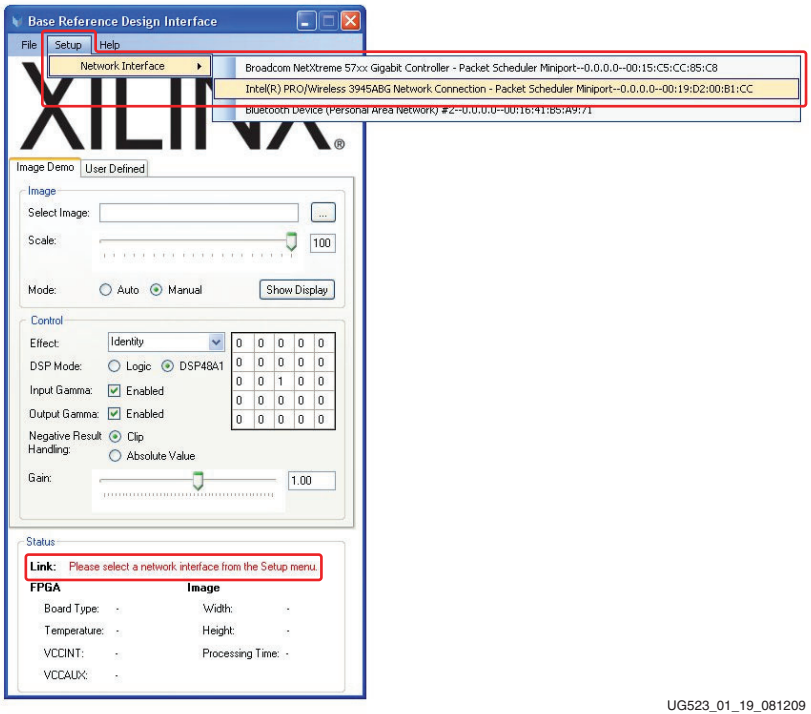


Figure 1-20: **Selecting a Network Application**

The Status field for the Link reads "**In addition**" and the Ethernet Link LEDs on the SP601 board will become active.

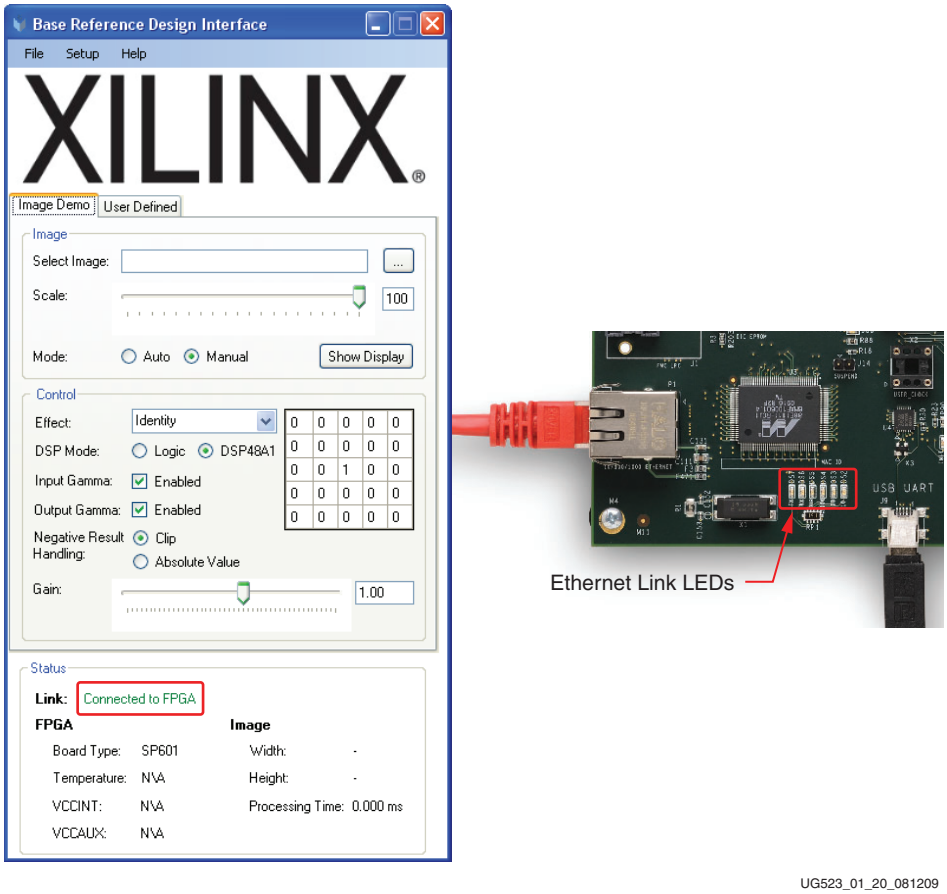


Figure 1-21: **Connected to the FPGA**

Select an image. It is best to select an image smaller than 1024 wide. In the `sp601_BRD_rdf0003_XX.X.zip` file there are a number if images to select or you can select one of your own images. To select one of the provided images, look in the directory `Base_System_Reference_Design ' Base_System_Images`. You could select Frack2.jpg. In the **Image** section of the GUI, use the browse button to navigate to an image.

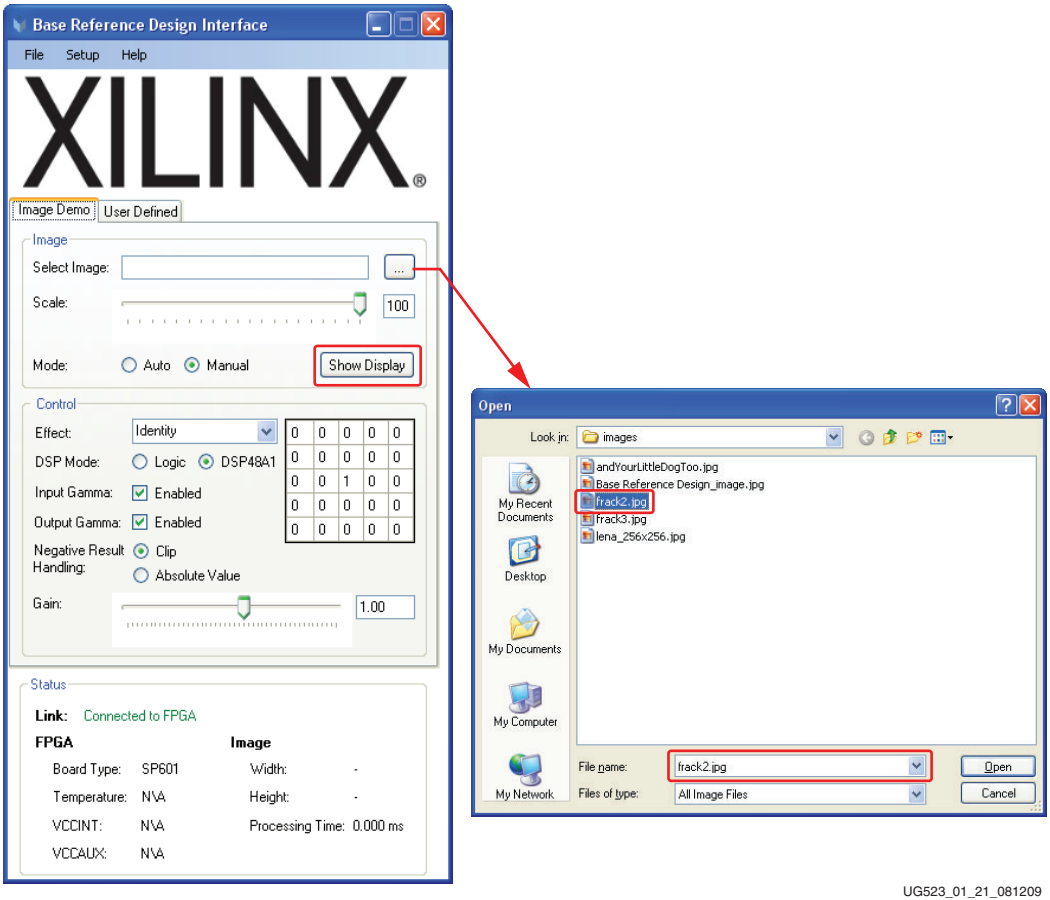


Figure 1-22: **Selecting an Image**

After you have selected the image, click the **Show Display** button. This will display side by side images. The left-most image is the unaltered image, and the-right most image is the image that is undergoing some type of filtering. Unless the effect has been changed, the default effect is **Identity**.

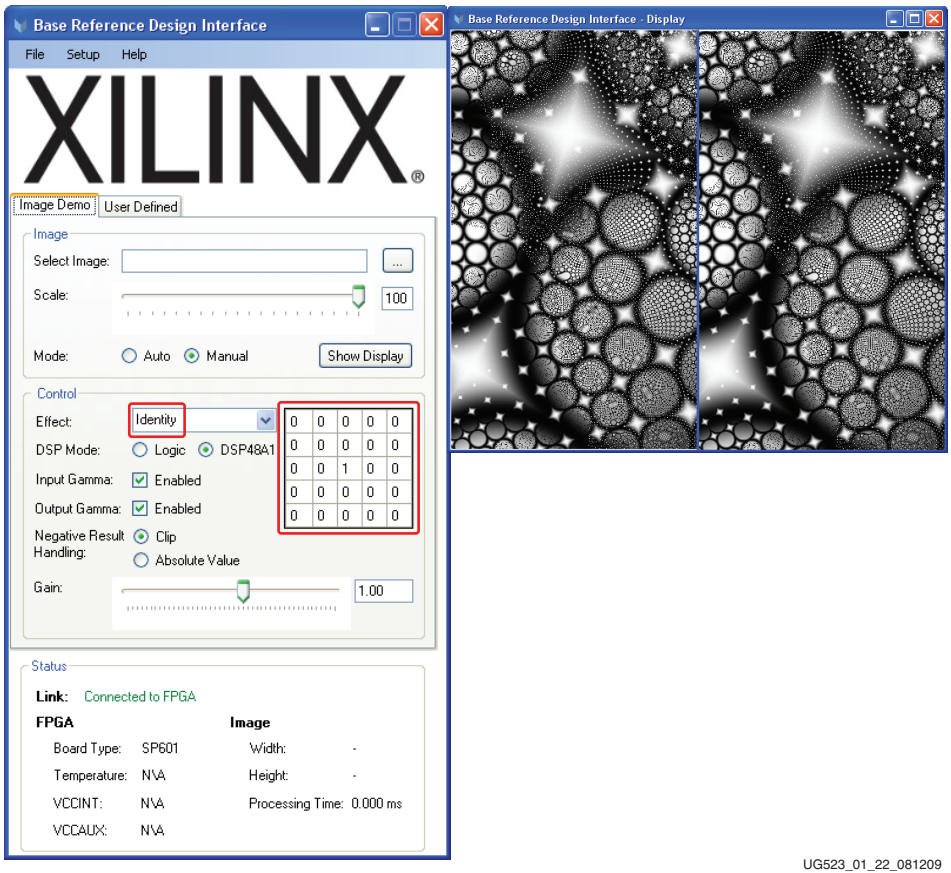


Figure 1-23: **Default Identity Display**

Using the pull down menu, select a different effect. For example, select **SobleX**. The filtering transform will display as shown in Figure 1-24. As you can see the image is updated with the selected filter. The settings for the different effects are also highlighted in the 5x5 grid in the Control section. These 25 squares represent each of the 25 DSP slices used in this design. The numbers within the squares represent the loaded coefficients.

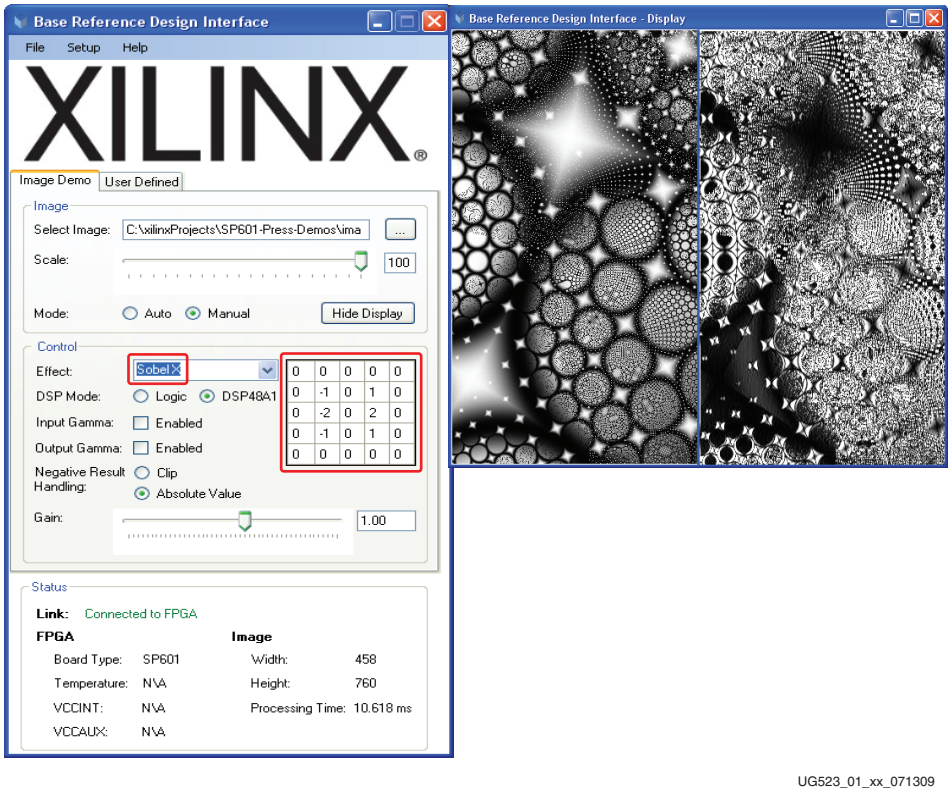


Figure 1-24: **SobleX Display**

Select Smooth effect and notice how the values change. Figure 1-25 shows how the image display changes as well.

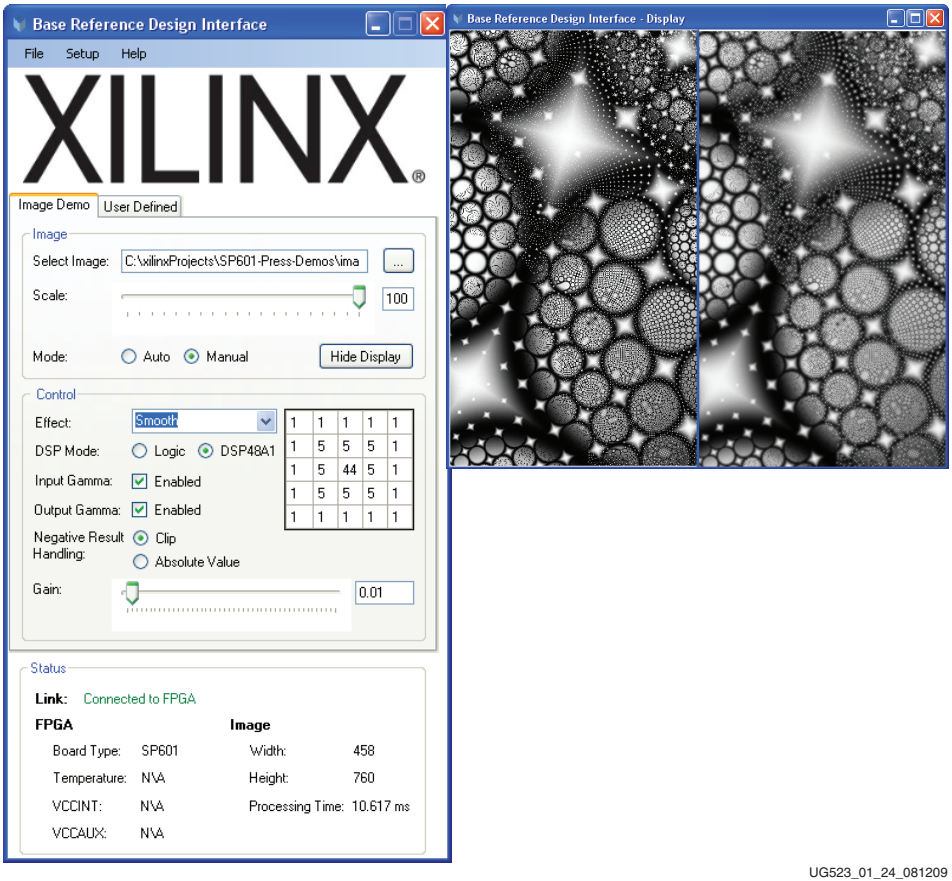


Figure 1-25: **Smooth Effect Display**

Choose **Edge Detect** from the effect menu. The filtering transform shown in Figure 1-26 will be displayed.:

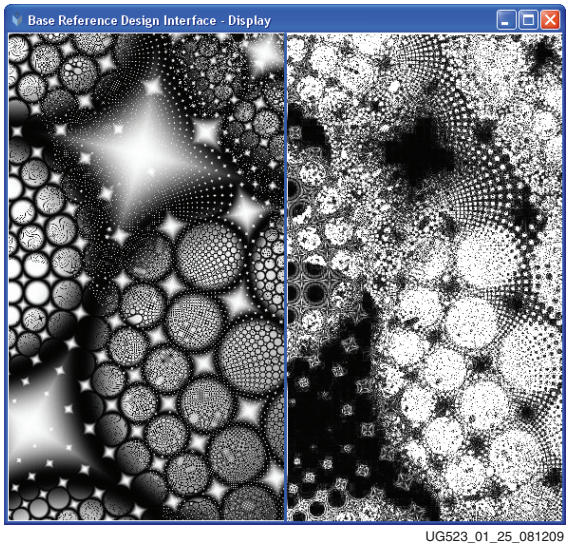


Figure 1-26: **Edge Detect Effect Display**

Increase the gain from 1.00 to 1.740.

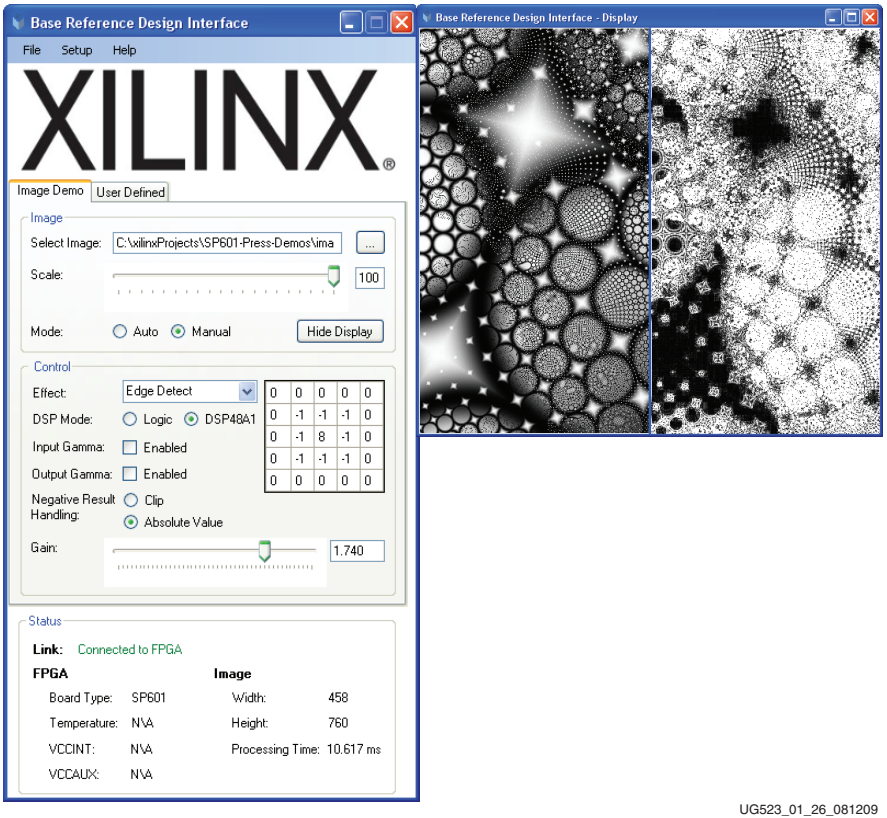


Figure 1-27: **Increase Gain**

Notice that the application GUI has the "DSP48A1" mode selected. This indicates that the hardware design in the FPGA is using the Spartan-6 FPGA DSP48 blocks to implement the filtering transform. You will also notice that in this case the processing time is 10.617 ms.

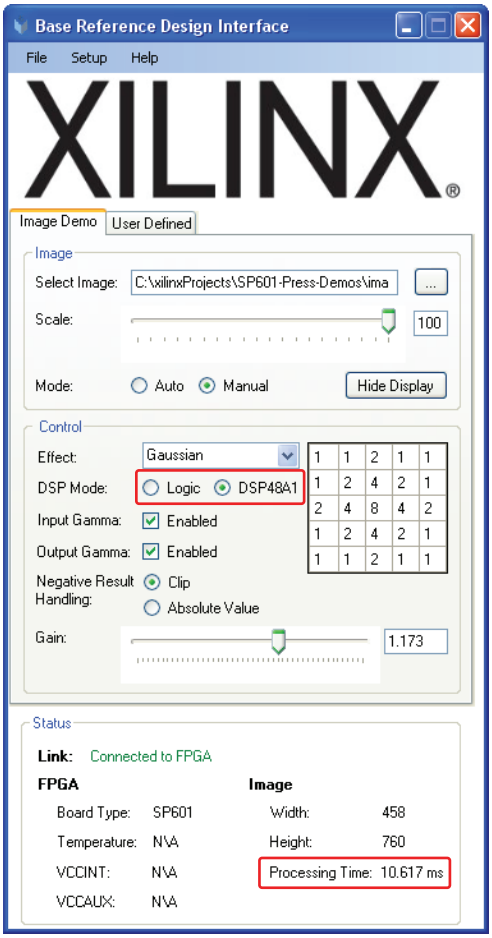


Figure 1-28: **DSP48 Processing Time**

The Base Reference Design enables you to evaluate different alternative implementation using resources within the FPGA. The Spartan-6 LX16 FPGA contains over 14K of logic, 576K Block RAM, and 32 DSP slices among other resources. To demonstrate tradeoffs in how a design can be implemented using these resources, you can select a different implementation

If you change the selection of the DSP Mode from DSP48A1 to Logic, this will change the hardware implementation from using the efficient DSP48 blocks, and will implement the filter transform in standard Spartan-6 FPGA logic slices.

When you select “Logic” or “DSP48” alternately, you are causing the FPGA to load a new bitstream implementing each option. For now, please select the DSP mode to be “Logic”.

You should notice that the FPGA DONE pin flashes off, then on, and the Ethernet link is reacquired.

Now you will notice that the processing time is 53.086 ms. But even more noticeable is the reduced filter precision.

The image processing using logic resources is not as precise as the implementation using DSP48 slices. When using Logic Slices the precision of the filtering is effected.With the default settings, the logic mode is very different than DSP mode because the logic values overflow. If you take the gain down to <1.0 in Edge Detect, then the filter stops overflowing, but the lack of precision is very evident in that the image bleeds through.

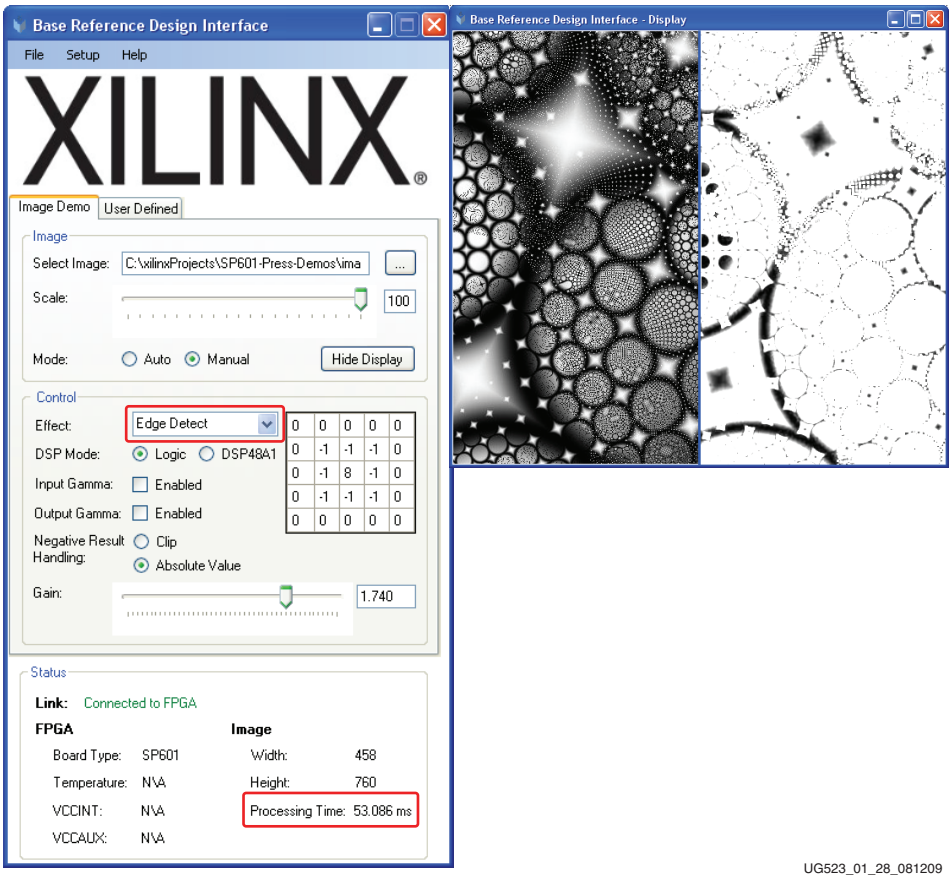


Figure 1-29: **Logic Selection and Processing Time**

Switch back to DSP48A1 and note how the image quality improves. So in addition to increased precision, the DSP slice implementation is operating 5x faster than the logic implementation. This is a convincing example of a reason to use the available hard IP available to achieve higher performance and greater precision. The hard IP resources use minimal or no logic resources, so the customer can use these extra resources for other functions or to reduce costs by moving to a smaller FPGA.

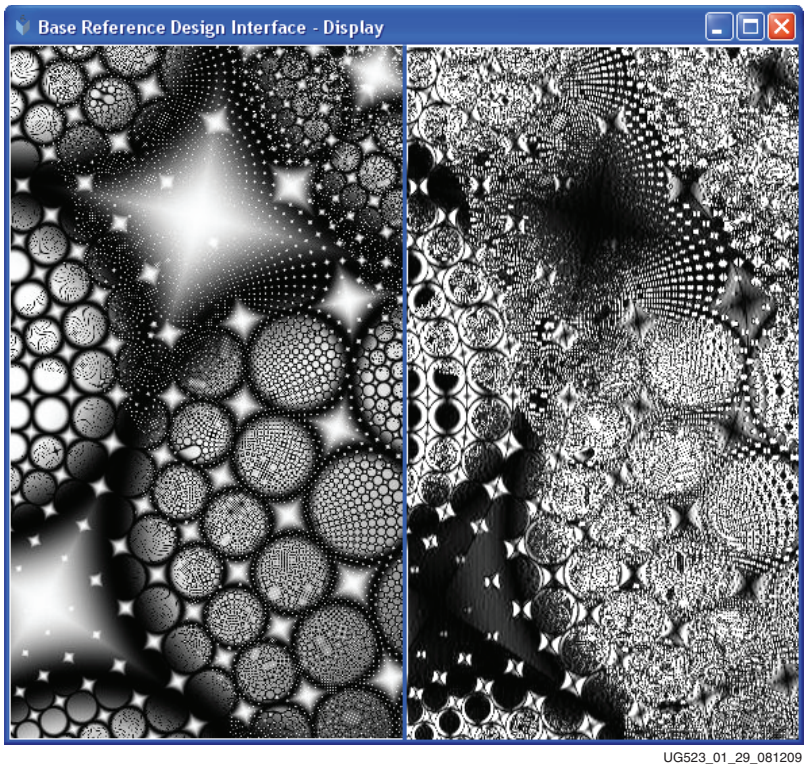


Figure 1-30: **Switch Back to DSP48**

You have now completed running the reference design. Within minutes you have completed the following:

Evaluated Reference Design

Configured using Multi-boot

Evaluated alternative implementations

Installing Software

This SP601 evaluation kit comes with "entitlement" to a seat of the ISE Design Suite: WebPACK Edition, which can be installed from the DVD or the latest version, can be downloaded online at http://www.xilinx.com/tools/webpack.htm

If you already have installed ISE WebPACK or a Full seat if ISE Logic, embedded, DSP or System Edition, installed, then you may already have the software you need. Please still check for any updates. Go to http://www.xilinx.com/support/download/index.htm and click the tab "Product Updates". If you have installed an ISE software product, you can skip to the next section.

If you still need to install the ISE WebPACK software, you may install it from the included ISE DVD or On-Line. You can download WebPACK from http://www.xilinx.com/tools/webpack.htm.

Locate the ISE software DVD provided in the SP601 box, and insert it into your DVD drive. You will be prompted with a Welcome dialog window. Follow the instructions provided in the Installation dialog boxes.

When installation process is complete, reboot the system. The latest version of the Xilinx webPACK software is installed on your system.

Now What?

After following the steps in this Getting Started Guide, you should have been able to set up and test your hardware. You will have been able to test the features of the SP601 board using the SP601 Board Diagnostic FLASH demo. This will have let you test the key features of the board to make sure they were working. You have also been able to run the Base System Reference Design, where you were able to see a more complex design exercising key features of the Spartan-6 FPGA.

You should now have a complete and updated installation of the Xilinx ISE WebPACK software, and should be ready to open your first project.

Additional resource for the SP601 Board can be found on the SP601 product page found at http://www.xilinx.com/sp601. You are encouraged to check the SP601 Evaluation Kit home page regularly for the latest in documentation, FAQs, Reference Design examples, product updates, and known issues.

Getting Additional Help and Support

Support

For questions regarding products within your Product Entitlement Account or if you feel you have received this notification in error, send an email message to your regional Customer Service Representative:

Canada, USA and South America - isscs_cases@xilinx.com

Europe, Middle East, and Africa - eucases@xilinx.com

Asia Pacific including Japan - apaccase@xilinx.com

For technical support including the installation and use of your product license file you may contact Xilinx Online Technical Support at www.support.xilinx.com. On this site you will also find the following resources for assistance:

Software, IP and Documentation Updates

Access to Technical Support Web Tools

Searchable Answer Database with Over 4,000 Solutions

User Forums

Warranty

THIS LIMITED WARRANTY applies solely to standard hardware development boards and standard hardware programming cables manufactured by or on behalf of Xilinx ("Development Systems"). Subject to the limitations herein, Xilinx warrants that Development Systems, when delivered by Xilinx or its authorized distributor, for ninety (90) days following the delivery date, will be free from defects in material and workmanship and will substantially conform to Xilinx publicly available specifications for such products in effect at the time of delivery. This limited warranty excludes:
(i) engineering samples or beta versions of Development Systems (which are provided "AS IS" without warranty); (ii) design defects or errors known as "errata";
(iii) Development Systems procured through unauthorized third parties; and
(iv) Development Systems that have been subject to misuse, mishandling, accident, alteration, neglect, unauthorized repair or installation. Furthermore, this limited warranty shall not apply to the use of covered products in an application or environment that is not within Xilinx specifications or in the event of any act, error, neglect or default of Customer. For any breach by Xilinx of this limited warranty, the exclusive remedy of Customer and the sole liability of Xilinx shall be, at the option of Xilinx, to replace or repair the affected products, or to refund to Customer the price of the affected products. The availability of replacement products is subject to product discontinuation policies at Xilinx. Customer may not return product without first obtaining a customer return material authorization (RMA) number from Xilinx.

THE WARRANTIES SET FORTH HEREIN ARE EXCLUSIVE. XILINX DISCLAIMS ALL OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT, AND ANY WARRANTY THAT MAY ARISE FROM COURSE OF DEALING, COURSE OF PERFORMANCE, OR USAGE OF TRADE. (2008.10)

Do not throw Xilinx products marked with the "crossed out wheelie bin" in the trash. Directive 2002/96/EC on waste electrical and electronic equipment (WEEE) requires the separate collection of WEEE. Your cooperation is essential in ensuring the proper management of WEEE and the protection of the environment and human health from potential effects arising from the presence of hazardous substances in WEEE. Return the marked products to Xilinx for proper disposal. Further information and instructions for free-of-charge return available at: http:\\www.xilinx.com\ehs\weee.htm.