

FreescalE TRK-S12ZVL

CUSTOMER EVB

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Revisions			
Rev	Description	Designer	Date
AX1	Initial Draft A070 Release	Carlos Aceff	04/23/14
B	Prototype Release	Carlos Aceff	05/05/14
C,D	Prototype Release	Carlos Aceff	10/07/14
E	Fixes and Components consolidation	J.Sanchez	11/26/14

Signals (ports) have not been routed via busses as this makes it harder to determine where each signal goes.


User notes are given throughout the schematics.


Specific PCB LAYOUT notes are detailed in *ITALICS*


CAUTION:

This schematic is provided for reference purposes only. As such, Freescale does not make any warranty, implied or otherwise, as to the suitability of circuit design or component selection (type or value) used in these schematics for hardware design using the Freescale HALO family of Microprocessors. Customers using any part of these schematics as a basis for hardware design, do so at their own risk and Freescale does not assume any liability for such a hardware design.

3 Different test points used in design: TPV? TPV?

TPVx - Through Hole Pad small  TPVx

TPHx - Through Hole Pad Large (for standard 0.1" header). Also used on IO Matrix (IOMx)  TPHx

TPX - Surface Mount Wire Loop  TPX

Notes:

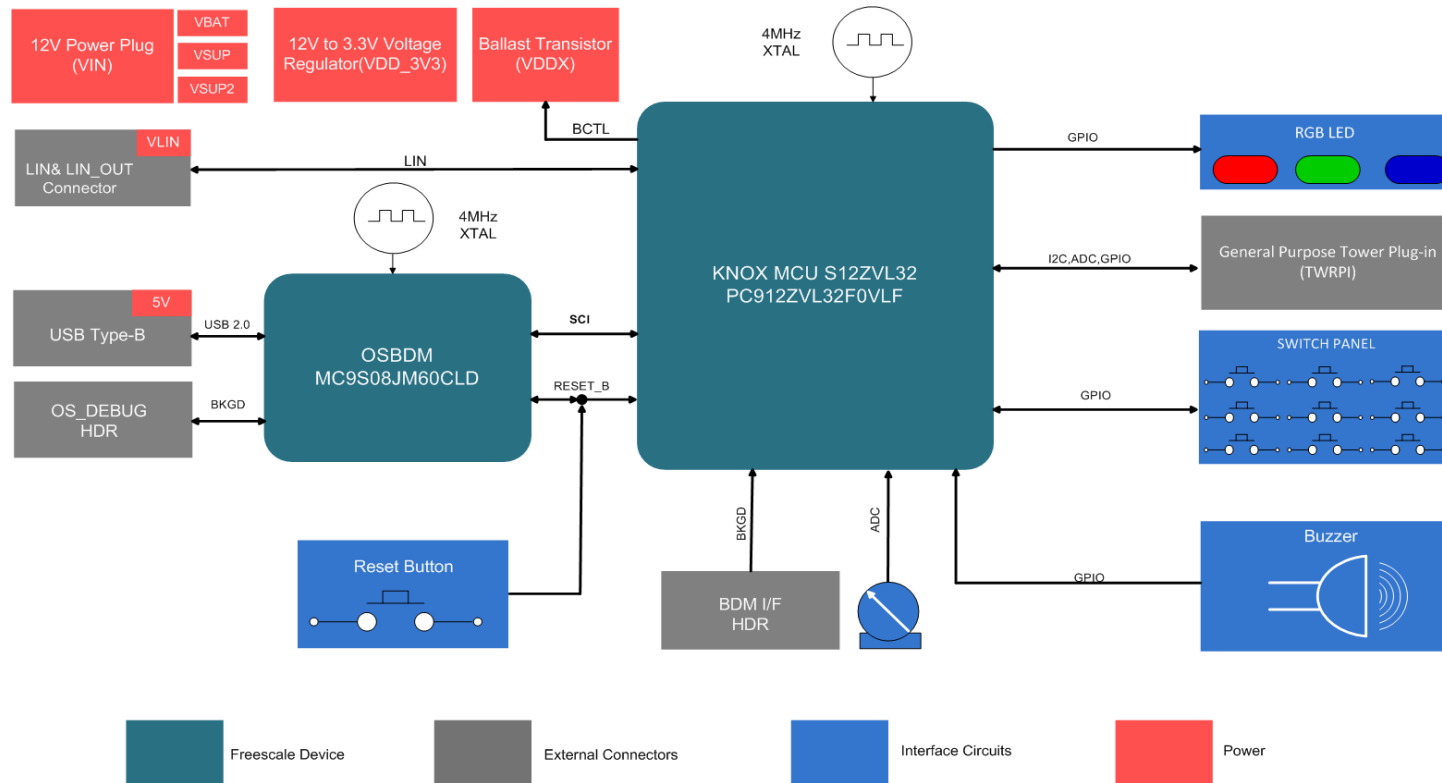
- All components and board processes are to be ROHS compliant
- All connectors and headers are denoted Jx/Px and are 2.54mm pitch unless otherwise stated
- All jumpers are denoted Jx. Jumpers are 2mm pitch
- Jumper default positions are shown in the schematics. For 3 way jumpers, default is always posn 1-2.
- 2 Pin jumpers generally have the "source" on pin 1.
- All switches are denoted SWx
- All test points (SMT wire loop style) are denoted TPx
- Test point Vias (just through hole pads) are denoted TPVx

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ICAP Classification:		FCP:	FIUC: X PUBL:
Designer: Carlos Aceff	Drawing Title: TRK-S12ZVL		
Drawn by: Velmurugan	Page Title: TITLE PAGE		
Approved: Carlos Aceff	Size B	Document Number SCH-28001: SPF-28001	Rev E
Date:	Thursday, November 27, 2014	Sheet	1 of 5

- Unless Otherwise Specified:
All resistors are in ohms, 5%, 1/8 Watt
All capacitors are in uF, 20%, 50V
All voltages are DC
All polarized capacitors are aluminum electrolytic
- Interrupted lines coded with the same letter or letter combinations are electrically connected.
- Device type number is for reference only. The number varies with the manufacturer.
- Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals
- Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

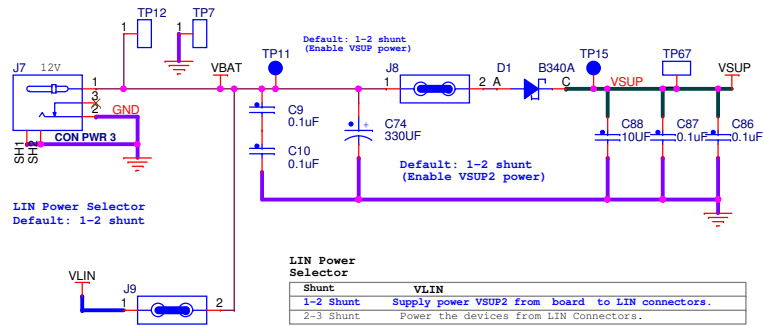
Power & Ground Nets		
NET	VOLTAGE	DESCRIPTION
VBAT	12V	Main Supply input or supply from LIN Connector.
VSUP	12V	Jumpered output of VBAT
VDDA	5V	MCU's analog voltage reference input
VDDX	5V	Output of Internal Voltage Regulator.
VDD_3V3	3.3V	3.3V to TWRPI
+5VU	5V	5V Input from USB Type-B Connector.
+5V_SW	5V	Controlled output 5V from USB.
GND	0V	Digital Ground
VSSA	0V	Analog Ground(Connected to Ground through Zero Ohm Cut trace)

BLOCK DIAGRAM

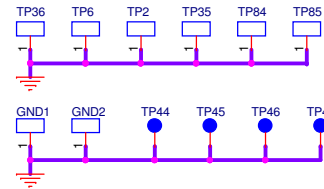


TRK-S12ZVL - Power Supply and LIN Switch Interface

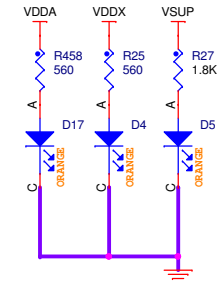
Power Supply Input and Filter



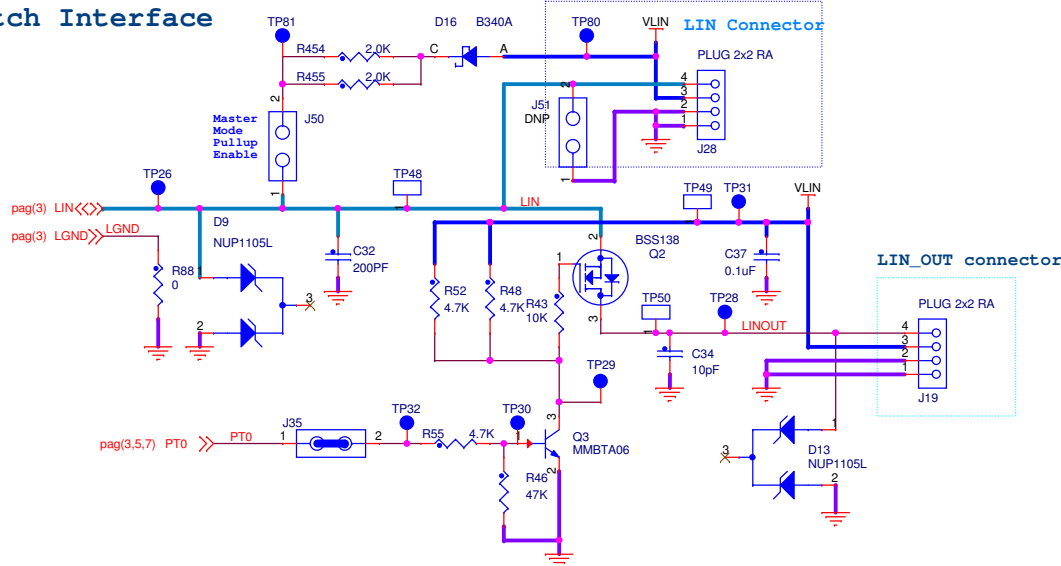
GND Test points



Power LEDs



LIN Switch Interface

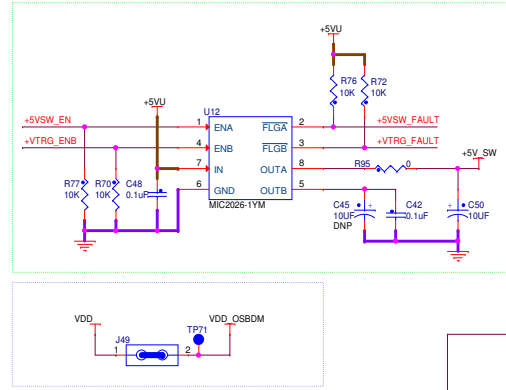
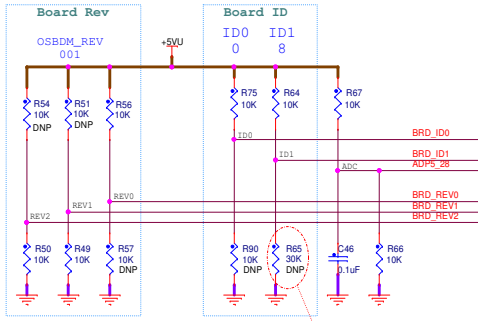


ICAP Classification: FCP: ___ FIUO: X PUBI: ___			
Drawing Title: TRK-S12ZVL			
Page Title: POWER SUPPLY/ LIN			
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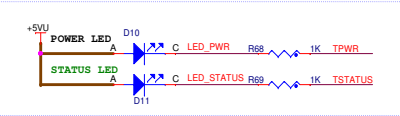
TRK-S12ZVL - OSBDM Interface

BOARD ID RESISTANCE SELECTION TABLE

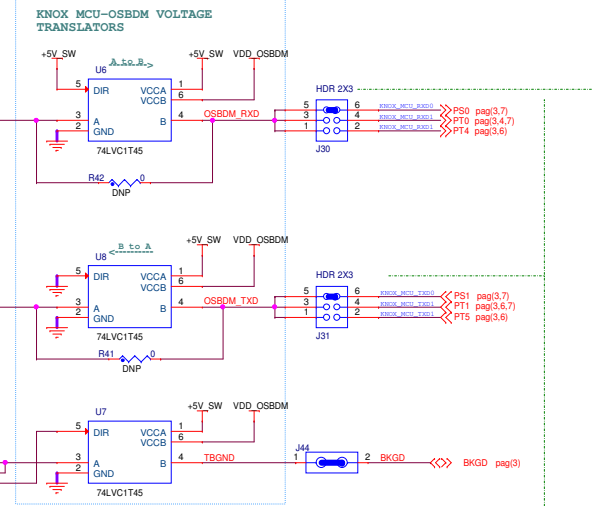
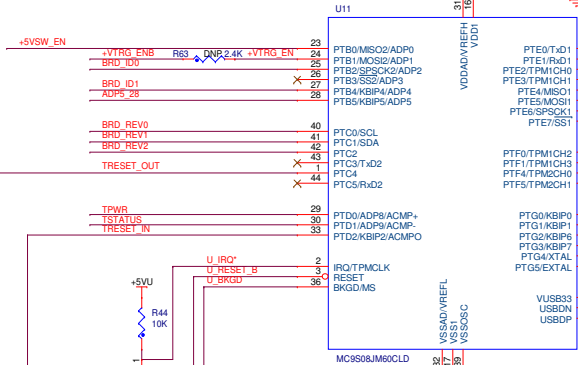
#	Pull-Up	Pull-Down
0	10K	0
1	10K	1.3K
2	10K	3.3K
3	10K	5.6K
4	10K	10K
5	10K	18K
6	10K	30K
7	10K	62K
8	10K	(NC)



TX / RX (R456 and R457)
 POKA-YORK: Place both jumpers with the same orientation and provide same alloy between their terminals in a square fashion.



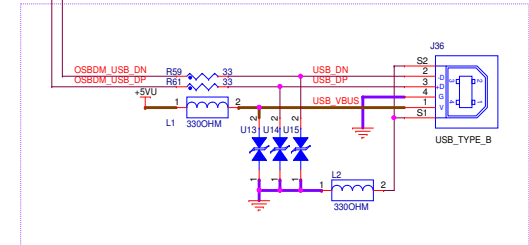
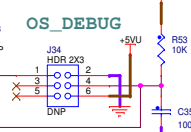
Place one 0.1uF cap near Pin11(VDD1) & another 0.1uF cap near Pin31(VDDAD/VREFP)



KNOX MCU SCI Source Selector

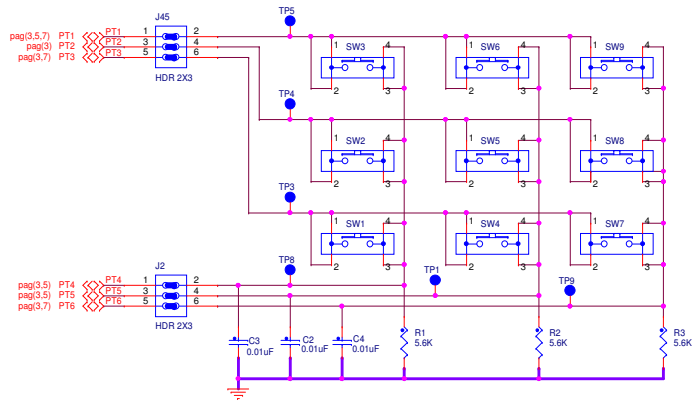
Shunt	KNOX MCU SCI SOURCE
1-2 Shunt	Knox MCU SCI TXD0 (PT5) & RXD0 (PT0)
3-4 Shunt	Knox MCU SCI TXD1 (PT1) & RXD1 (PT0)
5-6 Shunt	Knox MCU SCI TXD1 (PT5) & RXD1 (PT4)

Place the components as close as possible to the OSBDM MCU pins.

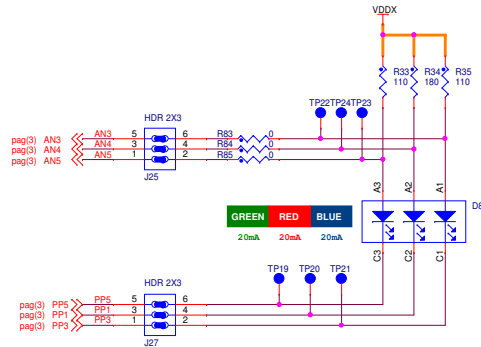


TRK-S12ZVL - User Peripherals

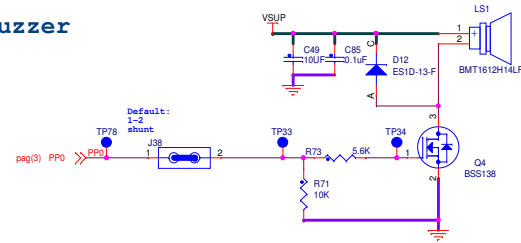
Switch Panel



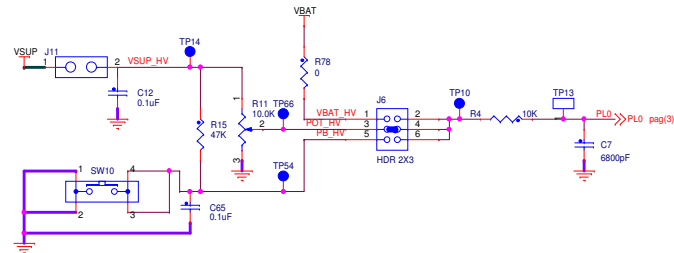
RGB LED



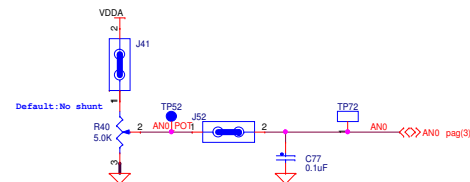
Buzzer



High Voltage Input (HVI)



ADC Potentiometer



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TRK-S12ZVL - TWRPI Interface

