System Demonstration Platform Breakout Board User Guide

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ANALOG DEVICES

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Regulatory Compliance

The ADZS-BRKOUT-EX3 is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADZS-BRKOUT-EX3 board has been certified to comply with the essential requirements of the European EMC directive 89/36/EC amended by 93/68/EEC and therefore carries the "**CE**" mark.

The ADZS-BRKOUT-EX3 board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused ADZS-BRKOUT-EX3 boards in the protective shipping package.

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PREFACE

Thank you for purchasing the ADZS-BRKOUT-EX3 System Demonstration Platform (SDP) breakout board from Analog Devices, Inc. The SDP breakout board can be used in conjunction with the SDP board and daughter boards designed on the SDP system. The breakout board allows signals travelling between the SDP board and compatible daughter boards to be monitored, through the insertion of the breakout board between the SDP board and the daughter board.

The SDP is used as part of the evaluation system for many ADI components. The SDP breakout board exposes each of the 120 pins of the SDP board's connector allowing users to monitor signals between the controlling SDP board and the attached daughter evaluation board or Circuit from the Lab (CftL) board.

Product Overview

The board features:

- 4 x 120-pin small foot print connectors
    - Hirose FX8 -120P-SV1(91),120 Pin Header
    - Hirose FX8 - 120S-SV(21), 120 Pin Receptacle
- ID EEPROM
- 240 Through Hole Probe Points

For more information, go to http://www.analog.com/sdp.

Purpose of This Manual

The *SDP Breakout Board User Guide* provides information on the capabilities and intended purpose of the SDP breakout board (ADZS-BRKOUT-EX3).

Intended Audience

The primary audience for this manual is a system engineer who is using the SDP platform and seeks to understand how to use the SDP breakout board when designing SDP compatible hardware and software.

Manual Contents

The manual consists of:

- Chapter 1, "Getting Started" on page 1-1
  Provides information on how to use the SDP breakout board as a debug tool for the SDP's 120 pin connector signals.
- Chapter 2, "Hardware Description" on page 2-1
  Describes the ADZS-BRKOUT-EX3 hardware. This includes details of the connectors on the board and how these signals are exposed.
- Chapter 3, "Schematic" on page 3-1
  Provides ADZS-BRKOUT-EX3 schematics.

What's New in This Manual

Revision 1.1 of the SDP Breakout Board User Guide revises the document's name to "System Demonstration Platform Breakout Board User Guide".

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the SDP Web site at
  http://www.analog.com/sdp
- E-mail processor questions to
  processor.support@analog.com (World wide support)
  processor.europe@analog.com (Europe support)
  processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
  Analog Devices, Inc.
  One Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Product Information

Product information can be obtained from the Analog Devices Web site.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

Also note, MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Visit MyAnalog.com to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the **Close** command appears on the **File** menu).
{this | that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as this or that. One or the other is required.
[this | that]	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional this or that.
[this,…]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of this.

Example	Description
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	Note: For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	Caution: Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	Warning: Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 GETTING STARTED

This chapter provides specific information to assist you with using the SDP breakout board with the SDP board.

The following topics are covered.

- "Package Contents"
- "PC Configuration"
- "Breakout Board Installation"

Package Contents

Your ADZS-BRKOUT-EX3 board package contains the following items.

- ADZS-BRKOUT-EX3 board

Contact the vendor where you purchased your SDP breakout board or contact Analog Devices, Inc. if any item is missing.

PC Configuration

For correct operation of the SDP board and SDP breakout board, your computer must have the following minimum configuration

- Windows XP Service Pack 2 or Windows Vista
- USB 2.0 port

The SDP board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused SDP boards in the protective shipping package.	

When removing the SDP breakout board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components.

Breakout Board Installation

The SDP breakout board is designed for use with an SDP board. The SDP breakout board must be connected to a PC via the SDP board and a USB cable. Figure 1-1 shows the SDP Breakout board connected to an SDP board and a Circuit from the Lab (CftL) or component evaluation board.

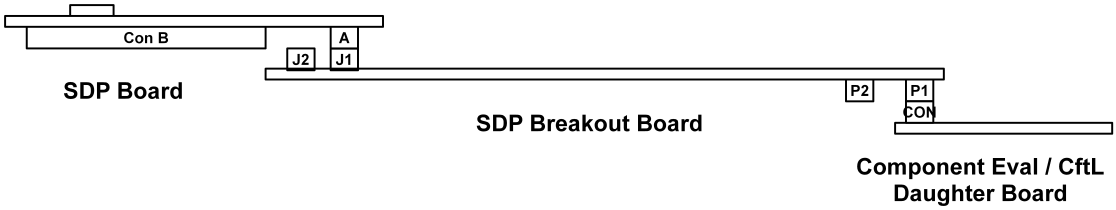


Figure 1-1. Connecting the SDP Breakout Board

The SDP breakout board exposes each of the 120 pins on the SDP board connector. The breakout board has a 120 pin receptacle connector (J1) which attaches to the SDP boards 120 pin connector, and has a 120 pin header connector (P1) for attaching SDP compatible daughter boards to the system.

Pin1 to Pin 30 and Pin 91 to Pin 120 from receptacle J1 are exposed in the P6 Probe Points. Pin 31 to Pin 90 are exposed in the P5 set of probe Points

In this way the SDP breakout board can be used to monitor signals travelling between the SDP and the attached daughter board.

The SDP breakout board can also be used as a proof of concept tool through the insertion of pin headers in the exposed relevant signal through hole locations. These pin headers can be connected to existing hardware when building up a mock up system prior to the design of SDP specific hardware.

2 HARDWARE DESCRIPTION

This chapter describes the hardware design of the ADZS-BRKOUT-EX3 board.

The following topics are covered.

- "LEDs" — Describes the SDP breakout board LEDs.
- "Through Hole Probe Points" — Provides layout of through hole probe points on SDP breakout board
- "Connector Pin Assignments" — Details the pin assignments on the 120 pin connectors

LEDs

There is a single LED located on the SDP breakout board. It is connected to the input power line on the 120 pin header connector on the SDP Breakout board. Therefore when power is being provided from an attached daughter board this LED will be on. If there is no power coming through the VIN pin on P1 this LED will remain off.

Through Hole Probe Points

The SDP breakout boards contains 240 through hole probe points, 2x 120 pin receptacle connector and 2 x120 pin header connectors. One of the 120 pin receptacle connectors (J1) can be used to connect to either connector on an SDP board. One of the 120 pin header connector (P1), on

the back of the SDP board, can be used to connect to a daughter board (P1). Figure 2-1 and Figure 2-2 show both sides of the SDP breakout board and the shading is used to indicate the signal path from the receptacle to the header via the through hole probe points.

Connector J2 and P2 are for use with future Blackfin EZ-Kit products. The signal lines between these two connectors are exposed through the probe points on P3 and P4.

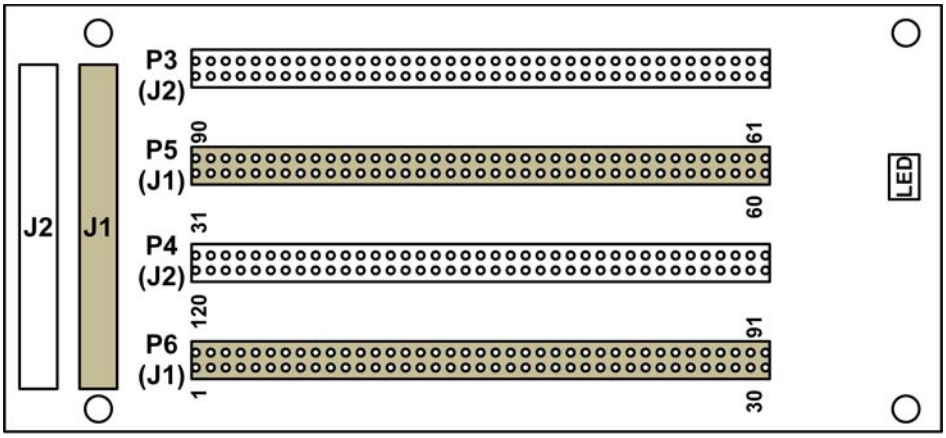


Figure 2-1. SDP Breakout Board — Top View

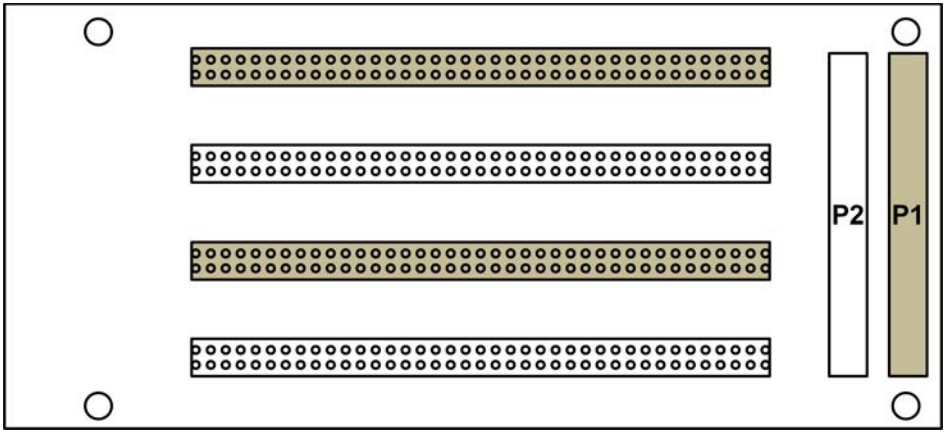


Figure 2-2. SDP Breakout Board — Bottom View

Connector Pin Assignments

The SDP breakout board should be connected to the SDP board via connector J1 and to an SDP daughter board via connector P1. With this configuration, pin assignments for P6 and P5 through hole probe points are listed in Table 2-1.

Table 2-1. 120 Pin Connector Pin Assignments

Pin No.	Pin Name	Description
1	VIN	Power to SDP board. Requires 200mA @ 4 – 7 Volts.
2	NC	No Connect. Leave this pin unconnected. Do not ground.
3	GND	Connect to ground plane of board.
4	GND	Connect to ground plane of board.
5	USB_VBUS	Connected directly to the USB +5v Supply.
6	GND	Connect to ground plane of board.
7	PAR_D23	Parallel Data Bus Bit 23.[1] (No connect.)
8	PAR_D21	Parallel Data Bus Bit 21.[1] (No connect.)

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
9	PAR_D19	Parallel Data Bus Bit 19.[1] (No connect.)
10	PAR_D17	Parallel Data Bus Bit 17.[1] (No connect.)
11	GND	Connect to ground plane of board.
12	PAR_D14	Parallel Data Bus Bit 14.
13	PAR_D13	Parallel Data Bus Bit 13.
14	PAR_D11	Parallel Data Bus Bit 11.
15	PAR_D9	Parallel Data Bus Bit 9.
16	PAR_D7	Parallel Data Bus Bit 7.
17	GND	Connect to ground plane of board.
18	PAR_D5	Parallel Data Bus Bit 5.
19	PAR_D3	Parallel Data Bus Bit 3.
20	PAR_D1	Parallel Data Bus Bit 1.
21	$\overline{\text{PAR_RD}}$	Asynchronous Parallel Read Strobe.
22	$\overline{\text{PAR_CS}}$	Asynchronous Parallel Chip Select.
23	GND	Connect to ground plane of board.
24	PAR_A3	Parallel Address Bus Bit 3.
25	PAR_A1	Parallel Address Bus Bit 1.
26	PAR_FS3	Synchronous (PPI) Parallel Frame Sync 3.
27	PAR_FS1	Synchronous (PPI) Parallel Frame Sync 1.
28	GND	Connect to ground plane of board.
29	SPORT_DR3	SPORT Data Receive 3.[1] (No connect.)
30	SPORT_DR2	SPORT Data Receive 2.[1] (No connect.)
31	SPORT_DR1	SPORT Data Receive 1. Secondary SPORT Data into processor.
32	SPORT_DT1	SPORT Data Transmit 1. Secondary SPORT Data from processor.
33	SPORT_DT2	SPORT Data Transmit 2.[1] (No connect.)

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
34	SPORT_DT3	SPORT Data Transmit 3.[1] (No connect.)
35	SPORT_INT	SPORT Interrupt. Used to trigger a non-periodic SPORT event.
36	GND	Connect to ground plane of board.
37	SPI_SEL_B	SPI Chip Select B. Use this to control a second device on the SPI bus.
38	SPI_SEL_C	SPI Chip Select C. Use this for a third device on the SPI bus.
39	SPI_SEL1/SPI_SS	SPI Chip Select 1.[2] Used to connect to SPI Boot Flash if required. Also used as Chip Select when Blackfin processor is operating as SPI Slave.
40	GND	Connect to ground plane of board.
41	SDA_1	I^2C Data 1.[2]
42	SCL_1	I^2C Data 1.[2]
43	GPIO0	General Purpose Input/Output.
44	GPIO2	General Purpose Input/Output.
45	GPIO4	General Purpose Input/Output.
46	GND	Connect to ground plane of board.
47	GPIO6	General Purpose Input/Output.[2]
48	TMR_A	Timer A flag pin. Use as first Timer if required.
49	TMR_C	Timer C flag pin.[1] (No connect.)
50	NC	No Connect. Leave this pin unconnected. Do not ground.
51	NC	No Connect. Leave this pin unconnected. Do not ground.
52	GND	Connect to ground plane of board.
53	NC	No Connect. Leave this pin unconnected. Do not ground.
54	NC	No Connect. Leave this pin unconnected. Do not ground.
55	NC	No Connect. Leave this pin unconnected. Do not ground.
56	EEPROM_A0	EEPROM A0. Connect to A0 Address line of the EEPROM

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
57	NC	No Connect. Leave this pin unconnected. Do not ground.
58	GND	Connect to ground plane of board.
59	UART_RX	UART Receive Data.[2]
60	$\overline{\text{RESET_IN}}$	Active low pin to reset ADZS-BRKOUT-EX3 board.
61	BMODE1	Boot Mode 1. Pull up with 10kΩ resistor to set SDP to boot from SPI Flash. Enabled on Connector A only.
62	UART_TX	UART Receive Data.[2]
63	GND	Connect to ground plane of board.
64	NC	No Connect. Leave this pin unconnected. Do not ground.
65	NC	No Connect. Leave this pin unconnected. Do not ground.
66	NC	No Connect. Leave this pin unconnected. Do not ground.
67	NC	No Connect. Leave this pin unconnected. Do not ground.
68	NC	No Connect. Leave this pin unconnected. Do not ground.
69	GND	Connect to ground plane of board.
70	NC	No Connect. Leave this pin unconnected. Do not ground.
71	NC	No Connect. Leave this pin unconnected. Do not ground.
72	TMR_D	Timer D flag pin.[2]
73	TMR_B	Timer B flag pin. Use as second Timer if required.
74	GPIO7	General Purpose Input/Output.[2]
75	GND	Connect to ground plane of board.
76	GPIO5	General Purpose Input/Output.
77	GPIO3	General Purpose Input/Output.
78	GPIO1	General Purpose Input/Output.
79	SCL_0	I^2C Clock 0. Daughter Board EEPROM must be connected to this bus.

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
80	SDA_0	I^2C Data 0. Daughter Board EEPROM must be connected to this bus.
81	GND	Connect to ground plane of board.
82	SPI_CLK	SPI Clock.
83	SPI_MISO	SPI Master In, Slave Out Data.
84	SPI_MOSI	SPI Master Out, Slave In Data.
85	SPI_SEL_A	SPI Chip Select A. Use this to control the first device on the SPI bus.
86	GND	Connect to ground plane of board.
87	SPORT_TSCLK	SPORT Transmit Clock.
88	SPORT_DT0	SPORT Data Transmit 0. Primary SPORT Data from processor.
89	SPORT_TFS	SPORT Transmit Frame Sync.
90	SPORT_RFS	SPORT Receive Frame Sync.
91	SPORT_DR0	SPORT Data Receive 0. Primary SPORT Data into processor.
92	SPORT_RSCLK	SPORT Receive Clock
93	GND	Connect to ground plane of board.
94	PAR_CLK	Clock for Synchronous Parallel Interface (PPI).
95	PAR_FS2	Synchronous (PPI) Parallel Frame Sync 2.
96	PAR_A0	Parallel Address Bus Bit 0.
97	PAR_A2	Parallel Address Bus Bit 2.
98	GND	Connect to ground plane of board.
99	PAR_INT	Parallel Interrupt. Used to trigger a non-periodic Parallel event.
100	$\overline{\text{PAR_WR}}$	Asynchronous Parallel Write Strobe.
101	PAR_D0	Parallel Data Bus Bit 0.
102	PAR_D2	Parallel Data Bus Bit 2.
103	PAR_D4	Parallel Data Bus Bit 4.

Table 2-1. 120 Pin Connector Pin Assignments (Cont'd)

Pin No.	Pin Name	Description
104	GND	Connect to ground plane of board.
105	PAR_D6	Parallel Data Bus Bit 6.
106	PAR_D8	Parallel Data Bus Bit 8.
107	PAR_D10	Parallel Data Bus Bit 10.
108	PAR_D12	Parallel Data Bus Bit 12.
109	GND	Connect to ground plane of board.
110	PAR_D15	Parallel Data Bus Bit 15.
111	PAR_D16	Parallel Data Bus Bit 16.[1] (No connect.)
112	PAR_D18	Parallel Data Bus Bit 18.[1] (No connect.)
113	PAR_D20	Parallel Data Bus Bit 20.[1] (No connect.)
114	PAR_D22	Parallel Data Bus Bit 22.[1] (No connect.)
115	GND	Connect to ground plane of board.
116	VIO(+3.3V)	+3.3V Output. 20mA max current available to power IO voltage on daughter board.
117	GND	Connect to ground plane of board.
118	GND	Connect to ground plane of board.
119	NC	No Connect. Leave this pin unconnected. Do not ground.
120	NC	No Connect. Leave this pin unconnected. Do not ground.

1 Functionality not implemented on the SDP board.
2 Shared across SDP board both connectors.

Each interface provided by the SDP is available on unique pins of the SDP's 120 pin connector. The connector pin numbering scheme is outline in Figure 2-3.

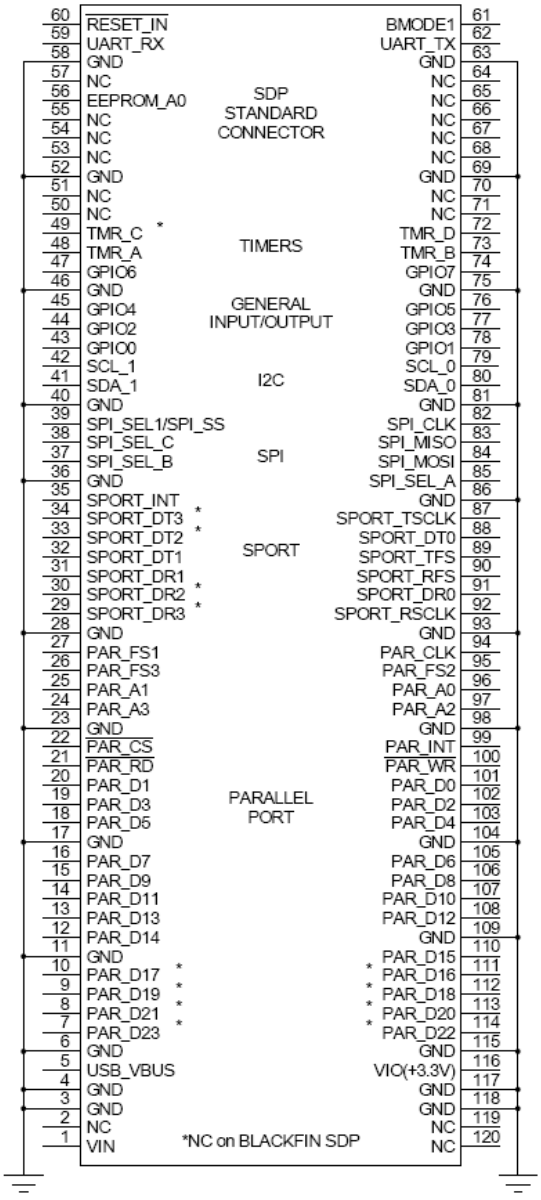
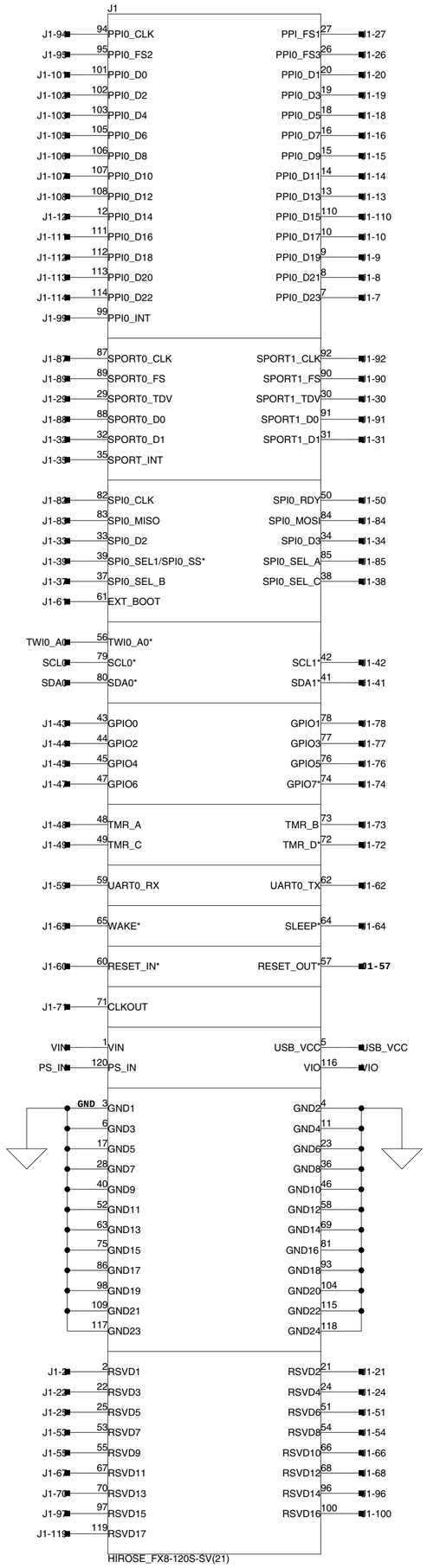


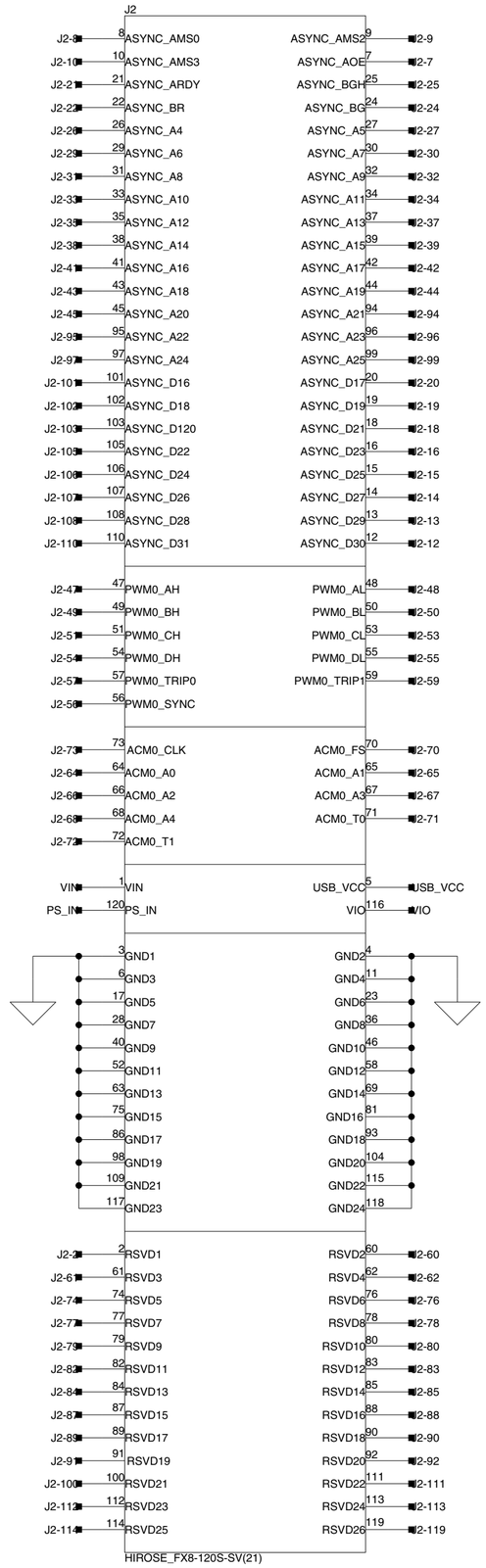
Figure 2-3. 120 Pin Connector Outline

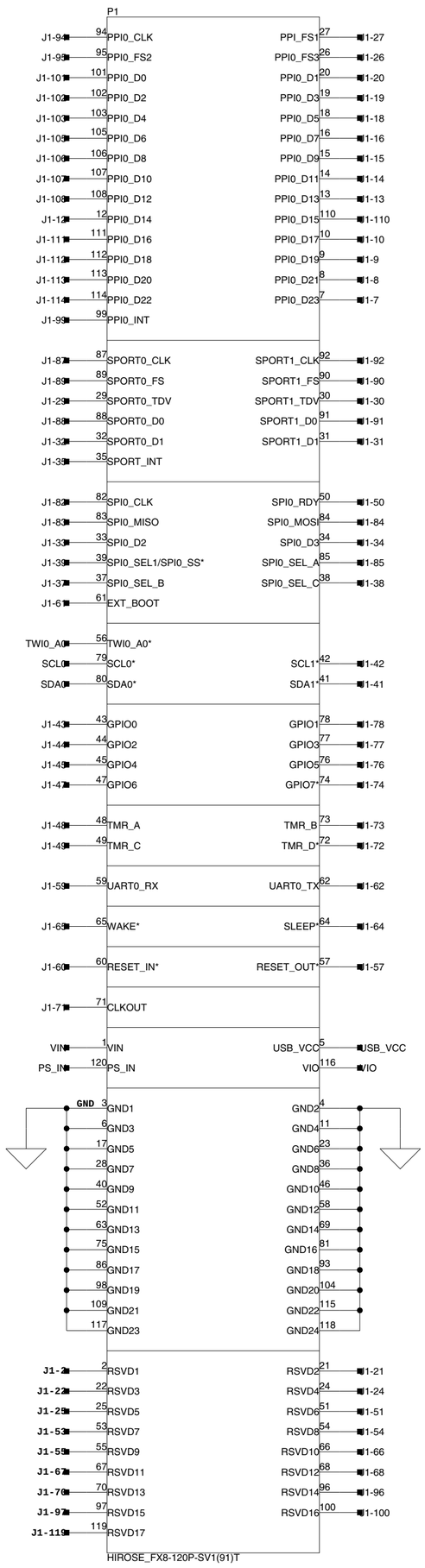
3 SCHEMATIC

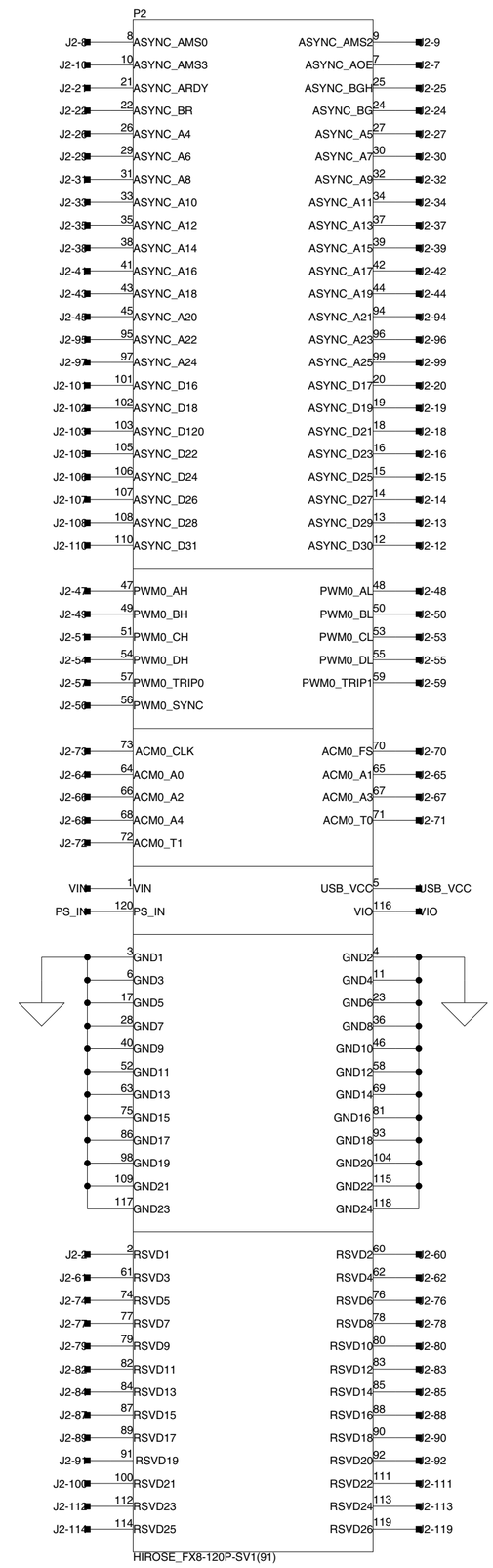
This chapter provides the schematic drawings for the EVAL- SDP -CB1Z board. The schematic pages include:

- SDP Breakout Board—EI3 Connectors
- SDP Breakout Board—Probing Connectors
- SDP Breakout Board—EEPROM and Power









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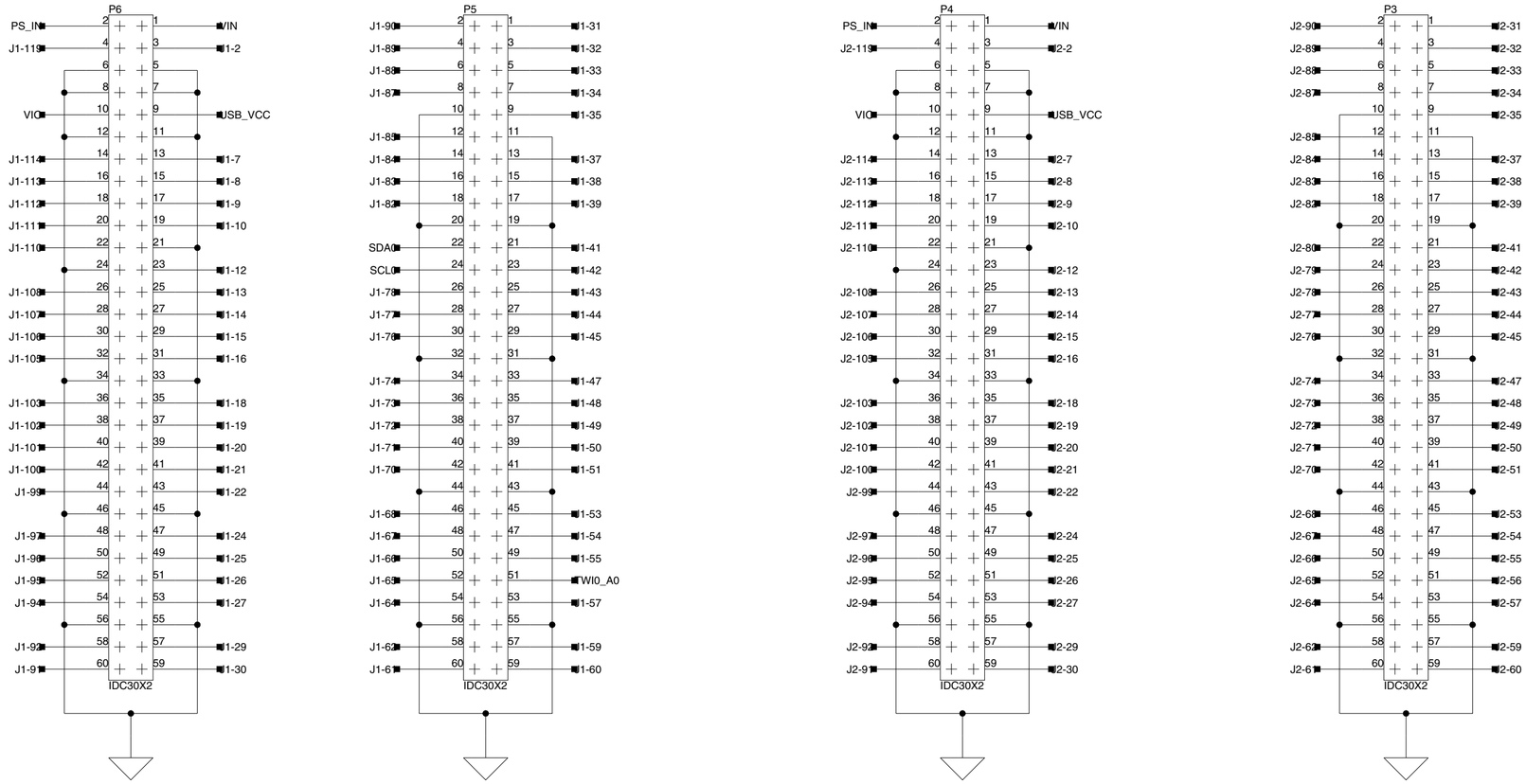
Nashua, NH 03063
PH: 1-800-ANALOGD

Title EI3 Probing Adapter
EI3 Connectors

Size	Board No.	Rev
C	_____	0.1

Date	Sheet	of
07/27/2010	1	3



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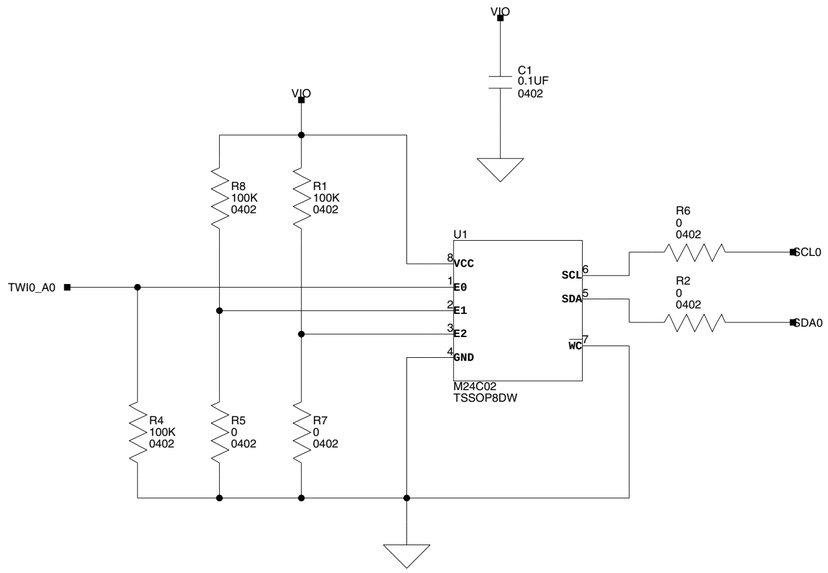
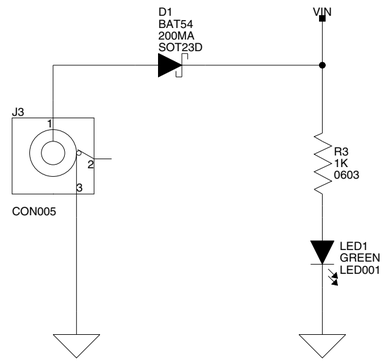
Size C	**Board No.** _____	**Rev** 0.1
Date 07/27/2010	**Sheet** 2 **of** 3	





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Title	EI3 Probing Adapter EEPROM and Power	
Size C	Board No. _____	Rev 0.1
Date 07/27/2010	Sheet 3 of 3	