ADS855xEVM

This users guide describes the characteristics, operation, and use of the ADS855xEVM 16/14/12-bit parallel analog to digital converter Evaluation Board. A complete circuit description as well as schematic diagram and bill of materials is included.

Contents

List of Figures

List of Tables

1 EVM Overview

1.1 Features

- Full-featured Evaluation Board for the ADS8556/ADS8557 or ADS8558 16/14/12-Bit, 6-Channel Simultaneous Sampling Analog to Digital Converters
- Analog inputs can be configured for direct application to the ADC or applied through buffer circuits
- On board external reference option
- Supports Serial or High-Speed Parallel Interface Modes

1.2 Introduction

The ADS855xEVM is an evaluation board for the ADS8556, ADS8557 and ADS8558 family of high precision analog to digital converters. The ADS8556 is featured throughout this Users Guide, but the ADS8557 or the ADS8558 device may be installed on the evaluation board. All EVM functions are identical regardless of the installed device.

The ADS8556 is a high speed, low power, six channel 16-bit A/D converter that operates from independent ±HVDD (±5V to ±15V), +5V AVdd and DVdd supplies. The digital output is delivered through a built in buffer circuit that can be powered from DVdd or separate 2.7-5.25V (BVdd) sources. This allows for flexibility when designing within mixed voltage environments.

The six sample and hold circuits are divided into three pairs (A, B and C). Each pair of channels has a hold signal (CONVST_A, CONVST_B, and CONVST_C) which, when strobed together, allows simultaneous sampling on all 6 analog inputs. The part accepts bipolar analog input voltages in the range of up to ±12V.

Conversion time for the ADS8556 is 1.19µs maximum when operated in hardware mode. Throughput is up to 670kSPS when operated in the parallel interface mode or 470kSPS when operated in serial interface mode. To achieve the maximum throughput of 800kSPS (530kSPS serial), the EVM allows the user to apply an external conversion clock and reference.

1.3 Analog Interface

The analog circuit of the board is divided in four parts. The first part is the analog input buffer or front-end circuit of the A/D converter. Its function is to provide optional gain and impedance matching of the input signal. The analog power supplies for both the high voltage rails on the ADC and the input buffer is part two. The final parts of the analog input include the basic analog functions of the ADS8556 and the optional external reference circuit. Each of these is described below.

1.3.1 Analog Inputs

The analog input to the ADS855xEVM board is comprised of three independent THS4032 operational amplifiers. The THS4032's are powered from a user provided (up to) ±15V analog supply. The amplifiers are arranged as non-inverting unity gain buffers by default. The input circuit for CHA is shown in Figure 1 and is typical of all six input channels. JPx can be used to bypass the input buffer circuit.

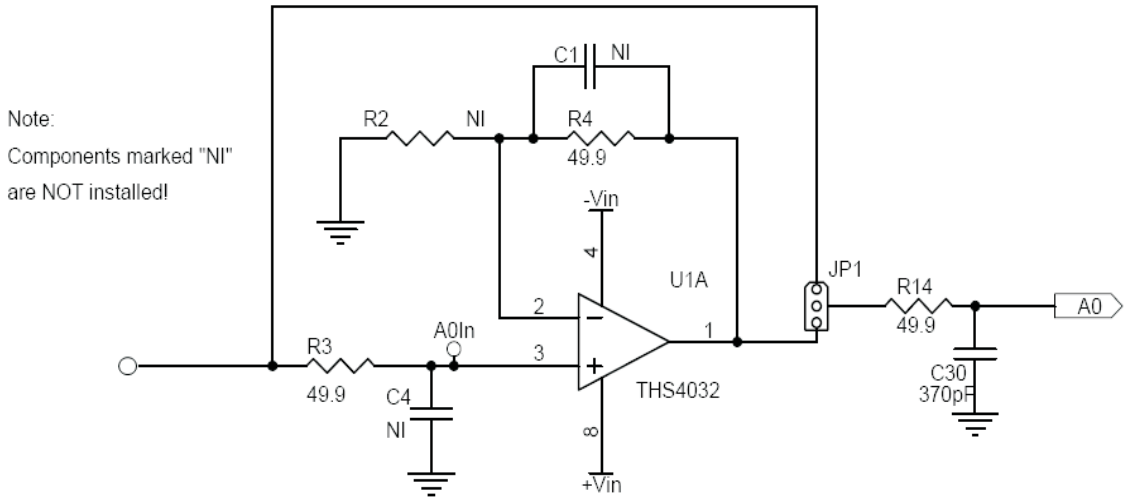

Figure 1. ADS855xEVM Schematic – Typical Analog Input Section

1.3.2 Analog Supplies – Input Buffers and ADS8556 HV Supplies

The ADS855xEVM Board is configured at the factory for ±12V analog operation. The EVM can tolerate maximum power supplies of ±15VDC. Care must be taken to ensure the user supplied ±15VDC limit is not exceeded, or potential damage to the op-amps and the device under test circuits can occur. The user supplied voltage is filtered and applied to the HVDD and HVSS pins of the ADS8556. The ±HV voltages are to be applied to J3 pins 1 (HVDD) and 2 (HVSS) referenced to pin 5 (AGND).

1.3.3 Analog +5V Supply

The ADS8556EVM Board requires an independent +5V supply to power the analog portion of the device under test, the external reference and the external reference buffer. This voltage is applied to J3 pin 3 and is denoted as AVdd. This supply can be monitored at TP3.

1.3.4 Internal and Reference Voltages

The ADS8556 has an internal programmable 2.5 to 3.0V reference source, which is enabled through the REFen pin (in hardware mode) or bit C18 in the configuration register (in software mode).

If an external reference is desired, the internal reference must first be disabled. The ADS855xEVM provides a 2.5V reference source via U11. To use the REF5025 reference, a shunt jumper must be placed on JP12. Test points 10 and 11 are provided to allow the user to monitor the reference voltage (internal or external) and may also be used to connect a user provided reference voltage in the range of 0.5 to 3.025V.

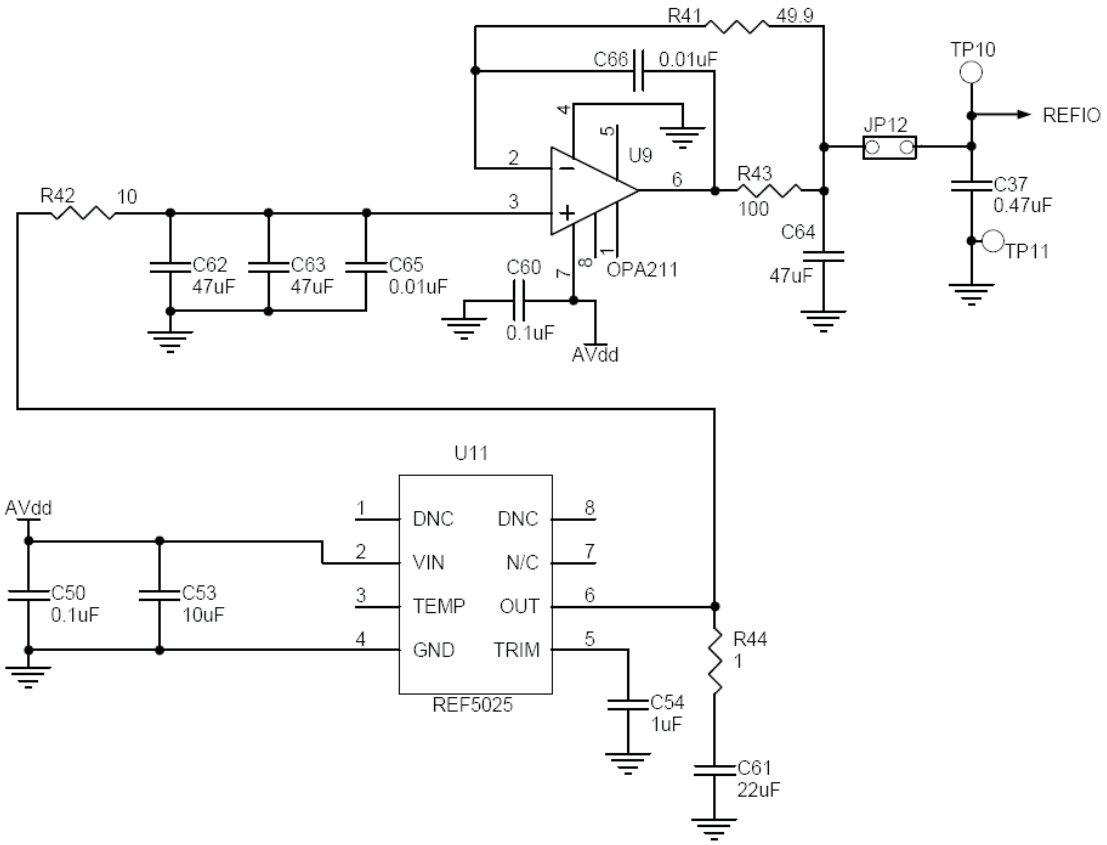

Figure 2. ADS855xEVM External Reference Circuit

2 Digital Interface

The ADS8556 EVM is designed for easy interfacing with the 5-6K Interface Board for use with the C5000 and C6000 series DSK platforms from Texas Instruments. The ADS855xEVM features common 0.1 inch male (top side) and female (bottom side) connectors to all analog inputs and digital control functions making it easy to use with common ribbon cables and laboratory prototyping equipment. The details of the digital portion of the EVM are broken into the following sections which cover the power supply requirements and the interface/control requirements.

2.1 Digital Power – Buffer I/O Supply

The Buffer I/O Supply of the ADS8556 is to be powered from an external source via J3. Connector J3 has a +3.3V and +5V digital supply defined on pins 9 and 10 (respective) as per the *TI Modular EVM Design Guideline* (TI Document SLAA185, see Table 3). Jumper JP4 on the EVM allows the user to select the default +5V or +3.3V for the device BVDD source. This voltage is also applied to the remaining digital circuitry on the EVM.

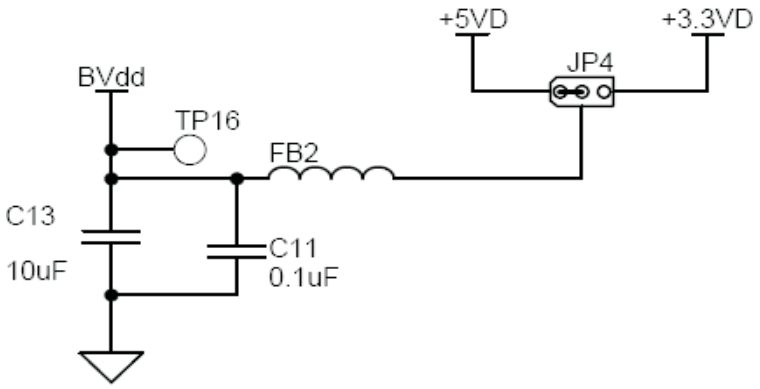

Figure 3. BVDD Voltage Selection

2.2 Control Signals

There are a variety of control lines associated with the ADS855xEVM that are user accessible through connectors J1, J4 and J5. The operating mode of the device determines which connectors are used to control the converter operation, the conversion timing and then to obtain the digital results. Switch SW1 configures the basic operation of the device under test.

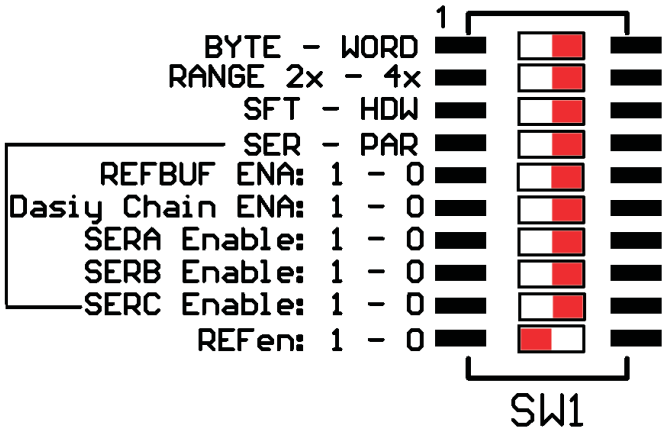

Figure 4. SW1 – Operational Controls

Options available on SW1 include Reference Enable, Serial or Parallel interface, Software or Hardware control and BYTE or WORD data bus width. The figure above represents the silkscreen on the ADS855xEVM. The default positions of the switch elements are indicated by the red blocks. All switch positions except for REFen apply logic '0' to their respective control lines. These individual functions are described in the following sections.

2.2.1 BYTE – WORD (SW1.1)

When Parallel mode is selected, SW1.1 controls the bus width of the output data. Switched to the right (default – logic 0), the data bus is 16-bits wide, when switched to the left BYTE mode is enabled and two 8-bit read accesses to the data bus are required to obtain the full conversion result. Consult the datasheet for a complete description of BYTE mode operation.

2.2.2 RANGE 2x – 4x (SW1.2)

The ADS8556 features two input range options. The default range for the analog input is four times the reference voltage. When SW1.2 is switched to logic 1 (moved to the left) the range becomes two times the reference input. Absolute input range is dependent on the reference input and the applied analog voltage. Consult the device data sheet for specific details.

2.2.3 SFT – HDW (SW1.3)

The ADS8556 has the ability to run in hardware mode (default) or software mode. The hardware mode of operation is the default condition for the EVM. When SW1.3 is switched to logic 1 (moved to the left) software mode is enabled. Note the software mode requires an external conversion clock.

2.2.3.1 Software Mode – External Conversion Clock Requirements

When using software mode, the user must apply an external conversion clock to SMA connector J6. Review the device datasheet for the external conversion clock speed/duty cycle and voltage level requirements. Switch SW1.3 will modify the function of pin 27 on the ADS8556 and route the clock applied to J6 through U10 to the ADC.

2.2.4 SER – PAR (SW1.4)

The ADS8556 also has the ability to communicate with the host controller through either a serial or a parallel interface. Switch position SW1.4 facilitates this feature of the device. When SW1.4 is in its default position (logic 0, pushed to the right) the parallel interface is selected. The 16-bit data bus is routed through a 2:1, 16-bit bus switch (U7 – an SN74CBT16233). In parallel mode, the user can implement the SFT – HDW switch, the RANGE switch, the BYTE switch and the REFen switch.

In serial mode (SW1.4 switched to the left), the serial clock, serial data input and serial data output are routed to connector J1 pins 3/5, 11 and 13 respectively. J1 pins 7and 9 are routed to the chip select input via jumper JP3.

Switch positions SW1.1 through SW1.3 have been described in the previous sections of this users guide. Switch position SW1.10 controls the internal reference; details on this switch are described below and in section 2.2.5 of this manual. Switch positions SW1.5–SW1.9 are described in the following sections.

2.2.4.1 Serial Interface – REFBUF ENA (SW1.5)

Switch SW1 position 5 controls the reference buffers. In hardware mode, when the switch is in its default state (logic 0) all reference buffers are enabled and the internal reference must be applied. When switched to the left, all reference buffers are disabled. In software mode, the internal reference buffers are controlled through bit 24 in the control register.

2.2.4.2 Serial Interface – Daisy Chain ENA (SW1.6)

Switch SW1 position 6 controls daisy chain mode. With the switch in its default state, DCIN[A..C] are connected to ground. When moved to the left (apply logic 1), pins 12–14 of the device under test are connected to test points 17, 15 and 4 respectively. These pins may be wired to another ADS855xEVM and serve as daisy chain inputs for channel pairs A, B and C.

2.2.4.3 Serial Interface – SERA/B/C Enable (SW1.7/8/9)

Switch SW1 positions 7–9 control the serial output of the ADS8556. When in the default states (logic 0), the respective serial output is disabled. When moved to the left, the respective serial output pin becomes active. Note the serial outputs B and C are routed to test points 12 and 13 only. Serial output A is routed to test point 5 and connector J1.13. When using the EVM in conjunction with a modular motherboard or interface card, the serial stream from the ADS855xEVM would be accessed through this connector.

2.2.5 REFen/WR (SW1.10)

Switch SW1 position 10 controls the internal reference of the ADS8556 and also directs the application of the /WR strobe to the ADC. This switch is used in concert with both the SFT-HDW switch (SW1.3) and SER-PAR switch (SW1.4).

2.2.5.1 Hardware Mode, Parallel Interface (EVM Default Condition)

In its default state (left – logic 1) the internal reference is enabled. When switched to the right, the internal reference is disabled.

2.2.5.2 Software Mode, Parallel Interface

When SW1.10 is in its default state (logic 1) the function of pin 63 changes from the reference enable to the write strobe input for the converter and the parallel data input is enabled when both /CS and /WR are low. The reference is enabled by writing to bit 25 in the configuration register.

2.2.5.3 Hardware Mode, Serial Interface

In its default state (left – logic 1) the internal reference is enabled. When switched to the right (logic 0), the internal reference is disabled and an external reference must be applied to REFIO.

2.2.5.4 Software Mode, Serial Interface

When operating in software mode with the serial interface, pin 63 should be tied to BGND or BVDD. The default state of SW1.10 applies BVDD to pin 63 through pull up resistor R37. When SW1.10 is moved to the right, BGND is applied to pin 63.

3 Power Supplies

Factory set up of the board is for a ±12V to ±15V analog front-end supply and the HV supplies on the ADS8556, +5VA for the AVdd supply, and either +5VD or +3.3VD for the BVDD supply. All power to the board is recommend to be sourced from a well regulated linear supply which has current limiting capabilities. Power is to be applied through J3 (top or bottom side or the EVM).Table 1 shows the pin out of J3.

Table 1. J3 – Power Supply Inputs

Signal	Pin Number		Signal
(+VA) connects to HVDD	**1**	**2**	(–VA) connects to HVSS
(+5VA) connects to AVdd, optional HVDD	**3**	**4**	(–5VA) optional HVSS
BGND	**5**	**6**	AGND
Unused	**7**	**8**	Unused
(+3.3V) optional BVDD	**9**	**10**	(+5VD) optional BVDD

For stand alone operation, power sources can be applied via various test points located on the EVM. Refer to the schematic at the end of this document for details. The HVDD and HVSS supplies to the ADS8556 can be selected through jumpers JP10 and JP11.

4 EVM Operation

The following section describes the default jumper locations on the ADS855xEVM along with details on connecting the analog inputs to the board as well as the digital control signals. Details on switching the EVM from the default parallel mode of operation to serial mode are also provided.

Table 2. Factory Jumper Defaults

Jumper	Function	Default Condition
JP1	Controls application of the applied analog signal to A0	1-2
JP2	Controls application of the applied analog signal to A1	1-2
JP3	Controls application the $\overline{CS}$ input – Default is from J1.7	7-8
JP4	Controls the applied BVDD – default is +5VD	1-2
JP5	Controls application of the applied analog signal to C0	1-2
JP6	Controls application of the applied analog signal to B0	1-2
JP7	Controls application of the applied analog signal to B1	1-2
JP8	Controls application of the applied analog signal to C1	1-2
JP9	Controls the application the CONVST inputs – Default is from J4.17	1-2, 4-5 and 7-8
JP10	Controls the applied HVDD – default is +12VD	2-3
JP11	Controls the applied HVSS – default is –12VD	2-3
JP12	Used to connect REFIO with on-board REF5025 (U11)	OPEN

4.1 Analog Inputs – J2

The analog inputs to the ADS8556EVM board can be applied to any one or all of the input channels. Bipolar single ended inputs are to be applied between analog ground (pins 1 through 11, ODD) and input channels A0, A1, B0, B1, C0, C1 located at J2 pins 2-12 (even) respectively. The range of the analog input is dependent on the range setting of the ADC through SW1 position two as mentioned in section 2.2.2 of this document.

CAUTION

Carefully review the data sheet for the limitations of the analog input range, the position of switch SW1.2, and ensure that the appropriate analog/digital voltages are applied prior to connecting any analog input to the EVM.

4.2 Digital Controls – J1, J4 and J5

The digital controls to the EVM can be split into two primary categories – serial or parallel. By default, the EVM is configured to operate in parallel mode under hardware control as discussed in section 2. Details of the signals supported on the EVM are provided in the following sections.

4.2.1 Serial Control –J1

Connector J1 is used primarily for serial control. All but one of the signals on this connector are routed to the ADS8556 through U7 and applied to the ADC when SW1.4 is in the OFF position. Details of J1 are contained in Table 3.

Table 3. J1 – Serial Control Inputs

Pin Number	Signal	Description
J1.1	RESET	Active HIGH RESET input. This pin is connected to digital ground through a 10K resistor R39. A high pulse of at least 50ns will abort any ongoing conversions and reset the internal control register to 0x000003FF
J1.3 J1.5	SCLK	External serial clock input
J1.7 J1.9	FS/CS	Active low chip select input. Routed through JP3 pins 7-8 via shunt jumper. The $\overline{CS}$ input to the ADS8556 has a pull up resistor R18 on the device side of JP3. $\overline{CS}$ input can be held low by placing a shunt jumper on J1 pins 9-10 and JP3 pins 7-8 (default).
J1.11	SDI	Serial data input to the ADS8556
J1.13	SDO	Serial Data A output from the ADS8556. When SERBen and SERCen are disabled, serial data from all three channel pairs is available on this pin.

Table 3. J1 – Serial Control Inputs (continued)

Pin Number	Signal	Description
J1.4 J1.10 J1.18	DGND	These pins are connected to digital ground.

4.2.2 Parallel Control –J4

Connector J4 contains parallel control signals such as write enable and read enable. Four address lines are also provided to allow the stacking of multiple ADS8556EVMs. The signals applied to this connector are routed to the ADS8556 through U7 when SW1.4 is in the ON position. Table 4 describes the control lines found on J4.

Table 4. J4 – Parallel Control

Pin Number	Signal	Description
J4.1	DC_CNTL	G2A input to address decoder U3. Default low by pull down resistor R33
J4.3	DC_AWE	Active low write enable input to ADS8556 – used with /CS to write to the configuration register
J4.5	DC_ARE	Active low read enable input to ADS8556 – used with /CS to read from the parallel data bus
J4.7	DC_A0	3 Line to 8 Line Address decoder input A
J4.9	DC_A1	3 Line to 8 Line Address decoder input B
J4.11	DC_A2	3 Line to 8 Line Address decoder input C
J4.13	DC_A3	3 Line to 8 Line Address decoder input G1 – must be high to enable address line decoder
J4.15	N/C	No Connection
J4.17	DC_TOUT	CONVST_A/B/C inputs when shunt jumpers are placed in their default states on JP9 as described in Table 2
J4.19	DC_INTa	Interrupt source to host processor – connects directly to pin 18 (BUSY) of the ADS8556
J4.2 thru J4.20 (even)	DGND	These pins are connected to digital ground.

4.2.3 Parallel Data – J5

Connector J5 contains parallel data lines. The signals applied to this connector are routed to the ADS8556 through U7 when SW1.4 is in the ON position. Table 5 describes the control lines found on J4.

Table 5. J4 – Parallel Control

Pin Number	Signal	Description
J5.1 thru J5.31 ODD	DC[D0..D15]	16-bit parallel data bus used when writing to or reading from the ADS8556 in parallel mode
J5.2 thru J5.32 EVEN	DGND	These pins are connected to digital ground.

5 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	Literature Number:
ADS8556	SBAS404
THS4032	SLOS224
OPA211	SBOS377
REF5025	SBOS410

SN74CBT16233	SCDS010
SN74LVC1G97	SCES416

6 Bill of Materials, Top Level Silkscreen and Schematic

The following pages contain the ADS855xEVM Bill of materials, top level silkscreen and circuit schematic diagrams.

6.1 Bill of Materials

Table 6. Bill of Materials

QTY	Designators	Description	Manufacturer	Mfg. Part Number
1	NA	Printed Wiring Board	TI	6509747
0	C1 C4 C7 C8 C10 C17 C18 C19 C20 C25 C26 C27	Not Installed		
25	C2 C3 C11 C12 C22 C24 C32–C36 C38–C42 C46 C47 C48 C50 C51 C52 C55 C59 C60	0.1 µF, 0603, Ceramic, X7R, 50V, 10%	TDK	C1608X7R1H104K
12	C5 C6 C9 C13 C15 C43 C44 C45 C53 C56 C57 C58	10 µF, 0805, Ceramic, X5R, 16V, 20%	TDK	C2012X5R1C106M
6	C14 C16 C28–C31	390 pF, 0603, Ceramic, C0G, 50V, 5%	TDK	C1608C0G1H391J
4	C21 C23 C49 C54	1 µF, 0603, Ceramic, X5R, 35V, 10%	Taiyo Yuden	GMK107BJ105KA-T
1	C37	0.47 µF, 0603, Ceramic, X5R, 10V, 10%	Murata	GRM188R61A474KA61D
1	C61	22µF, 0805, Ceramic, X5R, 6.3V, 10%	Taiyo Yuden	JMK212BJ226KG-T
3	C62 C63 C64	47µF, 0805, Ceramic, X5R, 6.3V, 10%	Taiyo Yuden	JMK212BJ476MG-T
2	C65 C66	0.01µF, 0603, Ceramic, X7R, 50V, 10%	Murata	GRM188R71H103KA01D
2	D1 D2	LED 565NM GRN DIFF 0603 SMD	Lumex	SML-LX0603GW-TR
6	FB1–FB6	FERRITE CHIP 600 Ω 500 mA 0805	TDK	MMZ2012R601A
3	J1 J2 J4 (Top Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
1	J3 (Top Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
1	J5 (Top Side)	16 Pin, Dual Row, SM Header (32 Pos.)	Samtec	TSM-116-01-T-DV-P
3	J1 J2 J4 (Bottom Side)	10 Pin, Dual Row, SM Header (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
1	J3 (Bottom Side)	5 Pin, Dual Row, SM Header (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
1	J5 (Bottom Side)	16 Pin, Dual Row, SM Header (32 Pos.)	Samtec	SSW-116-22-F-D-VS-K
1	J6	CONN SMA JACK STRAIGHT PCB	Amphenol	132134
			Emerson	142-0701-201
9	JP1 JP2 JP4 JP5–JP8 JP10 JP11	3 Pin 2mm Header	Samtec	TMM-103-01-T-S
1	JP3	4 Pin, Dual Row, Header (8 Pos.)	Samtec	TSW-104-07-T-D
1	JP9	3 Pin Triple Row, Header (9 Pos)	Samtec	TSW-103-07-T-T
1	JP12	2 Pin 0.1inch, Header	Samtec	TSW-102-07-T-S
19	R1 R3–R6 R8–R14 R19 R20 R21 R24 R28 R29 R41	49.9 Ω, 1/10W, 1% 0603, SMD	Yageo	RC0603FR-0749R9L
0	R2 R23 R25 R30 R31 R32	Not Installed		
1	R7	RES ARRAY 10 kΩ 16TERM 8RES SMD	CTS	742C163103JPTR
11	R15 R18 R22 R33–R40	10.0 kΩ, 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-0710KL
3	R16 R17 R42	10 Ω, 1/10W,1%, 0603, SMD	Yageo	RC0603FR-0710RL
2	R26 R27	2 kΩ, 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-072KL
1	R43	100 Ω, 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-07100RL
1	R44	1 Ω, 1/10W, 1%, 0603, SMD	Yageo	RC0603FR-071RL
1	R45	33.0 Ω, 1/10W, 1%, 0603, SMD	Yageo	311-33.0HRCT-ND

Table 6. Bill of Materials (continued)

QTY	Designators	Description	Manufacturer	Mfg. Part Number
1	SW1	SWITCH DIP HALF PITCH 10POS	CTS	218-10LPST
6	TP1 TP2 TP3 TP8 TP10 TP16	TEST POINT PC MINI .040"D RED	Keystone	5000
6	TP4 TP5 TP12 TP13 TP15 TP17	PC TEST POINT MINIATURE SMT	Keystone	5015
5	TP6 TP7 TP9 TP11 TP14	TEST POINT PC MINI 0.040" D BLACK	Keystone	5001
3	U1 U5 U6	IC OPAMP GP R-R 100MHZ DUAL 8SOIC	TI	THS4032ID
3	U2 U8 U10	IC CONFIG MULT-FUNC GATE SOT23-6	TI	SN74LVC1G97DBV
1	U3	IC 3-8 LINE DECODR/DEMUX 16-SOIC	TI	SN74AHC138D
0	U4	IC ADC 16BIT 6CH 630KSPS 64LQFP	TI	ADS8556IPM
0		IC ADC 14BIT 6CH 670KSPS 64LQFP	TI	ADS8557IPM
1		IC ADC 12BIT 6CH 730KSPS 64LQFP	TI	ADS8558IPM
1	U7	IC 16 BIT 1OF 2 MUX/DEMUX 56TSSOP	TI	SN74CBT16233DGGR
1	U9	IC OPAMP GP R-R 80 MHz SGL 8SOIC	TI	OPA211ID
1	U11	IC PREC V-REF 2.5V LN 8-SOIC	TI	REF5025AID
5	NA	0.100 Shunt - Black Shunts	Samtec	SNT-100-BK-T
9	NA	2mm Shunt -	Samtec	2SN-BK-T

6.2 Top Level Silkscreen

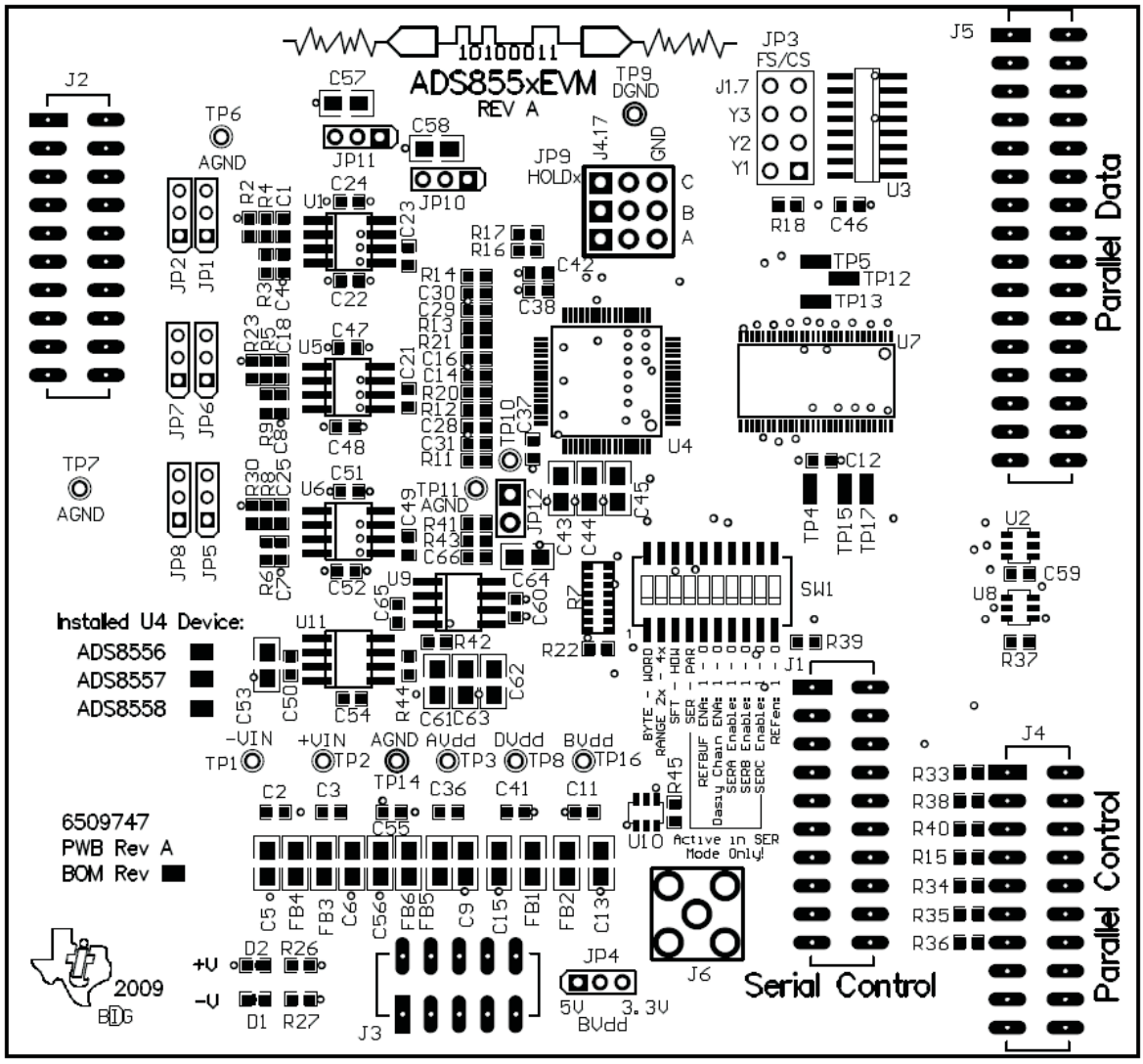

Figure 5. ADS855xEVM Silk Screen Drawing

6.3 Schematic

Revision History		
REV	ECN Number	Approved

Note:
Components marked "NI"
are NOT installed!

Op Amp Bypass
+Vin
C24 0.1uF
TP7
C21 1uF
C22 0.1uF
-Vin

Op Amp Bypass
+Vin
C47 0.1uF
C23 1uF
C48 0.1uF
-Vin

J2
1 2
3 4
5 6
7 8
9 10
11 12
13 14
15 16
17 18
19 20
Analog Input

C1 NI
R2 NI
R4 49.9
-Vin
U1A
JP1
R14 49.9
A0
A0In
R3 49.9
C4 NI
THS4032
+Vin
C30 370pF

C19 NI
R25 NI
R29 49.9
U1B
JP2
R13 49.9
A1
R28 49.9
C20 NI
THS4032
C29 370pF

C18 NI
R23 NI
R5 49.9
-Vin
U5A
JP6
R21 49.9
B0
R9 49.9
C8 NI
THS4032
+Vin
C16 370pF

C27 NI
R31 NI
R1 49.9
U5B
JP7
R20 49.9
B1
R24 49.9
C17 NI
THS4032
C14 370pF

Op Amp Bypass
+Vin
C51 0.1uF
TP6
C49 1uF
C52 0.1uF
-Vin

C25 NI
R30 NI
R8 49.9
-Vin
U6A
JP5
R12 49.9
C0
R6 49.9
C7 NI
THS4032
+Vin
C28 370pF

C26 NI
R32 NI
R19 49.9
U6B
JP8
R11 49.9
C1
R10 49.9
C10 NI
THS4032
C31 370pF

-5VA
FB6
C55 0.1uF
C56 10uF
HVSS
-VIN
JP11
TP1
-VA
R27 2K
FB4
D1 Green
C5 10uF
C2 0.1uF

AVdd
TP3
FB5
+5VA
C9 10uF
C36 0.1uF

+3.3VD +1.8VD +5VA +VA -VA -5VA +VD1 +5VD
J3
1 2
3 4
5 6
7 8
9 10
TP9
TP14

DVdd
TP8
FB1
+5VD
C15 10uF
C41 0.1uF

BVdd
TP16
FB2
+5VD
JP4
+3.3VD
C13 10uF
C11 0.1uF

AVdd HVDD +VIN
JP10
TP2
+VA
R26 2K
FB3
D2 Green
C6 10uF
C3 0.1uF

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: ADS8556 Evaluation Module			
Engineer: Tom Hendrick			
Drawn By: Tom Hendrick	SIZE: B	DATE: 9-Oct-2009	REV: A
FILE: ADS8556_A_SH1.Sch			SHEET: 1 OF: 2

ADC Bypass

AVdd
C40 0.1uF
C35 0.1uF
C34 0.1uF
C33 0.1uF
C32 0.1uF

AVdd
BVdd
BVdd
C39 0.1uF
R40 10K

U4
AVDD AVDD AVDD AVDD AVDD AVDD AVDD AVDD AVDD
60 57 47 46 41 40 35 34 26
BVDD 9

A0 33 CH_A0
32 AGND
A1 36 CH_A1
37 AGND
C43 10uF
54 REFC_A
B0 39 CH_B0
38 AGND
B1 42 CH_B1
43 AGND
C44 10uF
56 REFC_B
C0 45 CH_C0
44 AGND
C1 48 CH_C1
49 AGND
C45 10uF
58 REFC_C

HVSS HVDD
R16 10
31 HVDD
R17 10
30 HVSS
TP10
C57 10uF
C58 10uF
C38 0.1uF
C42 0.1uF
51 REFIO
C37 0.47uF
TP11
AGND AGND AGND AGND AGND AGND
52 53 55 57 59 25
BGND 8

WR/REFen 63 REFen/WR
/RD 20 DC_ARE#
/CS 19 CS#
BUSY 18 DC_INTa
HLDA 23 HOLD_A#
HLDB 22 HOLD_B#
HLDC 21 HOLD_C#
/STBY 24 STBY#
RESET 28 RESET

DB0 17 D0 24
DB1 16 D1 21
DB2 15 D2 18
DB3 14 D3 15
DB4 13 D4 10
DB5 12 D5 7
DB6 11 D6 4
DB7 10 D7 1
DB8 7 D8 54
DB9 6 D9 51
DB10 5 D10 48
DB11 4 D11 45
DB12 3 D12 40
DB13 2 D13 37
DB14 1 D14 34
DB15 64 D15 31

RANGE 27 Range/Extclk
BYTE 29
HW/SW PAR/SER 62
61
ADS8556

SW1
WORD_BYTE 1 20
Range 4x -2x 2 19
HDW - SFT 3 18
PAR - SER 4 17
REFBUFen 5 16
DCen 6 15
SERAen 7 14
SERBen 8 13
SERCen 9 12
REFen 10 11

10K BVdd
R7H
R7G
R7F
R7E
R7D
R7C
R7B
R7A
R22 10K

CS#
STBY#

BVdd
R18 10K
JP3

BVdd
16
C46 0.1uF
U3
15 Y0
14 Y1
13 Y2
12 Y3
11 Y4
10 Y5
9 Y6
7 Y7
VCC
GND
A
B
C
G1
G2A
G2B
1
2
3
6
4
5
SN74AHC138
8

BVdd BVdd BVdd BVdd
R15 10K
R34 10K
R35 10K
R36 10K
R33 10K
DC_A0
DC_A1
DC_A2
DC_A3
DC_CNTL

U7
ADC Data Bus
J5
DC_D0 33 1 2
DC_D1 36 3 4
DC_D2 39 5 6
DC_D3 42 7 8
DC_D4 47 9 10
DC_D5 50 11 12
DC_D6 53 13 14
DC_D7 56 15 16
DC_D8 2 17 18
DC_D9 5 19 20
DC_D10 8 21 22
DC_D11 11 23 24
DC_D12 16 25 26
DC_D13 19 27 28
DC_D14 22 29 30
DC_D15 25 31 32

15A 15B1
13A 13B1
11A 11B1
9A 9B1
7A 7B1
5A 5B1
3A 3B1
1A 1B1
2A 2B1
4A 4B1
6A 6B1
8A 8B1
10A 10B1
12A 12B1
14A 14B1
16A 16B1

15B2 32 SEL_A
13B2 35 SEL_B
11B2 38 SEL_C
SEL1 30
SEL2 29
9B2 41 DCIN_C
7B2 46 DCIN_B
5B2 49 DCIN_A
TEST1 27
TEST2 28
3B2 52
2B2 55 DCen
4B2 3 SDO_A
6B2 6 SDO_B
8B2 9 SDO_C
VCC 14
VCC 43
10B2 12
12B2 17 SDI
GND 44
GND 13
14B2 20
16B2 23 BUFen
26

TP4
TP15
TP17
TP5
TP12
TP13

BVdd
C12 0.1uF
SN74CBT16233
SEL = 0; A = B1
SEL = 1; A = B2

DC_CNTL
DC_AWE
DC_ARE#
DC_A0
DC_A1
DC_A2
DC_A3
DC_TOUT
DC_INTa
J4
Parallel Control

R39 10K
RESET
SCLK
FS/CS
J1
Serial Control

JP9
DC_TOUT
HOLD_C#
HOLD_B#
HOLD_A#

R41 49.9
C66 0.01uF
JP12
U9
R43 100
C64 47nF
R42 10
C62 47nF
C63 47nF
C65 0.01uF
C60 0.1uF
OPA211
AVdd

BVdd
U2
C59 0.1uF
IN2 IN1 IN0 Vcc GND Y
SN74LVC1G97
R37 10K

BVdd
U8
IN2 IN1 IN0 Vcc GND Y
SN74LVC1G97
REFen/WR
BVdd
R38 10K
DC_AWE

U11
AVdd
C50 0.1uF
C53 10uF
DNC DNC VIN N/C TEMP OUT GND TRIM
1 2 3 4 8 7 6 5
REF5025
R44 1
C54 1uF
C61 22uF

BVdd
U10
IN2 IN1 IN0 Vcc GND Y
SN74LVC1G97
Range/Extclk
J6
R45 33

TEXAS INSTRUMENTS
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Title: ADS8556 Evaluation Module			
Engineer: Tom Hendrick			
Drawn By: Tom Hendrick	SIZE: B	DATE: 9-Oct-2009	REV: A
FILE: EDGE # 6509747			SHEET: 2 OF: 2

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