

# NCV4266

## 150 mA Low-Dropout Voltage Regulator with Enable

The NCV4266 is a 150 mA output current integrated low dropout regulator family designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with fixed voltage version of 5.0 V available in 2% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable function for control of the state of the output voltage. The NCV4266 is available in SOT-223 surface mount package. The output is stable over a wide output capacitance and ESR range. The NCV4266 has improved startup behavior during input voltage transients.

### Features

- 5.0 V Output Voltage
- 150 mA Output Current
- 500 mV (max) Dropout Voltage
- Enable Input
- Very Low Current Consumption
- Fault Protection
  - ◆ +45 V Peak Transient Voltage
  - ◆ -42 V Reverse Voltage
  - ◆ Short Circuit
  - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Controls
- These are Pb-Free Devices

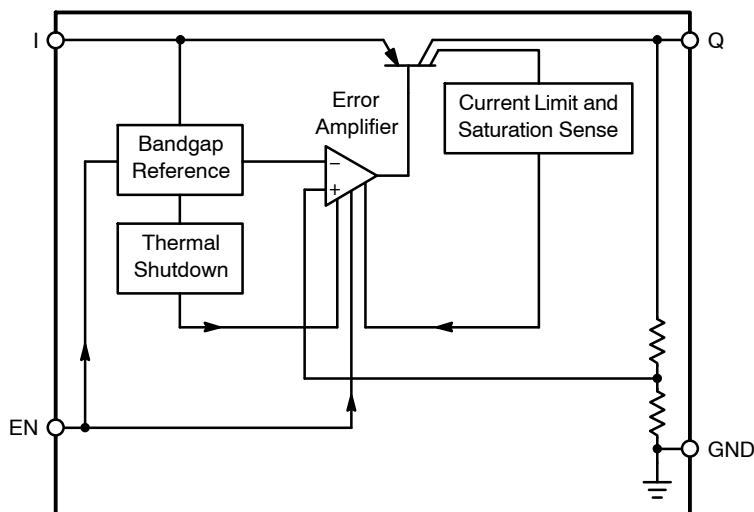


Figure 1. Block Diagram



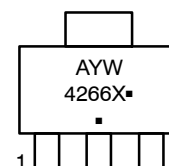
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM



SOT-223  
(TO-261)  
ST SUFFIX  
CASE 318E



A = Assembly Location  
Y = Year  
W = Work Week  
X = Voltage Option  
5.0 V (X = 5)  
▪ = Pb-Free Package

(\*Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 9 of this data sheet.

# NCV4266

## PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	I	Input; Battery Supply Input Voltage.
2	EN	Enable Input; low level disables the IC.
3	Q	Output; Bypass with a capacitor to GND.
4	GND	Ground.

## MAXIMUM RATINGS\*

Rating	Symbol	Min	Max	Unit
Input Voltage	$V_I$	-42	45	V
Input Peak Transient Voltage	$V_I$	-	45	V
Enable Input Voltage	$V_{EN}$	-42	45	V
Output Voltage	$V_Q$	-1.0	40	V
Ground Current	$I_q$	-	100	mA
Input Voltage Operating Range	$V_I$	5.5	40	V
ESD Susceptibility	(Human Body Model)	-	4.0	kV
	(Machine Model)	-	250	V
Junction Temperature	$T_J$	-40	150	°C
Storage Temperature	$T_{stg}$	-50	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

## LEAD TEMPERATURE SOLDERING REFLOW AND MSL (Note 1)

Rating	Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD styles only), Leaded, 60–150 s above 183, 30 s max at peak Reflow (SMD styles only), Free, 60–150 s above 217, 40 s max at peak Wave Solder (through hole styles only), 12 sec max	$T_{SLD}$	-	240 265 310	°C
Moisture Sensitivity Level	MSL	3		-

## THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)		Unit
	Min Pad Board (Note 2)	1" Pad Board (Note 3)	
Junction-to-Tab ( $\psi_{JL4}$ , $\psi_{JL4}$ )	15.7	18	C/W
Junction-to-Ambient ( $R_{\theta JA}$ , $\theta_{JA}$ )	96	77	C/W

- Per IPC / JEDEC J-STD-020C.
- 1 oz. copper, 0.26 inch<sup>2</sup> (168 mm<sup>2</sup>) copper area, 0.062" thick FR4.
- 1 oz. copper, 1.14 inch<sup>2</sup> (736 mm<sup>2</sup>) copper area, 0.062" thick FR4.

# NCV4266

## ELECTRICAL CHARACTERISTICS ( $V_I = 13.5\text{ V}$ ; $-40^\circ\text{C} < T_J < 150^\circ\text{C}$ ; unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>OUTPUT</b>						
Output Voltage	$V_Q$	$5.0\text{ mA} < I_Q < 150\text{ mA}$ , $6\text{ V} < V_I < 28\text{ V}$	4.9	5.0	5.1	V
Output Current Limitation	$I_Q$	$V_Q = 90\% V_{Q\text{TYP}}$	150	200	500	mA
Quiescent Current (Sleep Mode) $I_q = I_I - I_Q$	$I_q$	$V_{\text{EN}} = 0\text{ V}$	-	-	10	$\mu\text{A}$
Quiescent Current, $I_q = I_I - I_Q$	$I_q$	$I_Q = 1.0\text{ mA}$	-	130	200	$\mu\text{A}$
Quiescent Current, $I_q = I_I - I_Q$	$I_q$	$I_Q = 150\text{ mA}$	-	10	15	mA
Dropout Voltage	$V_{\text{DR}}$	$I_Q = 150\text{ mA}$ , $V_{\text{DR}} = V_I - V_Q$	-	250	500	mV
Load Regulation	$\Delta V_{Q,\text{LO}}$	$I_Q = 5.0\text{ mA}$ to $150\text{ mA}$	-	3.0	20	mV
Line Regulation	$\Delta V_Q$	$\Delta V_I = 6.0\text{ V}$ to $28\text{ V}$ , $I_Q = 5.0\text{ mA}$	-	10	25	mV
Power Supply Ripple Rejection	PSRR	$f_r = 100\text{ Hz}$ , $V_r = 0.5\text{ V}_{\text{PP}}$	-	70	-	dB
Temperature Output Voltage Drift	$dV_Q/dT$	-	-	0.5	-	mV/K

## ENABLE INPUT

Enable Voltage, Output High	$V_{\text{EN}}$	$V_Q \geq 4.9\text{ V}$	-	2.3	2.8	V
Enable Voltage, Output Low (Off)	$V_{\text{EN}}$	$V_Q \leq 0.1\text{ V}$	1.8	2.2	-	V
Enable Input Current	$I_{\text{EN}}$	$V_{\text{EN}} = 5.0\text{ V}$	5.0	10	20	$\mu\text{A}$

## THERMAL SHUTDOWN

Thermal Shutdown Temperature*	$T_{\text{SD}}$		150	-	210	$^\circ\text{C}$
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\*Guaranteed by design, not tested in production.

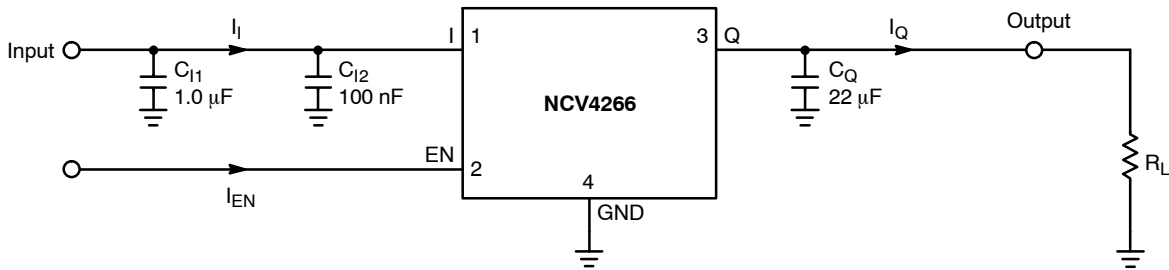


Figure 2. Applications Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

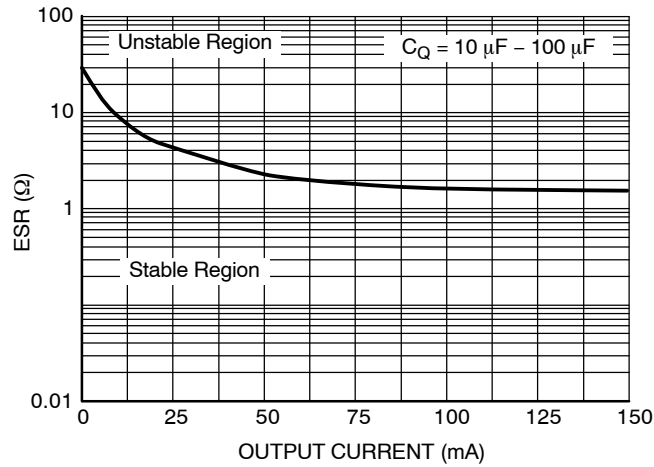


Figure 3. Output Stability with Output Capacitor ESR

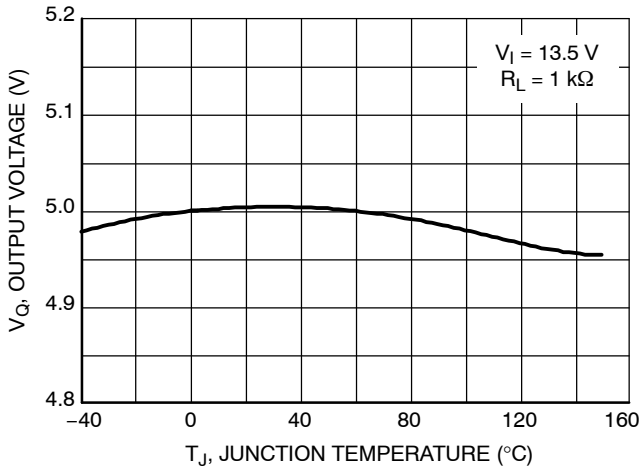


Figure 4. Output Voltage vs. Junction Temperature

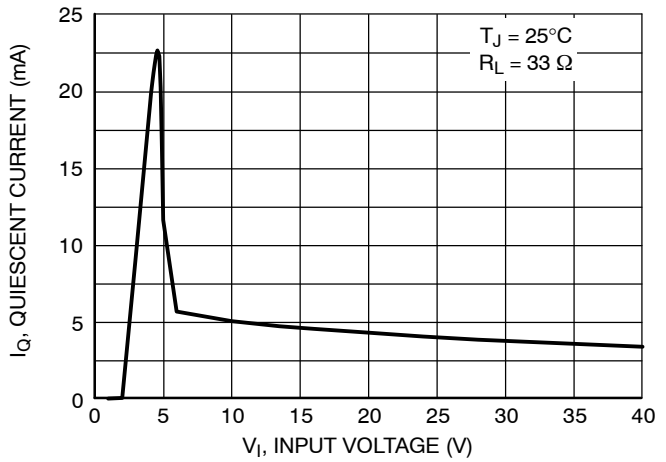


Figure 5. Quiescent Current vs. Input Voltage

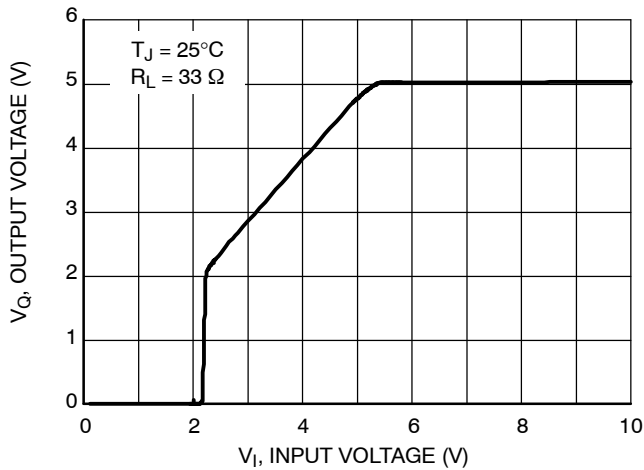


Figure 6. Output Voltage vs. Input Voltage

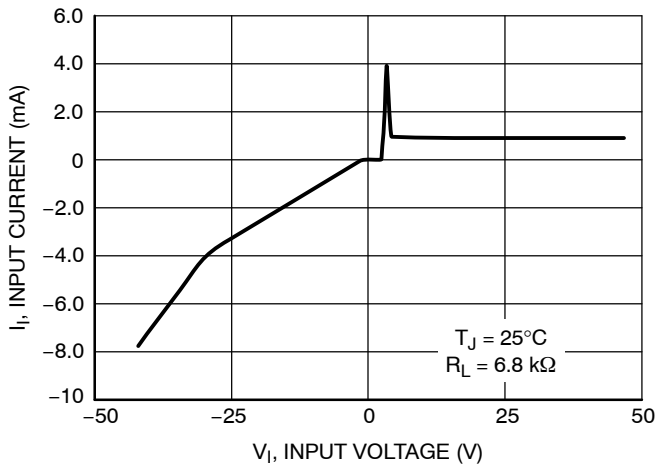


Figure 7. Input Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

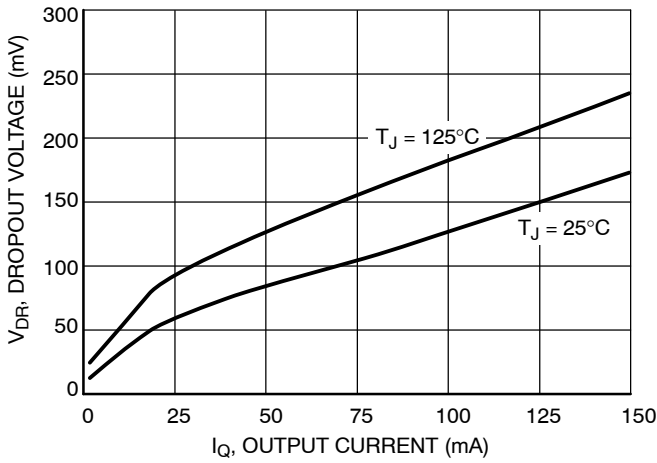


Figure 8. Dropout Voltage vs. Output Current

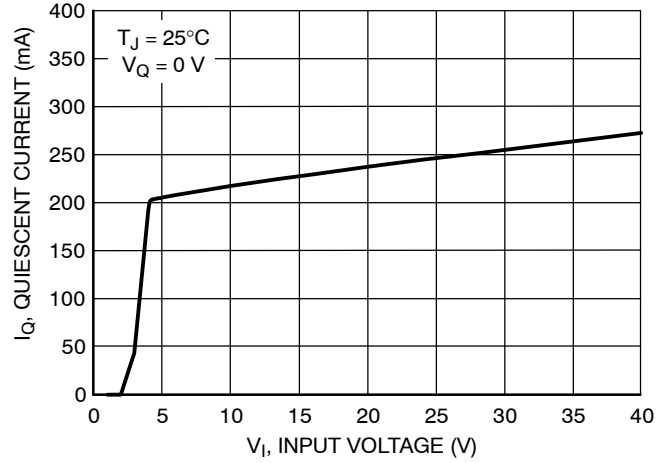


Figure 9. Quiescent Current vs. Input Voltage

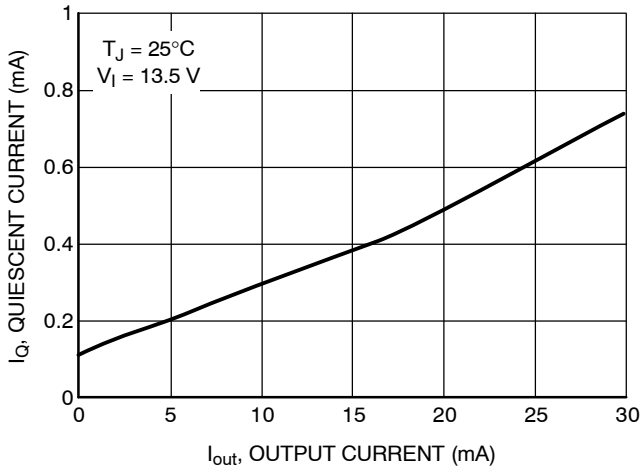


Figure 10. Quiescent Current vs. Input Voltage

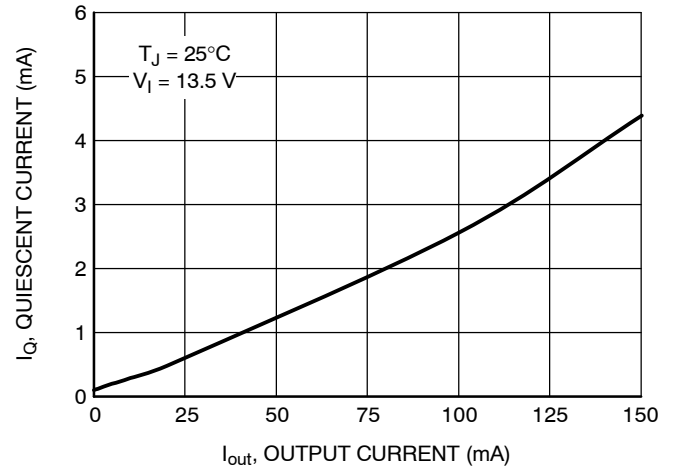


Figure 11. Current Consumption vs. Output Current (Low Load)

## Circuit Description

The NCV4266 is an integrated low dropout regulator that provides a regulated voltage at 150 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 150 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

## Regulator

The error amplifier compares the reference voltage to a sample of the output voltage ( $V_O$ ) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature-stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized. See Figure 2, Test Circuit, for circuit element nomenclature illustration.

## Regulator Stability Considerations

The input capacitors ( $C_{I1}$  and  $C_{I2}$ ) are necessary to stabilize the input impedance to avoid voltage line influences. Using a resistor of approximately 1.0  $\Omega$  in series with  $C_{I2}$  can stop potential oscillations caused by stray inductance and capacitance.

The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load

transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor  $C_O$ , shown in Figure 2, should work for most applications; see also Figure 3 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 3 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

## Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 1.8 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.8 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

**Calculating Power Dissipation in a Single Output Linear Regulator**

The maximum power dissipation for a single output regulator (Figure 12) is:

$$PD(max) = [V_{I(max)} - V_{Q(min)}] I_{Q(max)} + V_{I(max)} I_q \tag{1}$$

where

- $V_{I(max)}$  is the maximum input voltage,
- $V_{Q(min)}$  is the minimum output voltage,
- $I_{Q(max)}$  is the maximum output current for the application,
- $I_q$  is the quiescent current the regulator consumes at  $I_{Q(max)}$ .

Once the value of  $P_{D(max)}$  is known, the maximum permissible value of  $R_{\theta JA}$  can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \tag{2}$$

The value of  $R_{\theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\theta JA}$  less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

**Heatsinks**

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ :

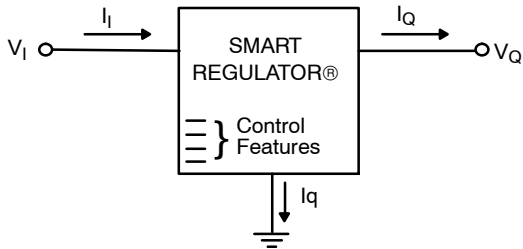
$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \tag{3}$$

where

- $R_{\theta JC}$  is the junction-to-case thermal resistance,
- $R_{\theta CS}$  is the case-to-heatsink thermal resistance,
- $R_{\theta SA}$  is the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$  appears in the package section of the data sheet. Like  $R_{\theta JA}$ , it too is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.



**Figure 12. Single Output Regulator with Key Performance Parameters Labeled**

# NCV4266

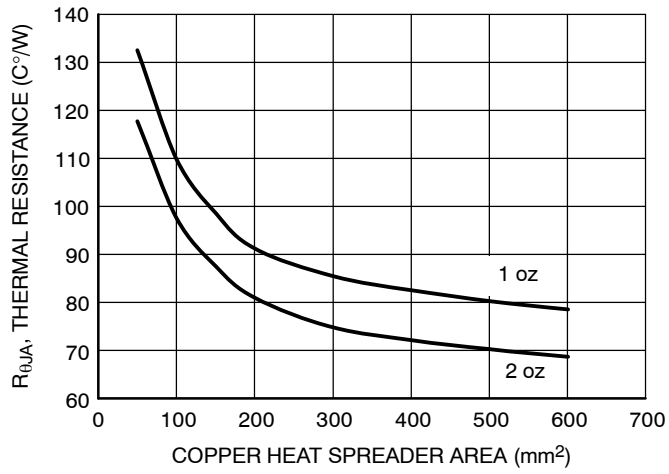


Figure 13. R<sub>θJA</sub> vs. Copper Spreader Area

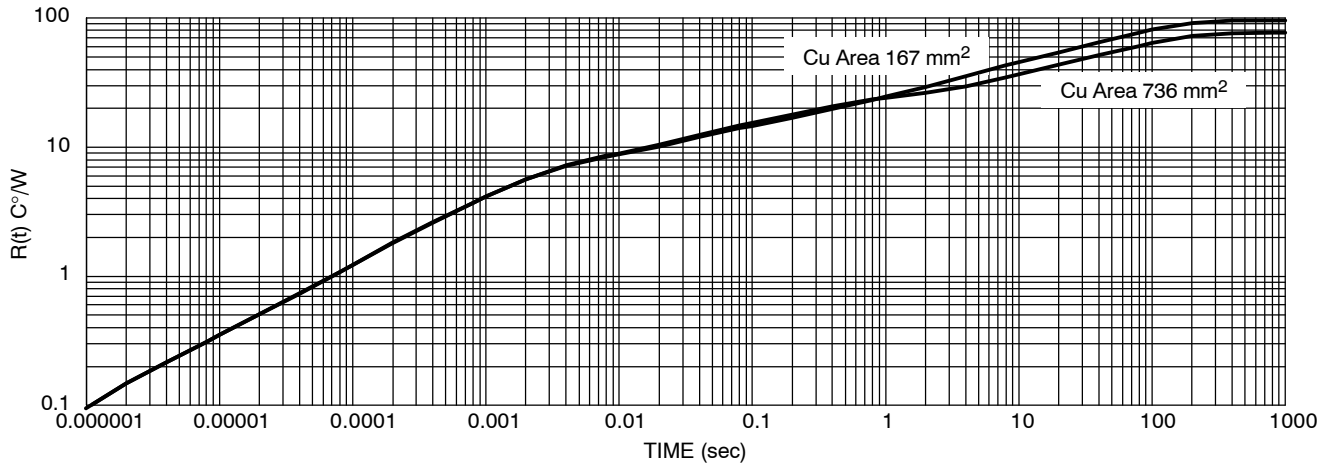


Figure 14. Single-Pulse Heating Curves

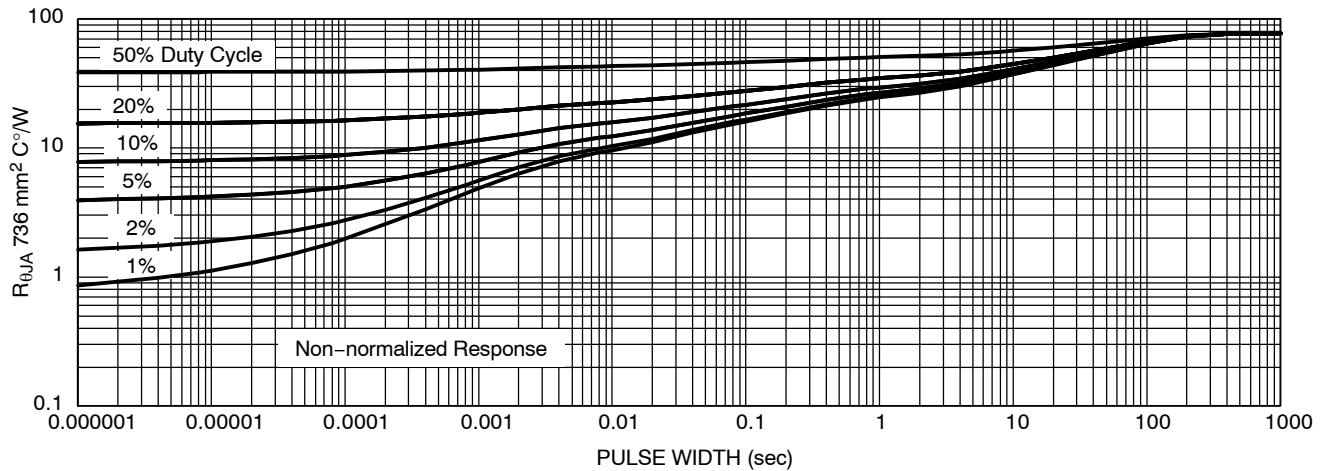


Figure 15. Duty Cycle for 1" Spreader Boards



# NCV4266

## ORDERING INFORMATION

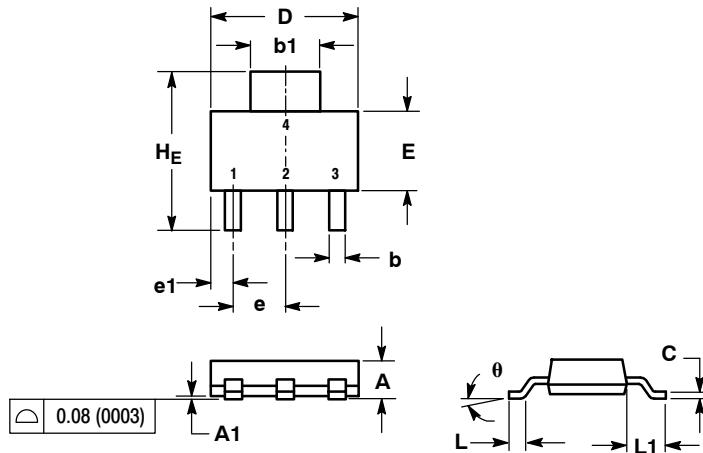
Device	Output Voltage	Package	Shipping†
NCV4266ST50T3G	5.0 V	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCV4266

## PACKAGE DIMENSIONS

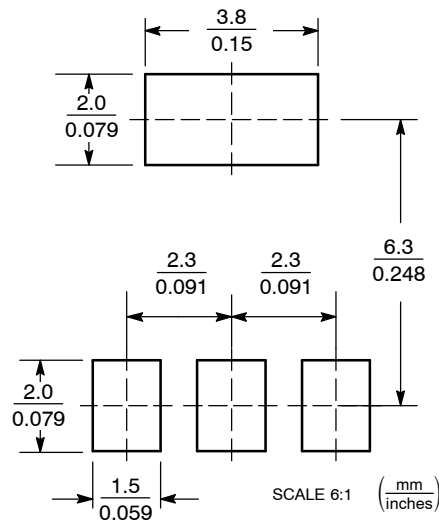
SOT-223 (TO-261)  
CASE 318E-04  
ISSUE N



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.  
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
$\theta$	0°	---	10°	0°	---	10°

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