

## 18-Mbit (512 K × 36/1 M × 18) Flow-through SRAM with NoBL™ Architecture

### Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133-MHz bus operations with zero wait states
  - Data is transferred on every clock
- Pin-compatible and functionally equivalent to ZBT™ devices
- Internally self-timed output buffer control to eliminate the need to use OE
- Registered inputs for flow through operation
- Byte write capability
- 3.3 V/2.5 V I/O power supply ( $V_{DDQ}$ )
- Fast clock-to-output times
  - 6.5 ns (for 133-MHz device)
- Clock enable ( $\overline{CEN}$ ) pin to enable clock and suspend operation
- Synchronous self-timed writes
- Asynchronous output enable
- Available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non Pb-free 119-ball BGA, and 165-ball FBGA packages
- Three chip enables for simple depth expansion
- Automatic power-down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG-compatible boundary scan
- Burst capability — linear or interleaved burst order
- Low standby power

### Selection Guide

Description	133 MHz	100 MHz	Unit
Maximum access time	6.5	8.5	ns
Maximum operating current	210	175	mA
Maximum CMOS standby current	70	70	mA

### Functional Description

The CY7C1371D/CY7C1373D<sup>[1]</sup> is a 3.3 V, 512 K × 36/1 M × 18 synchronous flow through burst SRAM designed specifically to support unlimited true back-to-back read/write operations with no wait state insertion. The CY7C1371D/CY7C1373D is equipped with the advanced No Bus Latency (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable ( $\overline{CEN}$ ) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133-MHz device).

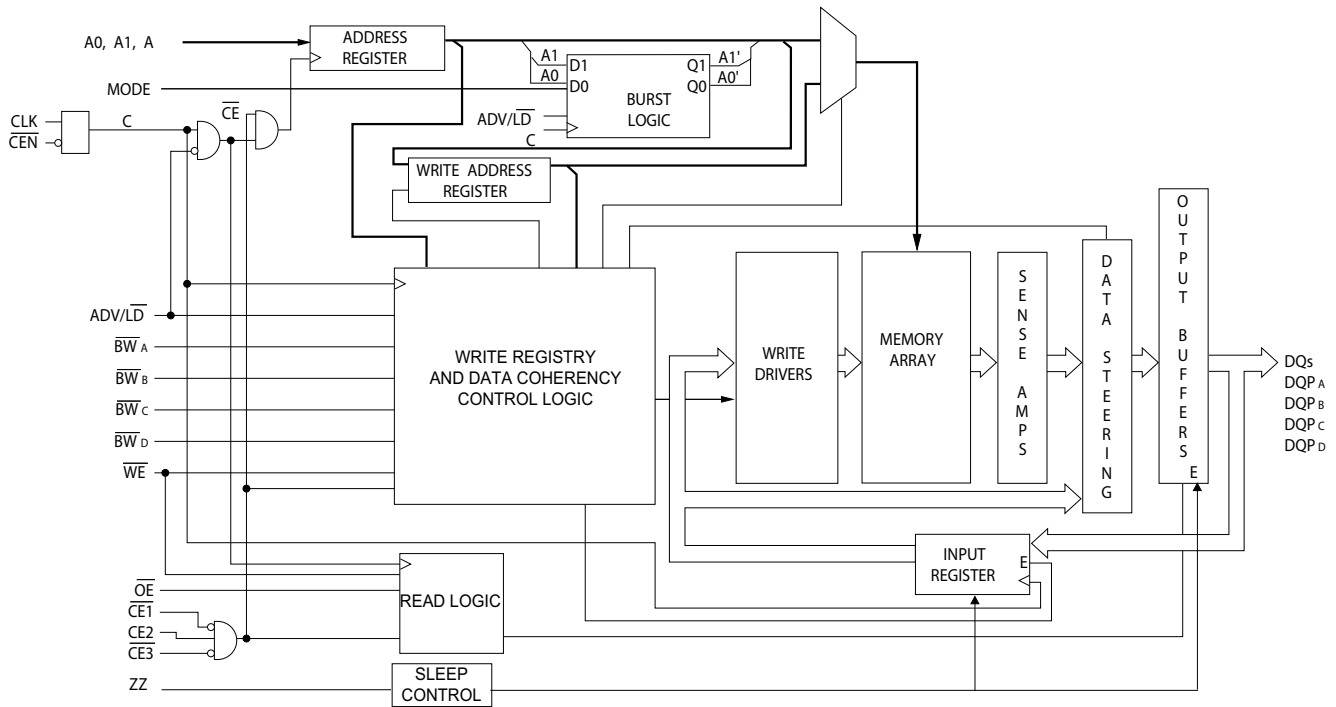
Write operations are controlled by the two or four byte write select ( $BW_X$ ) and a write enable ( $\overline{WE}$ ) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ ,  $\overline{CE}_3$ ) and an asynchronous output enable ( $\overline{OE}$ ) provide for easy bank selection and output tristate control. To avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

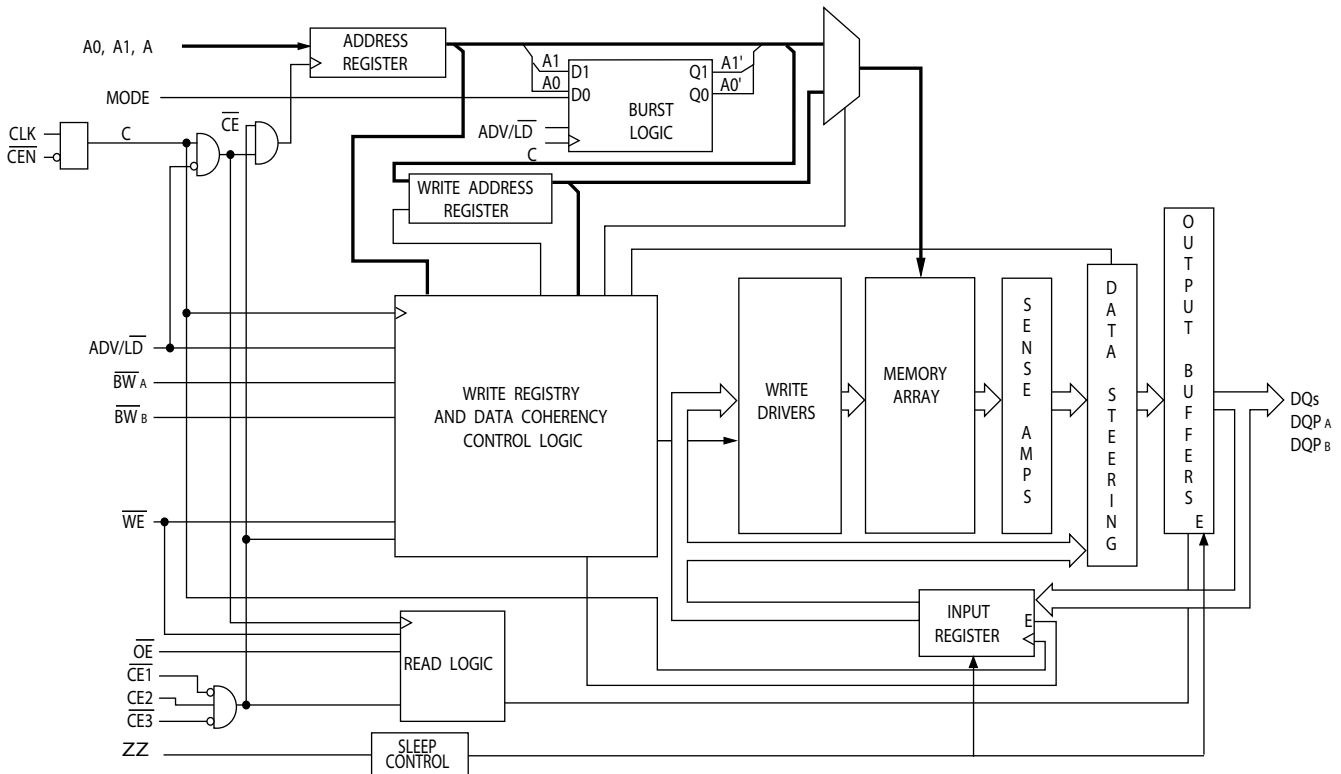
#### Note

1. For best practice recommendations, refer to [SRAM System Guidelines](#).

**Logic Block Diagram – CY7C1371D (512 K × 36)**



**Logic Block Diagram – CY7C1373D (1 M × 18)**

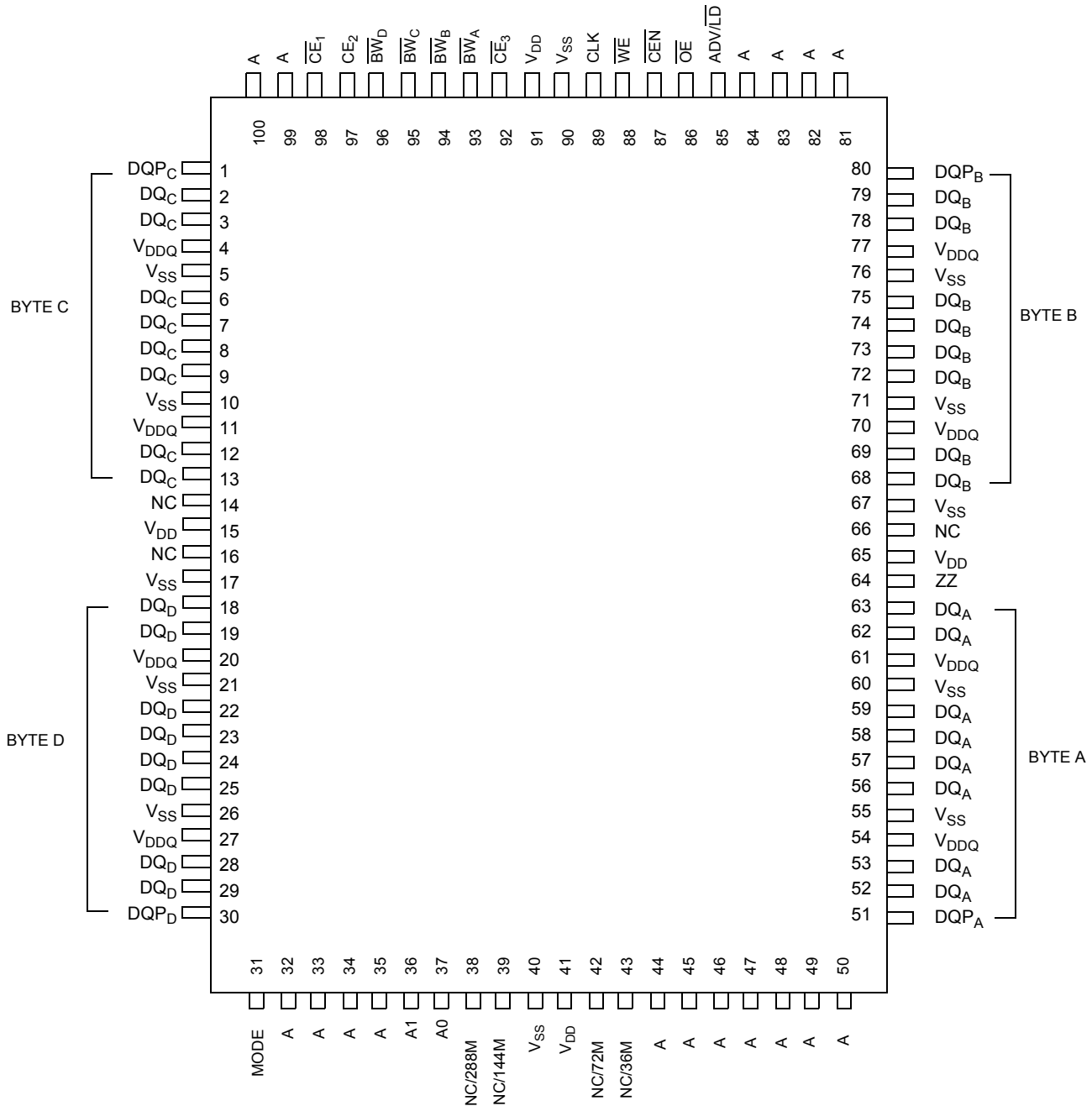


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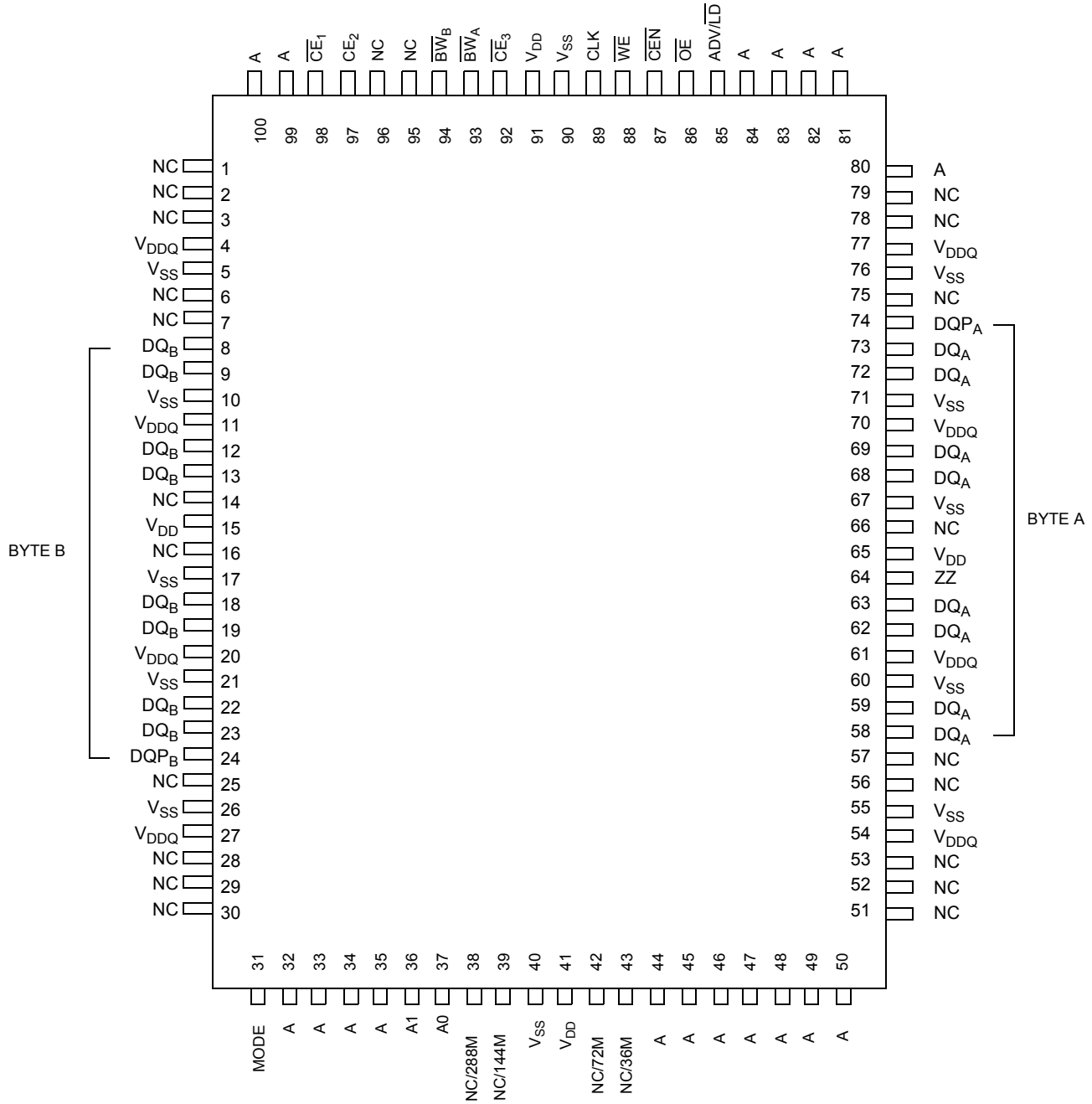
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## Pin Configurations

Figure 1. 100-pin TQFP Pinout (CY7C1371D)



**Figure 2. 100-pin TQFP Pinout (CY7C1373D)**



**Figure 3. 119-Ball BGA Pinout**

**CY7C1371D (512 K × 36)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	A	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/576M	CE <sub>2</sub>	A	ADV/LD	A	CE <sub>3</sub>	NC
<b>C</b>	NC/1G	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>C</sub>	DQP <sub>C</sub>	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	CE <sub>1</sub>	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	V <sub>DDQ</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	OE	V <sub>SS</sub>	DQ <sub>B</sub>	V <sub>DDQ</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	BW <sub>C</sub>	A	BW <sub>B</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>SS</sub>	WE	V <sub>SS</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	BW <sub>D</sub>	NC	BW <sub>A</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	CEN	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>P</b>	DQ <sub>D</sub>	DQP <sub>D</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	DQP <sub>A</sub>	DQ <sub>A</sub>
<b>R</b>	NC/144M	A	MODE	V <sub>DD</sub>	NC	A	NC/288M
<b>T</b>	NC	NC/72M	A	A	A	NC/36M	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**CY7C1373D (1 M × 18)**

	1	2	3	4	5	6	7
<b>A</b>	V <sub>DDQ</sub>	A	A	A	A	A	V <sub>DDQ</sub>
<b>B</b>	NC/576M	CE <sub>2</sub>	A	ADV/LD	A	CE <sub>3</sub>	NC
<b>C</b>	NC/1G	A	A	V <sub>DD</sub>	A	A	NC
<b>D</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	NC	V <sub>SS</sub>	DQP <sub>A</sub>	NC
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CE <sub>1</sub>	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>F</b>	V <sub>DDQ</sub>	NC	V <sub>SS</sub>	OE	V <sub>SS</sub>	DQ <sub>A</sub>	V <sub>DDQ</sub>
<b>G</b>	NC	DQ <sub>B</sub>	BW <sub>B</sub>	A	NC	NC	DQ <sub>A</sub>
<b>H</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	WE	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>J</b>	V <sub>DDQ</sub>	V <sub>DD</sub>	NC	V <sub>DD</sub>	NC	V <sub>DD</sub>	V <sub>DDQ</sub>
<b>K</b>	NC	DQ <sub>B</sub>	V <sub>SS</sub>	CLK	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>L</b>	DQ <sub>B</sub>	NC	NC	NC	BW <sub>A</sub>	DQ <sub>A</sub>	NC
<b>M</b>	V <sub>DDQ</sub>	DQ <sub>B</sub>	V <sub>SS</sub>	CEN	V <sub>SS</sub>	NC	V <sub>DDQ</sub>
<b>N</b>	DQ <sub>B</sub>	NC	V <sub>SS</sub>	A1	V <sub>SS</sub>	DQ <sub>A</sub>	NC
<b>P</b>	NC	DQP <sub>B</sub>	V <sub>SS</sub>	A0	V <sub>SS</sub>	NC	DQ <sub>A</sub>
<b>R</b>	NC/144M	A	MODE	V <sub>DD</sub>	NC	A	NC/288M
<b>T</b>	NC/72M	A	A	NC/36M	A	A	ZZ
<b>U</b>	V <sub>DDQ</sub>	TMS	TDI	TCK	TDO	NC	V <sub>DDQ</sub>

**Figure 4. 165-Ball FBGA Pinout**

**CY7C1371D (512 K × 36)**

	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>
<b>A</b>	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_C$	$\overline{BW}_B$	$\overline{CE}_3$	$\overline{CEN}$	ADV/LD	A	A	NC
<b>B</b>	NC/1G	A	CE2	$\overline{BW}_D$	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	DQP <sub>C</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>B</sub>
<b>D</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>E</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>F</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>G</b>	DQ <sub>C</sub>	DQ <sub>C</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>B</sub>	DQ <sub>B</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>K</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>L</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>M</b>	DQ <sub>D</sub>	DQ <sub>D</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	DQ <sub>A</sub>
<b>N</b>	DQP <sub>D</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>P</b>	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

**CY7C1373D (1 M × 18)**

	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>
<b>A</b>	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_B$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/LD	A	A	A
<b>B</b>	NC/1G	A	CE2	NC	$\overline{BW}_A$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
<b>C</b>	NC	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	DQP <sub>A</sub>
<b>D</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>E</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>F</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>G</b>	NC	DQ <sub>B</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	DQ <sub>A</sub>
<b>H</b>	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	ZZ
<b>J</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>K</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>L</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>M</b>	DQ <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	DQ <sub>A</sub>	NC
<b>N</b>	DQP <sub>B</sub>	NC	V <sub>DDQ</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC
<b>P</b>	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
<b>R</b>	MODE	NC/36M	A	A	TMS	A0	TCK	A	A	A	A

## Pin Definitions

Name	I/O	Description
A <sub>0</sub> , A <sub>1</sub> , A	Input-synchronous	<b>Address inputs used to select one of the address locations.</b> Sampled at the rising edge of the CLK. A <sub>[1:0]</sub> are fed to the two-bit burst counter.
$\overline{BW}_A$ , $\overline{BW}_B$ $\overline{BW}_C$ , $\overline{BW}_D$	Input-synchronous	<b>Byte write inputs, active LOW.</b> Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{WE}$	Input-synchronous	<b>Write enable input, active LOW.</b> Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/ $\overline{LD}$	Input-synchronous	<b>Advance/load input.</b> Used to advance the on-chip address counter or load a new address. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/ $\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-clock	<b>Clock input.</b> Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$ . CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-synchronous	<b>Chip enable 1 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_2$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_2$	Input-synchronous	<b>Chip enable 2 input, active HIGH.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-synchronous	<b>Chip enable 3 input, active LOW.</b> Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_2$ to select/deselect the device.
$\overline{OE}$	Input-asynchronous	<b>Output enable, asynchronous input, active LOW.</b> Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
$\overline{CEN}$	Input-synchronous	<b>Clock enable input, active LOW.</b> When asserted LOW the Clock signal is recognized by the SRAM. When deasserted HIGH the Clock signal is masked. While deasserting $\overline{CEN}$ does not deselect the device, use $\overline{CEN}$ to extend the previous cycle when required.
ZZ	Input-asynchronous	<b>ZZ “sleep” input.</b> This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull-down.
DQ <sub>s</sub>	I/O-synchronous	<b>Bidirectional data I/O lines.</b> As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ . When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ <sub>s</sub> and DQP <sub>[A:D]</sub> are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$ .
DQP <sub>x</sub>	I/O-synchronous	<b>Bidirectional data parity I/O lines.</b> Functionally, these signals are identical to DQ <sub>s</sub> .
MODE	Input strap pin	<b>Mode input. Selects the burst order of the device.</b> When tied to Gnd selects linear burst sequence. When tied to V <sub>DD</sub> or left floating selects interleaved burst sequence.
V <sub>DD</sub>	Power supply	<b>Power supply inputs to the core of the device.</b>
V <sub>DDQ</sub>	I/O power supply	<b>Power supply for the I/O circuitry.</b>
V <sub>SS</sub>	Ground	<b>Ground for the device.</b>



**Pin Definitions** (continued)

Name	I/O	Description
TDO	JTAG serial output synchronous	<b>Serial data-out to the JTAG circuit.</b> Delivers data on the negative edge of TCK. If the JTAG feature is not being used, this pin must be left unconnected. This pin is not available on TQFP packages.
TDI	JTAG serial input synchronous	<b>Serial data-in to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be left floating or connected to V <sub>DD</sub> through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG serial input synchronous	<b>Serial data-in to the JTAG circuit.</b> Sampled on the rising edge of TCK. If the JTAG feature is not being used, this pin can be disconnected or connected to V <sub>DD</sub> . This pin is not available on TQFP packages.
TCK	JTAG-clock	<b>Clock input to the JTAG circuitry.</b> If the JTAG feature is not being used, this pin must be connected to V <sub>SS</sub> . This pin is not available on TQFP packages.
NC	–	<b>No connects.</b> Not internally connected to the die. NC/(36 M, 72 M, 144 M, 288M, 576M, 1G) are address expansion pins and are not internally connected to the die.

**Functional Overview**

The CY7C1371D/CY7C1373D is a synchronous flow through burst SRAM designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. Maximum access delay from the clock rise (t<sub>CDV</sub>) is 6.5 ns (133-MHz device).

Accesses can be initiated by asserting all three chip enables (CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub>) active at the rising edge of the clock. If clock enable (CEN) is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable (WE). BW<sub>X</sub> can be used to conduct byte write operations.

Write operations are qualified by the write enable (WE). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables (CE<sub>1</sub>, CE<sub>2</sub>, CE<sub>3</sub>) and an asynchronous output enable (OE) simplify depth expansion. All operations (reads, writes, and deselected) are pipelined. ADV/LD must be driven LOW after the device has been deselected to load a new address for the next operation.

**Single Read Accesses**

A read access is initiated when these conditions are satisfied at clock rise:

- CEN is asserted LOW
- CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub> are all asserted active
- The write enable input signal WE is deasserted HIGH
- ADV/LD is asserted LOW.

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133-MHz

device) provided OE is active LOW. After the first clock of the read access, the output buffers are controlled by OE and the internal control logic. OE must be driven LOW in order for the device to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tristated immediately.

**Burst Read Accesses**

The CY7C1371D/CY7C1373D has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in the [Single Read Accesses](#) section above. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A<sub>0</sub> and A<sub>1</sub> in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enable inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

**Single Write Accesses**

Write access are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE<sub>1</sub>, CE<sub>2</sub>, and CE<sub>3</sub> are all asserted active, and (3) the write signal WE is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tristated regardless of the state of the OE input signal. This allows the external logic to present the data on DQs and DQP<sub>X</sub>.

On the next clock rise the data presented to DQs and DQP<sub>X</sub> (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by BW<sub>X</sub> signals. The CY7C1371D/CY7C1373D provides byte write capability that is described in the truth table. Asserting the write

enable input ( $\overline{WE}$ ) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1371D/CY7C1373D is a common I/O device, data must not be driven into the device while the outputs are active. The output enable ( $\overline{OE}$ ) can be deasserted HIGH before presenting data to the DQs and DQP<sub>X</sub> inputs. Doing so tristates the output drivers. As a safety precaution, DQs and DQP<sub>X</sub> are automatically tristated during the data portion of a write cycle, regardless of the state of OE.

### Burst Write Accesses

The CY7C1371D/CY7C1373D has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the [Single Write Accesses](#) section above. When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ ) and WE inputs are ignored and the burst counter is incremented. The correct BW<sub>X</sub> inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

### Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses

pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode.  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$ , must remain inactive for the duration of  $t_{ZZREC}$  after the ZZ input returns LOW.

### Interleaved Burst Address Table (MODE = Floating or V<sub>DD</sub>)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

### Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

## ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
$I_{DDZZ}$	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	80	mA
$t_{ZZS}$	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
$t_{ZZREC}$	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
$t_{ZZI}$	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
$t_{RZZI}$	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

**Truth Table**<sup>[2, 3, 4, 5, 6, 7, 8]</sup>

Operation	Address Used	$\overline{CE}_1$	$CE_2$	$\overline{CE}_3$	ZZ	ADV/LD	$\overline{WE}$	$\overline{BW}_X$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tristate
Deselect cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tristate
Deselect cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tristate
Continue deselect cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tristate
Read cycle (begin burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data out (Q)
Read cycle (continue burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data out (Q)
NOP/dummy read (begin burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tristate
Dummy read (continue burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tristate
Write cycle (begin burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data in (D)
Write cycle (continue burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data in (D)
NOP/write abort (begin burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tristate
Write abort (continue burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tristate
Ignore clock edge (stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep mode	None	X	X	X	H	X	X	X	X	X	X	Tristate

**Partial Truth Table for Read/Write**<sup>[2, 3, 9]</sup>

Function (CY7C1371D)	$\overline{WE}$	$\overline{BW}_A$	$\overline{BW}_B$	$\overline{BW}_C$	$\overline{BW}_D$
Read	H	X	X	X	X
Write no bytes written	L	H	H	H	H
Write byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	L	L	H	H	H
Write byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	L	H	L	H	H
Write byte C – (DQ <sub>C</sub> and DQP <sub>C</sub> )	L	H	H	L	H
Write byte D – (DQ <sub>D</sub> and DQP <sub>D</sub> )	L	H	H	H	L
Write all Bytes	L	L	L	L	L

**Partial Truth Table for Read/Write**<sup>[2, 3, 9]</sup>

Function (CY7C1373D)	$\overline{WE}$	$\overline{BW}_A$	$\overline{BW}_B$
Read	H	X	X
Write - no bytes written	L	H	H
Write byte A – (DQ <sub>A</sub> and DQP <sub>A</sub> )	L	L	H
Write byte B – (DQ <sub>B</sub> and DQP <sub>B</sub> )	L	H	L
Write all bytes	L	L	L

**Notes**

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.  $\overline{BW}_X = 0$  signifies at least one byte write select is active,  $\overline{BW}_X = \text{valid}$  signifies that the desired byte write selects are asserted, see truth table for details.
- Write is defined by  $\overline{BW}_X$ , and  $\overline{WE}$ . See truth table for read/write.
- When a write cycle is detected, all I/Os are tristated, even during byte writes.
- The DQs and DQP<sub>X</sub> pins are controlled by the current cycle and the  $\overline{OE}$  signal.  $\overline{OE}$  is asynchronous and is not sampled with the clock.
- $\overline{CEN} = H$ , inserts wait states.
- Device powers up deselected and the I/Os in a tristate condition, regardless of  $\overline{OE}$ .
- $\overline{OE}$  is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP<sub>X</sub> = tristate when  $\overline{OE}$  is inactive or when the device is deselected, and DQs and DQP<sub>X</sub> = data when  $\overline{OE}$  is active.
- Table only lists a partial listing of the byte write combinations. Any Combination of  $\overline{BW}_X$  is valid. Appropriate write is based on which byte write is active.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

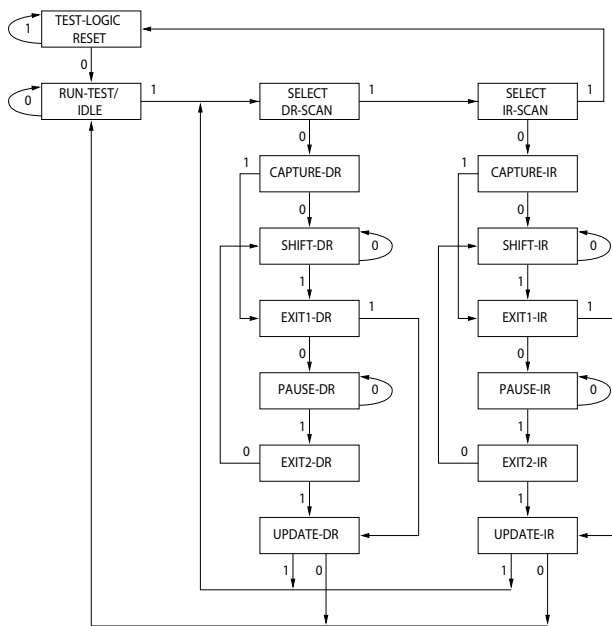
The CY7C1371D/CY7C1373D incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V or 2.5 V I/O logic levels.

The CY7C1371D/CY7C1373D contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to  $V_{DD}$  through a pull up resistor. TDO must be left unconnected. Upon power-up, the device is up in a reset state which does not interfere with the operation of the device.

### TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

### Test Access Port (TAP)

#### Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

#### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

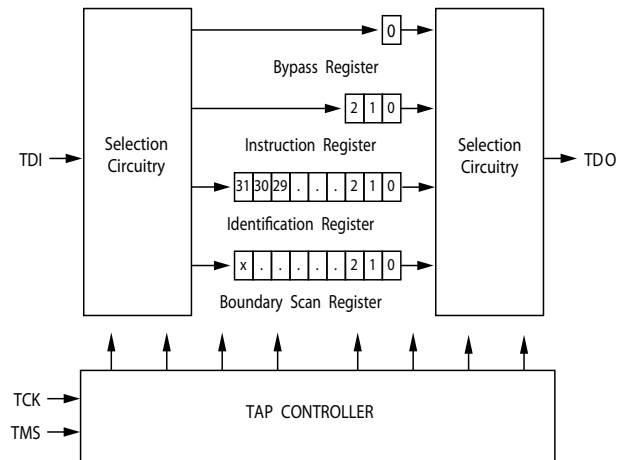
#### Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See [TAP Controller Block Diagram](#).)

#### Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See [TAP Controller State Diagram](#).)

### TAP Controller Block Diagram



### Performing a TAP Reset

A RESET is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high Z state.

### TAP Registers

Registers are connected between the TDI and TDO balls and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

#### Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the [TAP Controller Block Diagram](#). Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test data path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

### **TAP Instruction Set**

#### *Overview*

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller needs to be moved into the Update-IR state.

#### *EXTEST*

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

#### *IDCODE*

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is supplied a test logic reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO balls when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a high Z state.

#### *SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

#### *BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

### EXTEST Output Bus Tristate

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tristate mode.

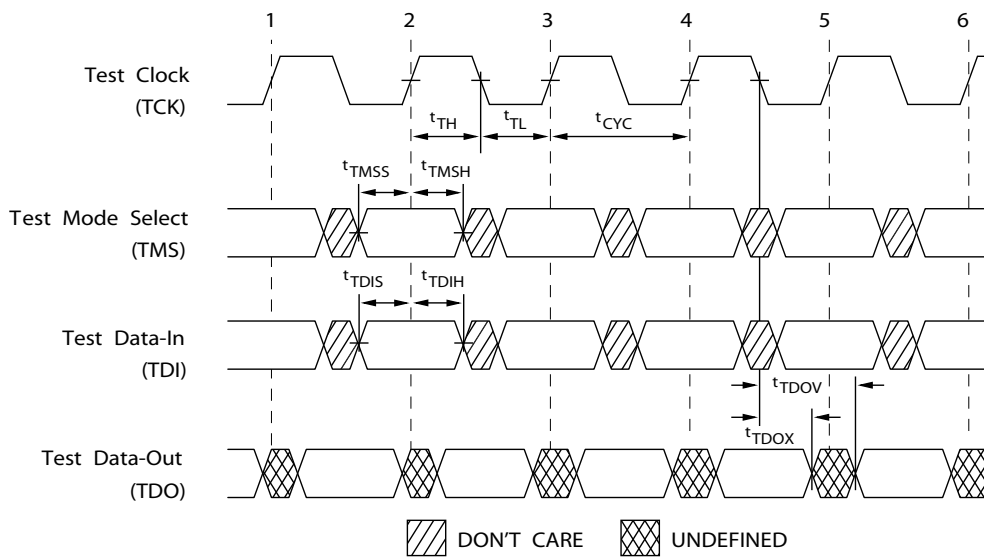
The boundary scan register has a special bit located at bit #85 (for 119-BGA package) or bit #89 (for 165-FBGA package). When this scan cell, called the “extest output bus tristate,” is latched into the preload register during the “Update-DR” state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a high Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the “Shift-DR” state. During “Update-DR,” the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is preset HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the “Test-Logic-Reset” state.

### Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

### TAP Timing



## TAP AC Switching Characteristics

Over the Operating Range<sup>[10, 11]</sup>

Parameter	Description	Min	Max	Unit
<b>Clock</b>				
$t_{TCYC}$	TCK clock cycle time	50	–	ns
$t_{TF}$	TCK clock frequency	–	20	MHz
$t_{TH}$	TCK clock HIGH time	20	–	ns
$t_{TL}$	TCK clock LOW time	20	–	ns
<b>Output Times</b>				
$t_{TDOV}$	TCK clock LOW to TDO valid	–	10	ns
$t_{TDOX}$	TCK clock LOW to TDO invalid	0	–	ns
<b>Setup Times</b>				
$t_{TMSS}$	TMS setup to TCK clock rise	5	–	ns
$t_{TDIS}$	TDI setup to TCK clock rise	5	–	ns
$t_{CS}$	Capture setup to TCK rise	5	–	ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK clock rise	5	–	ns
$t_{TDIH}$	TDI Hold after clock rise	5	–	ns
$t_{CH}$	Capture hold after clock rise	5	–	ns

### Notes

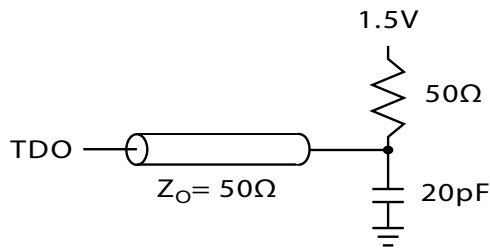
10.  $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.

11. Test conditions are specified using the load in TAP AC test Conditions.  $t_R/t_F = 1$  ns.

### 3.3 V TAP AC Test Conditions

Input pulse levels..... $V_{SS}$  to 3.3 V  
 Input rise and fall times..... 1 ns  
 Input timing reference levels..... 1.5 V  
 Output reference levels ..... 1.5 V  
 Test load termination supply voltage ..... 1.5 V

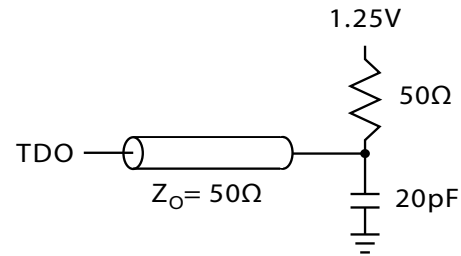
### 3.3 V TAP AC Output Load Equivalent



### 2.5 V TAP AC Test Conditions

Input pulse level..... $V_{SS}$  to 2.5 V  
 Input rise and fall time ..... 1 ns  
 Input timing reference levels..... 1.25 V  
 Output reference levels ..... 1.25 V  
 Test load termination supply voltage ..... 1.25 V

### 2.5 V TAP AC Output Load Equivalent



## TAP DC Electrical Characteristics and Operating Conditions

(0 °C < T<sub>A</sub> < +70 °C; V<sub>DD</sub> = 3.3 V ± 0.165 V unless otherwise noted)<sup>[12]</sup>

Parameter	Description	Description	Conditions	Min	Max	Unit
V <sub>OH1</sub>	Output HIGH voltage	I <sub>OH</sub> = -4.0 mA	V <sub>DDQ</sub> = 3.3 V	2.4	-	V
		I <sub>OH</sub> = -1.0 mA	V <sub>DDQ</sub> = 2.5 V	2.0	-	V
V <sub>OH2</sub>	Output HIGH voltage	I <sub>OH</sub> = -100 μA	V <sub>DDQ</sub> = 3.3 V	2.9	-	V
			V <sub>DDQ</sub> = 2.5 V	2.1	-	V
V <sub>OL1</sub>	Output LOW voltage	I <sub>OL</sub> = 8.0 mA	V <sub>DDQ</sub> = 3.3 V	-	0.4	V
		I <sub>OL</sub> = 1.0 mA	V <sub>DDQ</sub> = 2.5 V	-	0.4	V
V <sub>OL2</sub>	Output LOW voltage	I <sub>OL</sub> = 100 μA	V <sub>DDQ</sub> = 3.3 V	-	0.2	V
			V <sub>DDQ</sub> = 2.5 V	-	0.2	V
V <sub>IH</sub>	Input HIGH voltage		V <sub>DDQ</sub> = 3.3 V	2.0	V <sub>DD</sub> + 0.3	V
			V <sub>DDQ</sub> = 2.5 V	1.7	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage		V <sub>DDQ</sub> = 3.3 V	-0.5	0.7	V
			V <sub>DDQ</sub> = 2.5 V	-0.3	0.7	V
I <sub>X</sub>	Input load current	GND ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub>		-5	5	μA

**Note**  
12. All voltages referenced to V<sub>SS</sub> (GND).



## Identification Register Definitions

Instruction Field	CY7C1371D (512 K × 36)	CY7C1373D (1 M × 18)	Description
Revision number (31:29)	000	000	Describes the version number
Device depth (28:24)	01011	01011	Reserved for internal use
Device width (23:18)	001001	001001	Defines memory type and architecture
Cypress device ID (17:12)	100101	010101	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor
ID register presence indicator (0)	1	1	Indicates the presence of an ID register

## Scan Register Sizes

Register Name	Bit Size (× 36)	Bit Size (× 18)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan Order (119-ball BGA package)	85	85
Boundary Scan Order (165-ball FBGA package)	89	89

## Identification Codes

Instruction	Code	Description
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to high Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a high Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

**119-ball BGA Boundary Scan Order** <sup>[13, 14]</sup>

Bit #	Ball ID
1	H4
2	T4
3	T5
4	T6
5	R5
6	L5
7	R6
8	U6
9	R7
10	T7
11	P6
12	N7
13	M6
14	L7
15	K6
16	P7
17	N6
18	L6
19	K7
20	J5
21	H6
22	G7

Bit #	Ball ID
23	F6
24	E7
25	D7
26	H7
27	G6
28	E6
29	D6
30	C7
31	B7
32	C6
33	A6
34	C5
35	B5
36	G5
37	B6
38	D4
39	B4
40	F4
41	M4
42	A5
43	K4
44	E4

Bit #	Ball ID
45	G4
46	A4
47	G3
48	C3
49	B2
50	B3
51	A3
52	C2
53	A2
54	B1
55	C1
56	D2
57	E1
58	F2
59	G1
60	H2
61	D1
62	E2
63	G2
64	H1
65	J3
66	2K

Bit #	Ball ID
67	L1
68	M2
69	N1
70	P1
71	K1
72	L2
73	N2
74	P2
75	R3
76	T1
77	R1
78	T2
79	L3
80	R2
81	T3
82	L4
83	N4
84	P4
85	Internal

**Notes**

- 13. Balls which are NC (No Connect) are pre-set LOW.
- 14. Bit# 85 is pre-set HIGH.

**165-ball BGA Boundary Scan Order** <sup>[15, 16]</sup>

Bit #	Ball ID
1	N6
2	N7
3	N10
4	P11
5	P8
6	R8
7	R9
8	P9
9	P10
10	R10
11	R11
12	H11
13	N11
14	M11
15	L11
16	K11
17	J11
18	M10
19	L10
20	K10
21	J10
22	H9
23	H10
24	G11
25	F11
26	E11
27	D11
28	G10
29	F10
30	E10

Bit #	Ball ID
31	D10
32	C11
33	A11
34	B11
35	A10
36	B10
37	A9
38	B9
39	C10
40	A8
41	B8
42	A7
43	B7
44	B6
45	A6
46	B5
47	A5
48	A4
49	B4
50	B3
51	A3
52	A2
53	B2
54	C2
55	B1
56	A1
57	C1
58	D1
59	E1
60	F1

Bit #	Ball ID
61	G1
62	D2
63	E2
64	F2
65	G2
66	H1
67	H3
68	J1
69	K1
70	L1
71	M1
72	J2
73	K2
74	L2
75	M2
76	N1
77	N2
78	P1
79	R1
80	R2
81	P3
82	R3
83	P2
84	R4
85	P4
86	N5
87	P6
88	R6
89	Internal

**Note**  
15. Balls which are NC (No Connect) are pre-set LOW.  
16. Bit# 89 is pre-set HIGH.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature with power applied ..... -55 °C to +125 °C  
 Supply voltage on V<sub>DD</sub> relative to GND ..... -0.5 V to +4.6 V  
 Supply voltage on V<sub>DDQ</sub> relative to GND ..... -0.5 V to +V<sub>DD</sub>  
 DC voltage applied to outputs in tristate ..... -0.5 V to V<sub>DDQ</sub> + 0.5 V

DC input voltage ..... -0.5 V to V<sub>DD</sub> + 0.5 V  
 Current into outputs (LOW) ..... 20 mA  
 Static discharge voltage..... > 2001 V (MIL-STD-883, method 3015)  
 Latch up current..... > 200 mA

## Operating Range

Range	Ambient Temperature	V <sub>DD</sub>	V <sub>DDQ</sub>
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V <sub>DD</sub>
Industrial	-40 °C to +85 °C		

## Electrical Characteristics

Over the Operating Range<sup>[17, 18]</sup>

Parameter	Description	Test Conditions	Min	Max	Unit	
V <sub>DD</sub>	Power supply voltage		3.135	3.6	V	
V <sub>DDQ</sub>	I/O supply voltage	For 3.3 V I/O	3.135	V <sub>DD</sub>	V	
		For 2.5 V I/O	2.375	2.625	V	
V <sub>OH</sub>	Output HIGH voltage	For 3.3 V I/O, I <sub>OH</sub> = -4.0 mA	2.4	-	V	
		For 2.5 V I/O, I <sub>OH</sub> = -1.0 mA	2.0	-	V	
V <sub>OL</sub>	Output LOW voltage	For 3.3 V I/O, I <sub>OL</sub> = 8.0 mA	-	0.4	V	
		For 2.5 V I/O, I <sub>OL</sub> = 1.0 mA	-	0.4	V	
V <sub>IH</sub>	Input HIGH voltage <sup>[17]</sup>	For 3.3 V I/O	2.0	V <sub>DD</sub> + 0.3 V	V	
		For 2.5 V I/O	1.7	V <sub>DD</sub> + 0.3 V	V	
V <sub>IL</sub>	Input LOW voltage <sup>[17]</sup>	For 3.3 V I/O	-0.3	0.8	V	
		For 2.5 V I/O	-0.3	0.7	V	
I <sub>X</sub>	Input leakage current except ZZ and MODE	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5	5	μA	
	Input current of MODE	Input = V <sub>SS</sub>	-30	-	μA	
		Input = V <sub>DD</sub>	-	5	μA	
	Input current of ZZ	Input = V <sub>SS</sub>	-5	-	μA	
Input = V <sub>DD</sub>		-	30	μA		
I <sub>DD</sub>	V <sub>DD</sub> operating supply current	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	7.5 ns cycle, 133 MHz	-	210	mA
			10 ns cycle, 100 MHz	-	175	mA
I <sub>SB1</sub>	Automatic CE power-down current—TTL inputs	V <sub>DD</sub> = Max, device deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	-	140	mA
			10 ns cycle, 100 MHz	-	120	mA
I <sub>SB2</sub>	Automatic CE power-down current—CMOS inputs	V <sub>DD</sub> = Max, device deselected, V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3 V, f = 0, inputs static	All speeds	-	70	mA
I <sub>SB3</sub>	Automatic CE power-down current—CMOS inputs	V <sub>DD</sub> = Max, device deselected, or V <sub>IN</sub> ≤ 0.3 V or V <sub>IN</sub> ≥ V <sub>DDQ</sub> - 0.3 V, f = f <sub>MAX</sub> , inputs switching	7.5 ns cycle, 133 MHz	-	130	mA
			10 ns cycle, 100 MHz	-	110	mA
I <sub>SB4</sub>	Automatic CE power-down current—TTL inputs	V <sub>DD</sub> = Max, device deselected, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, inputs static	All Speeds	-	80	mA

### Notes

17. Overshoot: V<sub>IH</sub>(AC) < V<sub>DD</sub> + 1.5 V (Pulse width less than t<sub>CYC</sub>/2), undershoot: V<sub>IL</sub>(AC) > -2 V (Pulse width less than t<sub>CYC</sub>/2).  
 18. T<sub>Power-up</sub>: Assumes a linear ramp from 0 V to V<sub>DD</sub>(min) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.

### Capacitance<sup>[19]</sup>

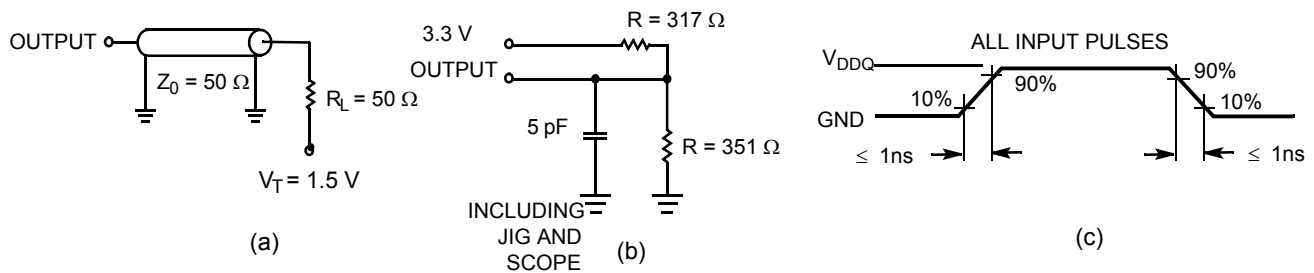
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>DD</sub> = 3.3 V V <sub>DDQ</sub> = 2.5 V	5	8	9	pF
C <sub>CLK</sub>	Clock input capacitance		5	8	9	pF
C <sub>IO</sub>	Input/output capacitance		5	8	9	pF

### Thermal Resistance<sup>[19]</sup>

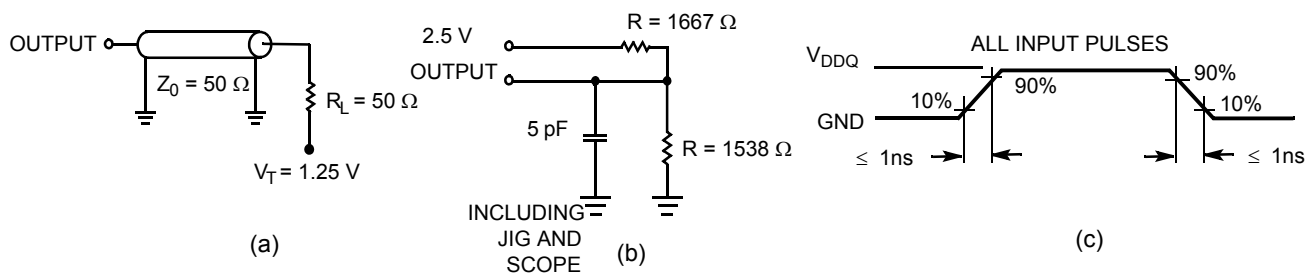
Parameter	Description	Test Conditions	100 TQFP Package	119 BGA Package	165 FBGA Package	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	28.66	23.8	20.7	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		4.08	6.2	4.0	°C/W

### AC Test Loads and Waveforms

#### 3.3 V I/O Test Load



#### 2.5 V I/O Test Load



**Note**  
19. Tested initially and after any design or process change that may affect these parameters.

## Switching Characteristics

Over the Operating Range<sup>[20, 21]</sup>

Parameter	Description	133 MHz		100 MHz		Unit
		Min	Max	Min	Max	
$t_{POWER}^{[22]}$		1	–	1	–	ms
<b>Clock</b>						
$t_{CYC}$	Clock cycle time	7.5	–	10	–	ns
$t_{CH}$	Clock HIGH	2.1	–	2.5	–	ns
$t_{CL}$	Clock LOW	2.1	–	2.5	–	ns
<b>Output Times</b>						
$t_{CDV}$	Data output valid after CLK rise	–	6.5	–	8.5	ns
$t_{DOH}$	Data output hold after CLK rise	2.0	–	2.0	–	ns
$t_{CLZ}$	Clock to low Z <sup>[23, 24, 25]</sup>	2.0	–	2.0	–	ns
$t_{CHZ}$	Clock to high Z <sup>[23, 24, 25]</sup>	–	4.0	–	5.0	ns
$t_{OE\bar{V}}$	$\overline{OE}$ LOW to output valid	–	3.2	–	3.8	ns
$t_{OE\bar{L}Z}$	$\overline{OE}$ LOW to output low Z <sup>[23, 24, 25]</sup>	0	–	0	–	ns
$t_{OE\bar{H}Z}$	$\overline{OE}$ HIGH to output high Z <sup>[23, 24, 25]</sup>	–	4.0	–	5.0	ns
<b>Setup Times</b>						
$t_{AS}$	Address setup before CLK rise	1.5	–	1.5	–	ns
$t_{ALS}$	ADV/LD setup before CLK rise	1.5	–	1.5	–	ns
$t_{WES}$	$\overline{WE}$ , $\overline{BW}_X$ setup before CLK rise	1.5	–	1.5	–	ns
$t_{CENS}$	$\overline{CEN}$ setup before CLK rise	1.5	–	1.5	–	ns
$t_{DS}$	Data input setup before CLK rise	1.5	–	1.5	–	ns
$t_{CES}$	Chip enable setup before CLK rise	1.5	–	1.5	–	ns
<b>Hold Times</b>						
$t_{AH}$	Address hold after CLK rise	0.5	–	0.5	–	ns
$t_{ALH}$	ADV/LD hold after CLK rise	0.5	–	0.5	–	ns
$t_{WEH}$	$\overline{WE}$ , $\overline{BW}_X$ hold after CLK rise	0.5	–	0.5	–	ns
$t_{CENH}$	$\overline{CEN}$ hold after CLK rise	0.5	–	0.5	–	ns
$t_{DH}$	Data input hold after CLK rise	0.5	–	0.5	–	ns
$t_{CEH}$	Chip enable hold after CLK rise	0.5	–	0.5	–	ns

### Notes

20. Timing reference level is 1.5 V when  $V_{DDQ} = 3.3$  V and is 1.25 V when  $V_{DDQ} = 2.5$  V.

21. Test conditions shown in (a) of AC Test Loads unless otherwise noted.

22. This part has a voltage regulator internally;  $t_{POWER}$  is the time that the power needs to be supplied above  $V_{DD}$ (minimum) initially, before a read or write operation can be initiated.

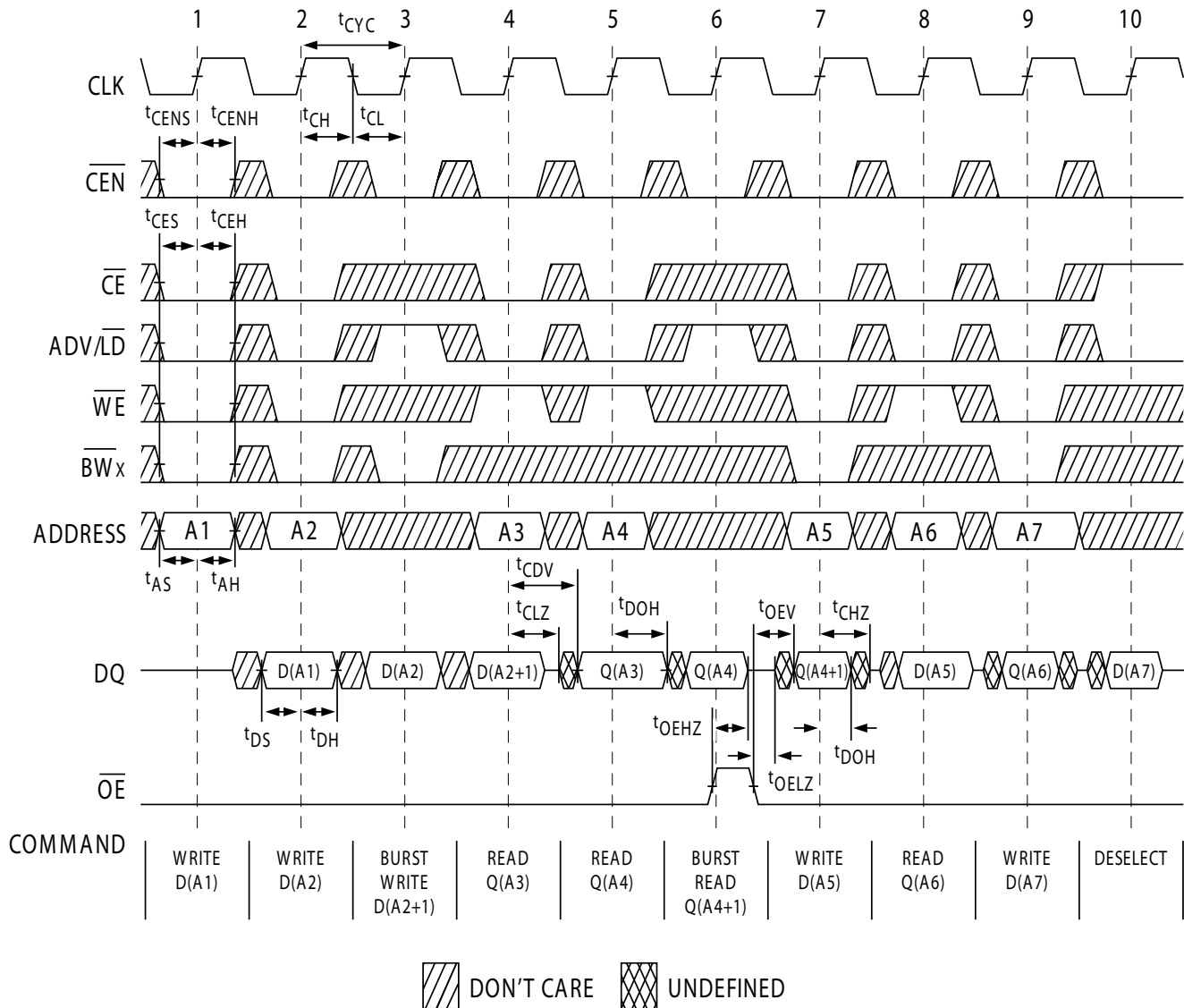
23.  $t_{CHZ}$ ,  $t_{CLZ}$ ,  $t_{OE\bar{L}Z}$ , and  $t_{OE\bar{H}Z}$  are specified with AC test conditions shown in part (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.

24. At any voltage and temperature,  $t_{OE\bar{H}Z}$  is less than  $t_{OE\bar{L}Z}$  and  $t_{CHZ}$  is less than  $t_{CLZ}$  to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.

25. This parameter is sampled and not 100% tested.

## Switching Waveforms

### Read/Write Waveforms<sup>[26, 27, 28]</sup>



#### Notes

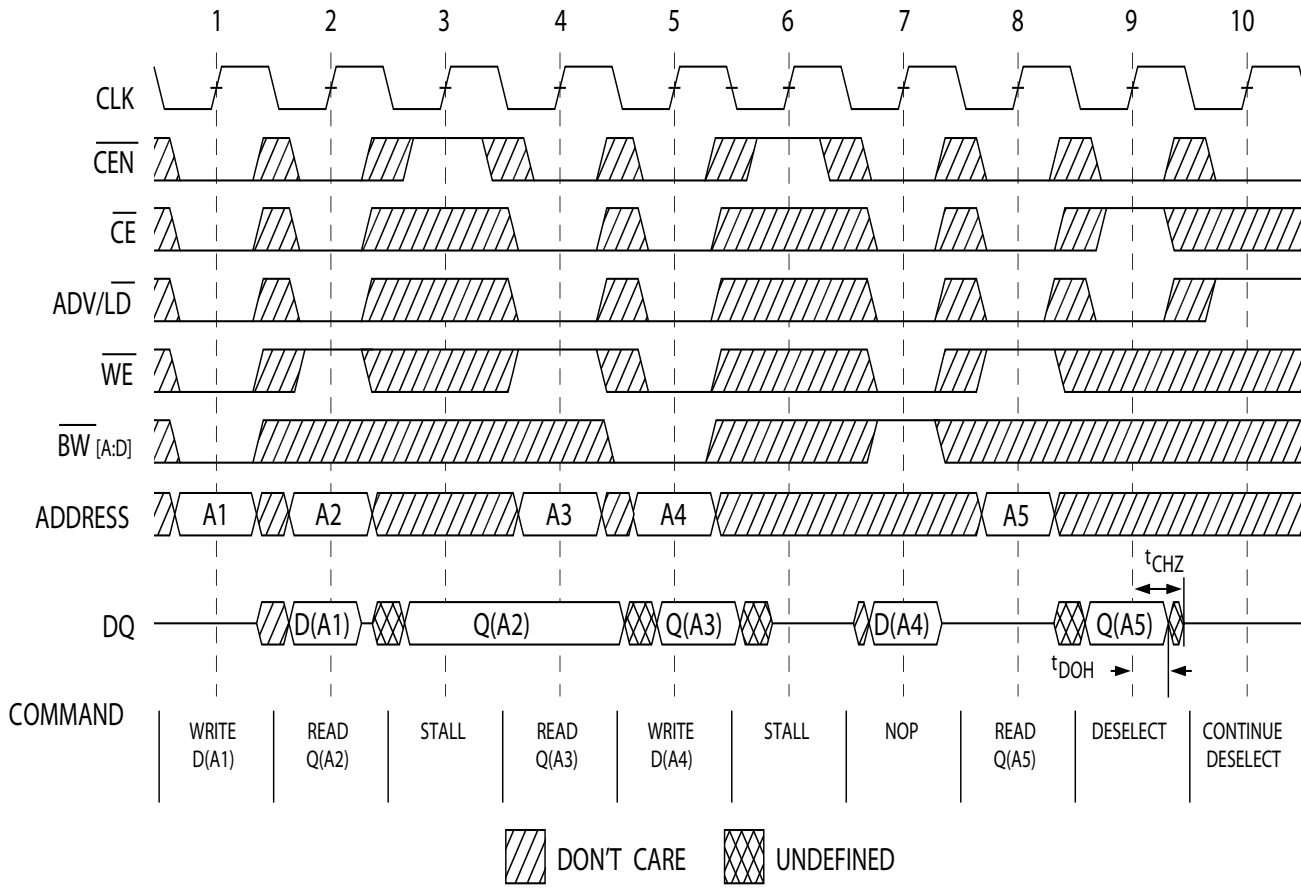
26. For this waveform ZZ is tied LOW.

27. When  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.

28. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

**Switching Waveforms** (continued)

**NOP, STALL AND DESELECT Cycles**<sup>[29, 30, 31]</sup>



**Notes**

29. For this waveform ZZ is tied LOW.

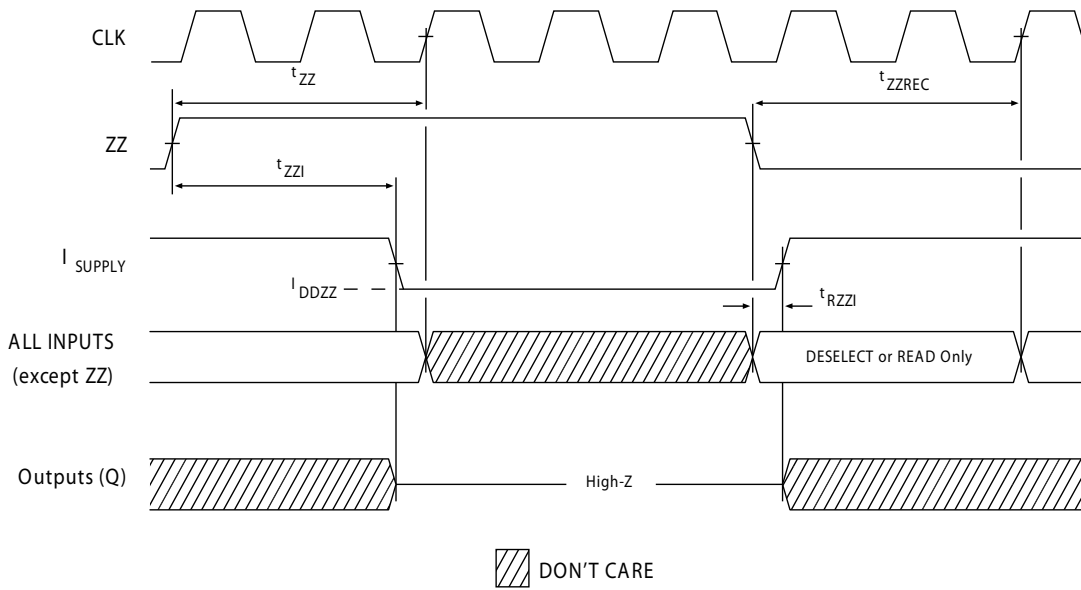
30. When  $\overline{CE}$  is LOW,  $\overline{CE}_1$  is LOW,  $\overline{CE}_2$  is HIGH and  $\overline{CE}_3$  is LOW. When  $\overline{CE}$  is HIGH,  $\overline{CE}_1$  is HIGH or  $\overline{CE}_2$  is LOW or  $\overline{CE}_3$  is HIGH.

31. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates CEN being used to create a pause. A write is not performed during this cycle.



**Switching Waveforms** (continued)

**ZZ Mode Timing**<sup>[32, 33]</sup>



**Notes**

- 32. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
- 33. DQs are in high Z when exiting ZZ sleep mode.

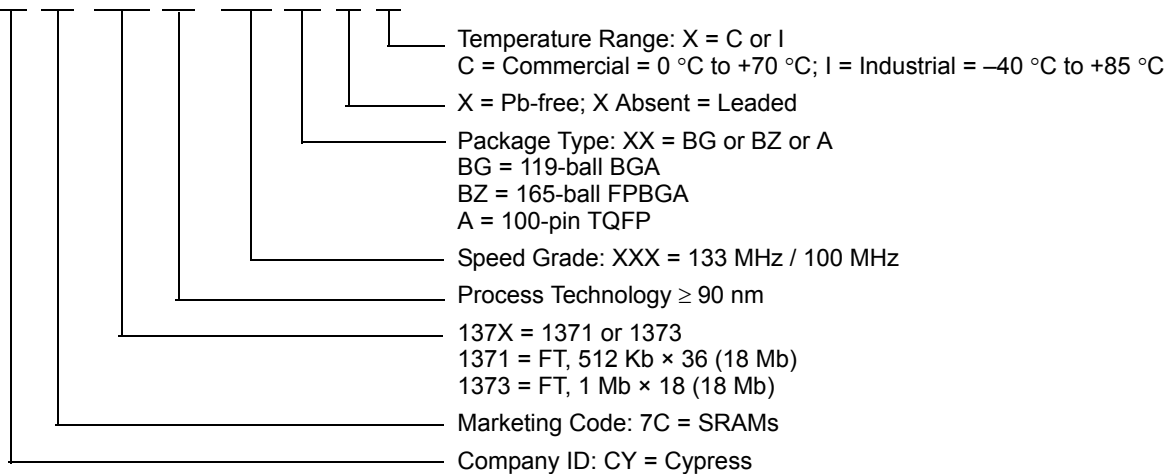
## Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1371D-133BGC	51-85115	119-ball Ball Grid Array (14 × 22 × 2.4 mm)	Commercial
	CY7C1373D-133BZI	51-85180	165-ball Fine-Pitch Ball Grid Array (13 × 15 × 1.4 mm)	Industrial
	CY7C1371D-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1373D-133AXI			Industrial
100	CY7C1371D-100AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1373D-100AXC			
	CY7C1371D-100AXI	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Industrial

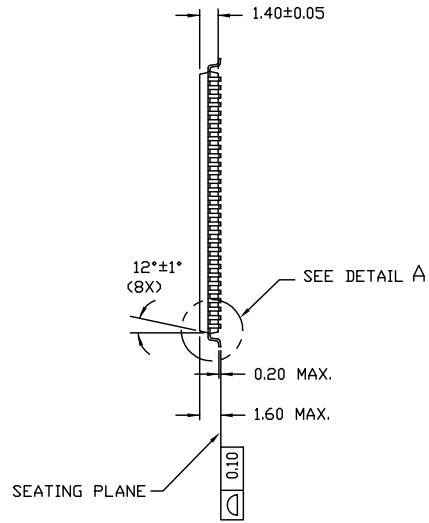
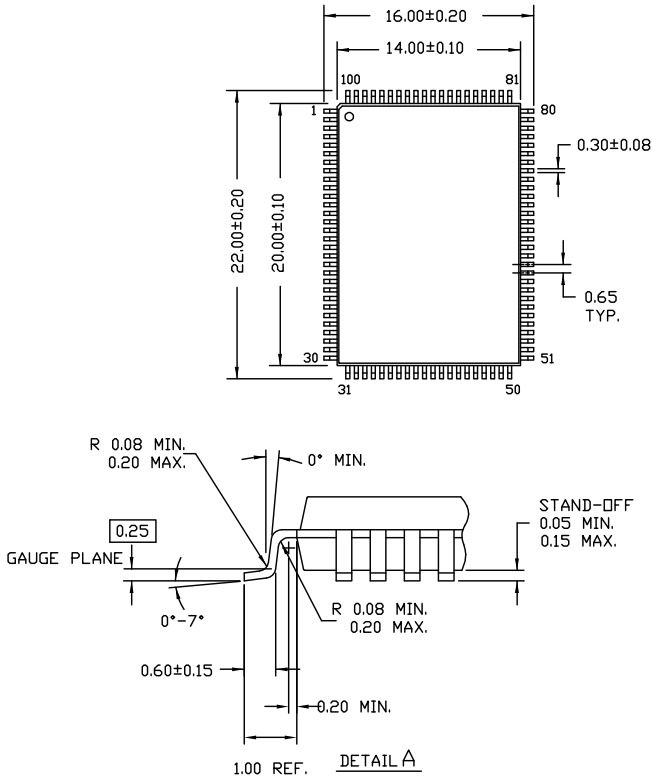
## Ordering Code Definitions

CY 7C 137X D - XXX XX X X



Package Diagrams

Figure 5. 100-pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm), 51-85050



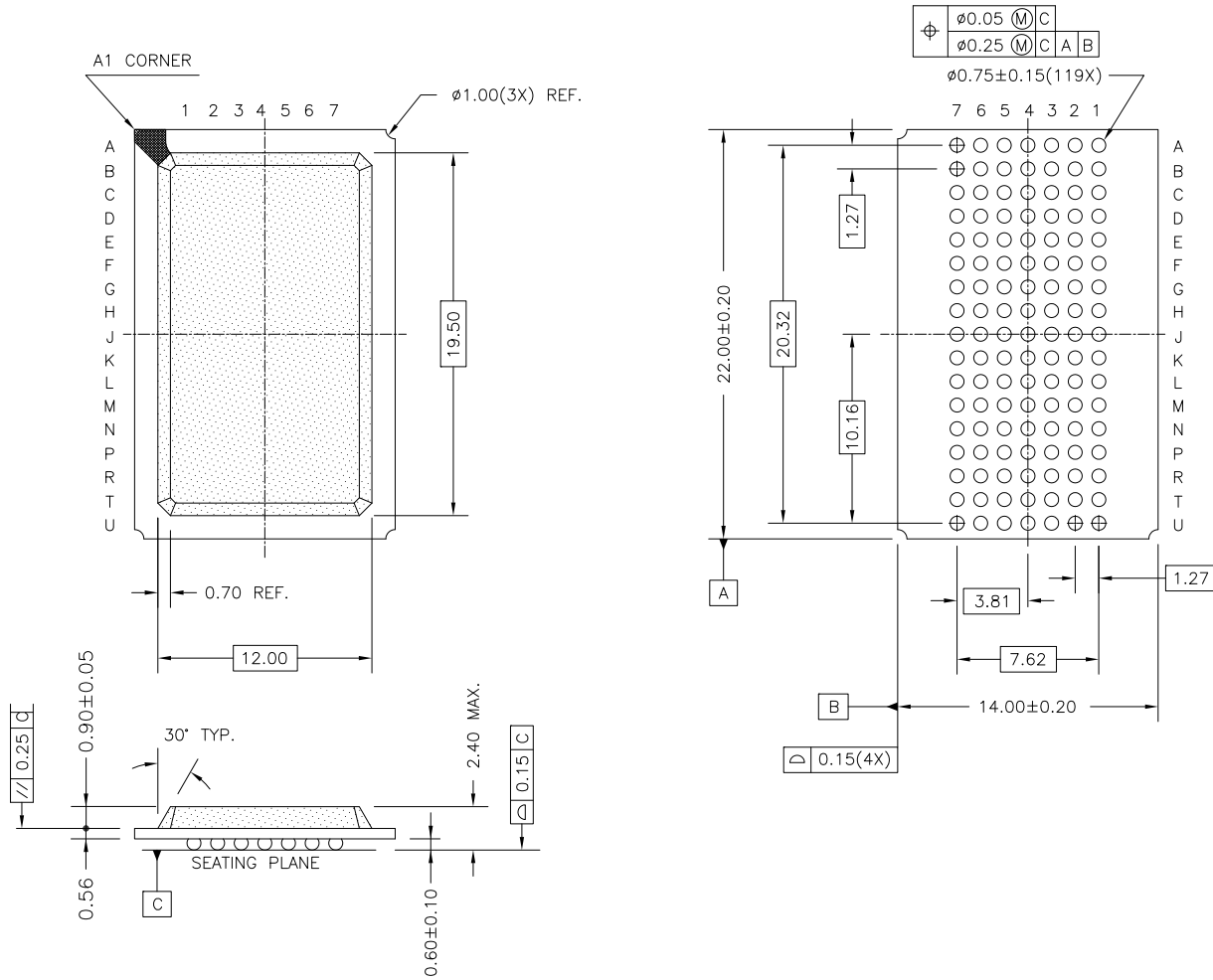
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE  
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85050 \*D

**Package Diagrams** (continued)

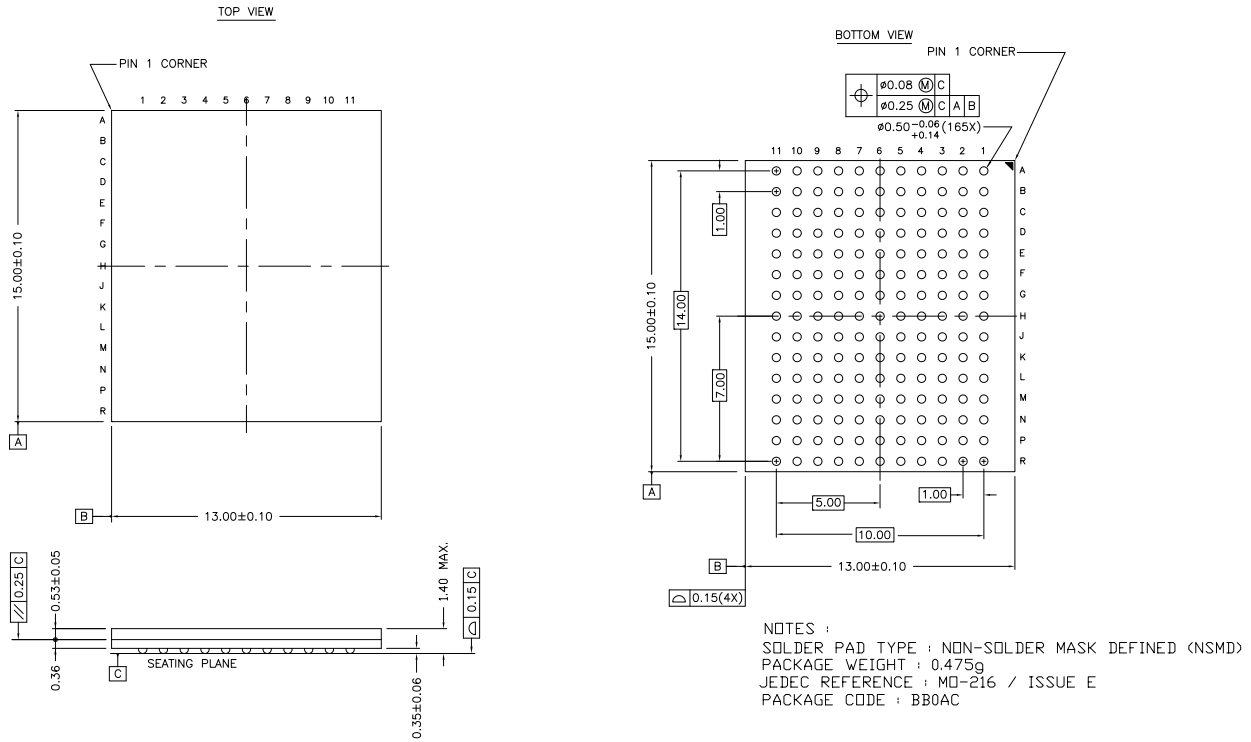
**Figure 6. 119-ball BGA (14 × 22 × 2.4 mm), 51-85115**



51-85115 °C

**Package Diagrams** (continued)

**Figure 7. 165-ball FPBGA (13 × 15 × 1.4 mm), 51-85180**



51-85180 \*C

## Acronyms

Acronym	Description
BGA	ball grid array
CMOS	complementary metal oxide semiconductor
CE	chip enable
CEN	clock enable
FPBGA	fine-pitch ball grid array
I/O	Input/Output
JTAG	Joint Test Action Group
NoBL	No Bus Latency
OE	output enable
SRAM	static random access memory
TCK	test clock
TDI	test data input
TMS	test mode select
TDO	test data output
TQFP	thin quad flat pack
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ms	milli seconds
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

**Document History Page**

Document Title: CY7C1371D/CY7C1373D 18-Mbit (512 K × 36/1 M × 18) Flow-through SRAM with NoBL™ Architecture Document Number: 38-05556				
REV.	ECN NO.	Submission Date	Orig. of Change	Description of Change
**	254513	See ECN	RKF	New data sheet
*A	288531	See ECN	SYT	Edited description under “IEEE 1149.1 Serial Boundary Scan (JTAG)” for non-compliance with 1149.1 Removed 117 Mhz Speed Bin Added Pb-free information for 100-Pin TQFP, 119 BGA and 165 FBGA Packages Added comment of ‘Pb-free BG packages availability’ below the Ordering Information
*B	326078	See ECN	PCI	Address expansion pins/balls in the pinouts for all packages are modified according to JEDEC standard Added description on EXTEST Output Bus tristate Changed description on the Tap Instruction Set Overview and Extest Changed $\Theta_{JA}$ and $\Theta_{JC}$ for TQFP Package from 31 and 6 °C/W to 28.66 and 4.08 °C/W respectively Changed $\Theta_{JA}$ and $\Theta_{JC}$ for BGA Package from 45 and 7 °C/W to 23.8 and 6.2 °C/W respectively Changed $\Theta_{JA}$ and $\Theta_{JC}$ for FBGA Package from 46 and 3 °C/W to 20.7 and 4.0 °C/W respectively Modified $V_{OL}$ , $V_{OH}$ test conditions Removed comment of ‘Pb-free BG packages availability’ below the Ordering Information Updated Ordering Information Table
*C	345117	See ECN	PCI	Updated Ordering Information Table Changed from Preliminary to Final
*D	416321	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court” In the Partial Truth Table for Read/Write on page # 10, the $\overline{BW}_A$ of Write Byte A – ( $DQ_A$ and $DQP_A$ ) and $BW_B$ of Write Byte B – ( $DQ_B$ and $DQP_B$ ) has been changed from H to L Changed the description of $I_x$ from Input Load Current to Input Leakage Current on page# 20 Changed the $I_x$ current values of MODE on page # 20 from -5 $\mu A$ and 30 $\mu A$ to -30 $\mu A$ and 5 $\mu A$ Changed the $I_x$ current values of ZZ on page # 20 from -30 $\mu A$ and 5 $\mu A$ to -5 $\mu A$ and 30 $\mu A$ Changed $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ on page # 20 Replaced Package Name column with Package Diagram in the Ordering Information table Updated Ordering Information Table
*E	475677	See ECN	VKN	Added the Maximum Rating for Supply Voltage on $V_{DDQ}$ Relative to GND Changed $t_{TH}$ , $t_{TL}$ from 25 ns to 20 ns and $t_{TDOV}$ from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*F	1274734	See ECN	VKN/AESA	Corrected typo in the “NOP, STALL and DESELECT Cycles” waveform
*G	2897120	03/22/2010	NJY	Removed inactive parts from Ordering Information table; Updated package diagram.
*H	3033272	09/19/2010	NJY	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Minor edits and updated in new template.
*I	3067448	10/21/2010	NJY	Updated <a href="#">Ordering Information</a> .
*J	3353119	08/24/2011	PRIT	Updated 100-pin TQFP package diagram. Modified Note 1 on page 1.

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