DCR720E

Phase Control Thyristor

Preliminary Information

DS5485-1.2 February 2002

FEATURES

- Double Side Cooling
- High Surge Capability
- Low Inductance Internal Construction

APPLICATIONS

- High Power Converters
- DC Motor Control
- High Voltage Power Supplies

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{DRM} V	Conditions
DCR720E18 DCR720E16 DCR720E14 DCR720E12	1800 1600 1400 1200	T_{vj} = 0˚ to 125˚C, I_{DRM} = I_{RRM} = 30mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

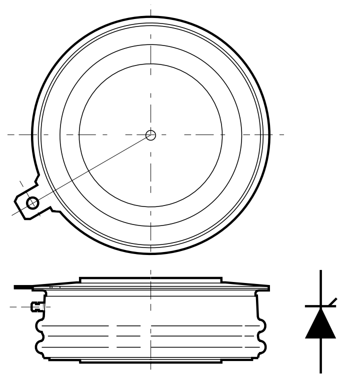
DCR720E16

Note: Please use the complete part number when ordering and quote this number in any future correspondance relating to your order.

KEY PARAMETERS

V_{DRM}	**1800V**
$I_{T(AV)}$	**724A**
I_{TSM}	**9800A**
dV/dt*	**1000V/µs**
dI/dt	**700A/µs**

***Higher dV/dt selections available**



Outline type code: E

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60˚C unless stated otherwise.

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	724	A
$I_{T(RMS)}$	RMS value	-	1140	A
I_T	Continuous (direct) on-state current	-	1025	A
Single Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	500	A
$I_{T(RMS)}$	RMS value	-	790	A
I_T	Continuous (direct) on-state current	-	670	A

T_{case} = 80˚C unless stated otherwise.

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	570	A
$I_{T(RMS)}$	RMS value	-	895	A
I_T	Continuous (direct) on-state current	-	790	A
Single Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	390	A
$I_{T(RMS)}$	RMS value	-	610	A
I_T	Continuous (direct) on-state current	-	505	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125˚C	7.8	kA
I^2t	I^2t for fusing	V_R = 50% V_{RRM} - 1/4 sine	0.3 x 10^6	A^2s
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125˚C	9.8	kA
I^2t	I^2t for fusing	V_R = 0	0.48 x 10^6	A^2s

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{RRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125˚C		-	30	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125˚C		-	1000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1100A	Repetitive 50Hz	-	350	A/µs
		Gate source 20V, 10Ω, $t_r \le$ 0.5µs, T_j = 125˚C	Non-repetitive	-	700	A/µs
$V_{T(TO)}$	Threshold voltage	At T_{vj} = 125˚C		-	0.88	V
r_T	On-state slope resistance	At T_{vj} = 125˚C		-	0.65	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 10V, 5Ω t_r = 0.5µs, Tj = 25˚C		-	1.5	µs
t_q	Turn-off time	I_T = 500A, t_p = 1ms, T_j =125˚C, V_R = 50V, dI_{RR}/dt = 20A/µs, V_{DR} = 67% V_{DRM}, dV_{DR}/dt = 20V/µs linear		300	400	µs
I_L	Latching current	T_j = 25˚C, V_D = 5V		-	500	mA
I_H	Holding current	T_j = 25˚C, V_D = 5V		-	70	mA

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance - junction to case	Double side cooled	DC	-	0.041	˚CW
		Single side cooled	Anode DC	-	0.074	˚CW
			Cathode DC	-	0.092	˚CW
$R_{th(c-h)}$	Thermal resistance - case to heatsink	Clamping force 8.0kN	Double side	-	0.018	˚CW
		(with mounting compound)	Single side	-	0.036	˚CW
T_{vj}	Virtual junction temperature	On-state (conducting)		-	135	˚C
		Reverse (blocking)		-	125	˚C
T_{stg}	Storage temperature range			–55	125	˚C
F_m	Clamping force			7.2	8.8	kN

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	3	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	150	mA
V_{GD}	Gate non-trigger voltage	At V_{DRM} T_{case} = 125°C	0.25	V
V_{FGM}	Peak forward gate voltage	Anode positive with respect to cathode	30	V
V_{FGN}	Peak forward gate voltage	Anode negative with respect to cathode	0.25	V
V_{RGM}	Peak reverse gate voltage	-	5	V
I_{FGM}	Peak forward gate current	Anode positive with respect to cathode	10	A
P_{GM}	Peak gate power	See table, gate characteristics curve	100	W
$P_{G(AV)}$	Mean gate power	-	5	W

CURVES

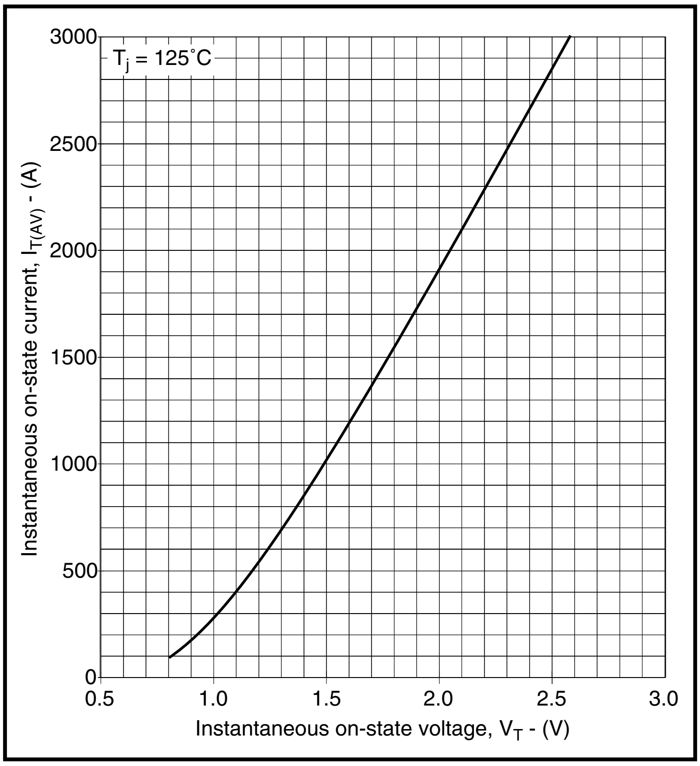


Fig.2 Maximum (limit) on-state characteristics

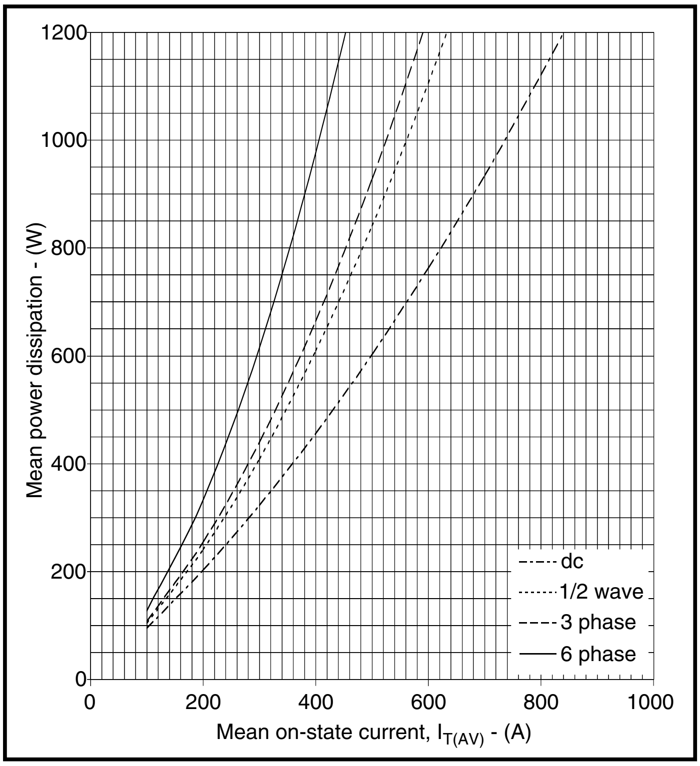


Fig.3 Power dissipation

V_{TM} Equation:-

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.2366
B = 0.1182
C = 0.0005
D = –0.0019

these values are valid for T_j = 125˚C for I_T 100A to 3000A

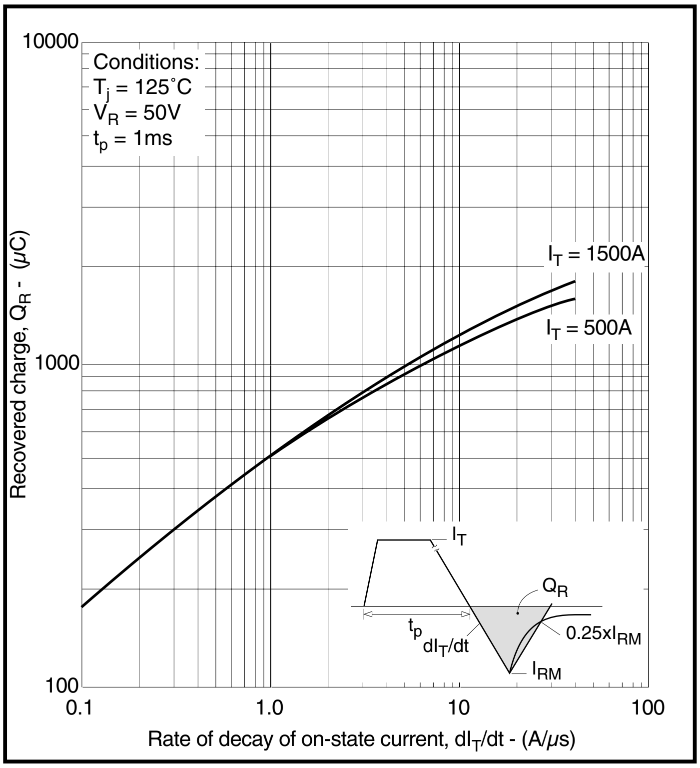
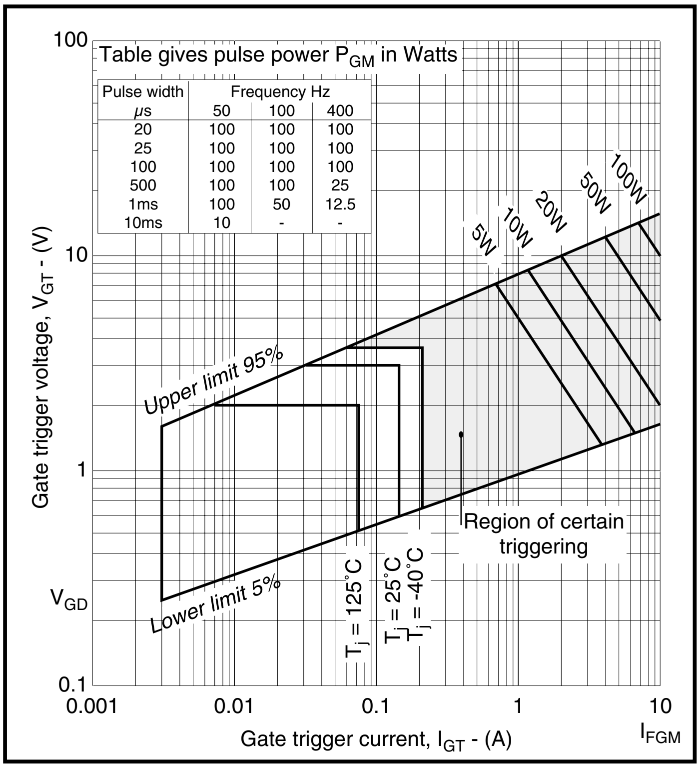
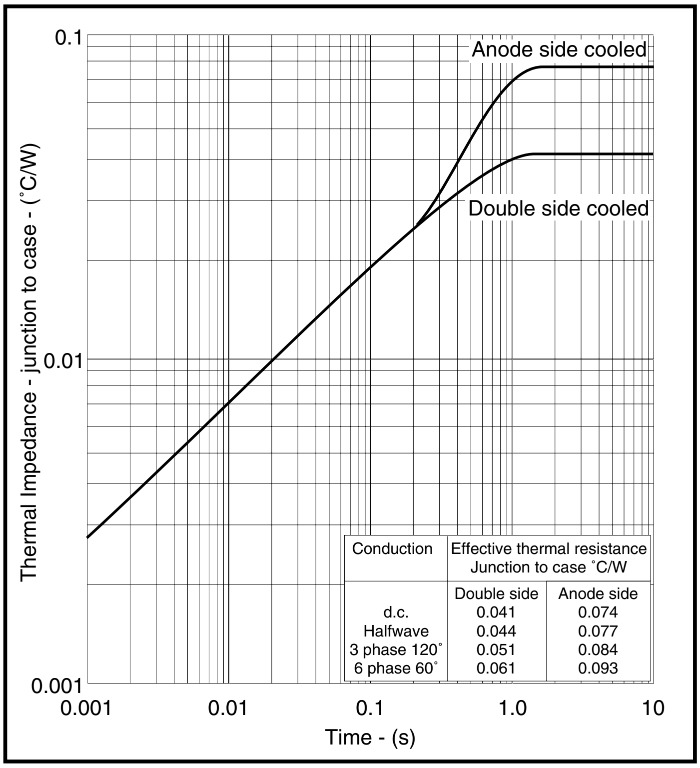


Fig.4 Stored charge



Pulse width μs	Frequency Hz 50	100	400
20	100	100	100
25	100	100	100
100	100	100	100
500	100	100	25
1ms	100	50	12.5
10ms	10	-	-

Fig.5 Gate characteristics



Conduction	Effective thermal resistance Junction to case ˚C/W	
	Double side	Anode side
d.c.	0.041	0.074
Halfwave	0.044	0.077
3 phase 120˚	0.051	0.084
6 phase 60˚	0.061	0.093

Fig.6 Maximum (limit) transient thermal impedance - junction to case (˚C/W)

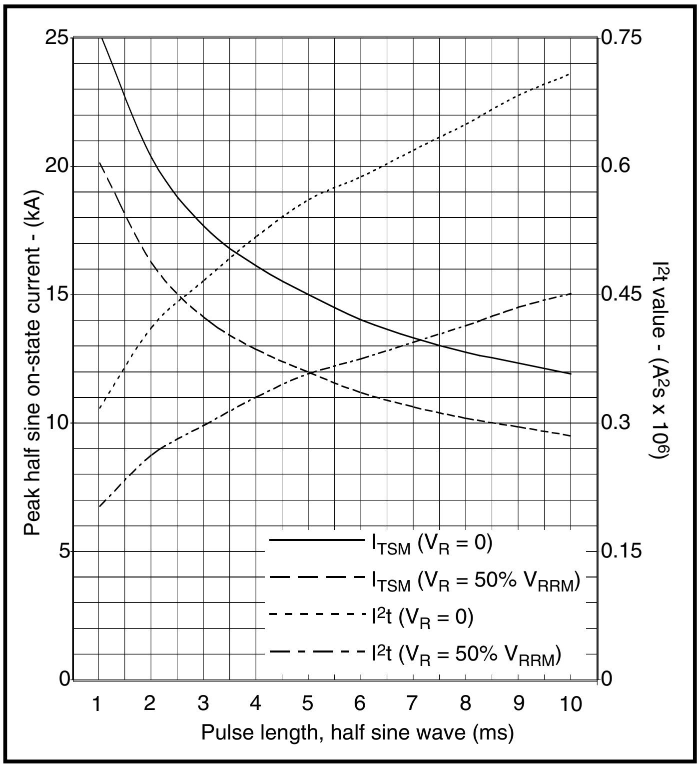


Fig.7 Sub-cycle surge currents

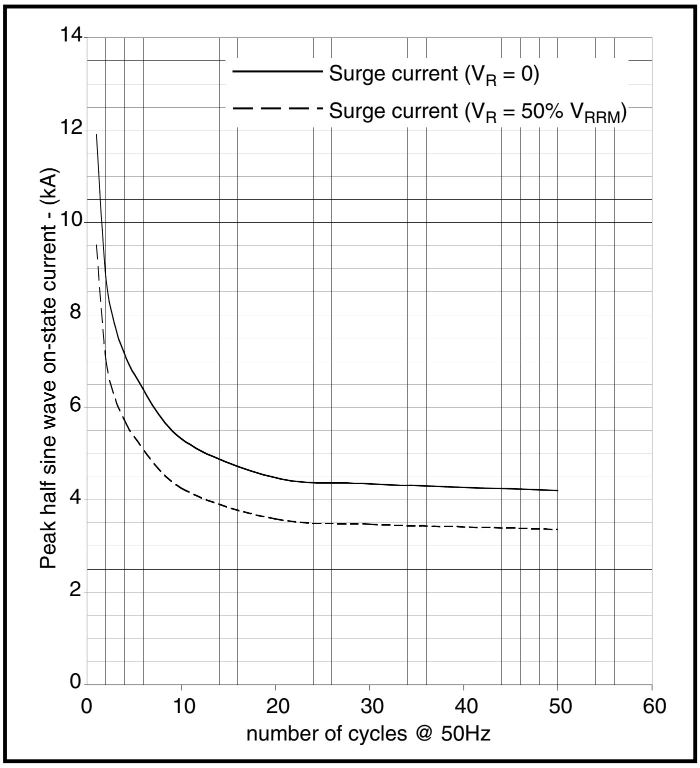
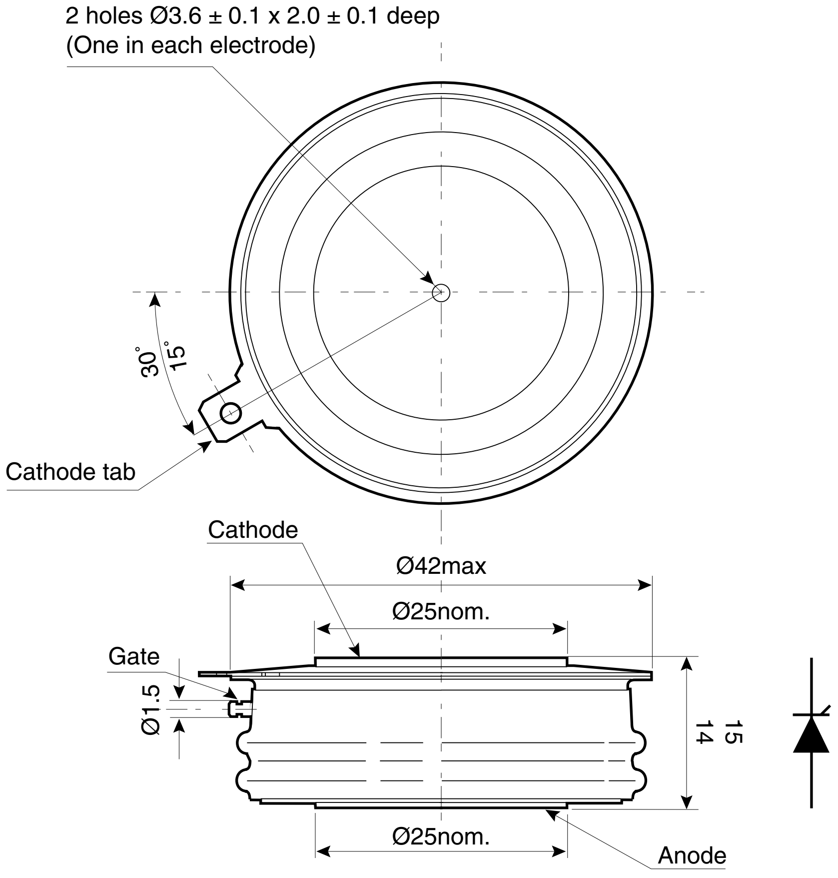


Fig.8 Multi-cycle surge currents

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise.
DO NOT SCALE.



Nominal weight: 82g
Clamping force: 8kN ±10%
Lead length: 420mm
Lead terminal connector: M4 ring

Package outine type code: E

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.

http://www.dynexsemi.com

e-mail: power_solutions@dynexsemi.com

HEADQUARTERS OPERATIONS
DYNEX SEMICONDUCTOR LTD
Doddington Road, Lincoln.
Lincolnshire. LN6 3LF. United Kingdom.
Tel: +44-(0)1522-500500
Fax: +44-(0)1522-500550

CUSTOMER SERVICE
Tel: +44 (0)1522 502753 / 502901. Fax: +44 (0)1522 500020