High Speed Difference Amplifier with Input Short-to-Battery Protection

Data Sheet

ADA4830-1/ADA4830-2

FEATURES

Input overvoltage (short-to-battery) protection of up to 18 V
Short-to-battery output flag for wire diagnostics
Wide input common-mode range with single 5 V supply
High performance video amplifier with 0.50 V/V gain
−3 dB bandwidth of 84 MHz
250 V/µs slew rate (2 V step)
Excellent video specifications
0.1 dB flatness to 28 MHz
SNR of 73 dB to 15 MHz
Differential gain of 0.1%
Differential phase of 0.1°
Wide supply range: 2.9 V to 5.5 V
Power-down/output disable mode
Space saving 3 mm × 3 mm LFCSP package
Wide operating temperature range: −40°C to +125°C

APPLICATIONS

Automotive vision systems
Automotive infotainment
Surveillance systems

GENERAL DESCRIPTION

The ADA4830-1 (single) and ADA4830-2 (dual) are monolithic, high speed difference amplifiers that integrate input overvoltage (short-to-battery) protection of up to 18 V with a wide input common-mode voltage range and excellent ESD robustness. They are intended for use as receivers for differential or pseudo differential CVBS and other high speed video signals in harsh, noisy environments such as automotive infotainment and vision systems. The ADA4830-1 and ADA4830-2 combine high speed and precision, which allows for accurate reproduction of CVBS video signals, yet rejects unwanted common-mode error voltages.

The short-to-battery protection that is integrated into the ADA4830-1 and ADA4830-2 employs fast switching circuitry to clamp and hold internal voltage nodes at a safe level when an input overvoltage condition is detected. This protection allows the inputs of the ADA4830-1 and ADA4830-2 to be directly connected to a remote video source, such as a rearview camera, without the need for large expensive series capacitors. The ADA4830-1 and ADA4830-2 can withstand direct short-to-battery voltages as high as 18 V on their input pins.

The ADA4830-1 and ADA4830-2 are designed to operate at supply voltages as low as 2.9 V and as high as 5.5 V, using only 6.8 mA of supply current per channel. These devices provide true single-supply capability, allowing the input signal to extend 8.5 V below ground rail and to 8.5 V above ground on a single 5 V supply. At the output, the amplifier can swing to within 250 mV of either supply rail into a 150 Ω load.

The ADA4830-1 and ADA4830-2 present a gain of 0.50 V/V at their output. This is designed to keep the video signal within the allowed range of the video decoder, which is typically 1 V p-p or less.

The ADA4830-1 and ADA4830-2 are available in 3 mm × 3 mm LFCSP packages, 8-lead and 16-lead, respectively, and are specified for operation over the automotive temperature range of −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

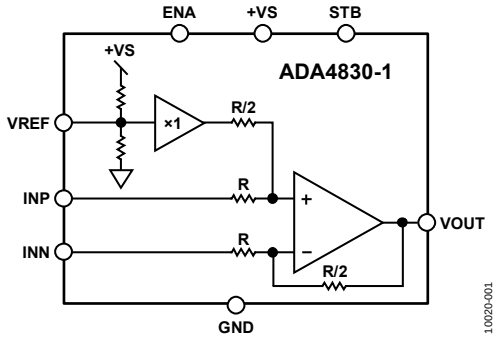

Figure 1.

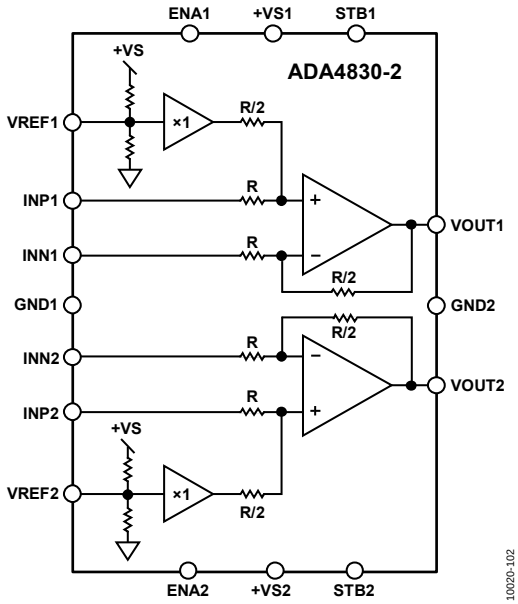

Figure 2.

Rev. A

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10/11—Revision 0: Initial Version

SPECIFICATIONS

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, R_L = 1 kΩ, V_{REF} = 2.5 V (floating), V_{INCM} = $+V_S$/2, R_{STB} = 5 kΩ to $+V_S$, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		71		MHz
	V_{OUT} = 0.1 V p-p, R_L = 1 kΩ		84		MHz
	V_{OUT} = 0.1 V p-p, R_L = 150 Ω		74		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		28		MHz
Slew Rate (t_R/t_F)	V_{OUT} = 2 V step		250/300		V/µs
Settling Time to 0.1%	V_{OUT} = 2 V step		25		ns
NOISE/DISTORTION PERFORMANCE					
Output Voltage Noise	f = 1 MHz		28		nV/√Hz
Differential Gain Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		%
Differential Phase Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		Degrees
Signal-to-Noise Ratio	f = 100 kHz to 15 MHz, V_{OUT} = 0.5 V p-p		73		dB
DC PERFORMANCE					
Nominal Gain	V_{IN} to V_{OUT}	0.49	0.50	0.51	V/V
Output Bias Voltage		2.45	2.50	2.55	V
INPUT CHARACTERISTICS					
Input Resistance (Differential Mode)			6.7		kΩ
Input Resistance (Common Mode)			2		kΩ
Input Common-Mode Voltage Range	V_{REF} voltage adjusted to optimized range	−10		+9.5	V
Common-Mode Rejection (CMR)	V_{IN} = ±5 V	42	65		dB
SHORT-TO-BATTERY CHARACTERISTICS					
Input Current	V_{IN} = 18 V (short-to-battery)		4.1		mA
Protected Input Voltage Range		−9		+20	V
Short-to-Battery Output Flag Trigger Level	Minimum V_{IN} needed to signal an input fault condition	9.8	10.3	10.8	V
VOLTAGE REFERENCE INPUT					
Input Voltage Range			0.2 to 3.9		V
Input Resistance			20		kΩ
Gain	V_{REF} to V_{OUT}		1		V/V
LOGIC OUTPUT/INPUT CHARACTERISTICS					
STB V_{OH}	V_{IN} ≤ 9.8 V (normal operation)		5.0		V
STB V_{OL}	V_{IN} ≥ 10.8 V (fault condition), ADA4830-1/ADA4830-2		110/253		mV
ENA V_{IH}	Voltage to enable device		≥3.0		V
ENA V_{IL}	Voltage to disable device		≤1.0		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω to ground		0.01 to 4.75		V
Output Current			125		mA
Short-Circuit Current	Sourcing/sinking		248/294		mA
Capacitive Load Drive	Peaking ≤ 3 dB		47		pF
POWER SUPPLY					
Operating Range	Operation outside of this range results in performance degradation	2.9		5.5	V
Quiescent Current per Amplifier	Enabled (ENA = 5 V), no load		6.8	10	mA
	Disabled (ENA = 0 V)		90		µA
	V_{IN} = 18 V (short-to-battery)		5.3		mA
Power Supply Rejection Ratio (PSRR)	$+V_S$ = 4.5 V to 5.5 V, V_{REF} is forced to 2.5 V		53		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

3.3 V OPERATION

T_A = 25°C, $+V_S$ = 3.3 V, R_L = 1 kΩ, V_{REF} = 1.65 V (floating), V_{INCM} = $+V_S$/2, R_{STB} = 5 kΩ to +Vs, unless otherwise specified.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		73		MHz
	V_{OUT} = 0.1 V p-p, R_L = 1 kΩ		89		MHz
	V_{OUT} = 0.1 V p-p, R_L = 150 Ω		78		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.5 V p-p, R_L = 150 Ω		20		MHz
Slew Rate (t_R/t_F)	V_{OUT} = 1 V step		165/180		V/µs
Settling Time to 0.1%	V_{OUT} = 1 V step		25		ns
NOISE/DISTORTION PERFORMANCE					
Output Voltage Noise	f = 1 MHz		28		nV/√Hz
Differential Gain Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		%
Differential Phase Error (NTSC)	R_L = 150 Ω, V_{IN} = 1 V p-p		0.1		Degrees
Signal-to-Noise Ratio	f = 100 kHz to 15 MHz, V_{OUT} = 0.5 V p-p		73		dB
DC PERFORMANCE					
Nominal Gain	V_{IN} to V_{OUT}	0.49	0.50	0.51	V/V
Output Bias Voltage		1.60	1.65	1.70	V
INPUT CHARACTERISTICS					
Input Resistance (Differential Mode)			6.7		kΩ
Input Resistance (Common Mode)			2		kΩ
Input Common-Mode Voltage Range	V_{REF} voltage adjusted to optimized range	−8		+6	V
Common-Mode Rejection (CMR)	V_{IN} = ±3.3 V	41	54		dB
SHORT-TO-BATTERY CHARACTERISTICS					
Input Current	V_{IN} = 18 V (short-to-battery)		4.4		mA
Protected Input Voltage Range		−9		+20	V
Short-to-Battery Output Flag Trigger Level	Minimum V_{IN} needed to signal an input fault condition	7.4	7.8	8.2	V
VOLTAGE REFERENCE INPUT					
Input Voltage Range			0.2 to 2.2		V
Input Resistance			20		kΩ
Gain	V_{REF} to V_{OUT}		1		V/V
LOGIC OUTPUT/INPUT CHARACTERISTICS					
STB V_{OH}	V_{IN} ≤ 7.4 V (normal operation)		3.3		V
STB V_{OL}	V_{IN} ≥ 8.2 V (fault condition), ADA4830-1/ADA4830-2		85/178		mV
ENA V_{IH}	Voltage to enable device		≥1.8		V
ENA V_{IL}	Voltage to disable device		≤0.8		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω to ground		0.01 to 3.08		V
Output Current			50		mA
Short-Circuit Current	Sourcing/sinking		85/180		mA
Capacitive Load Drive	Peaking ≤ 4 dB		47		pF
POWER SUPPLY					
Operating Range	Operation outside of this range results in performance degradation	2.9		5.5	V
Quiescent Current per Amplifier	Enabled (ENA = 3.3 V), no load		5.5	8.0	mA
	Disabled (ENA = 0 V)		60		µA
	V_{IN} = 18 V (short-to-battery)		4.3		mA
Power Supply Rejection Ratio (PSRR)	$+V_S$ = 3.0 V to 3.6 V, V_{REF} forced to 1.65 V		42		dB
OPERATING TEMPERATURE RANGE		−40		+125	°C

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage (+VS Pin)	6 V
Supply Voltage Delta	
+VS1 to +VS2, ADA4830-2 Only	0.5 V
Input Voltage Positive Direction (INNx, INPx)	22 V
Input Voltage Negative Direction (INNx, INPx)	−10 V
Reference Voltage (VREFx Pin)	$+V_S$ + 0.3 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	260°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device and its exposed paddle is soldered to a high thermal conductivity, 4-layer (2s2p) circuit board, as described in EIA/JESD 51-7.

Table 4.

Package Type	θ_{JA}	Unit
8-Lead LFCSP	116	°C/W
16-Lead LFCSP	54	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4830-1 and ADA4830-2 packages is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Exceeding a junction temperature of 150°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the supply voltage ($+V_S$) times the quiescent current (I_S). The power dissipated due to load drive depends on the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}.

Figure 3 shows the maximum power dissipation in the package vs. the ambient temperature for the 8-lead LFCSP (116°C/W) and the 16-lead LFCSP (54°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximate.

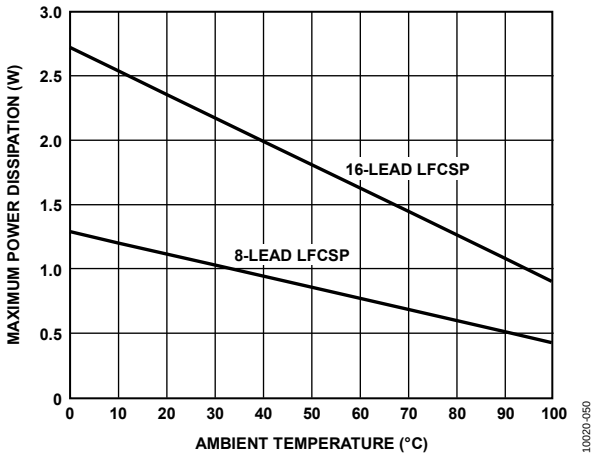


Figure 3. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

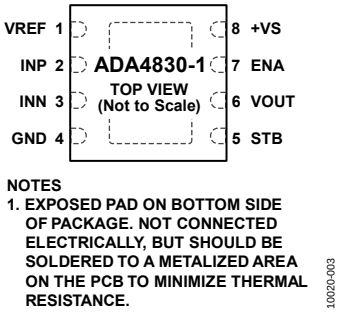


Figure 4. ADA4830-1 Pin Configuration

Table 5. ADA4830-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VREF	Voltage Reference Input. Sets the output dc bias voltage. Internally biased to $+V_S/2$ when left floating. See the Applications Information section.
2	INP	Positive Input.
3	INN	Negative Input.
4	GND	Power Supply Ground Pin.
5	STB	Short-to-Battery Indicator Output Pin. A logic low indicates an overvoltage condition (short-to-battery), whereas a logic high indicates normal operation. An open-drain configuration requires external pull-up resistor.
6	VOUT	Amplifier Output.
7	ENA	Enable Pin. Connect to $+V_S$ or float for normal operation. Connect to ground for device disable.
8	+VS	Positive Power Supply Pin. Bypass this pin with a 0.1 µF capacitor to ground.
	EPAD	Exposed Pad. The exposed pad is located on the bottom side of the package. The pad is not connected electrically but should be soldered to a metalized area on the printed circuit board (PCB) to minimize thermal resistance.

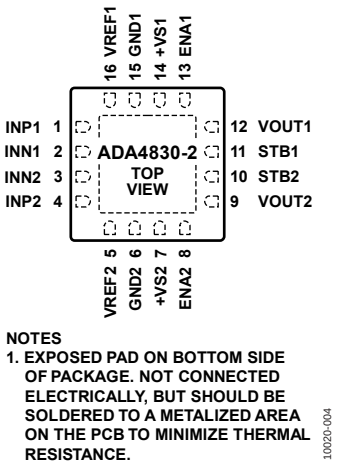


Figure 5. ADA4830-2 Pin Configuration

Table 6. ADA4830-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	INP1, INP2	Positive Inputs.
2, 3	INN1, INN2	Negative Inputs.
5, 16	VREF2, VREF1	Voltage Reference Inputs. Sets the output dc bias voltage. Internally biased to $+V_S/2$ when left floating. See the Applications Information section.
6, 15	GND2, GND1	Power Supply Ground Pins.
7, 14	+VS2, +VS1	Positive Power Supply Pins. These pins must be connected together, to the same voltage. Bypass these pins with a 0.1 µF capacitor to ground.
8, 13	ENA2, ENA1	Enable Pins. Connect to $+V_S$ or float for normal operation and to ground for device disable.
9, 12	VOUT2, VOUT1	Amplifier Outputs.
10, 11	STB2, STB1	Short-to-Battery Indicator Output Pins. A logic low indicates an overvoltage condition (short-to-battery), whereas a logic high indicates normal operation. An open-drain configuration requires an external pull-up resistor.
	EPAD	Exposed Pad. The exposed pad is located on the bottom side of the package. The pad is not connected electrically, but should be soldered to a metalized area on the PCB to minimize thermal resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, R_L = 1 kΩ, V_{REF} = 2.5 V (floating), V_{INCM} = $+V_S$/2, R_{STB} = 5 kΩ to $+V_S$, unless otherwise specified.

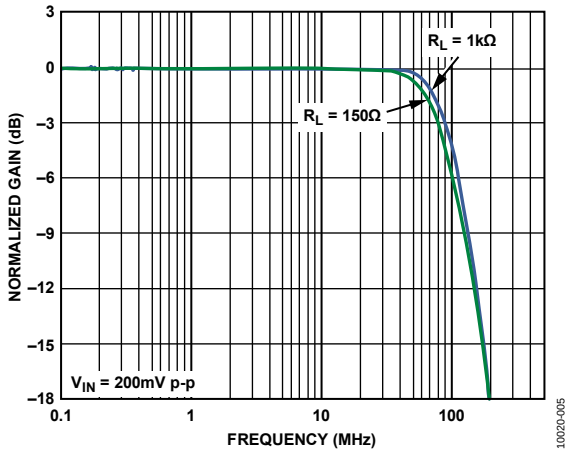


Figure 6. Small Signal Frequency Response for Various Loads

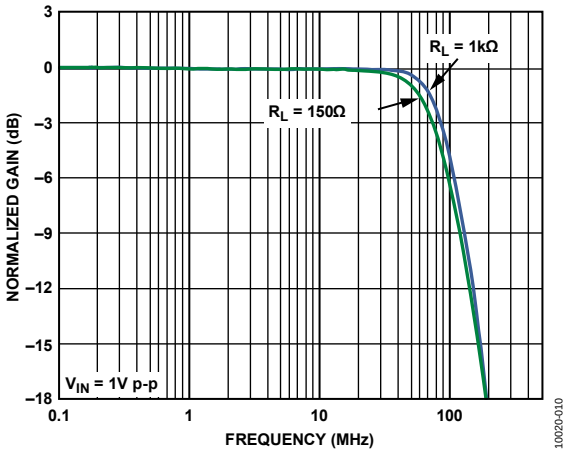


Figure 9. Large Signal Frequency Response for Various Loads

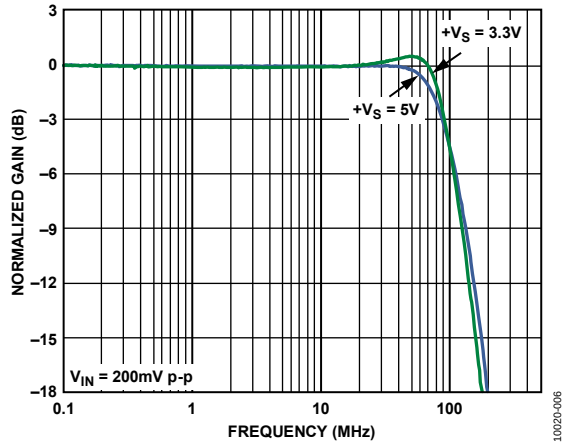


Figure 7. Small Signal Frequency Response for Various Supply Voltages

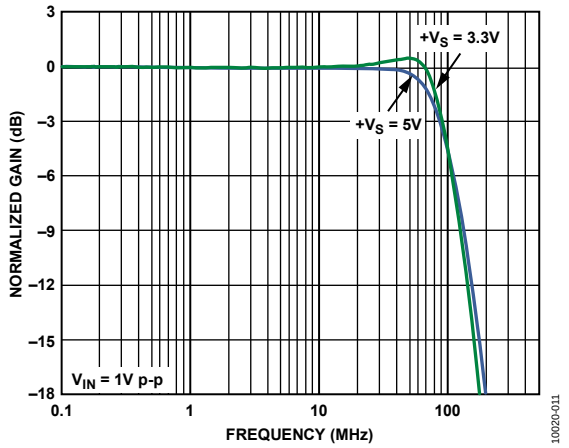


Figure 10. Large Signal Frequency Response for Various Supply Voltages

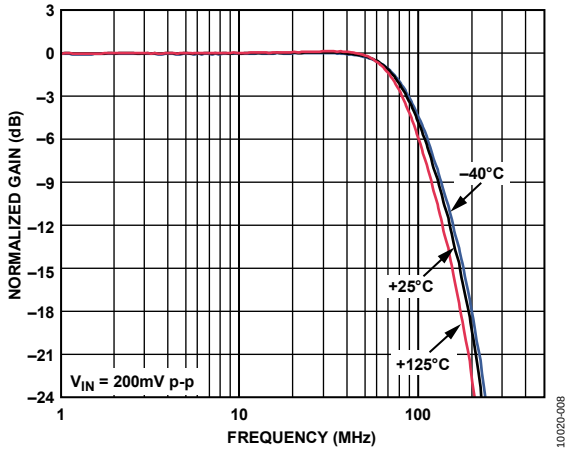


Figure 8. Small Signal Frequency Response for Various Temperatures

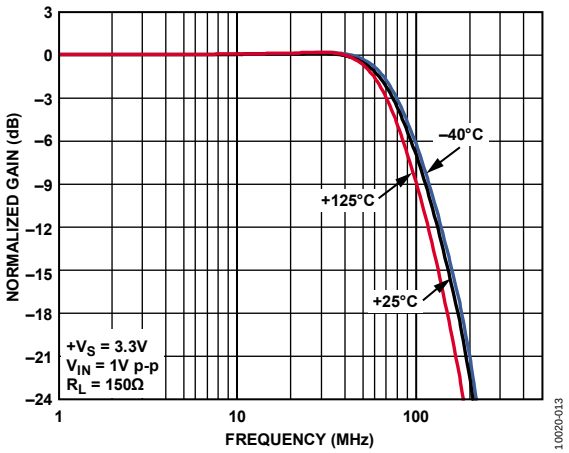


Figure 11. Large Signal Frequency Response for Various Temperatures

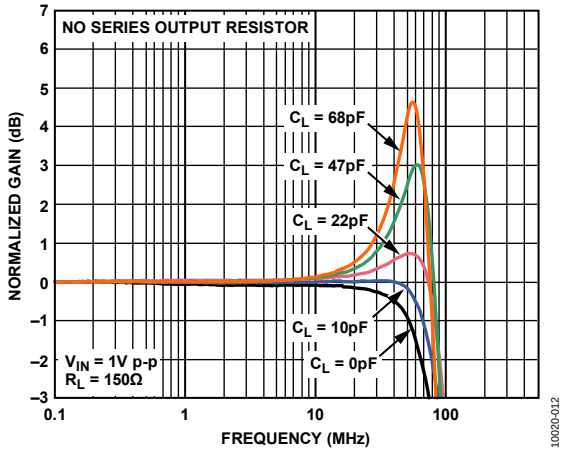


Figure 12. Large Signal Frequency Response for Various Capacitor Loads

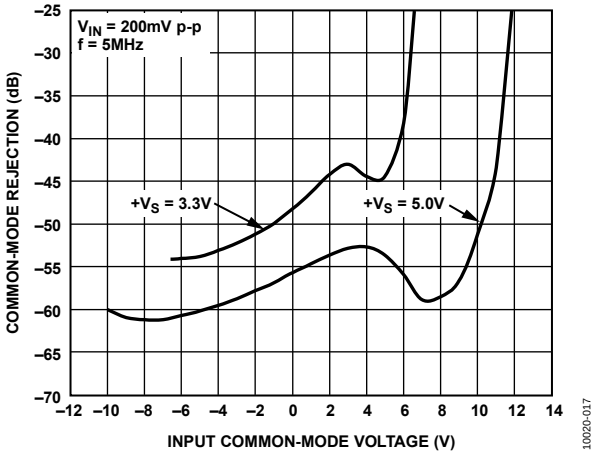


Figure 15. Small Signal CMR vs. V_{INCM} for Various Supply Voltages

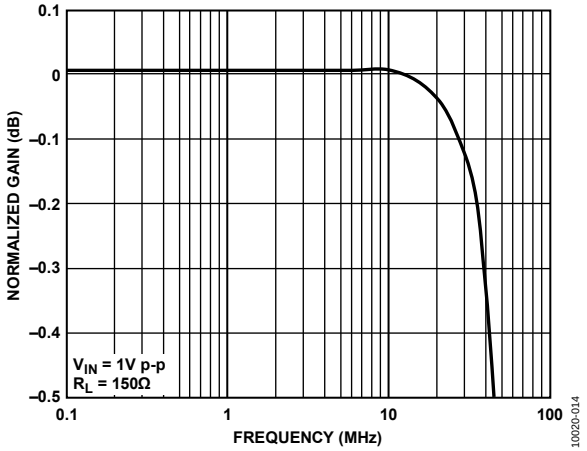


Figure 13. 0.1 dB Flatness

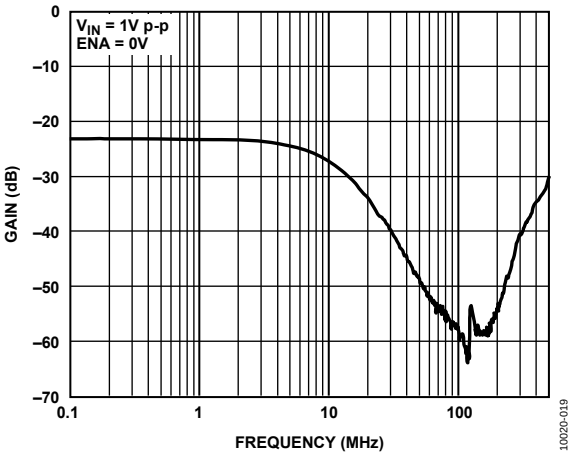


Figure 16. Input-to-Output Isolation with Device Disabled

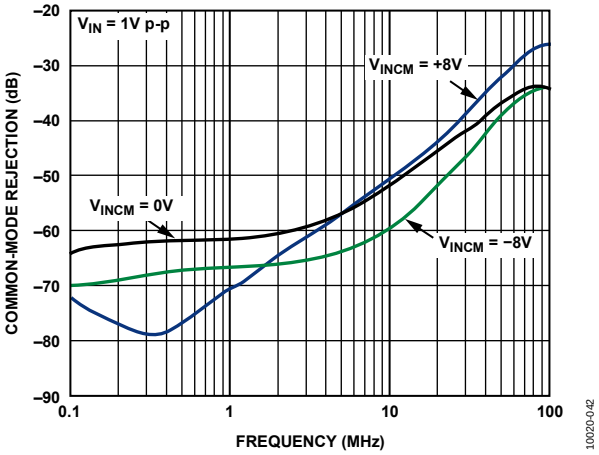


Figure 14. CMR Frequency Response for Various Input Common-Mode Voltages

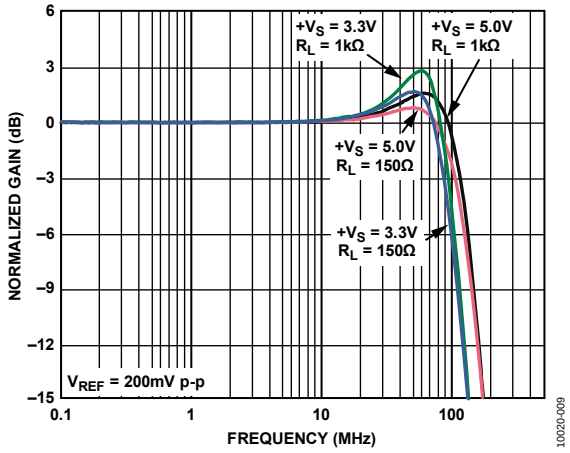


Figure 17. V_{REF} to V_{OUT} Frequency Response

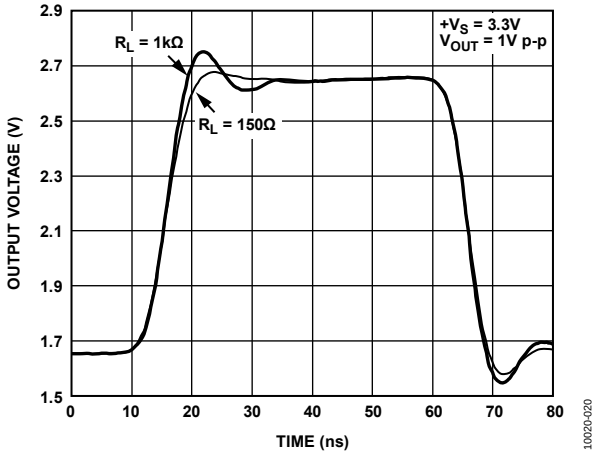


Figure 18. Pulse Response at $+V_S$ = 3.3 V

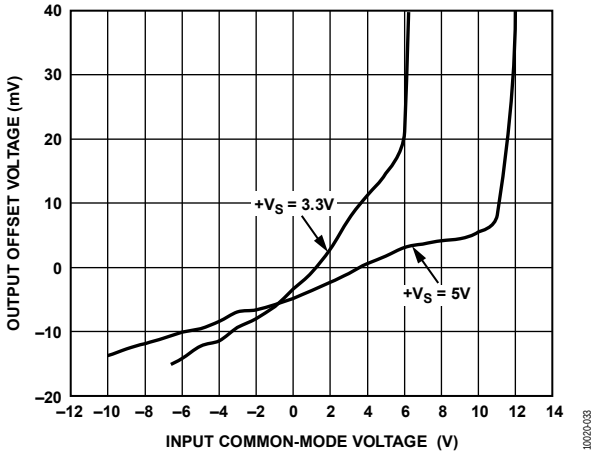


Figure 21. Output Offset Voltage (V_{OUT} – V_{REF}) vs. Input Common-Mode Voltage

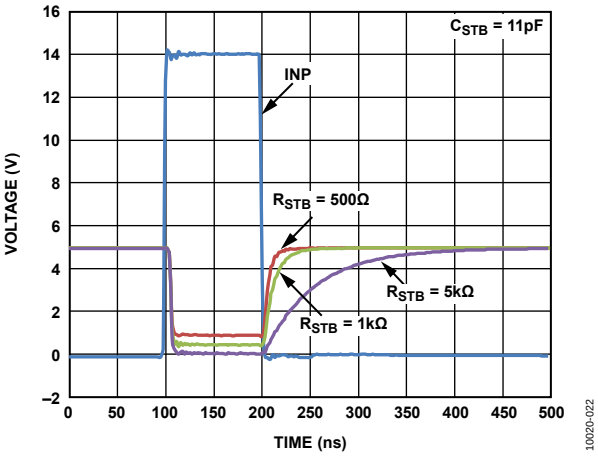


Figure 19. Short-to-Battery Output Flag Response for Various R_{STB}, ADA4830-1

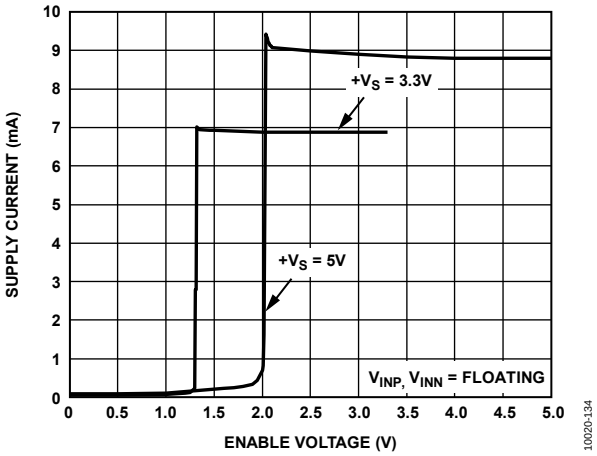


Figure 22. Supply Current vs. Enable Voltage

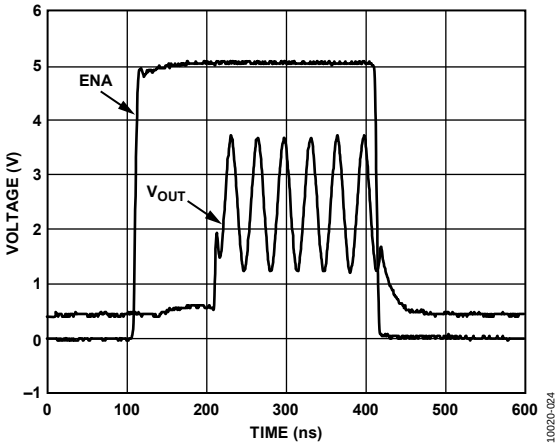


Figure 20. Enable Turn-on/Turn-off Time

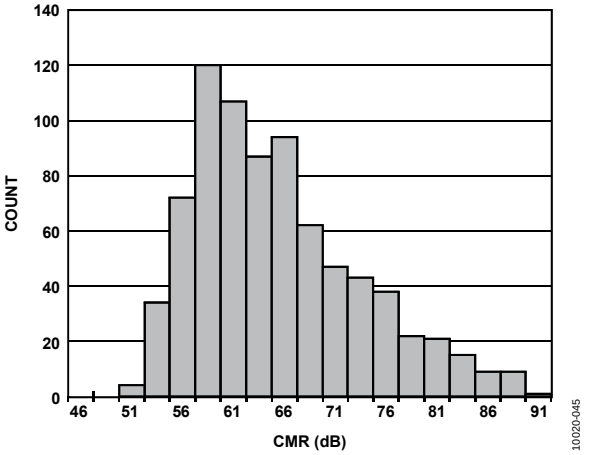


Figure 23. Typical Distribution of Common-Mode Rejection

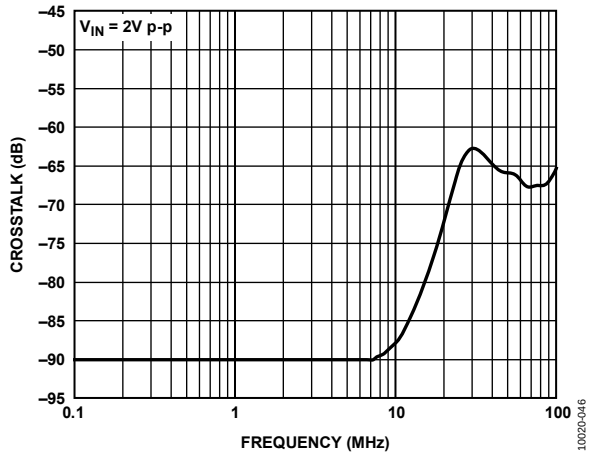


Figure 24. Crosstalk (Output-to-Output) vs. Frequency, ADA4830-2

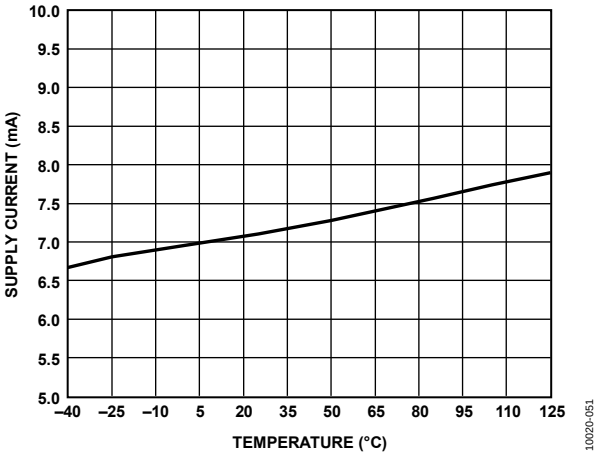


Figure 27. Supply Current vs. Temperature

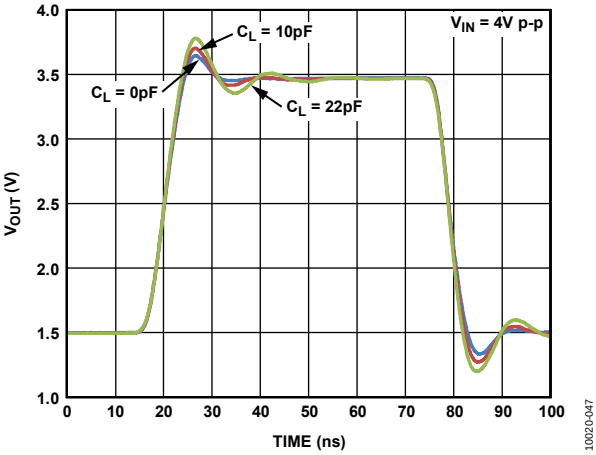


Figure 25. Pulse Response for Various Capacitor Loads

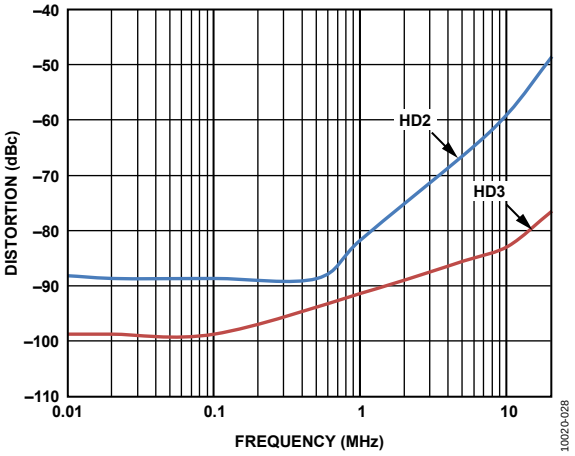


Figure 28. Harmonic Distortion Vs Frequency

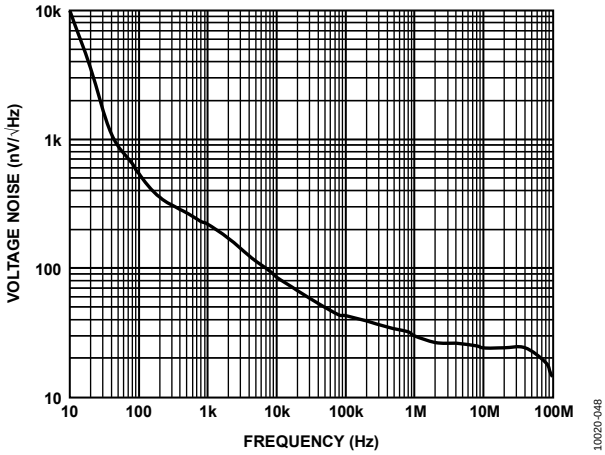


Figure 26. Total Output Voltage Noise vs. Frequency

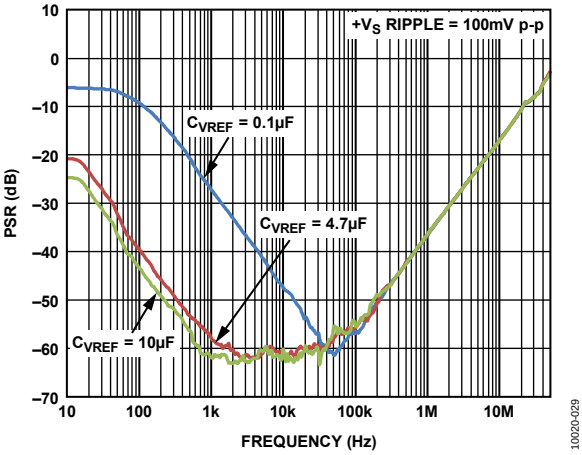


Figure 29. PSR vs. Frequency for Various VREF Bypass Capacitors

THEORY OF OPERATION

CORE AMPLIFIER

At the core of the ADA4830-1 and ADA4830-2 are high speed, rail-to-rail op amps that are built on a 0.35 µm CMOS process. Together with the core amplifier, the ADA4830-1 and ADA4830-2 combine four highly matched on-chip resistors into a difference amplifier function. Common-mode range extension at its inputs is achieved by employing a resistive attenuator. The closed-loop differential to single-ended gain of the video channel is internally fixed at 0.50 V/V (−6 dB) to ensure compatibility with video decoders whose input range is constrained to 1 V p-p or less. The transfer function of the ADA4830-1 and ADA4830-2 is

$$V_{OUT} = \frac{V_{INP} - V_{INN}}{2} + V_{REF}$$

where:
V_{OUT} is the voltage at the output pin, VOUT.
V_{INP} and V_{INN} are the input voltages at the INP and INN pins, respectively.
V_{REF} is the voltage at the VREF pin.

OVERVOLTAGE (SHORT-TO-BATTERY) PROTECTION

Robust inputs guarantee that sensitive internal circuitry is not subjected to extreme voltages or currents during a stressful event. A short-to-battery condition usually consists of a voltage on either input (or both inputs) that is significantly higher than the power supply voltage of the amplifier. Duration may vary from a short transient to a continuous fault.

The ADA4830-1 and ADA4830-2 can withstand voltages of up to 18 V on the inputs. Critical internal nodes are protected from exposure to high voltages by circuitry that clamps the inputs at a safe level and limits internal currents. This protection is available whether the device is enabled or disabled, even when the supply voltage is removed.

SHORT-TO-BATTERY OUTPUT FLAG

The short-to-battery output flag (STB pin) is functionally independent of the short-to-battery protection. Its purpose is to indicate an overvoltage condition on either input. Because protection is provided passively, it is always available; the flag merely indicates the presence or absence of a fault condition.

ESD PROTECTION

All pins on the ADA4830-1 and ADA4830-2 are protected with internal ESD protection structures connected to the power supply pins (+VS and GND). These structures provide protection during the handling and manufacturing process.

The inputs (INN and INP) of the ADA4830-1 and ADA4830-2 can be exposed to dc voltages well above the supply voltage; therefore, conventional ESD structure protection cannot be used.

The ADA4830-1 and ADA4830-2 employ Analog Devices, Inc., proprietary ESD devices at the input pins (INN, INP) to allow for a wide common-mode voltage range and ESD protection well beyond the handling and manufacturing requirements.

POWER SUPPLY PINS (ADA4830-2)

As indicated in the Absolute Maximum Ratings section, the voltage difference between the +VS1 and +VS2 pins of the ADA4830-2 cannot exceed 0.5 V. To ensure compliance with the Absolute Maximum Ratings, it is recommended that these supply pins be connected together to the same power supply source.

APPLICATIONS INFORMATION

METHODS OF TRANSMISSION

Pseudo Differential Mode (Unbalanced Source Termination)

The ADA4830-1 and ADA4830-2 can be operated in a pseudo differential configuration with an unbalanced input signal. This allows the receiver to be driven by a single-ended source. Pseudo differential mode uses a single conductor to carry an unbalanced signal and connects the negative input terminal to the ground reference of the source.

Use the positive wire or coaxial center conductor to connect the source output to the positive input (INP) of the ADA4830-1 or ADA4830-2. Next, connect the negative wire or coaxial shield from the negative input (INN) back to a ground reference on the source printed circuit board (PCB). The input termination should match the source impedance and be referenced to the remote ground. An example of this configuration is shown in Figure 30.

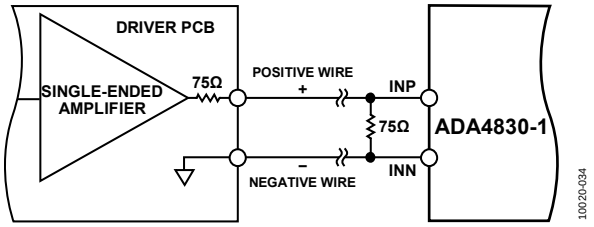


Figure 30. Pseudo Differential Mode

Pseudo Differential Mode (Balanced Source Impedance)

Pseudo differential signaling is typically implemented using unbalanced source termination, as shown in Figure 30. With this arrangement, however, common-mode signals on the positive and negative inputs receive different attenuation due to unbalanced termination at the source. This effectively converts some of the common-mode signal into differential mode signal, degrading the overall common-mode rejection of the system. System common-mode rejection can be improved by balancing the output impedance of the driver, as shown in Figure 31. Splitting the source termination resistance evenly between the hot and cold conductors results in matched attenuation of the common-mode signals, ensuring maximum rejection.

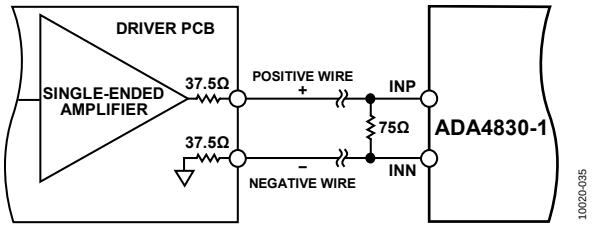


Figure 31. Pseudo Differential Mode with Balanced Source Impedance

Fully Differential Mode

The differential inputs of the ADA4830-1 and ADA4830-2 allow full balanced transmission using a differential source. In this configuration, the differential input termination is equal to twice the source impedance of each output. For example, a source with 37.5 Ω back termination resistors in each leg should be terminated with a differential resistance of 75 Ω. An illustration of this arrangement is shown in Figure 32.

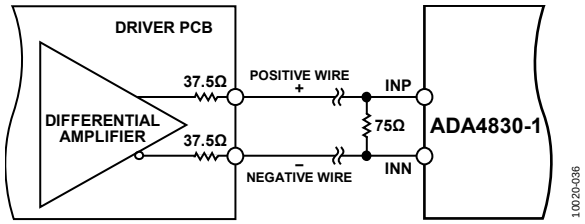


Figure 32. Fully Differential Mode

VOLTAGE REFERENCE (VREF PIN)

An internal reference level (V_{REF}) determines the output voltage when the differential input voltage is zero. A resistor divider connected between the supply rails sets the V_{REF} voltage. Built with a pair of matched 40 kΩ resistors, the divider sets this voltage to $+V_S/2$.

The voltage reference pin (VREF) normally floats at its default value of $+V_S/2$. However, it can be used to vary the output reference level from this default value. A voltage applied to VREF appears at the output with unity gain, within the bandwidth limit of the internal reference buffer. Figure 17 shows the frequency response of the VREF input.

Any noise on the $+V_S$ supply rail appears at the output with only 6 dB of attenuation (the divide-by-two provided by the reference divider). Even when this pin is floating, it is recommended that an external capacitor be connected from the reference node to ground to provide further attenuation of noise on the power supply line. A 4.7 µF capacitor combined with the internal 40 kΩ resistor sets the low-pass corner at under 1 Hz and results in better than 40 dB of supply noise attenuation at 100 Hz.

INPUT COMMON-MODE RANGE

In a standard four resistor difference amplifier with 0.50 V/V gain, the input common-mode (CM) range is three times the CM range of the core amplifier. In the ADA4830-1 and ADA4830-2, however, the input CM range has been extended to more than 18 V (with a 5 V supply). The input CM range can be approximated by using the following formulas:

For the maximum CM voltage,

$$5(+V_S - 1.25) - 4V_{REF} \approx V_{INCM(MAX)} \leq 9.5\ V$$

For the minimum CM voltage,

$$-10\ V \leq V_{INCM(MIN)} \approx -(1 + 4V_{REF})$$

Approximate minimum and maximum CM voltages are shown in Table 7 for several common supply voltages.

Table 7. Input Common-Mode Range Examples

$+V_S$ (V)	V_{REF} (V)	$V_{INCM(MIN)}$ (V)	$V_{INCM(MAX)}$ (V)
3.0	1.5[1]	−7.0	2.8
3.0	0.97	−4.9	4.9
3.3	1.65[1]	−7.6	3.6
3.3	1.15	−5.6	5.6
3.6	1.8[1]	−8.2	4.5
3.6	1.34	−6.4	6.4
5.0	2.5[1]	−10	8.7
5.0	2.22	−9.9	9.5

[1] Floating (default condition).

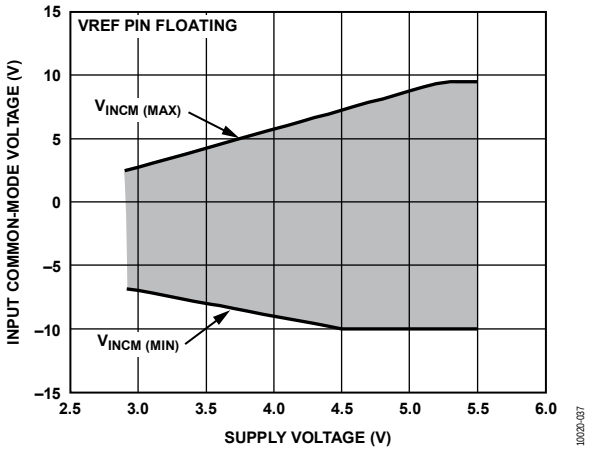


Figure 33. Input Common-Mode Range vs. Supply Voltage

SHORT-TO-BATTERY OUTPUT FLAG PIN

The flag output (STB) is an active low, open-drain logic configuration. A low level on this output indicates that an overvoltage event has been detected on either the positive or the negative input or both. Flags from multiple chips can be wire-OR'ed to form a single fault detection signal. The output is driven by a grounded source NMOS device, capable of sinking approximately 10 mA while pulling within a few hundred millivolts above ground. The output high level is set with an external pull-up resistor connected to the supply voltage of the logic family that is used to monitor the state of the flag.

In the falling direction, the speed with which the flag output responds primarily depends on the external capacitance attached to this node and the sink current that can be provided. For example, if the load is 10 pF, and the external pull-up voltage is 3.3 V, the fall time is a few nanoseconds. In the rising direction, the speed is determined by external capacitance and the magnitude of the pull-up resistor. For the case of 10 pF of external capacitance and a pull-up of 5 kΩ, the time constant of the rising edge is approximately 50 ns.

Table 8. STB Pin Function

STB Pin Output	Device State
High (Logic 1)	Normal operation
Low (Logic 0)	STB fault condition

ENABLE/DISABLE MODES (ENA PIN)

The power-down, or enable/disable (ENA) pin, is internally pulled up to $+V_S$ through a 250 kΩ resistor. When the voltage on this pin is high, the amplifier is enabled; pulling ENA low disables the channel. With no external connection, this pin floats high, enabling the amplifier channel.

Table 9. ENA Pin Function

ENA Pin Input	Device State
High (Logic 1)	Enabled
Low (Logic 0)	Disabled
High-Z (Floating)	Normal operation

PCB LAYOUT

As with all high speed applications, attention to PCB layout is of paramount importance. Adhere to standard high speed layout practices in designs using the ADA4830-1 and ADA4830-2. A solid ground plane is recommended, and placing a 0.1 µF surface-mount, ceramic power supply, decoupling capacitor as close as possible to the supply pin(s) is recommended.

Connect the GND pin(s) to the ground plane with a trace that is as short as possible. In cases where the ADA4830-1 and ADA4830-2 drive transmission lines, series terminate the outputs and use controlled impedance traces of the shortest length possible to connect to the signal I/O pins, which should not pass over any voids in the ground plane.

EXPOSED PADDLE (EPAD) CONNECTION

The ADA4830-1 and ADA4830-2 have an exposed thermal pad (EPAD) on the bottom of the package. This pad is not electrically connected to the die and can be left floating or connected to the ground plane. Should heat dissipation be a concern, thermal resistance can be minimized by soldering the EPAD to a metalized pad on the PCB. Connect this pad to the ground plane with multiple vias. Note that the thermal resistance (θ_{JA}) of the device is specified with the EPAD soldered to the PCB.

USING THE ADA4830-2 AS A LOW COST VIDEO SWITCH

Figure 34 shows a video multiplexer/switch using the ADA4830-2, dual, high speed difference amplifier. This circuit allows the user to input two remote video sources into a single channel of a video decoder, such as the ADV7180.

Traditional CMOS multiplexers and switches suffer several disadvantages at video frequencies where their on-resistance introduces distortion, degrades differential gain and phase performance, and interacts with the termination resistor to attenuate the incoming video signal and affect the luminance. System designers generally address these issues by adding external buffers to add gain and increase drive capability.

Video multiplexing can be simplified by using high speed video amplifiers with a disable/enable function (sometimes called power-down). When the amplifier is disabled, its output stage goes into a high impedance state, allowing several amplifier outputs to be wired together. High speed video op amps have all the key features required to make them ideal for this function. Their high input impedance does not affect the characteristic impedance of the transmission line, thus allowing back termination. They also have inherently good video specifications, including differential gain and phase, slew rate, bandwidth, and 0.1 dB flatness.

Each channel of the ADA4830-2 is a high speed difference amplifier circuit that eliminates common-mode noise and phase noise caused by ground potential differences between the incoming video signal and the receiver. The ADA4830-2 also offers integrated short-to-battery protection and heightened ESD tolerance in a small foot print. The fault detection output (the STB pins) of the ADA4830-2 allows for proactive wire diagnostics when connected to a microcontroller or video decoder and are used to generate an interrupt during a fault condition.

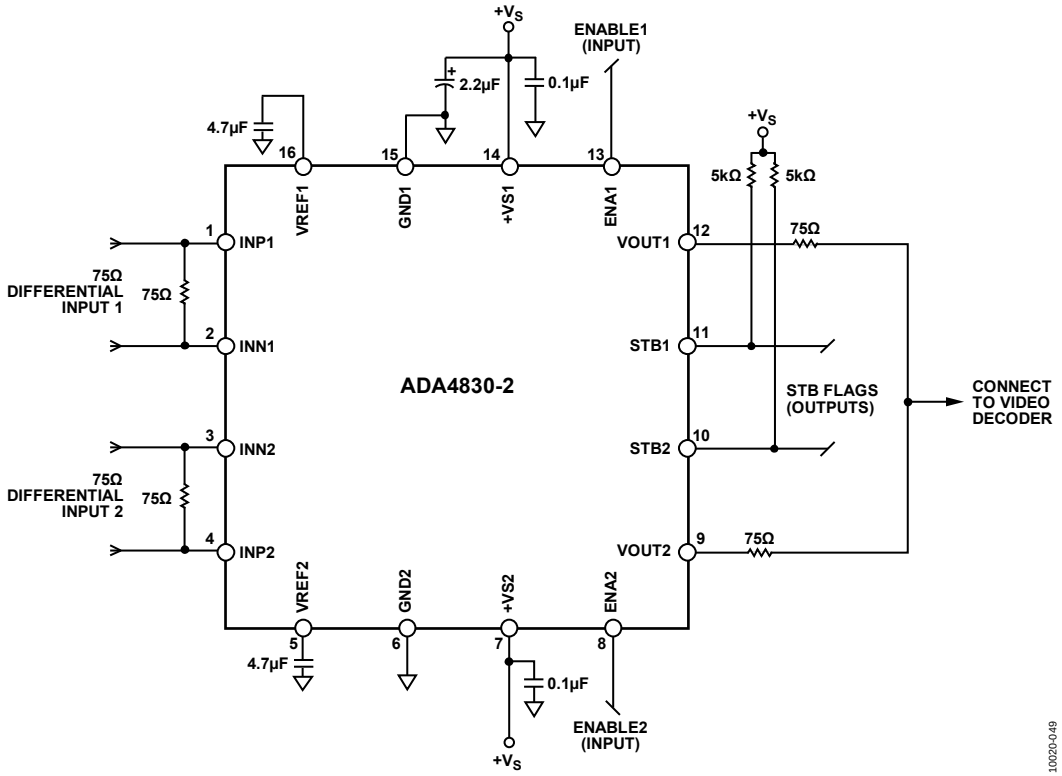


Figure 34. Low Cost Video Switch Using the ADA4830-2

DRIVING CAPACITIVE LOADS

The ADA4830-1 and ADA4830-2 are capable of driving large capacitive loads while maintaining its rated performance. Several performance curves vs. capacitive load are shown in Figure 12 and Figure 25. Capacitive loads interact with an op amp's output impedance to create an extra delay in the feedback path. This reduces circuit stability and can cause unwanted ringing and oscillation.

The capacitive load drive of the ADA4830-1and ADA4830-2 can be increased by adding a low valued resistor, R_S, in series with the capacitive load. Figure 35 shows the test circuit.

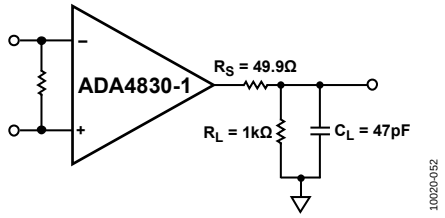


Figure 35. R_S Test Circuit

Introducing a series resistor tends to isolate the capacitive load from the feedback loop, thereby diminishing its influence. One drawback to this approach is a slight loss of signal amplitude. Figure 36 shows the effects of a series resistor on the capacitive drive. For very large capacitive loads, the frequency response of the amplifier is dominated by the roll-off of the series resistor and capacitive load.

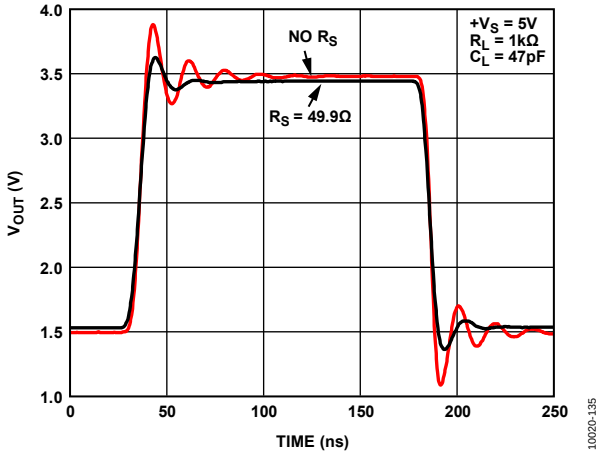


Figure 36. Pulse Response With and Without Series Resistor

Another method of reducing the resonant peaking caused by driving large capacitive loads at the output of the ADA4830-1 and ADA4830-2 is with the use of a R-C shunt circuit or a snubber circuit. This method acts to resistively load the amplifier output, thus reducing frequency response peaking. One drawback to this approach is a slight loss of signal bandwidth. Figure 37 shows a simple circuit representation of the implementation of the R-C snubber circuit with R_{SNT} and C_{SNT}. Figure 38 shows the effects of a R-C snubber circuit driving 47 pF, where R_{SNT} = 73.2 Ω and C_{SNT} = 0.1 µF.

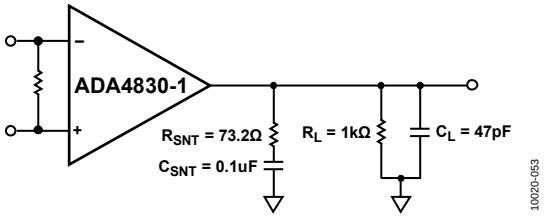


Figure 37. R-C Test Circuit

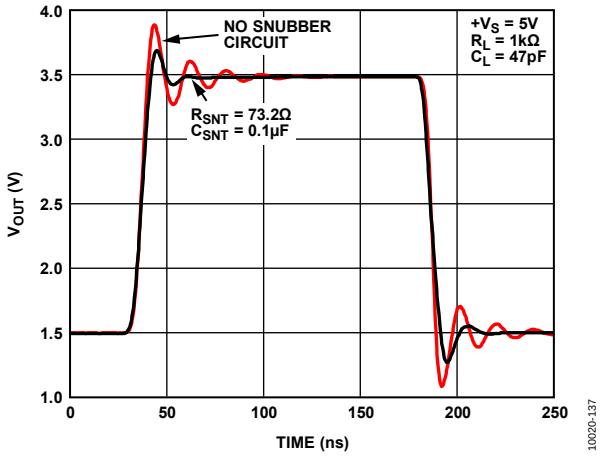


Figure 38. Pulse Response With and Without R-C Snubber Circuit

TYPICAL APPLICATIONS CIRCUITS

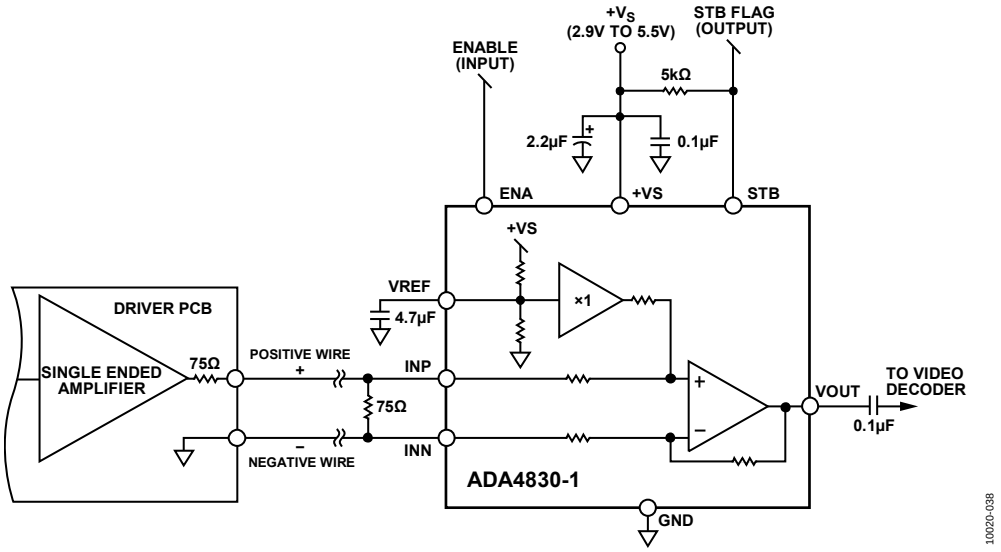


Figure 39. Typical Application with Pseudo Differential Input

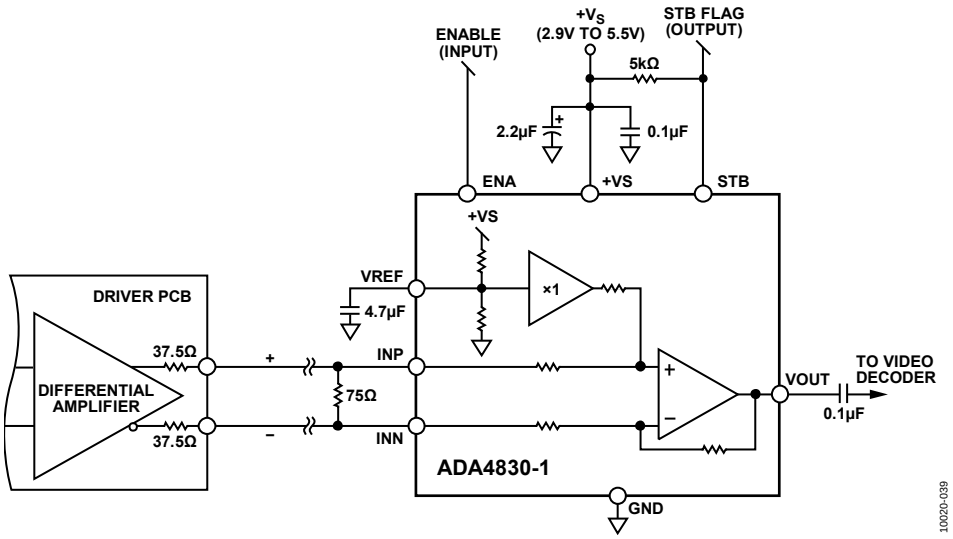


Figure 40. Typical Application with Fully Differential Input

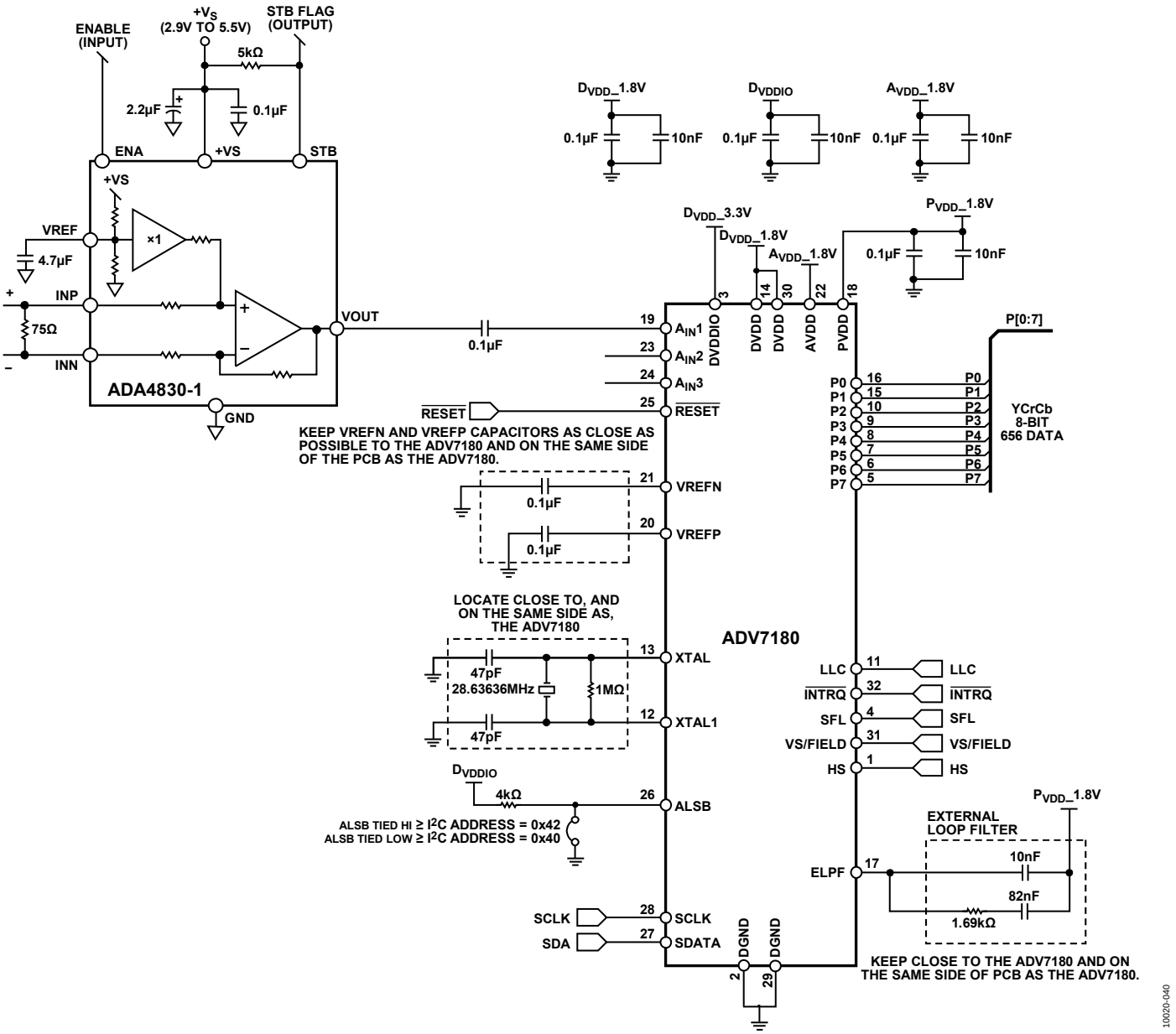


Figure 41. ADA4830-1 Driving an ADV7180 Video Decoder

The ADA4830-1 and ADA4830-2 are differential receivers whose overall performance is independent of the transmitter IC used and whether the transmission line is ac-coupled or dc-coupled.

The ADA4830-1 and ADA4830-2 are specifically designed to perform as differential line receivers. The circuit in Figure 41 shows a detailed schematic of the ADA4830-1 and the ADV7180 configured for this function. The signal is received differentially relative to the common of the source circuitry, and that voltage is exactly reproduced with an attenuating gain of 0.50 V/V. This is designed to keep the video signal within the allowed range of the video decoder, which is typically 1 V p-p or less.

The common-mode rejection vs. frequency, shown in Figure 14, typically 65 dB at low frequencies, enables the recovery of video signals in the presence of large common-mode noise. The high input impedance permits the ADA4830-1 and ADA4830-2 to operate as a bridging amplifier across low impedance terminations with negligible loading.

FULLY DC-COUPLED TRANSMISSION LINE

The wide input common-mode range and high input impedance of the ADA4830-1 and ADA4830-2 allow them to be used in fully dc-coupled transmission line applications in which there may be a significant discrepancy between voltage levels at the ground pins of the driver and receiver. As long as the voltage difference between reference levels at the transmitter and receiver is within the common-mode range of the receiver, very little current flow results, and no image degradation should be anticipated.

Figure 42 shows an example configuration of a completely dc-coupled transmission using a low impedance differential driver.

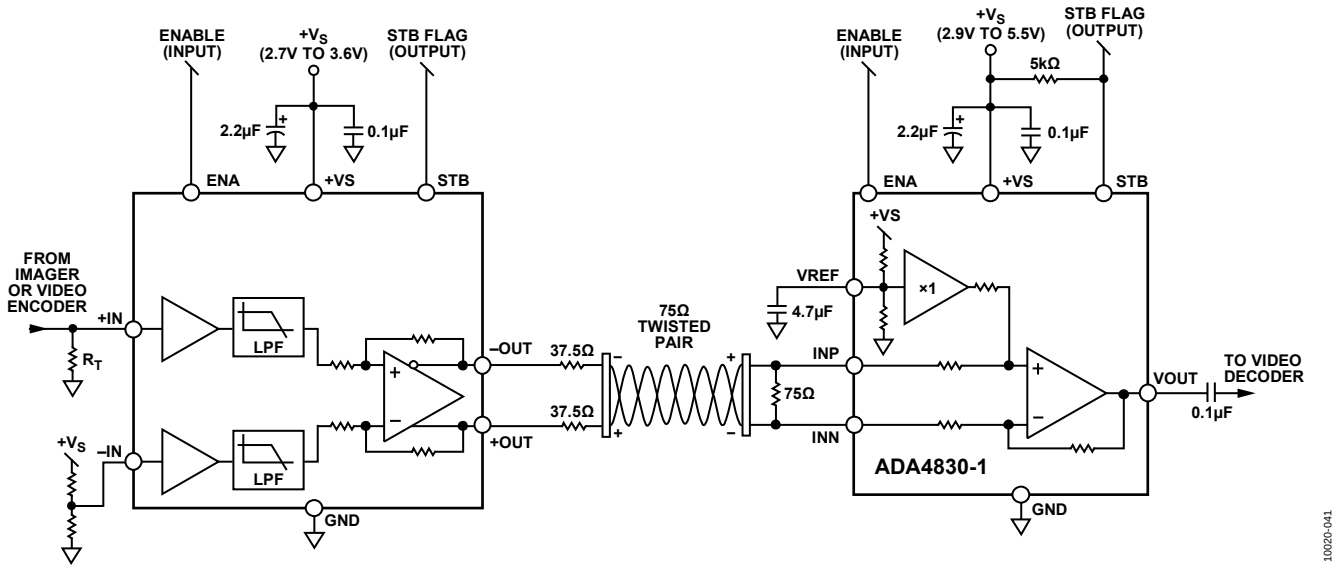
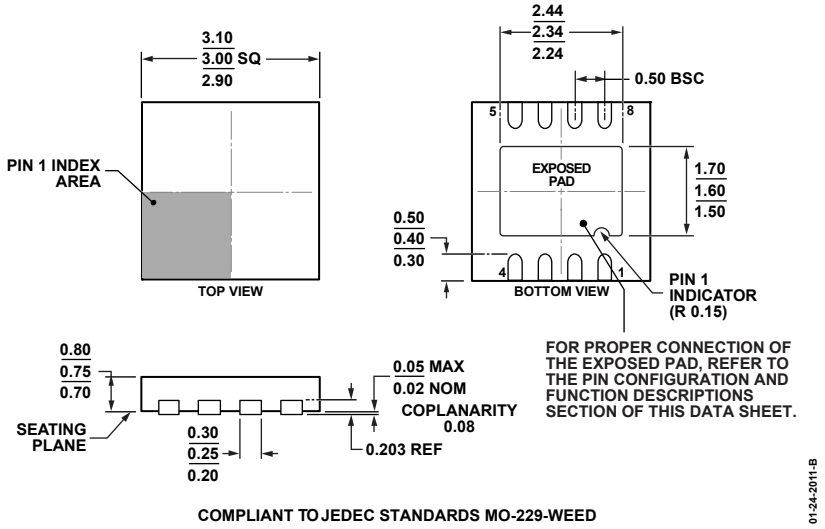


Figure 42. Differential Video Filter Driver and ADA4830-1 Difference Amplifier

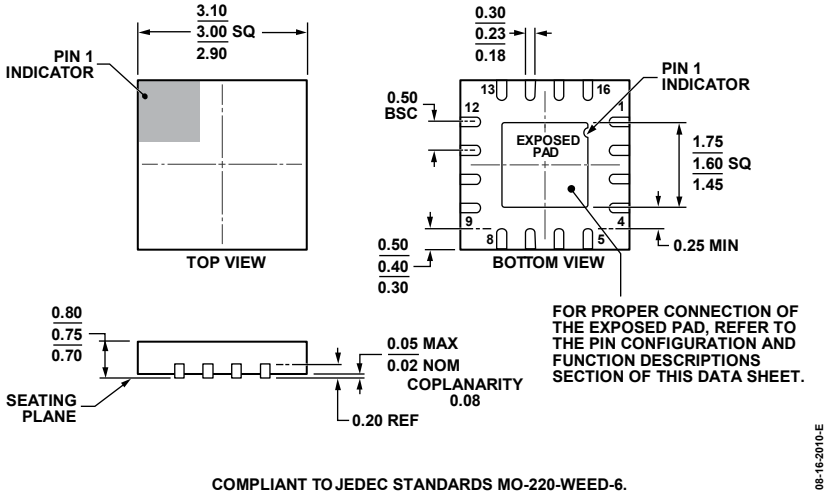
PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 43. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-8-11)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 44. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-16-22)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADA4830-1BCP-EBZ		Evaluation Board			
ADA4830-1BCPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	H30	1,500
ADA4830-1BCPZ-R2	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-11	H30	250
ADA4830-2BCPZ-R7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	H31	1,500
ADA4830-2BCPZ-R2	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-22	H31	250

[1] Z = RoHS Compliant Part.