

Quartus II Design Software

Fastest Path to Your Design

Quartus® II software is number one in performance and productivity for Altera® FPGAs, CPLDs, and HardCopy® ASICs, providing the fastest path to convert your concept into reality. Quartus II software can easily adapt to your specific needs in all phases of FPGA and CPLD design in different platforms.

Simulation and system-level tools integrated with Quartus II software design flow are as follows:

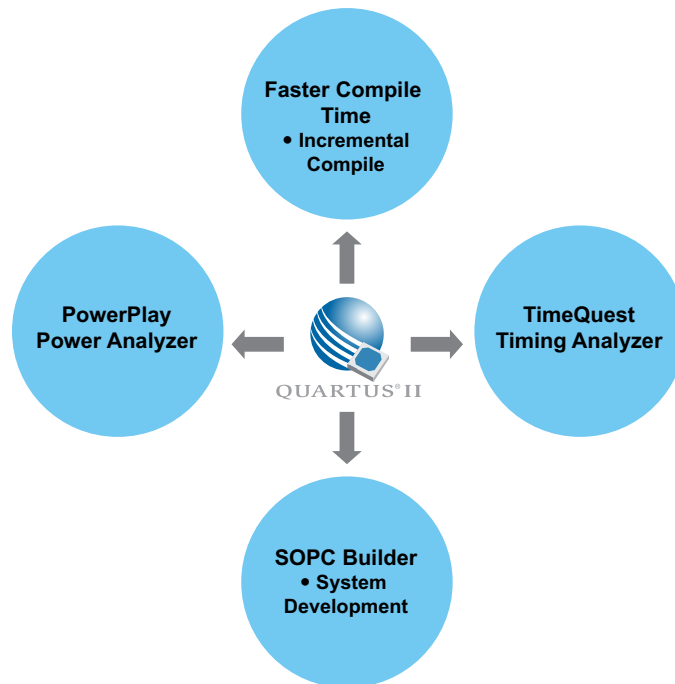
- ModelSim® software (included with free or subscription package)
- DSP Builder (requires additional license)
- Qsys (part of Quartus II software)
- Other third-party EDA tools

ModelSim

DSP Builder

 **Qsys**

Quartus II Software Key Features

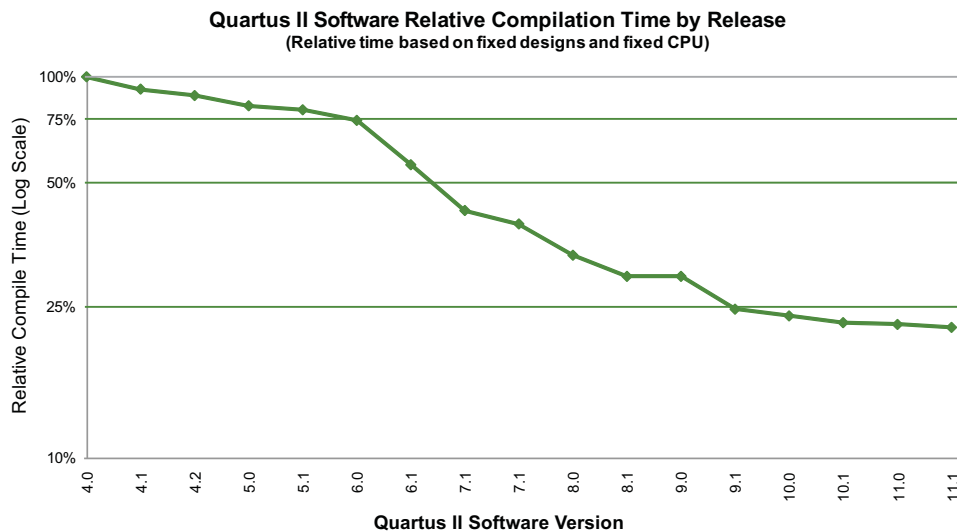


Industry-Leading Compile Time

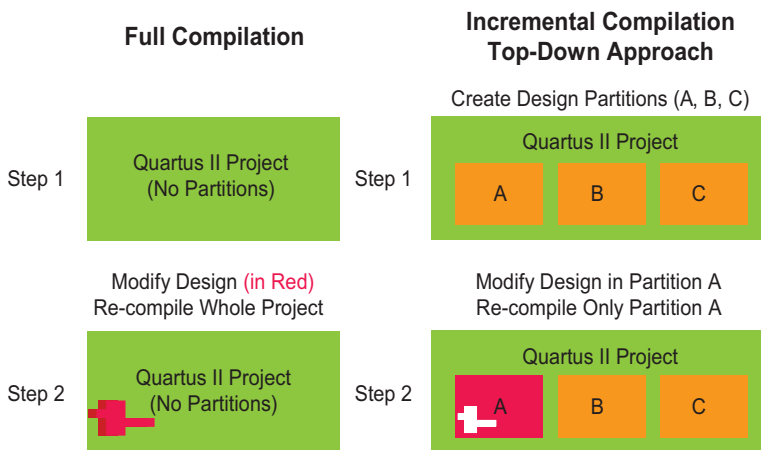
Quartus II software delivers superior synthesis and placement and routing, resulting in compilation time advantages for both Web Edition and Subscription Edition. Additional compilation time reduction features for Subscription Edition include the following:

- Multiprocessor support
- Rapid Recompile
- Incremental compile

Compile Time Comparison



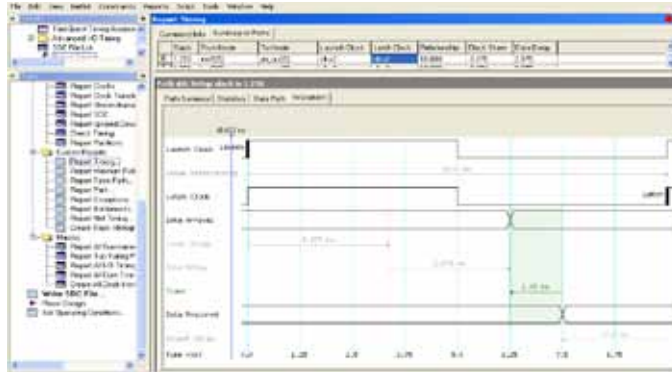
Compare Full and Incremental Compile



Incremental Compile

- Compiles only the changes in a partition to reduce compile time by up to 70 percent
- Preserves timing in unchanged partitions for performance preservation
- Enables team-based designs

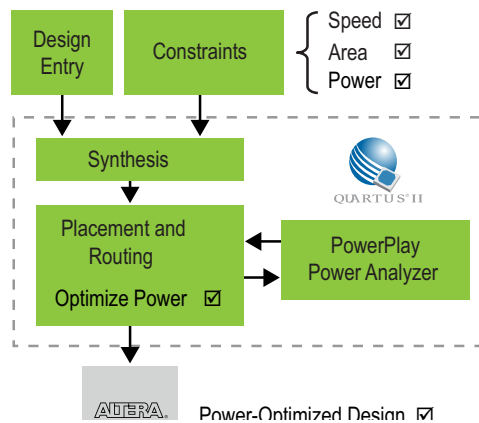
TimeQuest Timing Analyzer



TimeQuest Timing Analyzer GUI

- The only FPGA vendor with comprehensive Synopsys Design Constraints (SDC) support
- Second-generation, easy-to-use timing analyzer
- Complete GUI environment and scripting support to create timing constraints and reports
- Easy-to-use wizard to create SDC constraints

PowerPlay Power Analyzer Flow



PowerPlay Power Analyzer

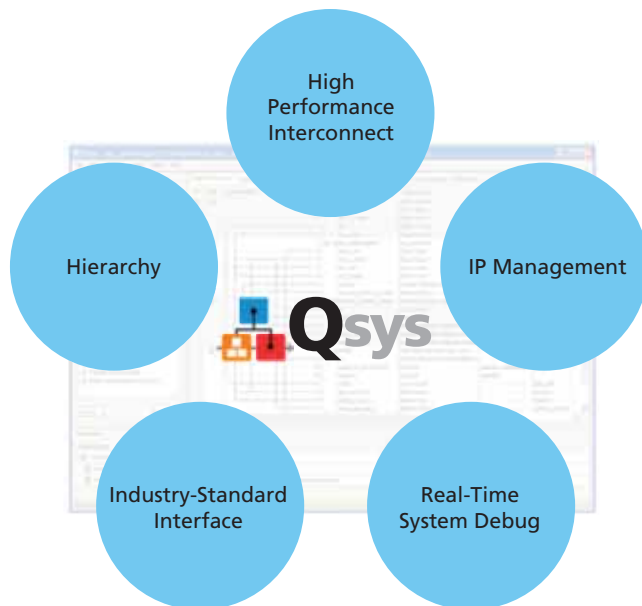
- Push-button power optimization technology
- Automated power optimization for an average 10 percent reduction in power consumption

Qsys System Integration Tool

The Qsys system integration tool saves significant time and effort in the FPGA design process by automatically generating interconnect logic to connect intellectual property (IP) functions and subsystems. Qsys is the next-generation SOPC Builder tool powered by a new FPGA-optimized network-on-a-chip (NoC) technology, delivering higher performance, improved design reuse, and faster verification compared to SOPC Builder.

- High-performance Qsys interconnect based on the NoC architecture and automatic pipelining delivers up to 2X higher performance compared to SOPC Builder's system interconnect fabric
- Hierarchical design flow enables scalable designs, supports team-based design, and maximizes design reuse
- Higher flexibility with support for mixing different industry-standard interfaces, such as the AMBA® AXI™ and Avalon® interfaces
- IP management capabilities enable designs and systems to appear as an IP for easier reuse
- Faster board bring-up with a system-level debug approach using address-based transactions and System Console

Qsys – Altera's System Integration Tool



Quartus II Software Design Flow

Quartus II Software Design Flow			
	Quartus II Software Key Features	Availability	
		Subscription Edition	Web Edition (Free)
Design Entry	Cyclone® FPGA and MAX® CPLD series device support	✓	✓
	Arria® and Stratix® FPGA series device support ¹	✓	
	HardCopy ASIC device support	✓	
	Multiprocessor support (Faster compile time support)	✓	
	IP Base Suite (Includes licenses for 14 popular IP cores)	✓	
	Qsys (Next-generation system integration tool)	✓	✓
	SOPC Builder (Legacy system development tool)	✓	✓
	Rapid Recompile (Faster compile for small design changes)	✓	
	Incremental compile (Performance preservation and team-based design)	✓	
Functional Simulation	ModelSim®-Altera Starter Edition	✓	✓
	ModelSim-Altera Edition	✓ ²	✓ ²
Synthesis	Quartus Integrated Synthesis (Synthesis tool)	✓	✓
Placement and Route	Fitter (Placement and routing tool)	✓	✓
Timing and Power Verification	TimeQuest tool (Static timing analysis)	✓	✓
	PowerPlay tool and optimization (Power analysis)	✓	✓
In-System Debug	SignalTap™ II logic analyzer (Embedded logic analyzer) ³	✓	
	Transceiver Toolkit (Transceiver interface and verification tool)	✓	
	Operating System Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 32-Bit support	✓	✓
	Windows/Linux 64-Bit support	✓	

¹Lowest density devices for Arria II FPGA series is included in Web Edition.

²Requires additional license.

³Available with talkback feature enabled in Web Edition.

Quartus II Software Ordering Information

Purchase Quartus II software and increase your productivity today.

Pricing	Description
\$2,995 (SW-QUARTUS-SE-FIX) Renewal \$2,495 (SWR-QUARTUS-SE-FIX)	Fixed-node license: Subscription for one year—Windows only
\$3,995 (SW-QUARTUS-SE-FLT) Renewal \$2,495 (SWR-QUARTUS-SE-FLT) Add seat \$3,995 (SW-QUARTUS-SE-ADD)	Floating-node license: Subscription for one year—Windows/Linux

ModelSim-Altera Edition	
\$945 (SW-MODELSIM-AE) Renewal \$945 (SWR-MODELSIM-AE)	ModelSim-Altera Edition is available as a \$945 option for both Quartus II Subscription Edition and Web Edition software. It's 33 percent faster than Starter Edition with no line limitation.
ModelSim-Altera Starter Edition	
Free	Free for both Quartus II Subscription Edition and Web Edition software with a 10,000 executable line limitation, ModelSim-Altera Starter Edition is recommended for simulating small FPGA designs.

Want to Dig Deeper?

Are you ready to accelerate your design process? Take these steps to gain proficiency in designing with Quartus II software:

- Download free Web Edition or 30-day Subscription Edition trial
- Get oriented with the Quartus II Software Interactive Tutorial
- Sign up for training.

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