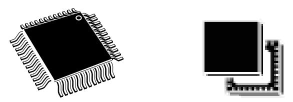
STM32F050x4 STM32F050x6

Low- and medium-density advanced ARM™-based 32-bit MCU with up to 32 Kbytes Flash, timers, ADC and comm. interfaces

Datasheet — production data

Features

- Operating conditions:
  - Voltage range: 2.0 V to 3.6 V
- ARM 32-bit Cortex®-M0 CPU (48 MHz max)
- Memories
  - 16 to 32 Kbytes of Flash memory
  - 4 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Reset and supply management
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Low power Sleep, Stop, and Standby modes
- V_{BAT} supply for RTC and backup registers
- 5-channel DMA controller
- 1 × 12-bit, 1.0 µs ADC (up to 10 channels)
  - Conversion range: 0 to 3.6V
  - Separate analog supply from 2.4 up to 3.6 V
- Up to 39 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 25 I/Os with 5 V tolerant capability
- 96-bit unique ID
- Serial wire debug (SWD)
- Up to 9 timers
  - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - One 32-bit and one 16-bit timer, with up to 4 IC/OC, usable for IR control decoding



LQFP48 7x7 UFQFPN32 5x5

  - One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - One 16-bit timer, with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - One 16-bit timer with 1 IC/OC
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
- Communication interfaces
  - One I^2C interface; supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, and wakeup from STOP
  - One USART supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA capability auto baud rate detection and wakeup feature
  - One SPI (18 Mbit/s) with 4 to 16 programmable bit frame, with I^2S interface multiplexed

Table 1. Device summary

Reference	Part number
STM32F050x4	STM32F050K4, STM32F050C4
STM32F050x6	STM32F050K6, STM32F050C6

Contents

List of tables

List of figures

1 Description

The STM32F050xx family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz maximum frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 4 Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I^2C, one SPI, one I2S, and one USART), one 12-bit ADC, up to five general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F050xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F050xx family includes devices in two different packages ranging from 32 pins to 48 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of peripherals proposed in this family.

These features make the STM32F050xx microcontroller family suitable for a wide range of applications such as control application and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F050xx family device features and peripheral counts

Peripheral		STM32F050Kx		STM32F050Cx	
Flash (Kbytes)		16	32	16	32
SRAM (Kbytes)		4		4	
Timers	Advanced control	1 (16-bit)			
	General purpose	4 (16-bit) 1 (32-bit)			
Comm. interfaces	SPI (I2S)(1)	1			
	I^2C	1			
	USART	1			
12-bit synchronized ADC (number of channels)		1 (10 ext. + 3 int.)			
GPIOs		27		39	
Max. CPU frequency		48 MHz			
Operating voltage		2.0 to 3.6 V			
Operating temperature		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 °C to 125 °C			
Packages		UFQFPN32		LQFP48	

1. The SPI interface can be used either in SPI mode or in I2S audio mode.

2 Device overview

Figure 1. Block diagram

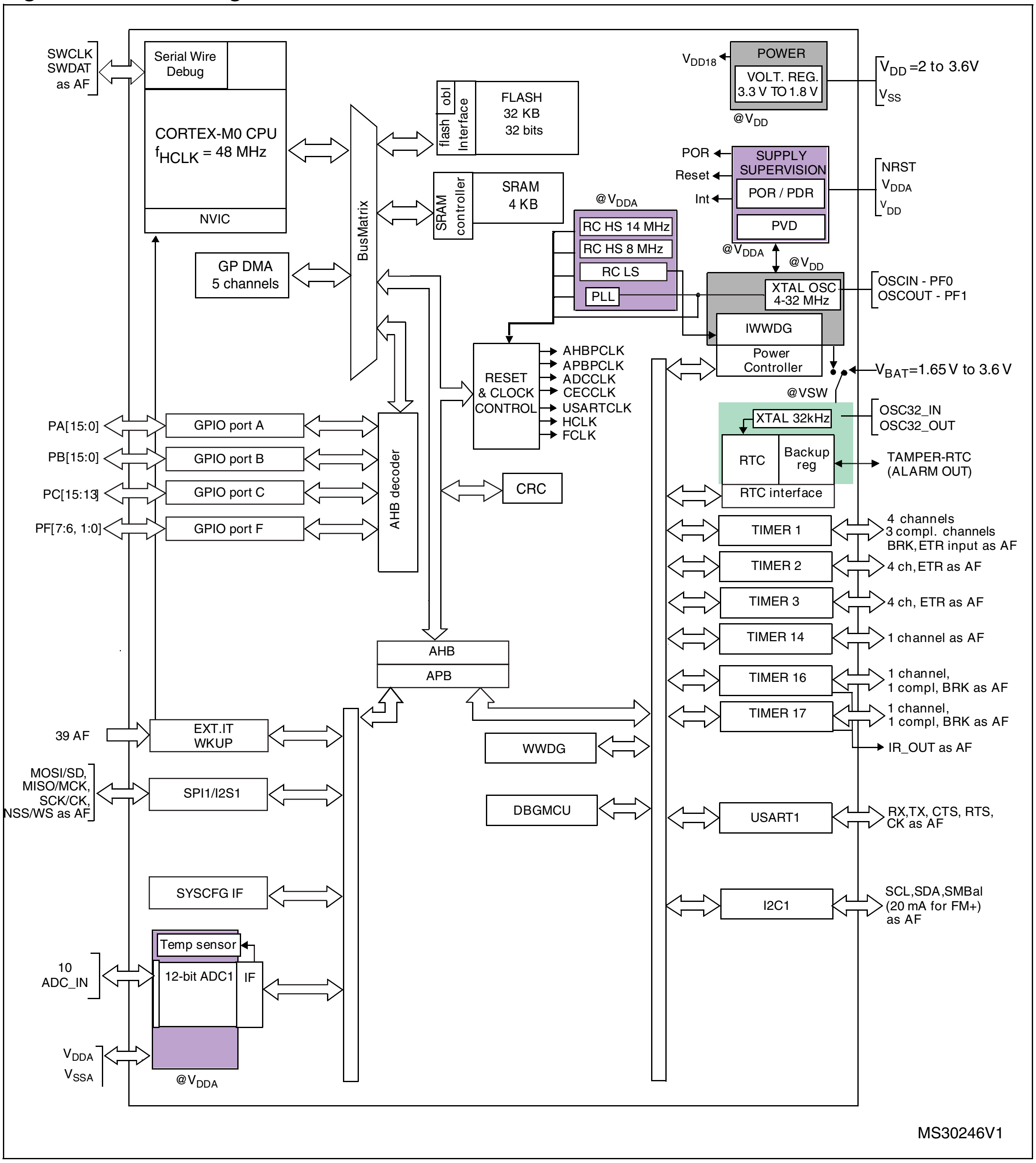
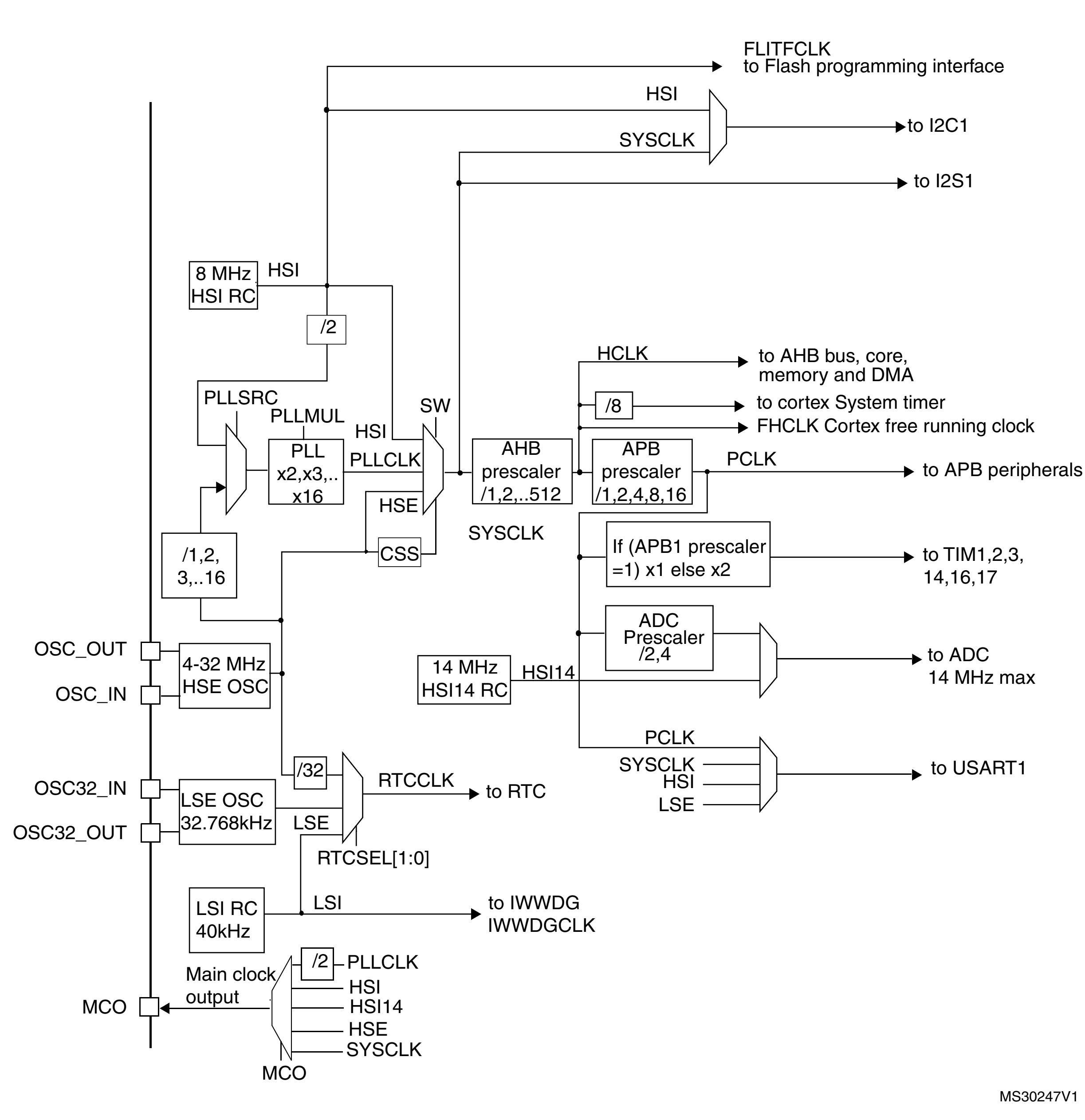


Figure 2. Clock tree



3 Functional overview

3.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F050xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

3.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 96-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.4 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.5 Nested vectored interrupt controller (NVIC)

The STM32F050xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.6 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 39 GPIOs can be connected to the 16 external interrupt lines.

3.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

3.8 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

3.9 Power management

3.9.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.6 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.9.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.9.3 Voltage regulator

The regulator has three operating modes: main (MR), low power (LPR) and power down.

- MR is used in normal operating mode (Run)
- LPR can be used in Stop mode where the power demand is reduced
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

3.10 Low-power modes

The STM32F050xx family supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, I2C1 or USART1.

  The I2C1 and the USART1 can be configured to enable the HSI RC oscillator for processing incoming data. If this is used, the voltage regulator should not be put in the low-power mode but kept in normal mode.
- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pins, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.11 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

3.12 Timers and watchdogs

The STM32F050xx family devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes

3.12.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.12.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F050xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F050xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM16 and TIM17 timers can work together via the Timer Link feature for synchronization or event chaining.

TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

3.12.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.12.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HCLK or HCLK/8)

3.13 Inter-integrated circuit interface (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave mode. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). It also includes programmable analog and digital noise filters.

Table 4. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	$\geq$ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

3.14 Universal synchronous/asynchronous receiver transmitter (USART)

The device embeds an universal synchronous/asynchronous receiver transmitters (USART1), which communicates at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. It also supports SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing it to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

3.15 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

The SPI (SPI1) is able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at simplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

3.16 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.17 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.17.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 5. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C V_{DDA}= 3.3 V	0x1FFF F7C2 - 0x1FFF F7C3

3.17.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 6. Temperature sensor calibration values

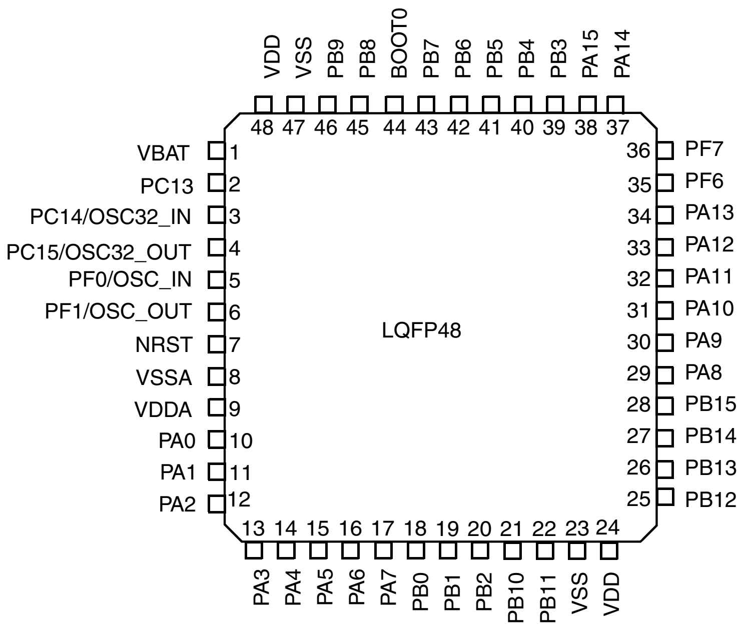
Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C V_{DDA}= 3.3 V	0x1FFF F7BA - 0x1FFF F7BB

3.18 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

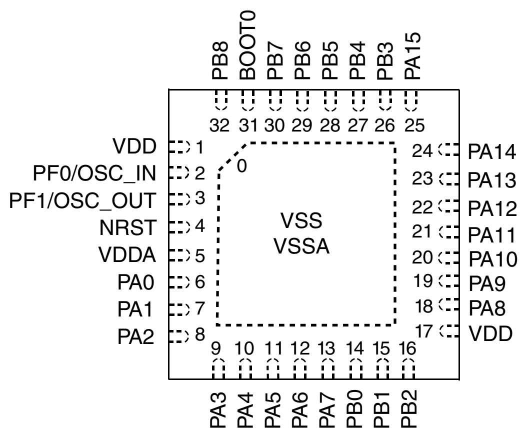
4 Pinouts and pin description

Figure 3. LQFP48 48-pin package pinout



MS19842V1

Figure 4. UFQFPN32 32-pin package pinout



MS19844V2

Table 7. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. Pin definitions

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32					Alternate functions	Additional functions
1		VBAT	S			Backup power supply	
2		PC13	I/O	TC	(1)(2)		RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3		PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)		OSC32_IN
4		PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)		OSC32_OUT
5	2	PF0-OSC_IN (PF0)	I/O	FT			OSC_IN
6	3	PF1-OSC_OUT (PF1)	I/O	FT			OSC_OUT
7	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	

Table 8. Pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32					Alternate functions	Additional functions
8	0	VSSA	S			Analog ground	
9	5	VDDA	S			Analog power supply	
10	6	PA0	I/O	TTa		TIM2_CH1_ETR	ADC_IN0, RTC_TAMP2, WKUP1
11	7	PA1	I/O	TTa		TIM2_CH2, EVENTOUT	ADC_IN1
12	8	PA2	I/O	TTa		TIM2_CH3	ADC_IN2
13	9	PA3	I/O	TTa		TIM2_CH4	ADC_IN3
14	10	PA4	I/O	TTa		SPI1_NSS/I2S1_WS, TIM14_CH1	ADC_IN4
15	11	PA5	I/O	TTa		SPI1_SCK/I2S1_CK, TIM2_CH_ETR	ADC_IN5
16	12	PA6	I/O	TTa		SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6
17	13	PA7	I/O	TTa		SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
18	14	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
19	15	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
20	16	PB2	I/O	FT			
21		PB10	I/O	FT		TIM2_CH3	
22		PB11	I/O	FT		TIM2_CH4, EVENTOUT	
23	0	VSS	S			Digital ground	
24	17	VDD	S			Digital power supply	
25		PB12	I/O	FT		TIM1_BKIN, EVENTOUT	
26		PB13	I/O	FT		TIM1_CH1N,	
27		PB14	I/O	FT		TIM1_CH2N	
28		PB15	I/O	FT		TIM1_CH3N,	RTC_REFIN
29	18	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	
30	19	PA9	I/O	FT		USART1_TX, TIM1_CH2	

Table 8. Pin definitions (continued)

Pin number		Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32					Alternate functions	Additional functions
31	20	PA10	I/O	FT		USART1_RX, TIM1_CH3, TIM17_BKIN	
32	21	PA11	I/O	FT		USART1_CTS, TIM1_CH4, EVENTOUT	
33	22	PA12	I/O	FT		USART1_RTS, TIM1_ETR, EVENTOUT	
34	23	PA13 (SWDAT)	I/O	FT	(3)	IR_OUT, SWDAT	
35		PF6	I/O	FT			
36		PF7	I/O	FT			
37	24	PA14 (SWCLK)	I/O	FT	(3)	SWCLK	
38	25	PA15	I/O	FT		SPI1_NSS/I2S1_WS, TIM2_CH_ETR, EVENTOUT	
39	26	PB3	I/O	FT		SPI1_SCK/I2S1_CK, TIM2_CH2, EVENTOUT	
40	27	PB4	I/O	FT		SPI1_MISO/I2S1_MCK, TIM3_CH1, EVENTOUT	
41	28	PB5	I/O	FT		SPI1_MOSI/I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	
42	29	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N	
43	30	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N	
44	31	BOOT0	I	B		Boot memory selection	
45	32	PB8	I/O	FTf		I2C1_SCL, TIM16_CH1	
47	0	VSS	S			Digital ground	
48	1	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as a current sources (e.g. to drive an LED).
2. After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the STM32F05xx reference manual.
3. After reset, these pins are configured as SWDAT and SWCLK alternate functions, and the internal pull-up on SWDAT pin and internal pull-down on SWCLK pin are activated.

Table 9. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0			TIM2_CH1_ ETR					
PA1	EVENTOUT		TIM2_CH2					
PA2			TIM2_CH3					
PA3			TIM2_CH4					
PA4	SPI1_NSS/ I2S1_WS				TIM14_CH1			
PA5	SPI1_SCK/ I2S1_CK	CEC	TIM2_CH1_ ETR					
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN			TIM16_CH1	EVENTOUT	
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N		TIM14_CH1	TIM17_CH1	EVENTOUT	
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT				
PA9		USART1_TX	TIM1_CH2					
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3					
PA11	EVENTOUT	USART1_CTS	TIM1_CH4					
PA12	EVENTOUT	USART1_RTS	TIM1_ETR					
PA13	SWDAT	IR_OUT						
PA14	SWCLK							
PA15	SPI1_NSS/ I2S1_WS		TIM2_CH1_ ETR	EVENTOUT				

Table 10. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	
PB2				
PB3	SPI1_SCK/I2S1_CK	EVENTOUT	TIM2_CH2	
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	EVENTOUT	
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	
PB8		I2C1_SCL	TIM16_CH1	
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10			TIM2_CH3	
PB11	EVENTOUT		TIM2_CH4	
PB12		EVENTOUT	TIM1_BKIN	
PB13			TIM1_CH1N	
PB14			TIM1_CH2N	
PB15			TIM1_CH3N	

5 Memory mapping

Figure 5. STM32F050xx memory map

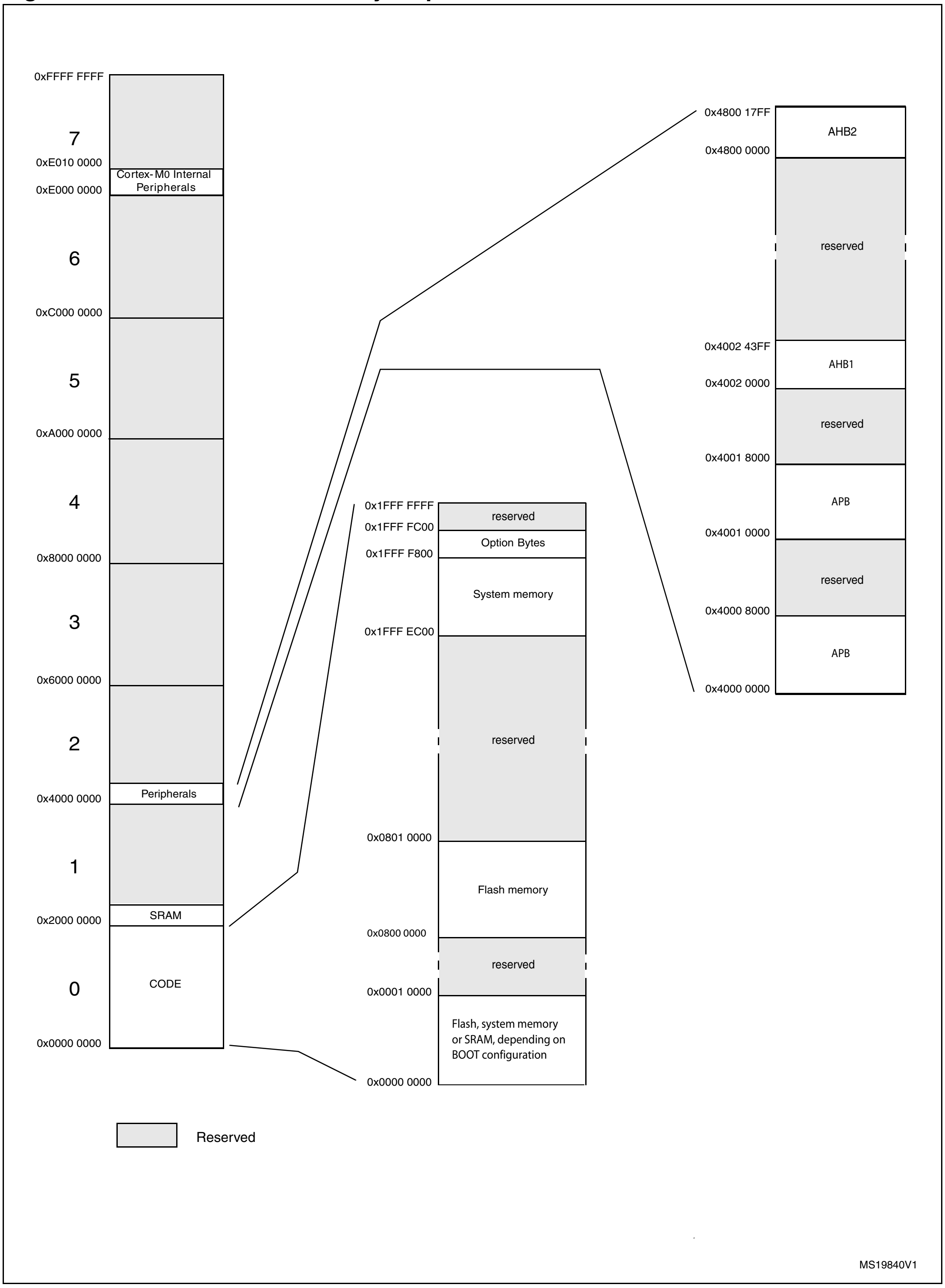


Table 11. STM32F050x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1KB	Reserved
	0x4002 3400 - 0x4002 3FFF	3KB	Reserved
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4002 2400 - 0x4002 2FFF	3KB	Reserved
	0x4002 2000 - 0x4002 23FF	1KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3KB	Reserved
	0x4002 1000 - 0x4002 13FF	1KB	RCC
	0x4002 0400 - 0x4002 0FFF	3KB	Reserved
	0x4002 0000 - 0x4002 03FF	1KB	DMA
	0x4001 8000 - 0x4001 FFFF	32KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 4000 - 0x4001 43FF	1KB	Reserved
	0x4001 3C00 - 0x4001 3FFF	1KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32KB	Reserved

Table 11. STM32F050x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1KB	Reserved
	0x4000 7400 - 0x4000 77FF	1KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1KB	Reserved
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1KB	Reserved
	0x4000 3C00 - 0x4000 43FF	2KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1KB	Reserved
	0x4000 3400 - 0x4000 37FF	1KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3KB	Reserved
	0x4000 1000 - 0x4000 13FF	1KB	Reserved
	0x4000 0800 - 0x4000 0FFF	2KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

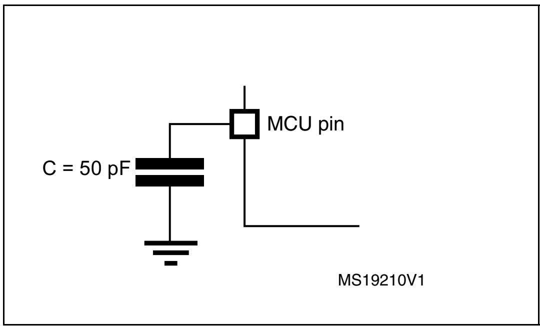
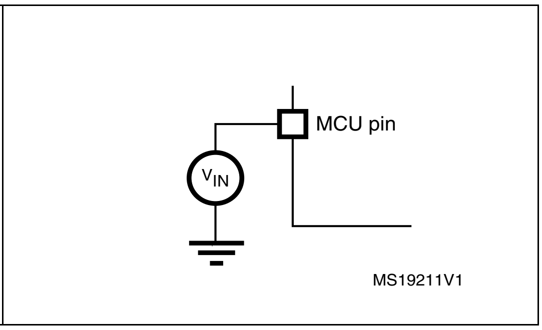
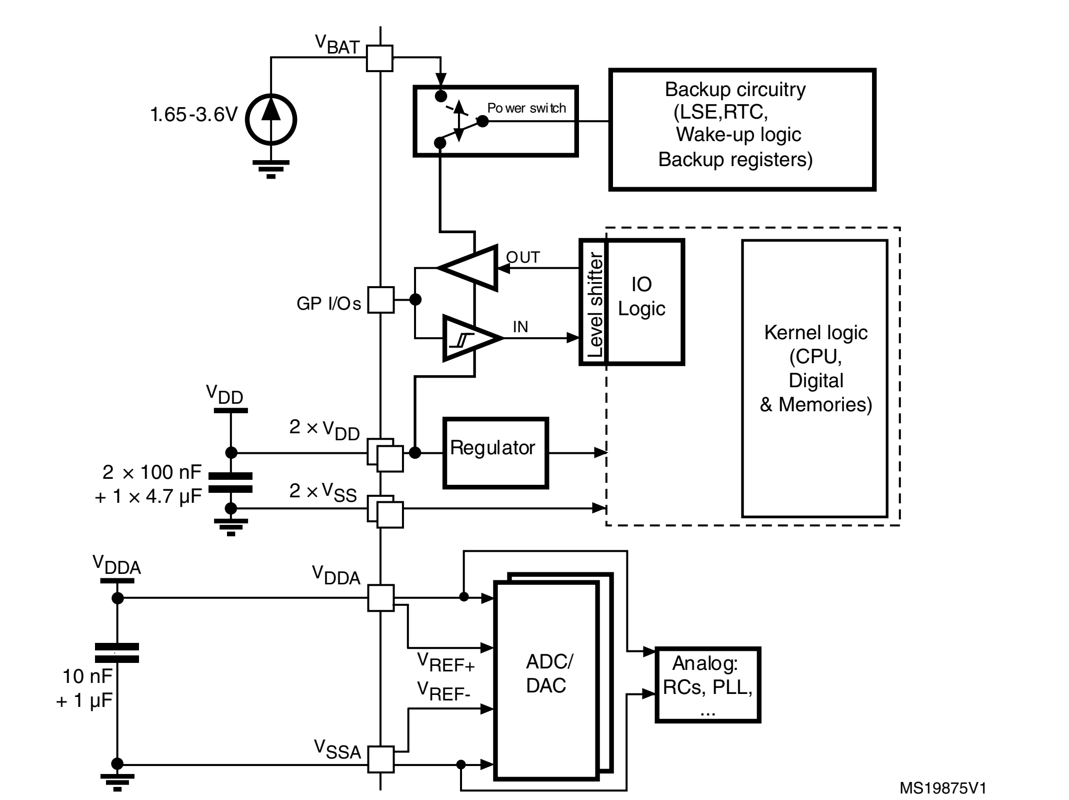


Figure 7. Pin input voltage



6.1.6 Power supply scheme

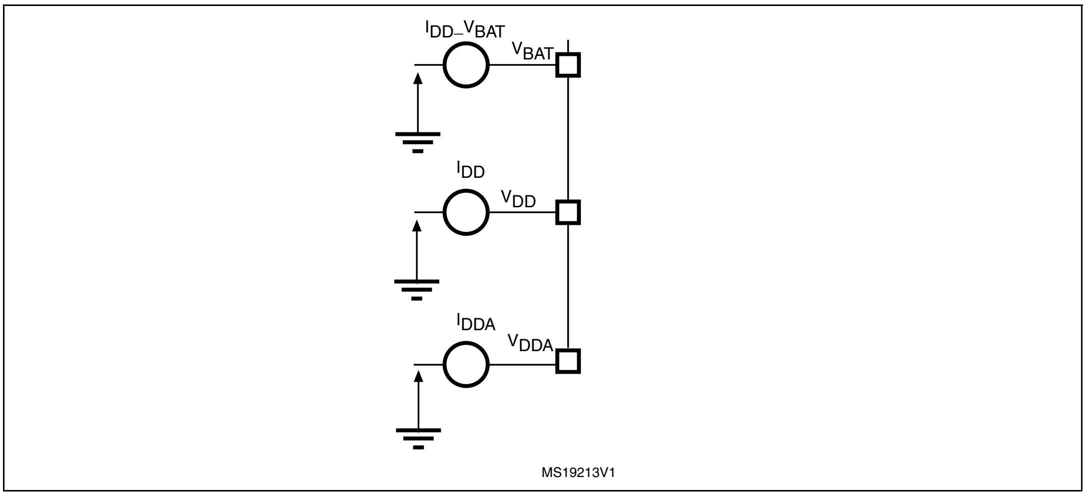
Figure 8. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc..) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 12: Voltage characteristics*, *Table 13: Current characteristics*, and *Table 14: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 12. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})	–0.3	4.0	V
$V_{DD}–V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$		0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DD} + 4.0$	
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins		50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 13: Current characteristics* for the maximum allowed injected current values.

Table 13. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	TBD	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	TBD	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	− 25	
$I_{INJ(PIN)}$(2)	Injected current on FT and FTf pins	-5(3)	
	Injected current on any other pin	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(4)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 12: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2 below *Table 58 on page 75*.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 14. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 15. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK}	Internal APB clock frequency		0	48	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.65	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP48		364	mW
		UFQFPN32		526	
TA	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
TJ	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 56: ADC characteristics*.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Table 14: Thermal characteristics*).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Table 14: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 16* are derived from tests performed under the ambient temperature condition summarized in *Table 15*.

Table 16. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate		0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 17* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 17. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$ [1]	Power on/power down reset threshold	Falling edge	1.8[2]	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$ [1]	PDR hysteresis			40		mV
$t_{RSTTEMPO}$ [3]	Reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 18. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$ [2]	PVD hysteresis			100		mV
$I_{DD(PVD)}$	PVD current consumption			0.15	0.26	µA

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 19* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 19. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
$T_{S\_vrefint}$(2)	ADC sampling time when reading the internal reference voltage			5.1	17.1(3)	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV			10(3)	mV
T_{Coeff}	Temperature coefficient				100(3)	ppm/°C

1. Data based on characterization results, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.
3. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:
- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz and 1 wait state above 24 MHz)
- Prefetch is ON when the peripherals are enabled, otherwise it is OFF (to enable prefetch the PRFTBE bit in the FLASH_ACR register must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 20* to *Table 24* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 15*.

Table 20. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	HSE bypass, PLL on	48 MHz	22	22.8	22.8	23.8	11.8	12.7	12.7	13.3	mA
			32 MHz	15	15.5	15.5	16.0	7.6	8.7	8.7	9.0	
			24 MHz	12.2	13.2	13.2	13.6	7.2	7.9	7.9	8.1	
		HSE bypass, PLL off	8 MHz	4.4	5.2	5.2	5.4	2.7	2.9	2.9	3.0	
			1 MHz	1	1.3	1.3	1.4	0.7	0.9	0.9	0.9	
		HSI clock, PLL on	48 MHz	22	22.8	22.8	23.8	11.8	12.7	12.7	13.3	
			32 MHz	15	15.5	15.5	16.0	7.6	8.7	8.7	9.0	
			24 MHz	12.2	13.2	13.2	13.6	7.2	7.9	7.9	8.1	
		HSI clock, PLL off	8 MHz	4.4	5.2	5.2	5.4	2.7	2.9	2.9	3.0	
	Supply current in Run mode, code executing from RAM	HSE bypass, PLL on	48 MHz	22.2	23.2(2)	23.2	24.4(2)	12.0	12.7(2)	12.7	13.3(2)	
			32 MHz	15.4	16.3	16.3	16.8	7.8	8.7	8.7	9.0	
			24 MHz	11.2	12.2	12.2	12.8	6.2	7.9	7.9	8.1	
		HSE bypass, PLL off	8 MHz	4.0	4.5	4.5	4.7	1.9	2.9	2.9	3.0	
			1 MHz	0.6	0.8	0.8	0.9	0.3	0.6	0.6	0.7	
		HSI clock, PLL on	48 MHz	22.2	23.2	23.2	24.4	12.0	12.7	12.7	13.3	
			32 MHz	15.4	16.3	16.3	16.8	7.8	8.7	8.7	9.0	
			24 MHz	11.2	12.2	12.2	12.8	6.2	7.9	7.9	8.1	
		HSI clock, PLL off	8 MHz	4.0	4.5	4.5	4.7	1.9	2.9	2.9	3.0	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	14	15.3(2)	15.3	16.0(2)	2.8	3.0(2)	3.0	3.2(2)	
			32 MHz	9.5	10.2	10.2	10.7	2.0	2.1	2.1	2.3	
			24 MHz	7.3	7.8	7.8	8.3	1.5	1.7	1.7	1.9	
		HSE bypass, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	
			1 MHz	0.4	0.6	0.6	0.6	0.2	0.4	0.4	0.4	
		HSI clock, PLL on	48 MHz	14	15.3	15.3	16.0	3.8	4.0	4.1	4.2	
			32 MHz	9.5	10.2	10.2	10.7	2.6	2.7	2.8	2.8	
			24 MHz	7.3	7.8	7.8	8.3	2.0	2.1	2.1	2.1	
		HSI clock, PLL off	8 MHz	2.6	2.9	2.9	3.0	0.6	0.8	0.8	0.8	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production with code executing from RAM.

Table 21. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	150	170	178	182	164	183	195	198	µA
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	
	Supply current in Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	150	170	178	182	164	183	195	198	
			32 MHz	104	121	126	128	113	129	135	138	
			24 MHz	82	96	100	103	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
			1 MHz	2.0	2.7	3.1	3.3	3.5	3.8	4.1	4.4	
		HSI clock, PLL on	48 MHz	220	240	248	252	244	263	275	278	
			32 MHz	174	191	196	198	193	209	215	218	
			24 MHz	152	167	173	174	168	183	190	192	
		HSI clock, PLL off	8 MHz	72	79	82	83	83.5	91	94	95	

1. Current consumption from the V_{DDA} supply is independent of whether the peripherals are on or off. Furthermore when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production.

Table 22. Typical and maximum V_{DD} consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ @V_{DD} ($V_{DD} = V_{DDA}$)						Max[1]			Unit
			2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF	15	15.1	15.25	15.45	15.7	16	22[2]	48	64[2]	µA
		Regulator in low-power mode, all oscillators OFF	3.15	3.25	3.35	3.45	3.7	4	7[2]	32	45[2]	
	Supply current in Standby mode	LSI ON and IWDG ON	0.8	0.95	1.05	1.2	1.35	1.5				
		LSI OFF and IWDG OFF	0.65	0.75	0.85	0.95	1.1	1.3	2[2]	2.5	3[2]	

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 23. Typical and maximum V_{DDA} consumption in Stop and Standby modes

Symbol	Parameter		Conditions	Typ @V_{DD} (V_{DD} = V_{DDA})						Max(1)			Unit
				2.0 V	2.4 V	2.7 V	3.0 V	3.3 V	3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DDA}	Supply current in Stop mode	V_{DDA} monitoring ON	Regulator in run mode, all oscillators OFF	1.85	2	2.15	2.3	2.45	2.6	3.5	3.5	4.5	µA
			Regulator in low-power mode, all oscillators OFF	1.85	2	2.15	2.3	2.45	2.6	3.5	3.5	4.5	
	Supply current in Standby mode		LSI ON and IWDG ON	2.25	2.5	2.65	2.85	3.05	3.3				
			LSI OFF and IWDG OFF	1.75	1.9	2	2.15	2.3	2.5	3.5	3.5	4.5	
	Supply current in Stop mode	V_{DDA} monitoring OFF	Regulator in run mode, all oscillators OFF	1.11	1.15	1.18	1.22	1.27	1.35				
			Regulator in low-power mode, all oscillators OFF	1.11	1.15	1.18	1.22	1.27	1.35				
	Supply current in Standby mode		LSI ON and IWDG ON	1.5	1.58	1.65	1.78	1.91	2.04				
			LSI OFF and IWDG OFF	1	1.02	1.05	1.05	1.15	1.22				

1. Data based on characterization results, not tested in production.

Table 24. Typical and maximum current consumption from V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V_{BAT}						Max(1)			Unit
			= 1.65 V	= 1.8 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[1:0] = '00'	0.41	0.43	0.53	0.58	0.71	0.80	0.85	1.1	1.5	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.71	0.75	0.85	0.91	1.06	1.16	1.25	1.55	2	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- V_{DD}=V_{DDA}=3.3 V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state above)
- Prefetch is ON when the peripherals are enabled, otherwise it is OFF
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively
- A development tool is connected to the board and the parasitic pull-up current is around 30 µA

Table 25. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ		Unit
				Peripherals enabled	Peripherals disabled	
I_{DD}	Supply current in Run mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash	48 MHz	23.3	11.5	mA
			36 MHz	17.6	9.0	
			32 MHz	15.9	8.0	
			24 MHz	12.4	7.5	
			16 MHz	8.5	5.2	
			8 MHz	4.5	3.0	
			4 MHz	2.8	1.9	
			2 MHz	1.7	1.3	
			1 MHz	1.3	1.0	
			500 kHz	1.0	0.9	
I_{DDA}	Supply current in Run mode from V_{DDA} supply		48 MHz	158	158	µA
			36 MHz	120	120	
			32 MHz	108	108	
			24 MHz	83	83	
			16 MHz	60	60	
			8 MHz	2.43	2.43	
			4 MHz	2.43	2.43	
			2 MHz	2.43	2.43	
			1 MHz	2.43	2.43	
			500 kHz	2.43	2.43	

Table 26. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ: Peripherals enabled	Typ: Peripherals disabled	Unit
I_{DD}	Supply current in Sleep mode from V_{DD} supply	Running from HSE crystal clock 8 MHz, code executing from Flash or RAM	48 MHz	13.9	2.98	mA
			36 MHz	10.55	2.84	
			32 MHz	9.6	2.6	
			24 MHz	7.23	2.09	
			16 MHz	5.01	1.58	
			8 MHz	2.68	0.99	
			4 MHz	1.81	0.85	
			2 MHz	1.27	0.77	
			1 MHz	1.03	0.73	
			500 kHz	0.9	0.71	
			125 kHz	0.78	0.69	
I_{DDA}	Supply current in Sleep mode from V_{DDA} supply		48 MHz	158	157	µA
			36 MHz	119	119	
			32 MHz	108	107	
			24 MHz	83	83	
			16 MHz	60	60	
			8 MHz	2.36	2.38	
			4 MHz	2.36	2.38	
			2 MHz	2.36	2.38	
			1 MHz	2.36	2.38	
			500 kHz	2.36	2.38	
			125 kHz	2.36	2.38	

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 45: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 28: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 27. Switching output I/O current consumption

Symbol	Parameter	Conditions(1)	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DD} = 3.3 V C =C_{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V_{DD} = 3.3 Volts C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DD} = 3.3 Volts C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V_{DD} = 3.3 Volts C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DD} = 3.3 Volts C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V_{DD} = 3.3 Volts C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V_{DD} = 2.4 Volts C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 28*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 12*

Table 28. Peripheral current consumption(1)

Peripheral	Typical consumption at 25 °C		Unit
	I_{DD}	I_{DDA}	
ADC(2)	0.53	0.964	mA
CRC	0.10		
DBGMCU	0.18		
DMA	0.35		
GPIOA	0.48		
GPIOB	0.58		
GPIOC	0.12		
GPIOF	0.06		
I2C1	0.43		
PWR	0.22		
SPI1/I2S1	0.63		
SYSCFG	0.28		
TIM1	1.01		
TIM2	1.00		
TIM3	0.78		
TIM6	0.32		
TIM14	0.45		
TIM16	0.57		
TIM17	0.59		
USART1	1.07		
WWDG	0.22		

1. f_{HCLK} = 48 MHz, $f_{PCLK} = f_{HCLK}$, default prescaler value for each peripheral.
2. ADC is in ready state after setting the ADEN bit in the ADC_CR register (ADRDY bit in ADC_ISR is high).

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

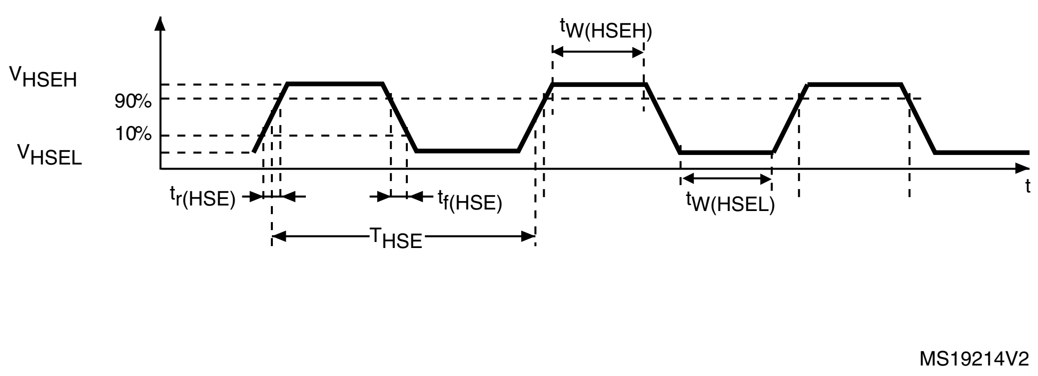
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 10*.

Table 29. High-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		15			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time				20	

1. Guaranteed by design, not tested in production.

Figure 10. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

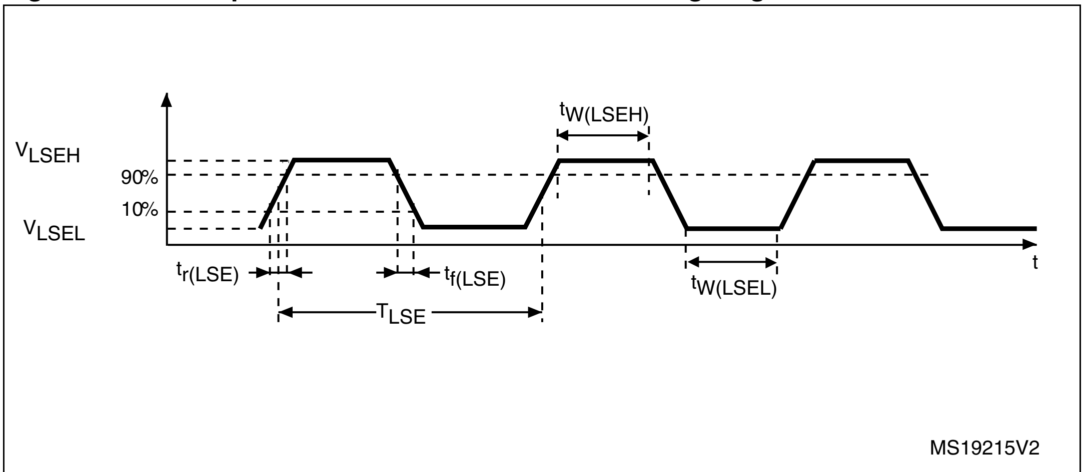
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 11*.

Table 30. Low-speed external user clock characteristics

Symbol	Parameter[1]	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time				50	

1. Guaranteed by design, not tested in production.

Figure 11. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 31. HSE oscillator characteristics

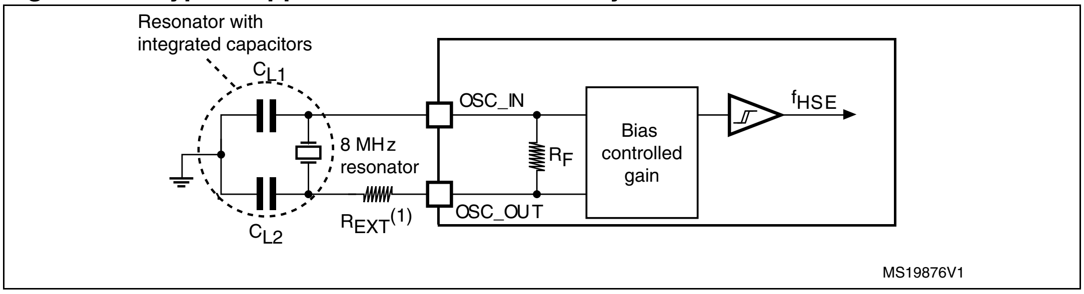
Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistor			200		kΩ
I_{DD}	HSE current consumption	During startup(3)			8.5	mA
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@8 MHz		0.4		
		V_{DD}=3.3 V, Rm= 45Ω, CL=10 pF@8 MHz		0.5		
		V_{DD}=3.3 V, Rm= 30Ω, CL=5 pF@32 MHz		0.8		
		V_{DD}=3.3 V, Rm= 30Ω, CL=10 pF@32 MHz		1		
		V_{DD}=3.3 V, Rm= 30Ω, CL=20 pF@32 MHz		1.5		
g_m	Oscillator transconductance	Startup	10			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 12*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on electing the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 12. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 32*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

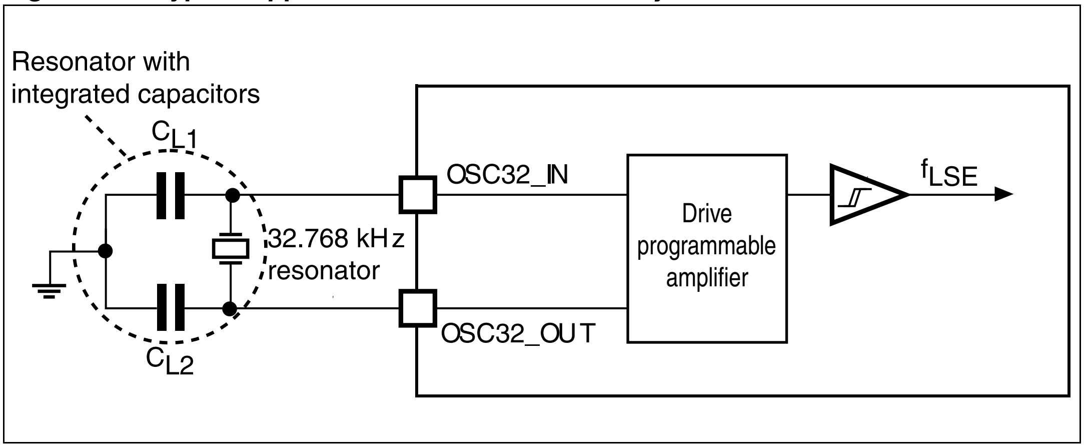
Table 32. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability		0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability			1	
		LSEDRV[1:0] = 10 medium high driving capability			1.3	
		LSEDRV[1:0]=11 higher driving capability			1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5			µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8			
		LSEDRV[1:0] = 10 medium high driving capability	15			
		LSEDRV[1:0]=11 higher driving capability	25			
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized		2		s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 13. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 33* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 15*.

High-speed internal (HSI) RC oscillator

Table 33. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
TRIM	HSI user trimming step				1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)		55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–2.4(3)		2.5(3)	%
		T_A = –10 to 85 °C	–2.2(3)		1.3(3)	%
		T_A = 0 to 70 °C	–1.9(3)		1.3(3)	%
		T_A = 25 °C	–1		1	%
$t_{su(HSI)}$	HSI oscillator startup time		1(2)		2(2)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 34. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency			14		MHz
TRIM	HSI14 user-trimming step				1(2)	%
$DuCy_{(HSI14)}$	Duty cycle		45(2)		55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	TBD(3)		TBD(3)	%
		T_A = –10 to 85 °C	TBD(3)		TBD(3)	%
		T_A = 0 to 70 °C	TBD(3)		TBD(3)	%
		T_A = 25 °C	-1		1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time		1(2)		2(2)	µs
$I_{DD(HSI14)}$	HSI14 oscillator power consumption			100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 35. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption		0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 36* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The event used to wake up the device depends from the current operating mode:

- Stop or sleep mode: the wakeup event is WFE
- The wakeup pin used in stop and sleep mode is PA0 and in standby mode is the PA1.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 36. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @VDD					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	4.2	4.2	4.2	4.2	4.2	5	µs
		Regulator in low power mode	8.05	7.05	6.6	6.27	6.05	9	
$t_{WUSTANDBY}$	Wakeup from Standby mode		60.35	55.6	53.5	52.02	50.96		
$t_{WUSLEEP}$	Wakeup from Sleep mode		1.1	1.1	1.1	1.1	1.1		

6.3.8 PLL characteristics

The parameters given in *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 15*.

Table 37. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)		60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)		48	MHz
t_{LOCK}	PLL lock time			200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter			300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 38. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms
I_{DD}	Supply current	Write mode			10	mA
		Erase mode			12	mA
V_{prog}	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

Table 39. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 40*. They are based on the EMS levels and classes defined in application note AN1709.

Table 40. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3$ V, LQFP64, $T_A = +25$ °C, $f_{HCLK} = 48$ MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3$ V, LQFP64, $T_A = +25$ °C, $f_{HCLK} = 48$ MHz conforms to IEC 61000-4-4	3B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 41. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	-3	dBµV
			30 to 130 MHz	28	
			130 MHz to 1GHz	23	
			SAE EMI Level	4	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 42. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	500	

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 43. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 44*

Table 44. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	TBD	TBD	mA
	Injected current on all FT pins	TBD	TBD	
	Injected current on all FTf pins	TBD	TBD	
	Injected current on all TTa pins	TBD	TBD	
	Injected current on any other pin	TBD	TBD	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 45 are derived from tests performed under the conditions summarized in Table 15. All I/Os are CMOS and TTL compliant.

Table 45. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage		–0.3		$0.3V_{DD}+0.07$	V
	TTa I/O input low level voltage		–0.3		$0.3V_{DD}+0.07$	
	FT and FTf(1) I/O input low level voltage		–0.3		$0.475V_{DD}-0.2$	
V_{IH}	Standard I/O input high level voltage		$0.445V_{DD}+0.398$		$V_{DD}+0.3$	
	TTa I/O input high level voltage		$0.445V_{DD}+0.398$		$V_{DD}+0.3$	
	FT and FTf(1) I/O input high level voltage		$0.5V_{DD}+0.2$		5.5	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)		200			mV
	TTa I/O Schmitt trigger voltage hysteresis(2)		200			
	FT and FTf I/O Schmitt trigger voltage hysteresis(2)		100			
I_{lkg}	Input leakage current (3)	$V_{SS} \leq V_{IN} \leq V_{DD}$ I/O TC, FT and FTf			±0.1	µA
		$V_{SS} \leq V_{IN} \leq V_{DD}$ $2\ V \leq V_{DD} \leq V_{DDA} \leq 3.6\ V$ I/O TTa used in digital mode			±0.1	
		$V_{IN} = 5\ V$ I/O FT and FTf			10	
		$V_{IN} = 3.6\ V$, $2\ V \leq V_{DD} \leq V_{IN}$ $V_{DDA} = 3.6\ V$ I/O TTa used in digital mode			1	
		$V_{SS} \leq V_{IN} \leq V_{DDA}$ $2\ V \leq V_{DD} \leq V_{DDA} \leq 3.6\ V$ I/O TTa used in analog mode			±0.2	

Table 45. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(4)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. To sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Data based on characterization, not tested in production.
3. Leakage could be higher than max. if negative current is injected on adjacent pins.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 14* and *Figure 15* for standard I/Os, and in *Figure 16* and *Figure 17* for 5 V tolerant I/Os.

Figure 14. TC and TTa I/O input characteristics - CMOS port

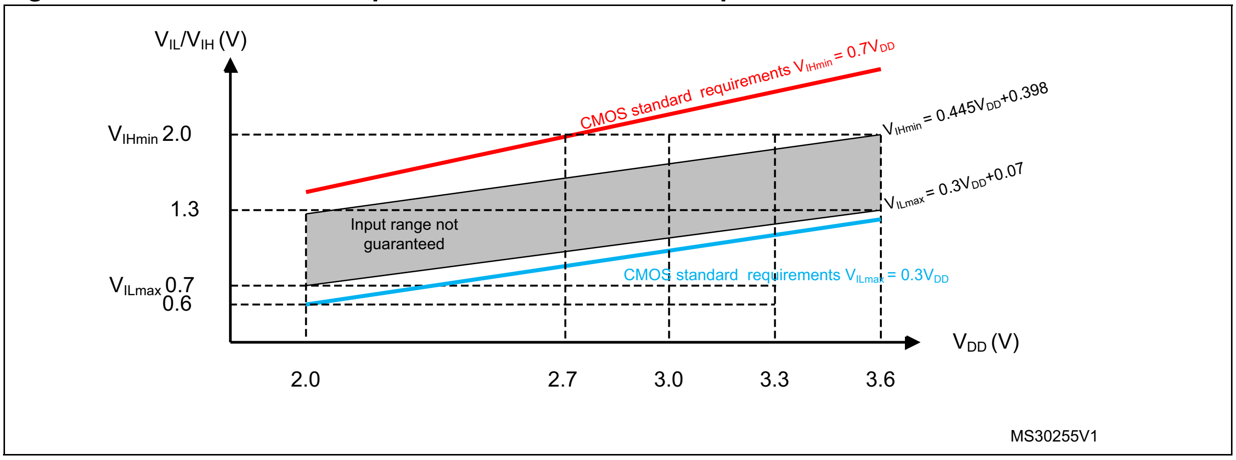


Figure 15. TC and TTa I/O input characteristics - TTL port

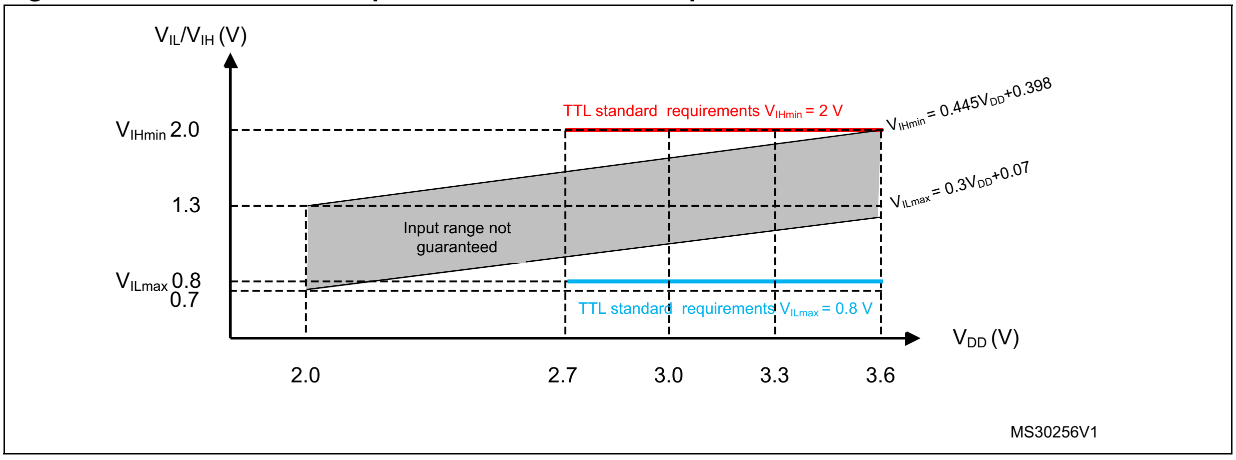


Figure 16. Five volt tolerant (FT and FTf) I/O input characteristics - CMOS port

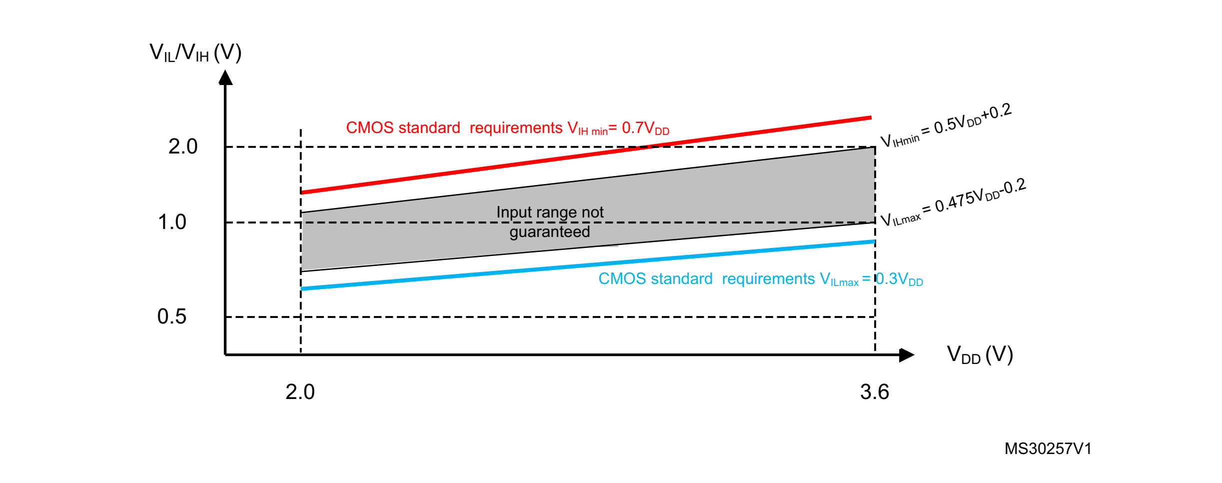
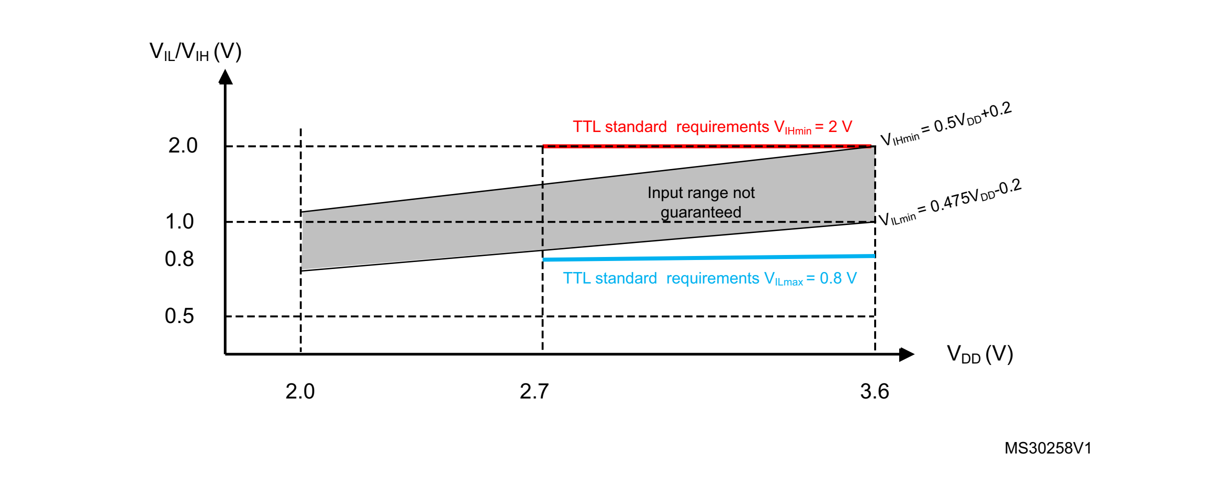


Figure 17. Five volt tolerant (FT and FTf) I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 13*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 13*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*. All I/Os are CMOS and TTL compliant (FT, TTa or TC unless otherwise specified).

Table 46. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		
V_{OLFM+}	Output low level voltage for an FTf I/O pin in FM+ mode	I_{IO} = +20 mA 2 V < V_{DD} < 3.6 V		0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Data based on characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 18* and *Table 47*, respectively.

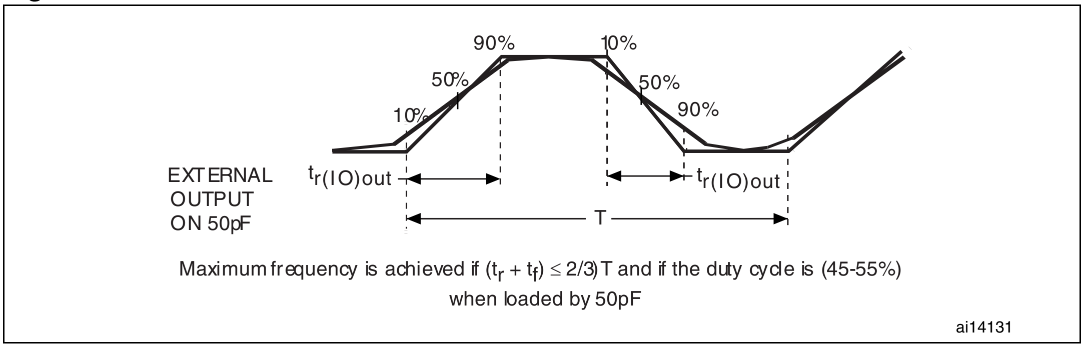
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 47. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
FM+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(2)	TBD		TBD	MHz
	$t_{f(IO)out}$	Output high to low level fall time	TBD		TBD	ns
	$t_{r(IO)out}$	Output low to high level rise time	TBD		TBD	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0091 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 18*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F05xxx reference manual RM0091 for a description of FM+ I/O mode configuration.

Figure 18. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 45*).

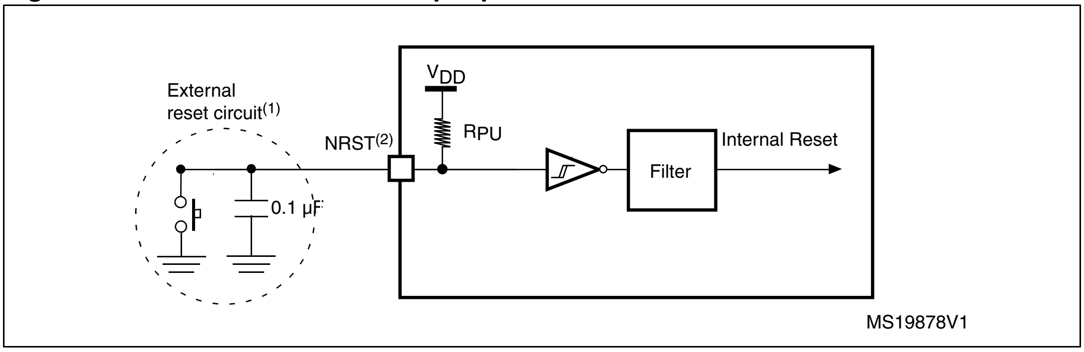
Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 15*.

Table 48. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.3		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.3	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 19. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 48*. Otherwise the reset will not be taken into account by the device.

6.3.15 Timer characteristics

The parameters given in *Table 49* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 49. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)		16	bit
		TIM2		32	
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz		89.48	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

Table 50. IWDG min/max timeout period at 40 kHz (LSI) [1]

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 51. WWDG min-max timeout value @48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.16 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in Table 52 are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in Table 15.

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in Table 52. Refer also to Section 6.3.13: I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

Table 52. I²C characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		0.26		µs
$t_{su(SDA)}$	SDA setup time	250		100		50		ns
$t_{h(SDA)}$	SDA data hold time	0(3)	3450(2)	0(3)	900(2)	0(4)	450(2)	ns
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300		120	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300		120	ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		0.26		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		0.26		µs
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		0.26		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		0.5		µs
C_b	Capacitive load for each bus line		400		400		550	pF

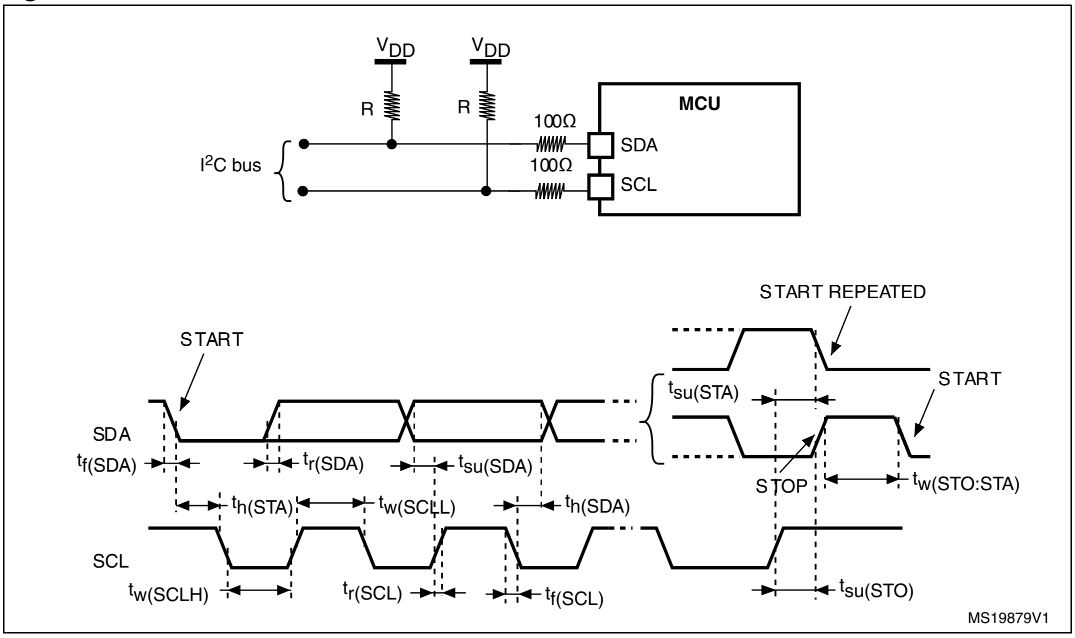
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.
2. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The device must internally provide a hold time of at least 120ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Table 53. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 20. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 54* for SPI or in *Table 55* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 54. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF		6	ns
$t_{su(NSS)}$[1]	NSS setup time	Slave mode	4Tpclk		ns
$t_{h(NSS)}$[1]	NSS hold time	Slave mode	2Tpclk + 10		
$t_{w(SCKH)}$[1] $t_{w(SCKL)}$[1]	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$[1] $t_{su(SI)}$[1]	Data input setup time	Master mode	4		
		Slave mode	5		
$t_{h(MI)}$[1]	Data input hold time	Master mode	4		
$t_{h(SI)}$[1]		Slave mode	5		
$t_{a(SO)}$[1][2]	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$[1][3]	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$[1]	Data output valid time	Slave mode (after enable edge)		22.5	
$t_{v(MO)}$[1]	Data output valid time	Master mode (after enable edge)		6	
$t_{h(SO)}$[1]	Data output hold time	Slave mode (after enable edge)	11.5		
$t_{h(MO)}$[1]		Master mode (after enable edge)	2		
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 21. SPI timing diagram - slave mode and CPHA = 0

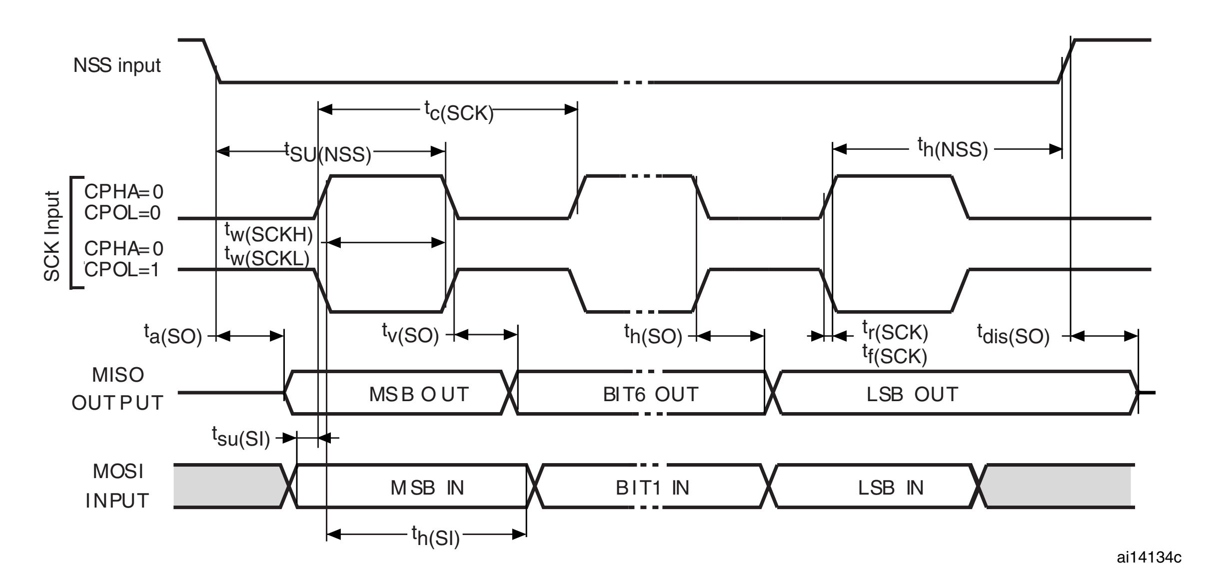
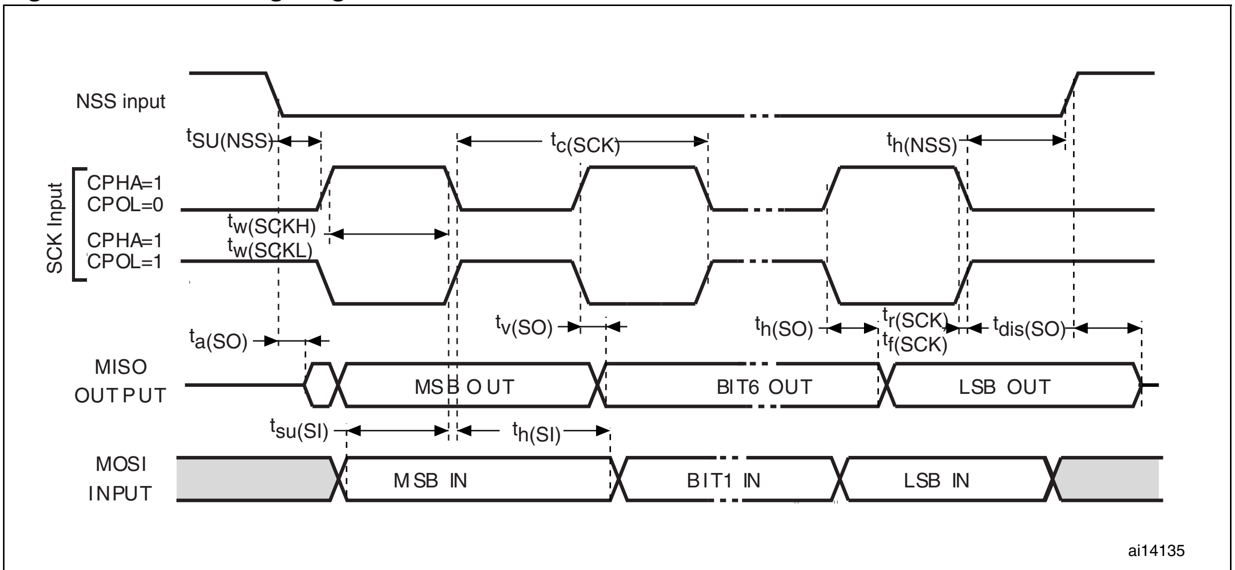
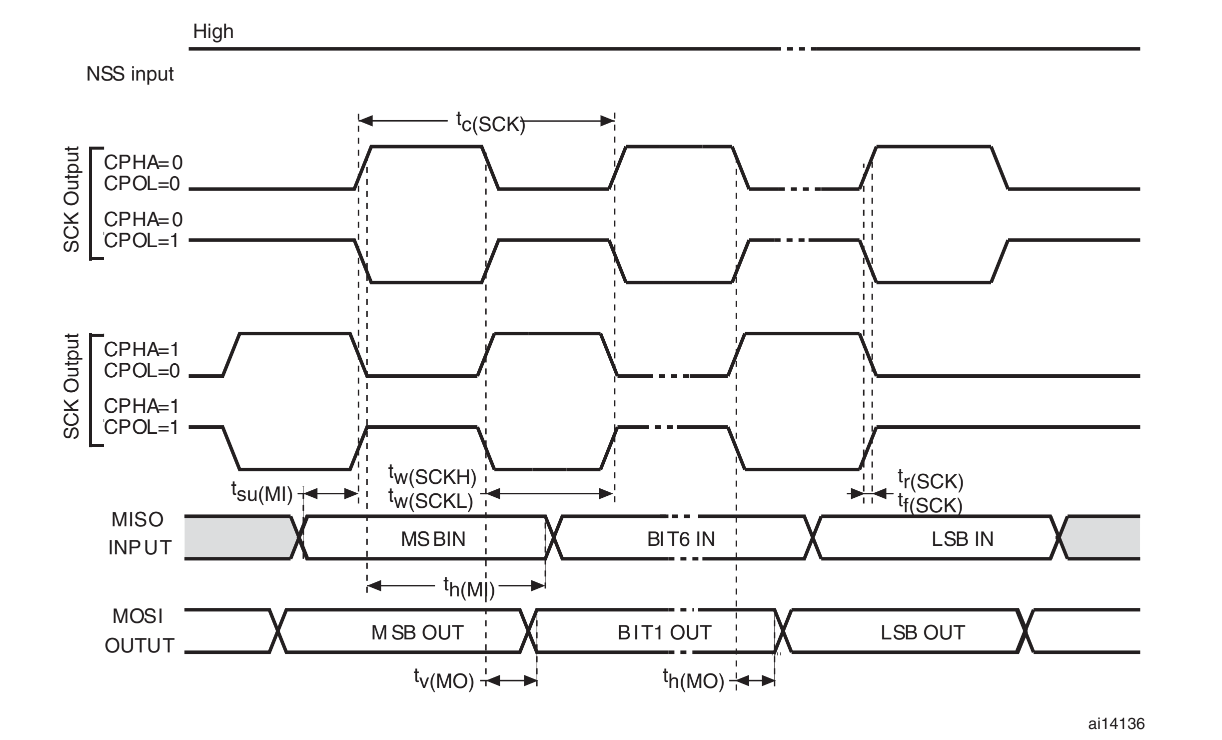


Figure 22. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 23. SPI timing diagram - master mode[1]



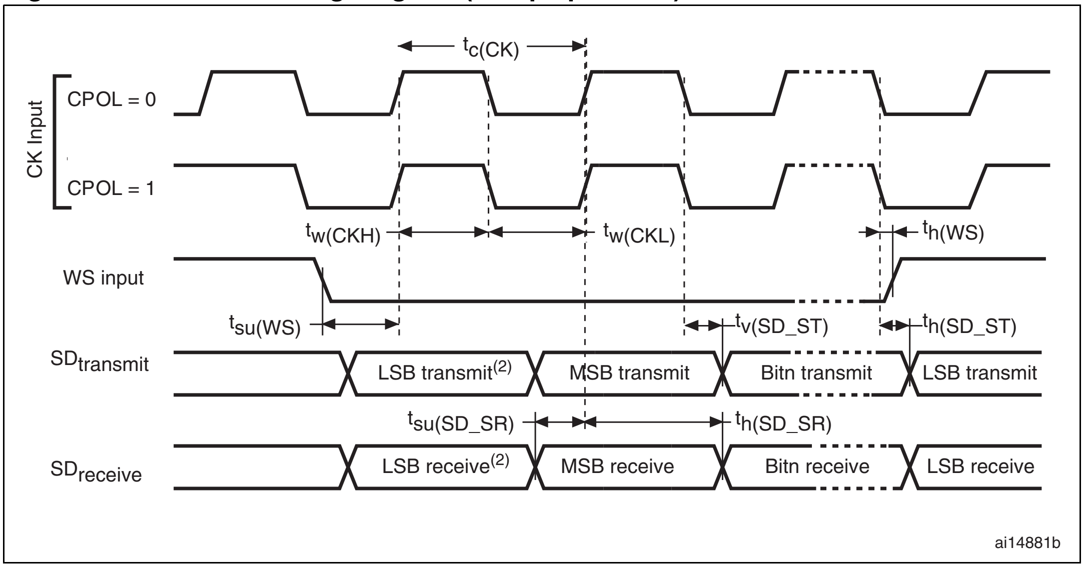
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 55. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF		10	ns
$t_{f(CK)}$	I^2S clock fall time			12	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306		
$t_{w(CKL)}$ (1)	I2S clock low time		312		
$t_{v(WS)}$ (1)	WS valid time	Master mode	2		
$t_{h(WS)}$ (1)	WS hold time	Master mode	2		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	7		
$t_{h(WS)}$ (1)	WS hold time	Slave mode	0		
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	%
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6		ns
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver	2		
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver	4		
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver	0.5		
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		31(3)	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	13		
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		4	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0		

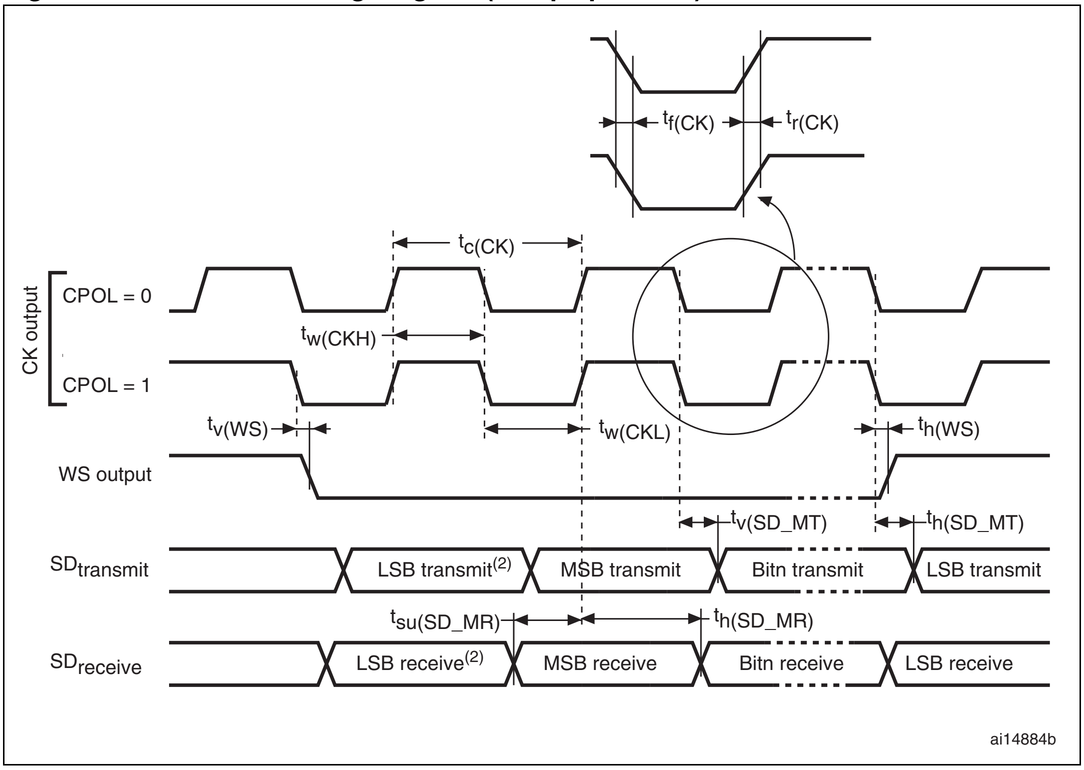
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.
3. REGOFF value was chosen but in REGON target value is 20 ns

Figure 24. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: 0.3 × V_{DD} and 0.7 × V_{DD}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 25. I²S master timing diagram (Philips protocol)(1)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 56 are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 15.

Note: It is recommended to perform a calibration after each power-up.

Table 56. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON		2.4		3.6	V
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(1)	Sampling rate		0.05		1	MHz
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_{AIN}(1)	External input impedance	See Equation 1 and Table 57 for details			50	kΩ
R_{ADC}(1)	Sampling switch resistance				1	kΩ
C_{ADC}(1)	Internal sample and hold capacitor				8	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.188		0.259	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$		1		$1/f_{HSI14}$
t_S(1)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(1)	Power-up time		0	0	1	µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 57. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 58. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.7 V to 3.6 V T_A = -40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 6.3.13 does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 26. ADC accuracy characteristics

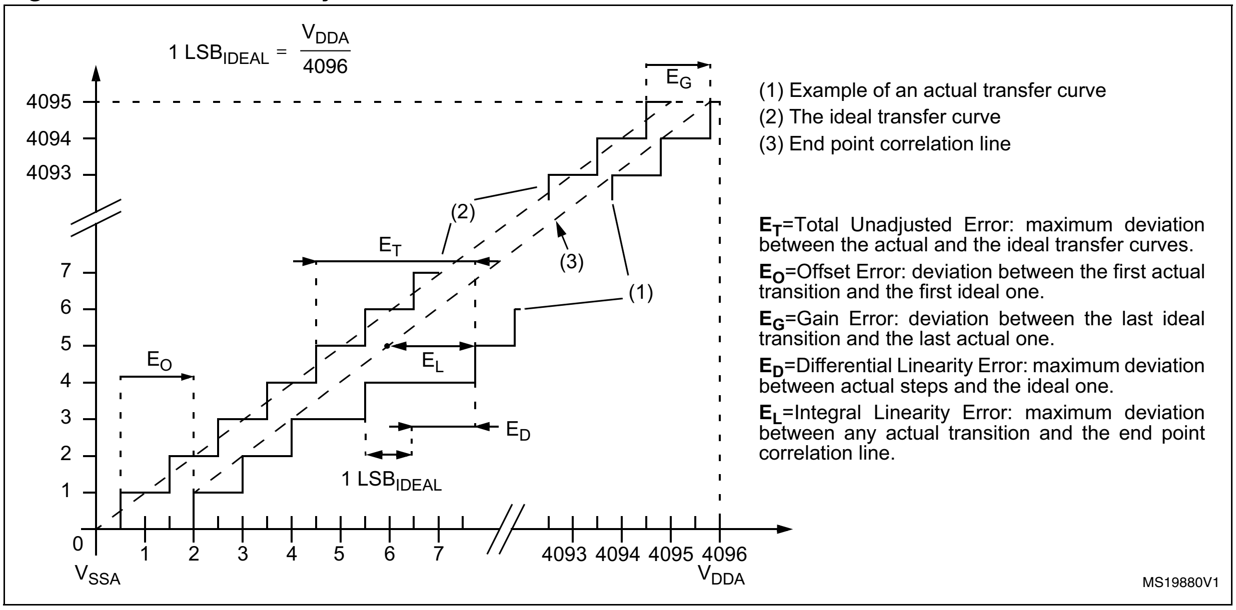
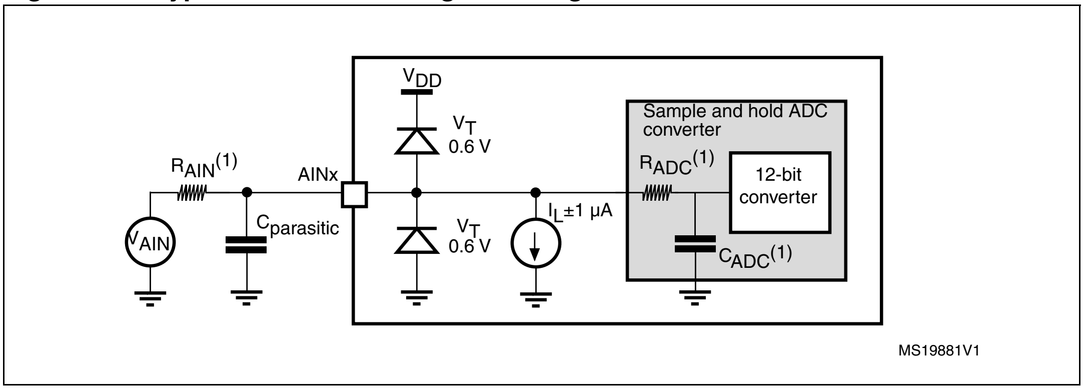


Figure 27. Typical connection diagram using the ADC



1. Refer to Table 56 for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in Figure 8. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.18 Temperature sensor characteristics

Table 59. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4		10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature			17.1	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.19 V_{BAT} monitoring characteristics

Table 60. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}		50		KΩ
Q	Ratio on V_{BAT} measurement		2		
Er(1)	Error on Q	–1		+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5			µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7 Package characteristics

7.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 28. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline(1)

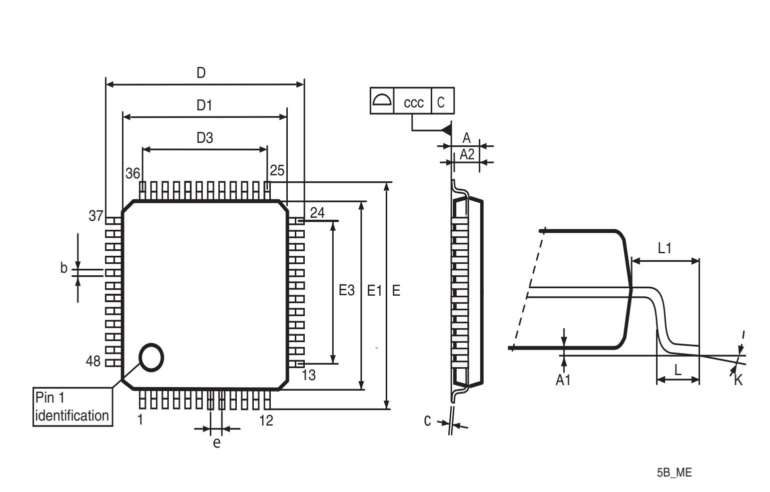
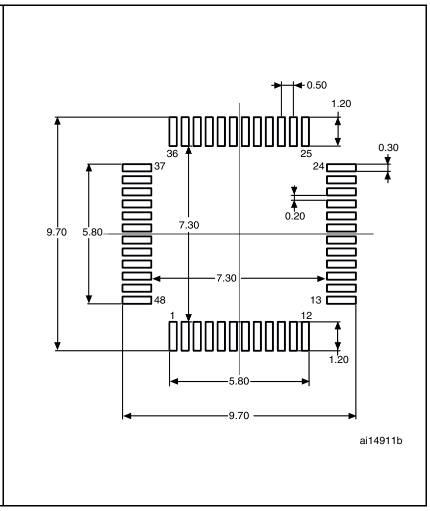


Figure 29. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 61. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 30. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)(1)(2)(3)

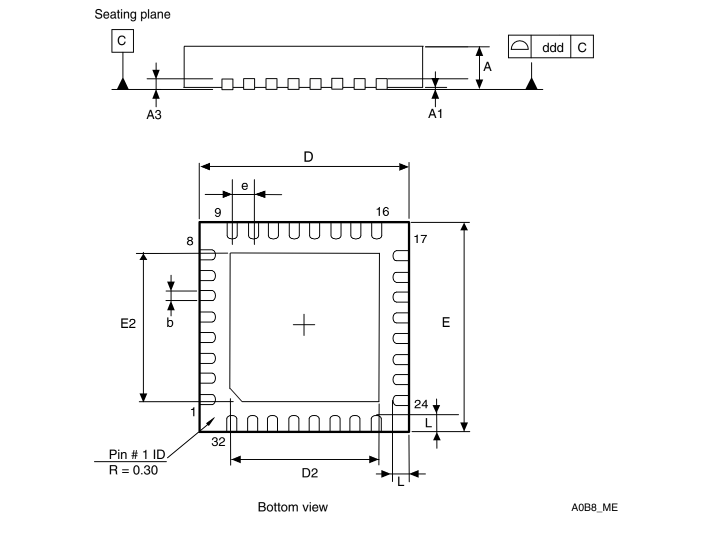
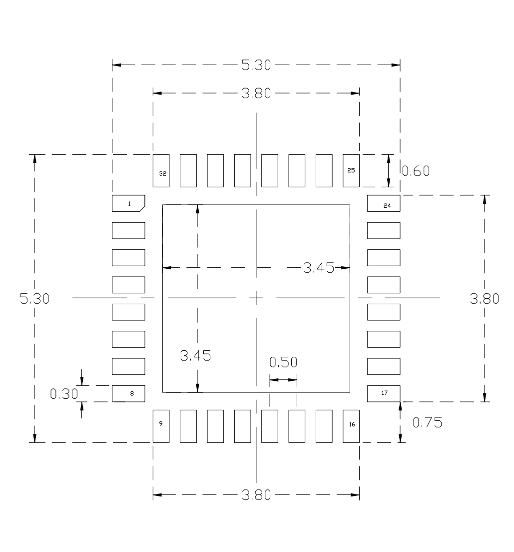


Figure 31. UFQFPN32 recommended footprint(1)(4)



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table 8: Pin definitions*.
4. Dimensions are in millimeters.

Table 62. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	0.00	0.02	0.05	0	0.0008	0.0020
A3		0.152			0.006	
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D2		3.50			0.1378	
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e		0.500			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	0.08			0.0031		
	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 15: General operating conditions on page 35*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 63. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	

7.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 10: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F05xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 80 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Using the values obtained in *Table 63* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

T_{Jmax} = 80 °C + (55°C/W × 447 mW) = 80 °C + 24.585 °C = 104.585 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Table 15: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 10: Ordering information scheme*).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: T_{Amax} = T_{Jmax} - (55°C/W × 447 mW) = 105-24.585 = 80.415 °C

Suffix 7: T_{Amax} = T_{Jmax} - (55°C/W × 447 mW) = 125-24.585 = 100.415 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 63* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

T_{Jmax} = 100 °C + (55 °C/W × 134 mW) = 100 °C + 7.37 °C = 107.37 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 10: Ordering information scheme*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

8 Ordering information scheme

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Example: STM32 F 050 C 6 T 6 A x

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = General-purpose

Sub-family
050 = STM32F050xx

Pin count

K = 32 pins
C = 48 pins

Code size
4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory

Package
U = UFQFN
T = LQFP

Temperature range
6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Internal code
A

Options
xxx = programmed parts
TR = tape and real

9 Revision history

Table 64. Document revision history

Date	Revision	Changes
25-Apr-2012	1	Initial release

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com