Quad Channel, 16-Bit, Serial Input, 4-20mA Output DAC, Dynamic Power Control, HART Connectivity

Preliminary Technical Data

AD5757/AD5737

FEATURES

16/12-bit resolution and monotonicity
Dynamic power control for thermal management
Current output ranges: 0 mA to 20 mA, 4 mA to 20 mA, or 0 mA to 24 mA
±0.05% total unadjusted error (TUE) maximum
User programmable offset and gain
On-chip diagnostics
On-chip reference (±5 ppm/°C typ)
–40°C to +105°C temperature range

APPLICATIONS

Process Control
Actuator Control
PLC's
HART Network Connectivity

GENERAL DESCRIPTION

The AD5757/AD5737 is a quad, current output DAC, which operates with a power supply of up to +33v. On chip dynamic power control minimizes package power dissipation in current mode. This is achieved by regulating the voltage on the output driver from between 7.4V-29.5V.

Each channel has a corresponding CHART pin so that HART signals can be coupled onto the AD5757/AD5737's current output.

The part uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz and that is compatible with standard SPI®, QSPI™, MICROWIRE™, DSP and microcontroller interface standards. The interface also features optional CRC-8 packet error checking as well as a watchdog timer that monitors activity on the interface.

PRODUCT HIGHLIGHTS

1. Dynamic power control for thermal management.
2. 16-bit performance.
3. Multichannel.
4. HART Compliant

Table 1. Complementary Devices

Part No.	Description
ADR445	5 V, ultralow noise, LDO XFET voltage reference with current sink and source
ADP2302/ADP2303	2 A/3 A, 20 V, 700 kHz, nonsynchronous step-down regulators

FUNCTIONAL BLOCK DIAGRAM

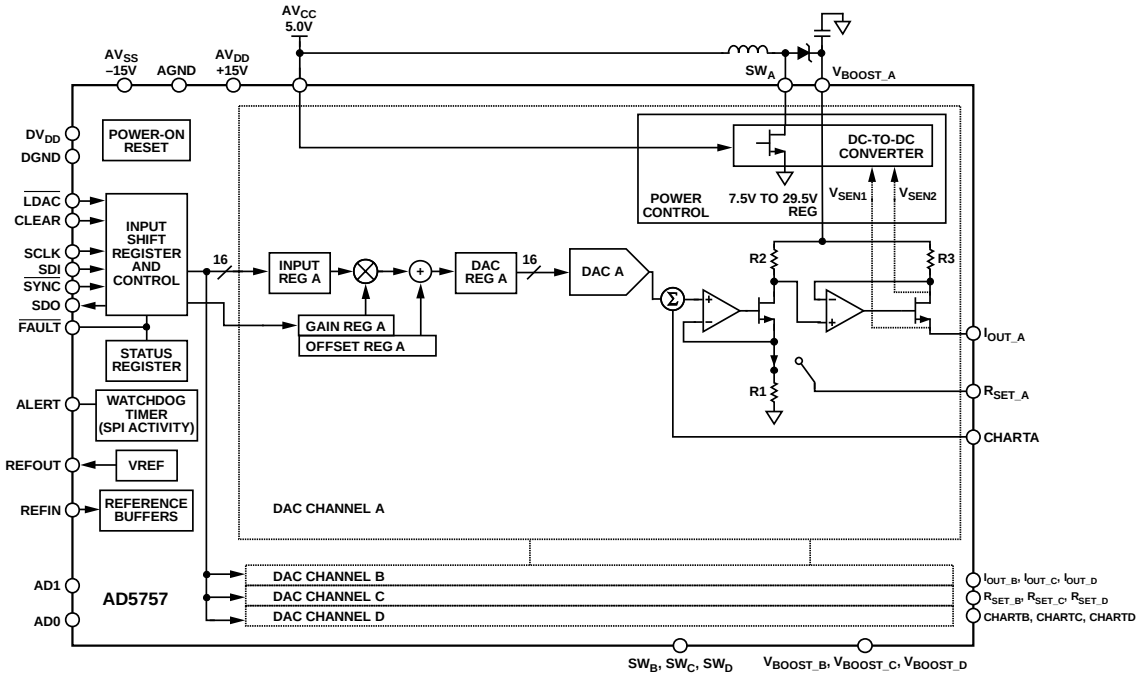

Figure 1.

PrF

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SPECIFICATIONS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled,;AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT OUTPUT					
Output Current Ranges	0		24	mA	
	0		20	mA	
	4		20	mA	
Resolution	16			Bits	
ACCURACY (External R_{Set})					
Total Unadjusted Error (TUE)	−0.05	±0.009	+0.05	% FSR	
Relative Accuracy (INL)	−0.006		+0.006	% FSR	AD5757
	−0.025		+0.025	% FSR	AD5737
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.05	±0.005	+0.05	% FSR	
Offset Error Drift[2]		±4		ppm FSR/°C	
Gain Error	−0.05	±0.004	+0.05	% FSR	
Gain TC[2]		±3		ppm FSR/°C	
Full-Scale Error	−0.05	±0.008	+0.05	% FSR	
Full-Scale TC[2]		±5		ppm FSR/°C	
ACCURACY (Internal R_{Set})					
Total Unadjusted Error (TUE)	−0.24		+0.24		
	−0.21	TBD	+0.21	% FSR	T_A = 25°C
TUE TC[2]		±TBD		ppm	
Relative Accuracy (INL)	−0.006		+0.006	% FSR	AD5757
	−0.025		+0.025	% FSR	AD5737
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic
Offset Error	−0.15		+0.15	% FSR	
	−0.14	TBD	+0.14	% FSR	T_A = 25°C
Offset Error Drift[2]		±6		ppm FSR/°C	
Gain Error	−0.12		+0.12	% FSR	
	−0.06	±0.002	+0.06	% FSR	T_A = 25°C
Gain TC[2]		±9		ppm FSR/°C	
Full-Scale Error	−0.14		+0.14	% FSR	
	−0.1	±0.007	+0.1	% FSR	T_A = 25°C
Full-Scale TC[2]		±14		ppm FSR/°C	
OUTPUT CHARACTERISTICS[2]					
Current Loop Compliance Voltage		V_{BOOST_X} − 2.4	V_{BOOST_X} − 2.7	V max	
Output Current Drift vs. Time					Drift after 1000 hours, ¾ scale output, T_J = 150°C
		90		ppm FSR	External R_{SET}
		140		ppm FSR	Internal R_{SET}
Resistive Load			1000	Ω	The dc-dc converter has been characterized with a maximum load of 1 kΩ, chosen such that compliance is not exceeded.
DC PSRR		0.02	1	µA/V	
Output Impedance		100		MΩ	
REFERENCE INPUT/OUTPUT					

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
Reference Input[2]					
Reference Input Voltage	4.95	5	5.05	V nom	For specified performance
DC Input Impedance	45	150		MΩ min	
Reference Output					
Output Voltage	4.995	5	5.005	V	T_A = 25°C
Reference TC[2,3]	−10	±5	+10	ppm/°C	
Output Noise (0.1 Hz to 10 Hz)[2]		7		µV p-p	
Noise Spectral Density[2]		100		nV/√Hz	At 10 kHz
Output Voltage Drift vs. Time[2]		180		ppm	Drift after 1000 hours, T_J = 150°C
Capacitive Load[2]		1000		nF	
Load Current		9		mA	
Short-Circuit Current		10		mA	
Line Regulation[2]		3		ppm/V	
Load Regulation[2]		95		ppm/mA	
Thermal Hysteresis[2]		160		ppm	First temperature cycle
		5		ppm	Second temperature cycle
DC-DC					
SWITCH					
SWITCH On Resistance		0.425		ohm	
SWITCH Leakage Current		10		uA	
Peak Current Limit		0.8		A	
OSCILLATOR					
Oscillator Frequency	11.5	13	14.5	KHz	This oscillator is divided down to give the dc-to-dc converter switching frequency
Maximum Duty Cycle		89.6		%	@410kHz DCDC switching frequency
DIGITAL INPUTS[2]					JEDEC compliant
V_{IH}, Input High Voltage	2			V	
V_{IL}, Input Low Voltage			0.8	V	
Input Current	−1		+1	µA	Per pin
Pin Capacitance		2.6		pF	Per pin
DIGITAL OUTPUTS[2]					
SDO, ALERT					
V_{OL}, Output Low Voltage			0.4	V	sinking 200 µA
V_{OH}, Output High Voltage	DVDD −0.5			V	sourcing 200 µA
High Impedance Leakage Current	−1		+1	µA	
High Impedance Output Capacitance		5		pF	
$\overline{\text{FAULT}}$					
V_{OL}, Output Low Voltage			0.4	V	10kΩ pull-up resistor to DVDD
V_{OL}, Output Low Voltage		0.6		V	At 2.5 mA
V_{OH}, Output High Voltage	3.6			V	10kΩ pull-up resistor to DVDD
POWER REQUIREMENTS					
AV_{DD}	12		33	V	
DV_{DD}	2.7		5.5	V	
AV_{CC}	4.5		5.5	V	
AI_{DD}			7.5	mA	
DI_{CC}		9.2	11	mA	V_{IH} = DVDD, V_{IL} = GND, Internal Oscillator running, Over supplies
AI_{CC}			1	mA	0mA output, Over supplies

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
AI_{BOOST}			1	mA	Per Channel
Power Dissipation		TBD		mW	AV_{DD} = 33V, outputs unloaded

[1]Temperature range: −40°C to +105°C; typical at +25°C.
[2] Guaranteed by characterization; not production tested.
[3] The on-chip reference is production trimmed and tested at 25°C and 85°C. It is characterized from −40°C to +105°C.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled; AGND = DGND = $GNDSW_x$ = 0 V; REFIN= 5 V; voltage outputs: R_L = 2 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Current Output					
Output Current Settling Time		15		µs typ	To 0.1% FSR (0-24mA)
		-		ms typ	See Figure 7
Output Noise (0.1 Hz to 10 Hz Bandwidth)		0.15		LSB p-p	(16-Bit LSB), 10V output, 0-10V range
Output Noise Spectral Density		0.5		nA/√Hz	Measured at 10 kHz, mid-scale output, 0-24mA range

[1] Guaranteed by characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = V_{BOOST_x} = 15 V; DV_{DD} = 2.7 V to 5.5 V; AV_{CC} = 4.5 V to 5.5 V; dc-to-dc converter disabled,;AGND = DGND = $GNDSW_x$ = 0 V; REFIN = 5 V; voltage outputs: R_L = 1 kΩ, C_L = 220 pF; current outputs: R_L = 300 Ω; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	198	ns min	$\overline{SYNC}$ high time
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9	20	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (all DACs updated or any channel has digital slew rate control enabled)
	5	µs min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge (single DAC updated)
t_{10}	10	ns min	$\overline{LDAC}$ pulse width low
t_{11}	500	ns max	$\overline{LDAC}$ falling edge to DAC output response time
t_{12}	See AC Performance Characteristics	µs max	DAC output settling time
t_{13}	10	ns min	CLEAR high time
t_{14}	5	µs max	CLEAR activation time
t_{15}	40	ns max	SCLK rising edge to SDO valid
t_{16}	21	µs min	$\overline{SYNC}$ rising edge to DAC output response time (LDAC = 0) (all DACs updated)
	5	µs min	$\overline{SYNC}$ rising edge to DAC output response time (LDAC = 0) (single DAC updated)
t_{17}	500	ns min	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge
t_{18}	800	ns min	$\overline{RESET}$pulse width
t_{19}[4]	20	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (Ramp enabled)
	5	µs min	$\overline{SYNC}$ high to next $\overline{SYNC}$ low (Ramp disabled)

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with t_R = t_F = 5 ns (10% to 90% of DVDD) and timed from a voltage level of 1.2 V.
[3] See Figure 2 , Figure 3 , Figure 4 and Figure 5
[4] This specification applies if $\overline{LDAC}$ is held low during the write cycle; otherwise, see t_9.

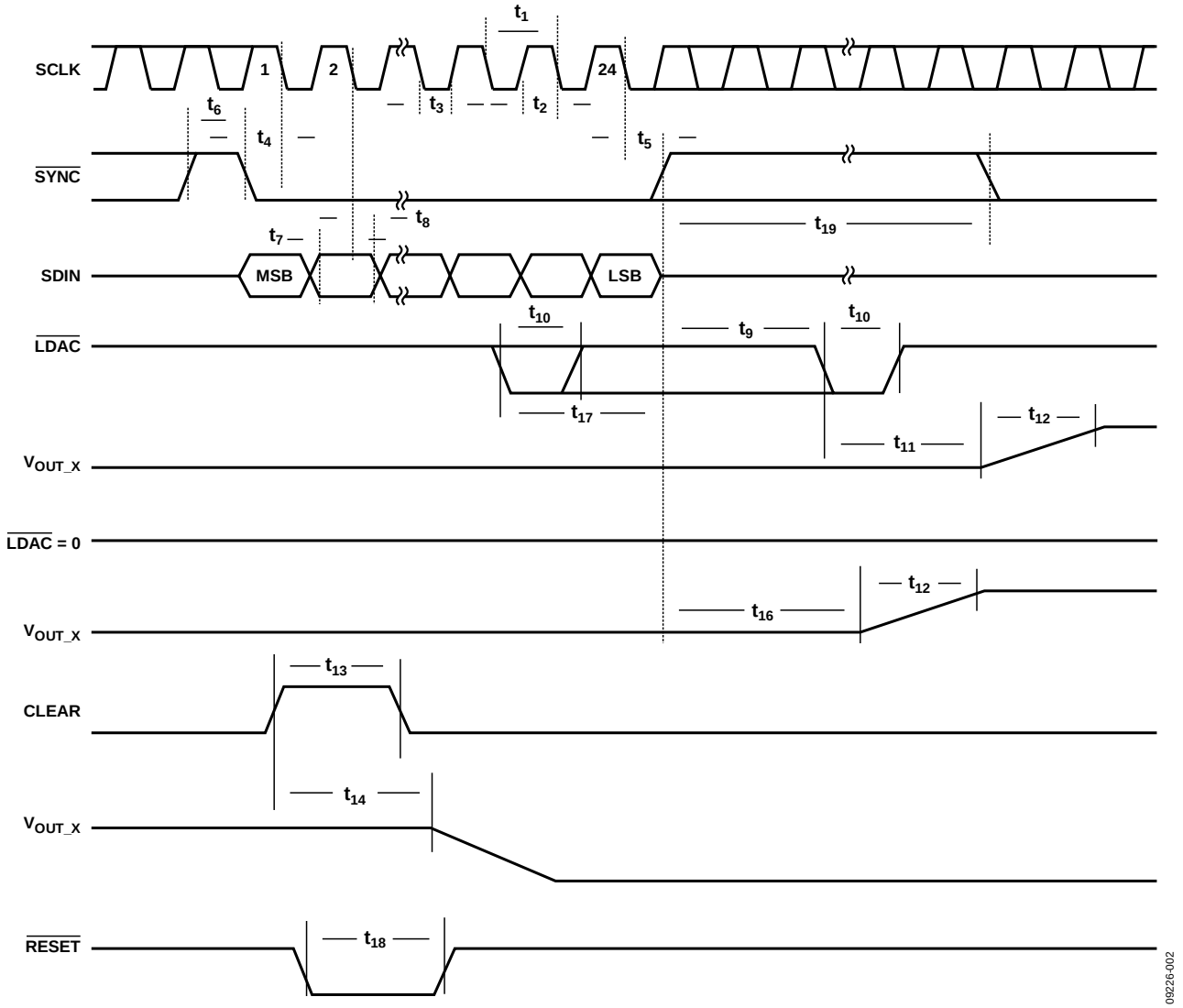


Figure 2. Serial Interface Timing Diagram

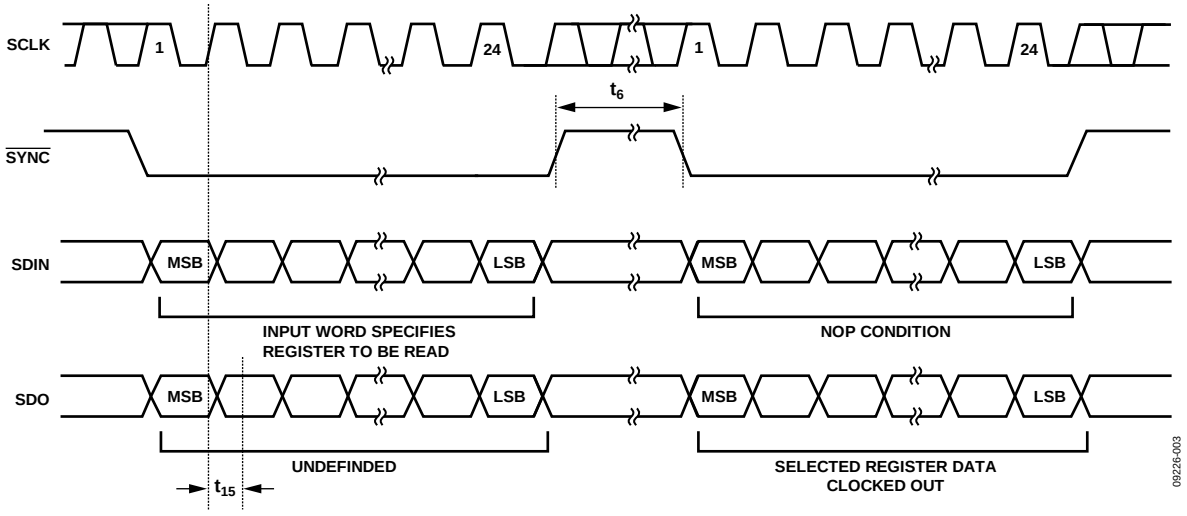


Figure 3. Readback Timing Diagram

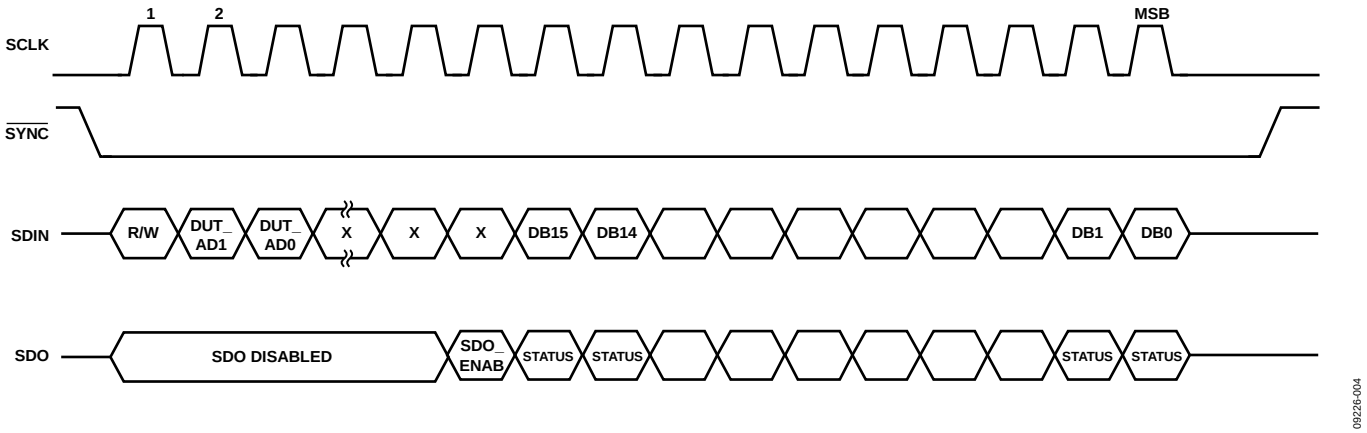


Figure 4. Status Readback during write

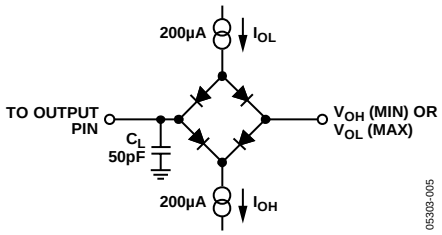


Figure 5. Load Circuit for SDO Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD}, $V_{BOOSTA,B,C,D}$ to AGND, DGND	−0.3 V to +33 V
AV_{cc} to AGND	−0.3 V to +7 V
DVDD to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DVDD + 0.3 V or +7 V (whichever is less)
Digital Outputs to DGND	−0.3 V to DVDD + 0.3 V or +7 V (whichever is less)
REFIN/REFOUT to AGND	−0.3 V to AVDD + 0.3 V or +7 V (whichever is less)
I_{OUT} A,B,C,D to AGND	−0.3 V to V_{BOOST} or 33V if using the DC-DC circuitry.
$SW_{A,B,C,D}$ to AGND	−0.3 to +33 V
$CHART_{A,B,C,D}$ to AGND	−0.3 V to +5 V
AGND, $GNDSW_{A,B,C,D}$ to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial[1]	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
64-Lead LFCSP	
θ_{JA} Thermal Impedance[2]	20°C/W
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C

[2] Based on a JEDEC 4 layer test board

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

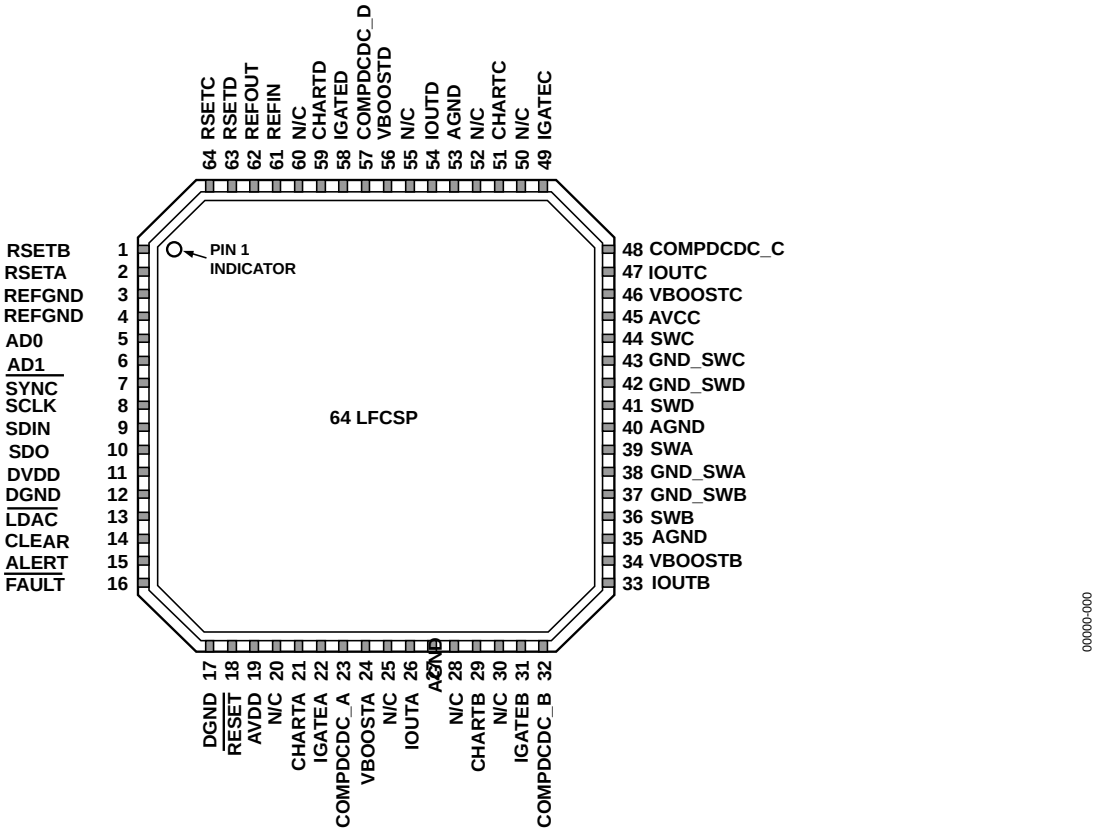


Figure 6. 64 LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	R_{SET_B}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_B} temperature drift performance. See the Features section.
2	R_{SET_A}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_A} temperature drift performance. See the Features section.
3	REFGND	Ground Reference Point for Internal Reference.
4	REFGND	Ground Reference Point for Internal Reference.
5	ADO	Address decode for the DUT on the board.
6	AD1	Address decode for the DUT on the board.
7	$\overline{SYNC}$	Active Low Input. This is the frame synchronization signal for the serial interface. While $\overline{SYNC}$ is low, data is transferred in on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds of up to 30 MHz.
9	SDIN	Serial Data Input. Data must be valid on the falling edge of SCLK.
10	SDO	Serial Data Output. Used to clock data from the serial register in readback mode. See Figure 3 and Figure 4.
11	DV_{DD}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
12	DGND	Digital Ground Pin.
13	$\overline{LDAC}$	Load DAC. Active Low Input. This is used to update the DAC registers and consequently the analog outputs. When tied permanently low the addressed DAC register is updated on the rising edge of $\overline{SYNC}$. If $\overline{LDAC}$ is held high during the write cycle the DAC input register is updated but the output update only takes place at the falling edge of $\overline{LDAC}$. See Figure 2. Using this mode all analog outputs can be updated simultaneously. The $\overline{LDAC}$ pin must not be left unconnected.
14	CLEAR	Active High, Edge Sensitive Input. Asserting this pin sets the Output Current/Voltage to the pre-programmed CLEAR CODE. Only channels enabled to be cleared will be cleared. See features section for

Pin No.	Mnemonic	Description
		more information. When CLEAR is active, the DAC register cannot be written to.
15	ALERT	Active High Output. This pin is asserted when there has been no SPI activity on the interface pins for a predetermined time. See features section for more information.
16	$\overline{\text{FAULT}}$	Active Low Output. This pin is asserted low when an open circuit in current mode is detected or a short circuit in voltage mode is detected or a PEC error is detected or an over temperature is detected (see Features section). Open Drain Output.
17	DGND	Digital Ground Pin.
18	$\overline{\text{RESET}}$	Hardware Reset. Active Low Input.
19	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8 V to 33 V.
20	N/C	No Connection. Do not connect to this pin.
21	CHARTA	Hart Input Connection for DAC Channel A
22	IGATEA	Optional connection for external pass transistor. Not required when using DC-DC. Should be left unconnected.
23	$COMP_{DCDC\_A}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AICC Supply Requirements—Slewing sections for more information).
24	V_{BOOST_A}	Supply for channel A's current output stage (See Figure 14). This is also the supply for the V_{OUT} stage, which is regulated to 15V by the DC-DC. To use the DC-DC feature of the device, connect as shown in Figure 21.
25	N/C	No Connection. Do not connect to this pin.
26	I_{OUT_A}	Current Output Pin for DAC Channel A.
27	AGND	Ground Reference Point for Analog Circuitry.
28	N/C	No Connection. Do not connect to this pin.
29	CHARTB	Hart Input Connection for DAC Channel B
30	N/C	No Connection. Do not connect to this pin.
31	IGATEB	Optional connection for external pass transistor. Not required when using DC-DC. Should be left unconnected.
32	$COMP_{DCDC\_B}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AICC Supply Requirements—Slewing sections for more information).
33	I_{OUT_B}	Current Output Pin for DAC Channel B.
34	V_{BOOST_B}	Supply for channel B's current output stage (See Figure 14). This is also the supply for the V_{OUT} stage, which is regulated to 15V by the DC-DC. To use the DC-DC feature of the device, connect as shown in Figure 21.
35	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
36	$SW_{\_B}$	Switching output for Channel B's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 1.
37	$GNDSW_{\_B}$	Ground connection for DC-DC switching circuit. This pin should always be connected to GND.
38	$GNDSW_{\_A}$	Ground connection for DC-DC switching circuit. This pin should always be connected to GND.
39	$SW_{\_A}$	Switching output for Channel A's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 1.
40	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
41	$SW_{\_D}$	Switching output for Channel D's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 1.
42	$GNDSW_{\_D}$	Ground connections for DC-DC switching circuit. This pin should always be connected to GND.
43	$GNDSW_{\_C}$	Ground connections for DC-DC switching circuit. This pin should always be connected to GND.
44	$SW_{\_C}$	Switching output for Channel C's DC-DC circuitry. To use the DC-DC feature of the device, connect as shown in Figure 1.
45	AV_{CC}	Supply for DC-DC circuitry.
46	V_{BOOST_C}	Supply for channel C's current output stage (See Figure 14). This is also the supply for the V_{OUT} stage, which is regulated to 15V by the DC-DC. To use the DC-DC feature of the device, connect as shown in Figure 21.
47	I_{OUT_C}	Current Output Pin for DAC Channel C.
48	$COMP_{DCDC\_C}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation

Pin No.	Mnemonic	Description
		Capacitors and the AICC Supply Requirements—Slewing sections for more information).
49	IGATEC	Optional connection for external pass transistor. Not required when using DC-DC. Should be left unconnected.
50	N/C	No Connection. Do not connect to this pin.
51	CHARTC	Hart Input Connection for DAC Channel B
52	N/C	No Connection. Do not connect to this pin.
53	AGND	Ground Reference Point for Analog Circuitry. This must be connected to 0 V.
54	I_{OUT_D}	Current Output Pin for DAC Channel D.
55	N/C	No Connection. Do not connect to this pin.
56	V_{BOOST_D}	Supply for channel D's current output stage (See Figure 14). This is also the supply for the V_{OUT} stage, which is regulated to 15V by the DC-DC. To use the DC-DC feature of the device, connect as shown in Figure 21.
57	$COMP_{DCDC\_D}$	DC-to-DC Compensation Capacitor. Connect a 10 nF capacitor from this pin to ground. Used to regulate the feedback loop of the dc-to-dc converter. Alternatively, if using an external compensation resistor, place a resistor in series with a capacitor to ground from this pin (see the DC-to-DC Converter Compensation Capacitors and the AICC Supply Requirements—Slewing sections for more information).
58	IGATED	Optional connection for external pass transistor. Not required when using DC-DC. Should be left unconnected.
59	CHARTD	Hart Input Connection for DAC Channel D
60	N/C	No Connection. Do not connect to this pin.
61	REFIN	External Reference Voltage Input.
62	REFOUT	Internal Reference Voltage Output.
63	R_{SET_D}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_D} temperature drift performance. See the Features section.
64	R_{SET_C}	An external, precision, low drift 15 kΩ current setting resistor can be connected to this pin to improve the I_{OUT_C} temperature drift performance. See the Features section.
	Exposed PADDLE	CONNECTED TO AGND

TYPICAL PERFORMANCE CHARACTERISTICS

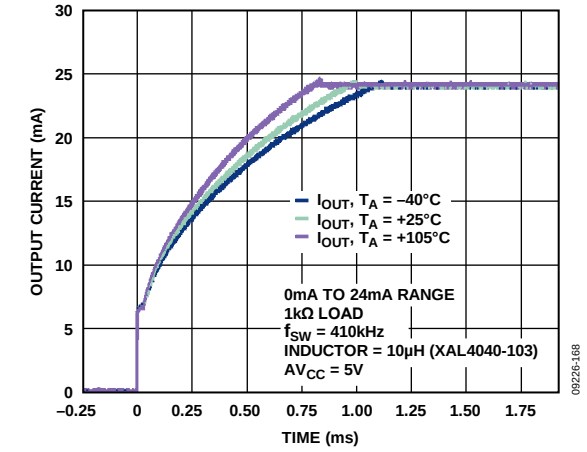


Figure 7. Output Current Settling with DC-to-DC Converter vs. Temperature (See Figure 21)

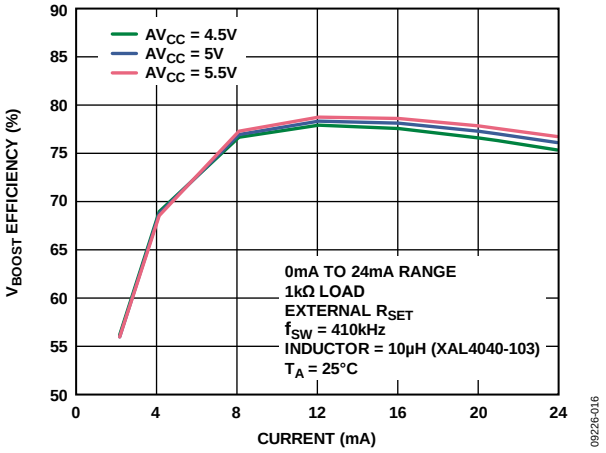


Figure 8. Efficiency at V_{BOOST_X} vs. Output Current (See Figure 21)

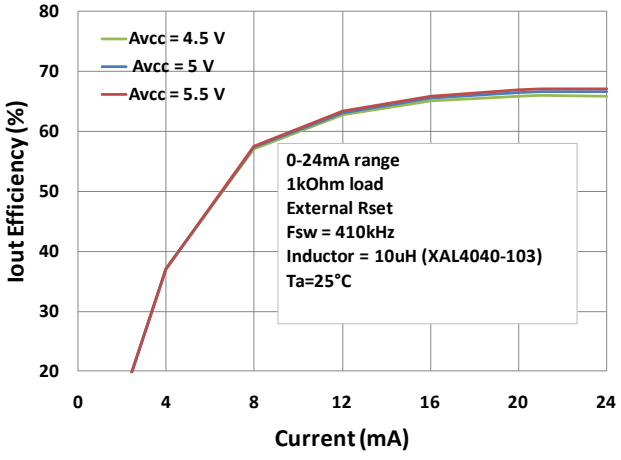


Figure 9. Output Efficiency vs. Output Current(See Figure 21)

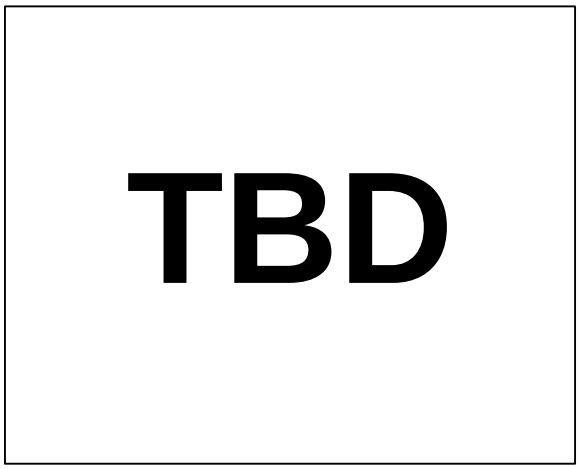


Figure 10

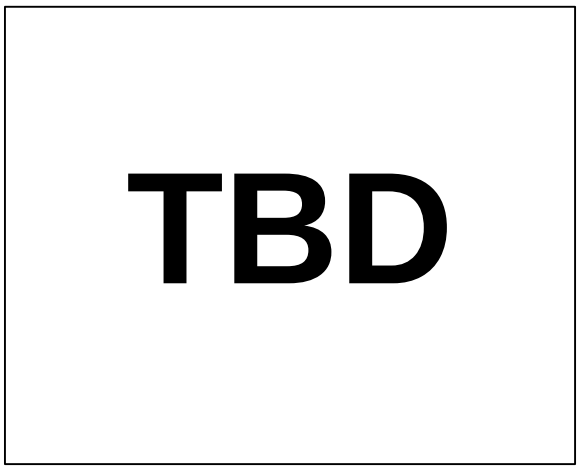


Figure 11

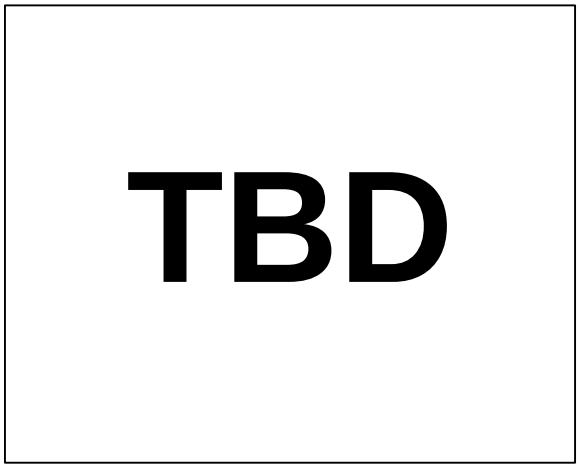


Figure 12

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity, is a measure of the maximum deviation, in LSBs, from the best fit line through the DAC transfer function.

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5757/AD5737 is monotonic over its full operating temperature range.

Negative Full-Scale Error/Zero-Scale Error
Negative full-scale error is the error in the DAC output voltage when 0x0000 (straight binary coding) is loaded to the DAC register.

Zero-Scale TC
This is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Bipolar Zero Error
Bipolar zero error is the deviation of the analog output from the ideal half-scale output of 0 V when the DAC register is loaded with 0x8000 (straight binary coding).

Bipolar Zero TC
Bipolar zero TC is a measure of the change in the bipolar zero error with a change in temperature. It is expressed in ppm FSR/°C.

Offset Error
In voltage output mode, offset error is the deviation of the analog output, when in bi-polar output ranges, from the ideal quarter-scale output when the DAC register is loaded with 0x4000 (straight binary coding).

In current output mode, offset error is the deviation of the analog output from the ideal zero-scale output when all DAC registers are loaded with 0x0000.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed in % FSR.

Gain TC
This is a measure of the change in gain error with changes in temperature. Gain Error TC is expressed in ppm FSR/°C.

Full-Scale Error
Full-Scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale − 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

Full Scale TC
Full-scale TC is a measure of the change in full-scale error with changes in temperature and is expressed in ppm FSR/°C.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, including INL error, offset error, gain error, temperature, and time. TUE is expressed in % FSR.

DC Crosstalk

This is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC while monitoring another DAC, which is at midscale.

Current Loop Compliance Voltage
The maximum voltage at the I_{OUT_x} pin for which the output current is equal to the programmed value.

Voltage Reference Thermal Hysteresis
Voltage reference thermal hysteresis is the difference in output voltage measured at +25°C compared to the output voltage measured at +25°C after cycling the temperature from +25°C to −40°C to +105°C and back to +25°C. The hysteresis is specified for the first and second temperature cycles and is expressed in mV.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. The output slewing speed of a voltage-output digital-to-analog converter is usually limited by the slew rate of the amplifier used at its output. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5757/AD5737 is powered-on. It is specified as the area of the glitch in nV-sec.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state, but the output voltage remains constant. It is normally

specified as the area of the glitch in nV-sec and is measured when the digital input code is changed by 1 LSB at the major carry transition (~0x7FFF to 0x8000).

Glitch Impulse Peak Amplitude
Glitch impulse peak amplitude is the peak amplitude of the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the amplitude of the glitch in mV and is measured when the digital input code is changed by 1 LSB at the major carry transition (~0x7FFF to 0x8000).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus.

DAC-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and a subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with LDAC low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-sec.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

Line Regulation

Line regulation is the change in reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

DC-to-DC Converter Headroom

This is the difference between the voltage required at the current output and the voltage supplied by the dc-dc converter.

Output Efficiency

$$\frac{I_{OUT}^2 \times R_{LOAD}}{AV_{CC} \times AI_{CC}}$$

This is defined as the power delivered to a channel's load vs. the power delivered to the channel's dc-to-dc input.

Efficiency at V_{BOOST_x}

$$\frac{I_{OUT} \times V_{BOOST}}{AV_{CC} \times AI_{CC}}$$

This is defined as the power delivered to a channel's V_{BOOST_x} supply vs. the power delivered to the channel's dc-to-dc input. The V_{BOOST_x} quiescent current is considered part of the dc-to-dc converter's losses.

THEORY OF OPERATION

The AD5757/AD5737 is a quad, precision digital to current loop converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop outputs. The current ranges available are; 0 to 20mA, 0 to 24mA and 4 to 20mA. The desired output configuration is user selectable via the DAC Control Register.

On chip dynamic power control minimizes package power dissipation in current mode.

DAC ARCHITECTURE

The DAC core architecture of the AD5757/AD5737 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 13. The 4 MSBs of the 16/12-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects 1 of 15 matched resistors to either ground or the reference buffer output. The remaining 12/8 bits of the data-word drive switches S0 to S11 /S7 of a 12/8-bit voltage mode R-2R ladder network.

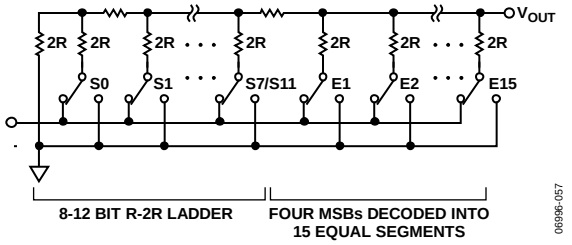


Figure 13. DAC Ladder Structure

The voltage output from the DAC core is converted to a current (see Figure 14) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground.

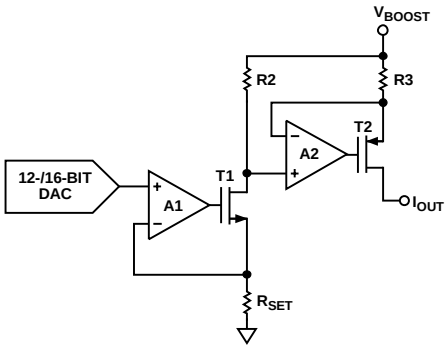


Figure 14. Voltage to Current conversion circuitry

Reference Buffers

The AD5757/AD5737 can operate with either an external or internal reference. The reference input has an input range of 4 V to 5 V, 5 V for specified performance. This input voltage is then buffered before it is applied to the DAC.

POWER ON STATE OF AD5757/AD5737

On initial power-up of the AD5757/AD5737 with the Iout pin in tri-state mode.

SERIAL INTERFACE

The AD5757/AD5737 is controlled over a versatile 3-wire serial interface that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI™, MICROWIRE™, and DSP standards. Data coding is always straight binary.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK.

If packet error checking, or PEC is enabled, an additional eight bits must be written to the AD5757/AD5737, creating a 32-bit serial interface.

There are two ways in which the DAC outputs can be updated: individual updating or simultaneous updating of all DACs.

Individual DAC Updating

In this mode, $\overline{\text{LDAC}}$ is held low while data is being clocked into the DAC data register. The addressed DAC output is updated on the rising edge of $\overline{\text{SYNC}}$.

Simultaneous Updating of All DACs

In this mode, $\overline{\text{LDAC}}$ is held high while data is being clocked into the DAC data register. Only the first write to each channel's DAC data register is valid after $\overline{\text{LDAC}}$ is brought high. Any subsequent writes while $\overline{\text{LDAC}}$ is still held high are ignored, though they are loaded into the DAC data register. All the DAC outputs are updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ is taken high.

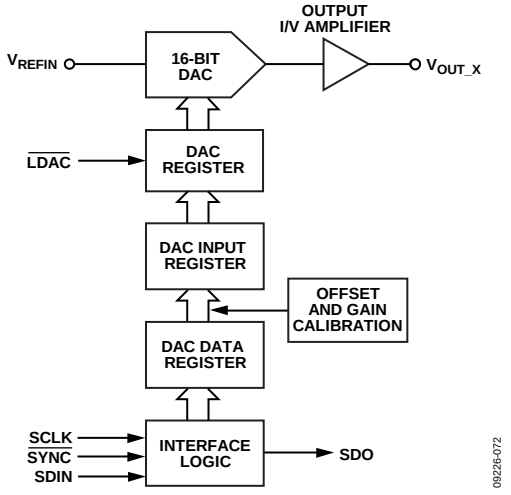


Figure 15. Simplified Serial Interface of Input Loading Circuitry for One DAC Channel

REGISTERS

Table 7 below shows an overview of the Registers for the AD5757/AD5737

Table 7. Data and Control Registers for AD5757/AD5737

DATA REGISTERS	**Description**
DAC Data Register (X4)	Used to write a DAC code to each DAC channel. AD5757 Data bits (D15 to D0), AD5737 Data Bits (D15 to D4). There are four DAC Data Registers, one per DAC Channel.
Gain Register (X4)	Used to program gain trim on per channel basis. AD5757 Data bits (D15 to D0), AD5737 Data Bits (D15 to D4). There are four Gain Registers, one per DAC channel.
Offset Register (X4)	Used to program offset tro, on per channel basis. AD5757 Data bits (D15 to D0), AD5737 Data Bits (D15 to D4). There are four Offset Registers, one per DAC channel.
Clear Code Register (X4)	Used to program Clear Code on per channel basis. AD5757 Data bits (D15 to D0), AD5737 Data Bits (D15 to D4). There are four Clear Code Registers, one per DAC channel.
CONTROL REGISTERS	
Main Control Register	Used to Configure the part for main operation. Sets functions such as status readback during write, enable output on all channels simultaneously, power on all DC-DC blocks simultaneously, enables and sets conditions of watchdog timer. See Features Section for more details.
Software Register	Has two functions. Used to perform a reset. Is also used as part of the watchdog timer feature to verify correct data communication operation.
Slew Rate Control Register (X4)	Use to program the slew rate of the output. There are four Slew Rate Control Registers, one per channel.
DAC Control Register (X4)	These registers are used to control the following: 1) Set the output range, e.g. 4-20ma. 2) Set whether Internal/External sense Resistor used. 3) Enable/Disable channel for CLEAR. 4) Enable/Disable output on a per channel basis. 5) Power on DC-DC on a per channel basis. There are four DAC Control Registers, one per DAC channel.
DC-DC Control Register	Use to set the DC-DC Control parameters. Can control DC-DC max voltage, phase and frequency.
READBACK	
Status Register	

PROGRAMMING SEQUENCE TO WRITE/ENABLE THE OUTPUT CORRECTLY

To correctly write to and set up the part from a power-on condition, use the following sequence.

1. Perform a hardware or software reset after initial power-on.
2. The dc-to-dc converter supply block must be configured. Set the dc-to-dc switching frequency, maximum output voltage allowed, and the phase that the four dc-to-dc channels clock at.
3. Configure the DAC control register on a per channel basis. The output range is selected, and the dc-to-dc converter block is enabled (DC_DC bit). Other control bits can be configured at this point; however, the output enable bit (OUTEN) bit should not be set.
4. Write the required code to the DAC data register. This implements a full DAC calibration internally.
5. Write to the DAC control register again to enable the output (set the OUTEN bit).

A flowchart of this sequence is shown in Figure 16.

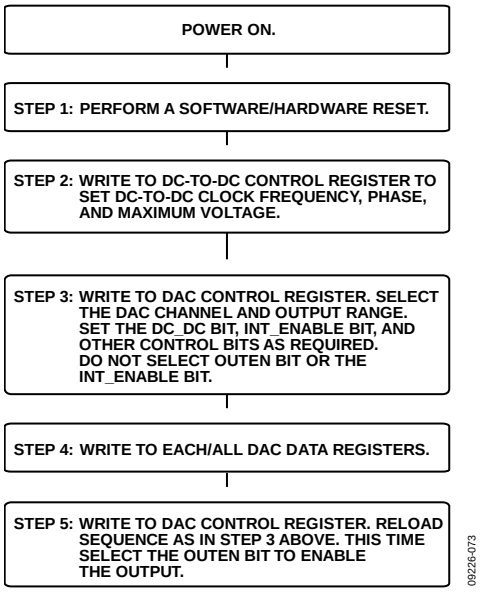


Figure 16. Programming Sequence for Enabling the Output Correctly

CHANGING AND REPROGRAMMING THE RANGE

When changing between ranges, the same sequence as described in the Programming Sequence to Write/Enable the Output Correctly section should be used. It is recommended to set the range to its zero point (can be midscale or zero scale) prior to disabling the output. Because the dc-to-dc switching frequency, maximum voltage, and phase have already been selected, there is no need to reprogram these. A flowchart of this sequence is shown in Figure 17.

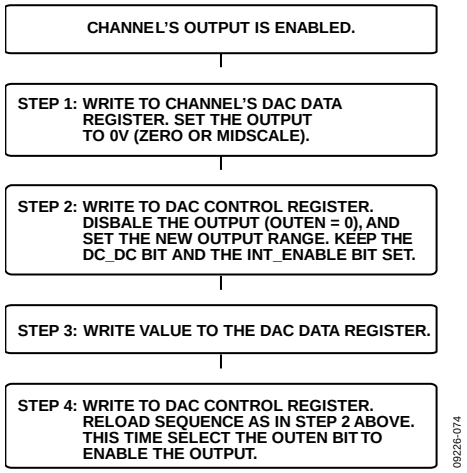


Figure 17. Steps for Changing the Output Range

DATA REGISTERS

The input register is 24 bits wide. When writing to a data register the following format must be used:

Table 8. AD5757/AD5737 Writing to a Data Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	

Table 9. AD5757/AD5737 Input Register Decode

Register	Function			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
DUT_AD1, DUT_AD0	Used in association with External Pins AD1, AD0 to determine which AD5757/AD5737 device is being addressed by the system controller.			
	DUT_AD1	**DUT_AD0**		**Function**
	0	0		Addresses Part with Pins AD1=0, AD0=0
	0	1		Addresses Part with Pins AD1=0, AD0=1
	1	0		Addresses Part with Pins AD1=1, AD0=0
	1	1		Addresses Part with Pins AD1=1, AD0=1
DREG2, DREG1, DREG0	Selects whether a data register or a control register is written to. If a control register is selected, a further decode of CREG bits is required to select the particular control register, as detailed below.			
	DREG2	**DREG1**	**DREG0**	**Function**
	0	0	0	Write to DAC Data Register (Individual Channel Write)
	0	1	0	Write to Gain Register
	0	1	1	Write to Gain Register (ALL DACS)
	1	0	0	Write to Offset Register
	1	0	1	Write to Offset Register (ALL DACS)
	1	1	0	Write to Clear Code Register
	1	1	1	Write to a Control Register
DAC_AD1, DAC_AD0	These bits are used to decode the DAC channel			
	DAC_AD1	**DAC_AD0**	**DAC Channel/ Register Address**	
	0	0	DAC A	
	0	1	DAC B	
	1	0	DAC C	
	1	1	DAC D	
	X	X	These are don't cares if they are not relevant to the operation being performed.	

DAC DATA REGISTER

Table 10. Programming the AD5757 DAC Data Registers

When writing to the AD5757 DAC Data Registers D15-D0 are used for DAC DATA bits. See Table x for input register decode.

MSB LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	DATA

Table 11. Programming the AD5737 DAC Data Registers

When writing to the AD5737 DAC Data Registers D15-D4 are used for DAC DATA bits. See Table x for input register decode.

MSB LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D4	D3	D2	D1	D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	DATA	X	X	X	X

GAIN REGISTER

The Gain Register stores the Gain Code (M) which is used in the DAC transfer function to calculated the overall DAC input code (see formula below). The Gain Register is addressed by setting DREG bits to '0,1,0'. The DAC address bits select which DAC channel the gain write is addressed to. It is possible to write the same gain code to all 4 DAC channels at the same time by setting the DREG bits to 011. The AD5757/AD5737 Gain Register is a 16/12 bit register (bits G15.. G0/G3) and allows the user to adjust the gain of each channel in steps of 1 LSB as shown in the Table below. For the AD5737, the last 4 bits should be set to 1. The Gain Register coding is straight binary. In theory the gain can be tuned across the full range of the output. In practice, the maximum recommended gain trim is about 50% of programmed range in order to maintain accuracy.

Table 12. Programming the AD5757 Gain Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	**D15-D0**
0	DEVICE ADDRESS		010			DAC Channel Address		G15 to G0

Table 13. Programming the AD5737 Gain Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	D15-D4	D3	D2	D1	D0
0	DEVICE ADDRESS		010			DAC Channel Address		G15 to G4	1	1	1	1

Table 14. AD5757 Gain Register

Gain Adjustment	**G15**	**G14**	**G13**	**G12 to G4**	**G3**	**G2**	**G1**	**G0**
+65535 LSBs	1	1	1	1	1	1	1	1
+65534 LSBs	1	1	1	1	1	1	0	0
	-	-	-	-	-	-	-	-
1 LSBs	0	0	0	0	0	0	0	1
0 LSBs	0	0	0	0	0	0	0	0

Table 15. AD5737 Gain Register

Gain Adjustment	**G15**	**G14**	**G13 to G5**	**G4**	**G3**	**G2**	**G1**	**G0**
+8192 LSBs	1	1	1	1	X	X	X	X
+8191 LSBs	1	1	1	0	X	X	X	X
	-	-	-	-	X	X	X	X
1 LSBs	0	0	0	1	X	X	X	X
0 LSBs	0	0	0	0	X	X	X	X

OFFSET REGISTER

The Offset Register is addressed by setting the DREG BITS to DREG2 =1 DREG1=0, DREG0=0. The DAC address bits select with which DAC channel the offset write is addressed to. It is possible to write the same offset code to all 4 DAC channels at the same time by setting the DREG bits to 101. The AD5757/AD5737 offset code is 16/12 bit (bits OF15.. OF0/OF3) and allows the user to adjust the offset of each channel by –32768/8192 LSBs to +32767/8191 LSBs in steps of 1 LSB as shown in the Table below. For the AD5737, the last 4 bits are ignored and should be set to zero. The Offset Register coding is straight binary. The default code in the Offset Register is 0x8000/0x800. This will result in zero offset programmed to the output.

Table 16. Programming the AD5757 Offset Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	D15 to D0
0	DEVICE ADDRESS		100			DAC Channel Address		OF15 to OF0

Table 17. Programming the AD5737 Offset Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	D15 to D4	D3	D2	D1	D0
0	DEVICE ADDRESS		100			DAC Channel Address		OF15 to OF4	0	0	0	0

Table 18. AD5757 Offset Register options

Offset Adjustment	OF15	OF14	OF13	OF12 to OF4	OF3	OF2	OF1	OF0
+32768 LSBs	1	1	1	1	1	1	1	1
+32767 LSBs	1	1	1	1	1	1	0	0
	-	-	-	-	-	-	-	-
No Adjustment (default)	1	0	0	0	0	0	0	0
	-	-	-	-	-	-	-	-
–32767 LSBs	0	0	0	0	0	0	0	0
–32768 LSBs	0	0	0	0	0	0	0	0

Table 19. AD5737 Offset Register options

Offset Adjustment	OF15	OF14	OF13	OF12 to OF4	OF3	OF2	OF1	OF0
+8192 LSBs	1	1	1	1	X	X	X	X
+8191 LSBs	1	1	1	1	X	X	X	X
	-	-	-	-	X	X	X	X
No Adjustment (default)	1	0	0	0	X	X	X	X
	-	-	-	-	X	X	X	X
–8191 LSBs	0	0	0	1	X	X	X	X
–8192 LSBs	0	0	0	0	X	X	X	X

CLEAR CODE REGISTER

There is a per channel Clear Code Register. The Clear Code Register is 16 bits wide and is addressed by setting the DREG bits to'1,1,0'. It is also possible, via software, to enable/disable on a per channel basis which channels will be cleared when the CLEAR pin is activated. The default clear code is all 0's. See Features section for more information.

Table 20. Programming AD5757 Clear Code Register

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	DREG2	DREG1	DREG0	DAC_AD1	DAC_AD0	CLEAR CODE
0	DEVICE ADDRESS		110			DAC Channel Address		DATA

Table 21. Programming the AD5737 Offset Register

R/$\overline{W}$	DUT_ AD1	DUT_ AD0	DREG2	DREG1	DREG0	DAC_ AD1	DAC_ AD0	D15 to D4	D3	D2	D1	D0
0	DEVICE ADDRESS		110			DAC Channel Address		CLEAR CODE	0	0	0	0

CONTROL REGISTERS

When writing to a data register the following format must be used:

Table 22. Writing to a control register

MSB LSB

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	1	1	1	DAC_AD1	DAC_AD0	CREG2	CREG1	CREG0	

See Table 9 for configuration on bits D23 to D16. The control registers are addressed by setting the DREG bits to DREG2 = 1, DREG1 = 1, DREG0=1 and then setting the CREG2, CREG1 and CREG0 bits to the appropriate decode address for that register as per **Table 23** below. These CREG bits select between the various control registers.

Table 23. Register Access Decode

CREG2, (D15)	CREG1, (D14)	CREG0, (D13)	
0	0	0	Slew Rate Control Register (one per channel)
0	0	1	Main Control Register
0	1	0	DAC Control Register (one per channel)
0	1	1	DC-DC Control Register
1	0	0	Software Register (one per channel)

MAIN CONTROL REGISTER

CREG2, CREG1, CREG0 are set to '0,0,1' to select the Main Control Register. The Main Control Register options are shown below.

Table 24. Programming the Main Control Register

MSB **LSB**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3 to D0
0	0	1	0	STATREAD	EWD	WD1	WD0	X	X	OUTEN ALL	DC-DC ALL	X

Table 25. Main Control Register Functions.

Option	Description
STATREAD	Enable status readback during a write. See Features section. STATREAD =1, Enable STATREAD =0, Disable
EWD	Enable Watchdog Timer. See features section for more information. EWD=1, Enable Watchdog EWD=0, Disable Watchdog
WD1, WD0	Timeout Select Bits. Used to select timeout period for watchdog timer. WD1 | WD0 | 0 | 0 | 5ms 0 | 1 | 10ms 1 | 0 | 100ms 1 | 1 | 200ms
OUTEN ALL	Enables the output on all 4 DAC simultaneously. Do not use the OUTEN ALL bit when using the OUTEN bit in the DAC Control Registers.
DC_DCALL	When set, Powers up the DC-DC on all 4 channels Simultaneously. To Power down the DC-DCs all channels outputs must first be disabled. Do not use the DC_DCALL bit when using the DC_DC bit in the DAC Control Registers.

DAC CONTROL REGISTER

The DAC Control Register is used to configure each DAC Channel. The DAC Control Register is selected by setting bits CREG2, CREG1, CREG0 to 0,1,0.

Table 26. Programming DAC Control Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

0	1	0	X	X	X	X	INT_ENABLE	CLR_EN	OUTEN	RSET	DC-DC	X	R2	R1	R0

Table 27. DAC Control Register Functions

Option	Description
INT_ENABLE	Powers up the DC-DC, DAC and internal amplifiers for the selected channel. Does not enable the output. Can only be done on a per channel basis.
CLR_EN	Per channel Clear Enable bit. Selects if this channel will clear when the CLEAR pin is activated. CLR_EN=1, channel will clear when part is cleared. CLR_EN=0, channel will not clear when part is cleared.
OUTEN	Enables/Disables the selected output channel OUTEN=1, Enables channel OUTEN=0, Disable channel
RSET	Selects internal or external current sense resistor for selected DAC channel RSET = 0 Selects external Resistor RSET = 1 Selects Internal Resistor
DC_DC	Powers the DC-DC on selected channel. DC_DC = 1, Power up DC_DC DC_DC = 0, Power down DC_DC This allows per channel DC_DC power up/down. To power down the DCDC, OUTEN and INT_ENABLE bits must also be set to 0. All DC-DCs can also be powered up simultaneously using DCDC_All bit in the Main Control Register.
R2,R1,R0	Selects output range enabled.

R2	R1	R0	Output Range Selected
1	0	0	4 to 20 mA Current Range
1	0	1	0 to 20 mA Current Range
1	1	0	0 to 24 mA Current Range

SOFTWARE REGISTER

The Software Register has three functions. It allows the user to perform a software reset to the part. It can be used to set bit D11 in the Status Register. Lastly it is also used as part of the watchdog feature to ensure that the SPI interface connections are working properly. To ensure all the datapath lines are working properly (i.e. SDI/SCLK/SYNC), the user must write 0x195 to the Software Register within the timeout period. If this command is not received within the timeout period, the ALERT pin will signal a fault condition. Note. This is only required when the Watchdog Timer function is enabled.

Table 28. Programming the Software Register

To program a software reset you need to write 1,0,0 to CREG2, CREG1, CREG0.

MSB				LSB
D15	**D14**	**D13**	**D12**	**D11 to D0**
1	0	0	User Program Bit	RESET CODE/SPI CODE

Table 29. Software Register Functions

User Program Bit	This bit is mapped to bit D11 of the Status Register. When this bit is set to 1 bit D11 of the Status Register is set to 1. Likewise when D12 is set to 0 bit D11 of the Status Register is also set to zero. This feature can be used to ensure the SPI pins are working correctly by writing known bit to this register and reading back corresponding bit from the Status Register.	
RESET CODE/SPI CODE	**Option**	**Description**
	RESET CODE	Writing 0x555 to D11-D0 performs a reset.
	SPI CODE	If Watchdog Timer feature enabled, 0x195 must be written to the Software Register (D11-D0) within every timeout period to ensure valid data communication path.

DC-DC CONTROL REGISTER

The DC-DC Control Register allows the user control over the DC-DC Switching Frequency, and of the phase of when the per channel switching starts. The maximum allowable DC-DC output frequency is also programmable.

Table 30. Programming the DC-DC Control Register

MSB							LSB
D15	**D14**	**D13**	**D12 to D7**	**D6**	**D5 to D4**	**D3 to D2**	**D1 to D0**
0	1	1	X	DC-DC Comp	DC-DC phase	DC-DC Freq	DC-DC MaxV

Table 31. DC-DC Control Register Options

Option	Description
DC-DC Comp	Selects between an internal and external compensation resistor for the dc-dc converter. See the DC-to-DC Converter Compensation Capacitors and AICC Supply Requirements—Slewing sections for more information. 0 = selects the internal 150 kΩ compensation resistor (default). 1 = bypasses the internal compensation resistor for the dc-to-dc converter. In this mode, an external dc-to-dc compensation resistor must be used; this is placed at the $COMP_{DCDC\_x}$ pin in series with the 10 nF dc-to-dc compensation capacitor to ground. Typically, a ~50 kΩ resistor is recommended.
DC-DC Phase	User programmable dc-to-dc converter phase (between channels). 00 = all dc-to-dc converters clock on same edge (default). 01 = Channel A and Channel B clock on same edge, Channel C and Channel D clock on opposite edge. 10 = Channel A and Channel C clock on same edge, Channel B and Channel D clock on opposite edge. 11 = Channel A, Channel B, Channel C, and Channel D clock 90° out of phase from each other.
DC-DC Freq	DC-to-DC switching frequency; these are divided down from the internal 13 MHz oscillator. 00 = 250 ± 10% kHz. 01 = 410 ± 10% kHz (default). 10 = 650 ± 10% kHz.
DC-DC MaxV	Maximum allowed V_{BOOST_x} voltage supplied by the dc-to-dc converter. 00 = 23 V + 1 V/−1.5 V (default). 01 = 24.5 V ± 1 V. 10 = 27 V ± 1 V 11 = 29.5 V ± 1V

SLEW RATE CONTROL REGISTER

This register is used to program the slew rate control for the selected DAC Channel. The CREG bits are set to '0,0,0' to select the Slew Rate Control Register. SR_CLOCK and SR_STEP allow the user to control the rate of the output SLEW. With the slew rate control feature disabled the output value will change at a rate limited by the output drive circuitry and the attached load. **SE** enables output slew rate control. It can be both programmed and enabled/disabled on a per channel basis. For more information see the features section.

Table 32. Programming the Slew Rate Control Register

D15	D14	D13	D12	D11-D7	D6 to D3	D2 to D0
0	0	0	SE	X	SR_CLOCK	SR_STEP

READBACK OPERATION

Readback mode is invoked by setting the R/$\overline{W}$ bit = 1 in the serial input register write. With R/$\overline{W}$ = 1, bits DUT_AD1, DUT_AD0, in association with bits RD4, RD3, RD2, RD1, RD0 (See Table 34), select the register to be read. The remaining data bits in the write sequence are don't care. During the next SPI transfer, the data appearing on the SDO output contains the data from the previously addressed register. The readback diagram in Figure 3 shows the readback sequence.

Table 33. Input Shift Register Contents for a read operation

D23	D22	D21	D20	D19	D18	D17	D16	D15 to D0
R/$\overline{W}$	DUT_AD1	DUT_AD0	RD4	RD3	RD2	RD1	RD0	X

Table 34. Read Address Decoding

RD4	RD3	RD2	RD1	RD0	Function
0	0	0	0	0	Read DACA Data Register
0	0	0	0	1	Read DACB Data Register
0	0	0	1	0	Read DACC Data Register
0	0	0	1	1	Read DACD Data Register
0	0	1	0	0	Read Control Register DAC A
0	0	1	0	1	Read Control Register DAC B
0	0	1	1	0	Read Control Register DAC C
0	0	1	1	1	Read Control Register DAC D
0	1	0	0	0	Read Gain Register A
0	1	0	0	1	Read Gain Register B
0	1	0	1	0	Read Gain Register C
0	1	0	1	1	Read Gain Register D
0	1	1	0	0	Read Offset Register A
0	1	1	0	1	Read Offset Register B
0	1	1	1	0	Read Offset Register C
0	1	1	1	1	Read Offset Register D
1	0	0	0	0	Clear Code Register DAC A
1	0	0	0	1	Clear Code Register DAC B
1	0	0	1	0	Clear Code Register DAC C
1	0	0	1	1	Clear Code Register DAC D
1	0	1	0	0	Slew Rate Control Register DAC A
1	0	1	0	1	Slew Rate Control Register DAC B
1	0	1	1	0	Slew Rate Control Register DAC C
1	0	1	1	1	Slew Rate Control Register DAC D
1	1	0	0	0	Read Status Register
1	1	0	0	1	Read Main Control Register
1	1	0	1	0	Read DC-DC Control Register

Read Back Example

To read back the Gain Register of Device #1 Channel A on the AD5757, the following sequence should be implemented:

1. Write 0xA80000 to the AD5757 input register. This configures the AD5757 device address #1 for read mode with the Gain Register of channel A selected.. Note that all the data bits, D15 to D0, are don't care.
2. Follow this with any read/write command. During this command, the data from the selected Gain Register is clocked out on the SDO line.

STATUS REGISTER

The status register is a read only register. This register contains any fault information as a well as a ramp active bit and a user toggle bit. By setting the STATREAD bit in the main control register, the status register contents can be read back on the SDO pin during every write sequence. Alternatively, if not setting the STATREAD bit, the status register can be read using the normal readback operation.

Table 35. Decoding the Status Register

MSB **LSB**

D15 to D12	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	DC-DCD	DC-DCC	DC-DCB	DC-DCA	User Toggle Bit	PEC ERROR	RAMP ACTIVE	OVER TEMP	X	X	X	X	I_{OUT_D} Fault	I_{OUT_C} Fault	I_{OUT_B} Fault	I_{OUT_A} Fault

Table 36. Status Register Options

Option	Description
DC-DCD	In current output, mode, this bit is set on Channel D if the dc-to-dc converter cannot maintain compliance (it may be hitting its V_{MAX} voltage). In this case, the I_{OUT_D} fault bit is also set. See the DC-to-DC Converter VMAX Functionality section for more information on this bit's operation under this condition. In voltage output mode, this bit is set if, on Channel D, the dc-dc converter is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{\text{FAULT}}$ pin going high.
DC-DCC	In current output mode, this bit is set on Channel C if the dc-to-dc converter cannot maintain compliance (it may be hitting its V_{MAX} voltage). In this case, the I_{OUT_C} fault bit is also set. See the DC-to-DC Converter VMAX Functionality section for more information on this bit's operation under this condition. In voltage output mode, this bit is set if, on Channel C, the dc-dc converter is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{\text{FAULT}}$ pin going high.
DC-DCB	In current output mode, this bit is set on Channel B if the dc-to-dc converter cannot maintain compliance (it may be hitting its V_{MAX} voltage). In this case, the I_{OUT_B} fault bit is also set. See the DC-to-DC Converter VMAX Functionality section for more information on this bit's operation under this condition. In voltage output mode, this bit is set if, on Channel B, the dc-dc converter is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{\text{FAULT}}$ pin going high.
DC-DC A	In current output mode, this bit is set on Channel A if the dc-to-dc converter cannot maintain compliance (it may be hitting its V_{MAX} voltage). In this case, the I_{OUT_A} fault bit is also set. See the DC-to-DC Converter VMAX Functionality section for more information on this bit's operation under this condition. In voltage output mode, this bit is set if, on Channel A, the dc-dc converter is unable to regulate to 15 V as expected. When this bit is set, it does not result in the $\overline{\text{FAULT}}$ pin going high.
User Toggle Bit	User Writable bit that the user can set and readback while doing a Status Register read. This can be used to verify data communications if needed.
PEC ERROR	Denotes a PEC Error on the SPI Interface Transmit.
OVER TEMP	This bit will be set if the AD5757/AD5737 core temperature exceeds approx. 150°C.
RAMP ACTIVE	This bit will be set while any one of the output channels are slewing (slew rate control enabled on at least one channel)
I_{OUT_D} Fault	This bit is set if a fault is detected on the I_{OUT_D} pin.
I_{OUT_C} Fault	This bit is set if a fault is detected on the I_{OUT_C} pin.
I_{OUT_B} Fault	This bit is set if a fault is detected on the I_{OUT_C} pin.
I_{OUT_A} Fault	This bit is set if a fault is detected on the I_{OUT_A} pin.

FEATURES

OUTPUT FAULT

The AD5757/AD5737 is equipped with a $\overline{\text{FAULT}}$ pin, an active low open-drain output allowing several AD5757/AD5737 devices to be connected together to one pull-up resistor for global fault detection. The $\overline{\text{FAULT}}$ pin is forced active by any one of the following fault scenarios:

- The voltage at I_{OUT_x} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with windowed limits because this requires an actual output error before the $\overline{\text{FAULT}}$ output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately 1 V of remaining drive capability. Thus, the $\overline{\text{FAULT}}$ output activates slightly before the compliance limit is reached.
- An interface error is detected due to a PEC failure. See the Packet Error Checking section.
- If the core temperature of the AD5757/AD5737 exceeds approximately 150°C.

The I_{OUT_X} fault, PEC error, and over TEMP bits bits of the Status Register are used in conjunction with the $\overline{\text{FAULT}}$ output to inform the user which one of the fault conditions caused the $\overline{\text{FAULT}}$ output to be activated.

DIGITAL OFFSET AND GAIN CONTROL

Each DAC channel has a gain (M) and offset (C) register, which allow trimming out of the gain and offset errors of the entire signal chain. Data from the DAC Data Register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the DAC2 register.

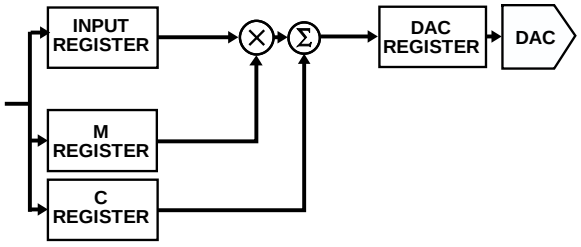


Figure 18. Digital Offset and Gain control

Although this diagram indicates a multiplier and adder for each channel, there is only one multiplier and one adder in the device, and they are shared among all 4 channels. This has implications for the update speed when several channels are updated at once.

Each time data is written to the M or C register the output is not automatically updated. Rather, the next write to the DAC channel will use these M&C values to perform a new calibration and automatically update the channel.

Data output from the DAC2 register is routed to the final DAC register by a multiplexer. Both the Gain Register and the Offset Register have 16 bits of resolution. The correct method to calibrate the gain/offset is firstly to calibrate out the gain and then calibrate the offset.

The value (in decimal) that is written to the DAC register can be calculated by:

$$Code_{DAC\ Register} = D \times \frac{(M+1)}{2^{16}} + C - 2^{15}$$

where:
D is the code loaded to the DAC channels input register.

M is the code in Gain Register – default code = $2^{16} - 1$

C is the code in Offset Register – default code = 2^{15}

STATUS READBACK DURING WRITE

The AD5757/AD5737 has the ability to read back the Status Register contents during every write sequence. This feature is enabled via the STATREAD bit in the Main Control Register. This allows the user to continuously monitor the Status Register and act quickly in the case of a fault.

When Status Readback During Write is enabled the contents of the 16bit Status register (See Table 36) is outputted on the SDO pin as indicated in Figure 4.

The AD5757/AD5737 will power up with this feature disabled. When this is enabled the normal readback feature is not available, except of the status register. To readback any other register set STATREAD low first before following the readback sequence. STATREAD may be set high again after the register read.

ASYNCHRONOUS CLEAR

CLEAR is an active high edge sensitive input that allows the output to be cleared to a pre programmed 16 bit code. This code is user programmable via a per-channel 16 bit Clear Code Register.

In order for a channel to clear, that channel must be enabled to be cleared via the CLR_EN bit in the channels DAC Control Register. If the channel is not enabled to be cleared then the output will remain in its current state independent of the CLEAR pin level.

When the CLEAR signal is returned low, the relevant outputs remains cleared until a new value is programmed.

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5757/AD5737 offers the option of packet error checking based on an 8-bit (CRC-8) cyclic redundancy check.

The device controlling the AD5757/AD5737 should generate an 8-frame check sequence using the polynomial

$$C(x) = x_8 + x_2 + x_1 + 1$$

This is added to the end of the data-word, and 32 bits are sent to the AD5757/AD5737 before taking SYNC high. If the AD5757/AD5737 sees a 32-bit frame, it performs the error check when SYNC goes high. If the check is valid, the data is written to the selected register. If the error check fails, the FAULT pin goes low and the PEC error bit in the status register is set. After reading the status register, FAULT returns high (assuming there are no other faults), and the PEC error bit is cleared automatically.

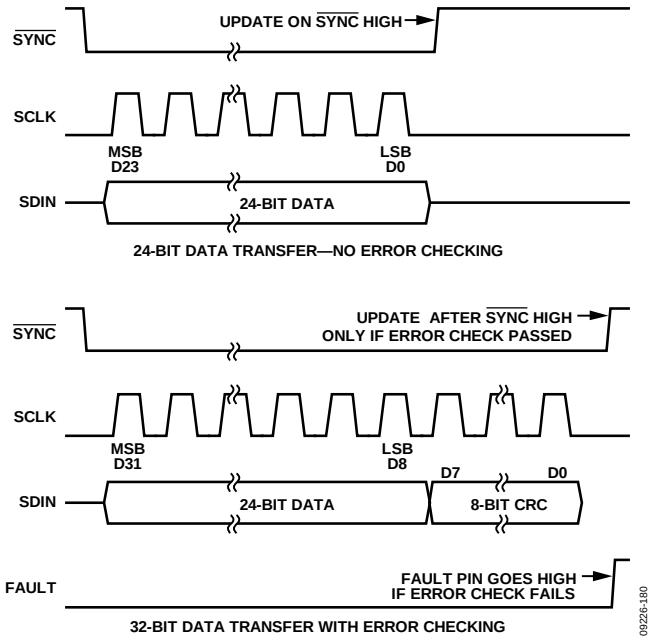


Figure 19. PEC Timing

The PEC can be used for both transmit and receive of data packets. If status readback during a write is enabled, the PEC values returned during the status readback during a write operation should be ignored. If status readback during a write is disabled, the user can still use the normal readback operation to monitor status register activity with PEC.

WATCHDOG TIMER

If enabled, an on chip watchdog timer will generate an alert signal if 0x195 has not been written to the Software Register within the programmed timeout period. This feature is useful to ensure communication has not been lost between the MCU and the AD5757/AD5737 and that these datapath lines are working properly (i.e. SDI/SCLK/SYNC). If 0x195 is not received by the Software Register within the timeout period, the ALERT pin will signal a fault condition. The ALERT signal is active high and can be connected directly to the CLEAR pin to enable a CLEAR in the event that data communications are lost from the MCU.

The watchdog timer is enabled and the timeout period (50,100,150 or 200ms) set in the control register (See Table 24).

OUTPUT ALERT

The AD5757/AD5737 is equipped with a ALERT pin, this is An active high CMOS output. The AD5757/AD5737 has an internal watchdog timer. If enabled, it will monitor SPI communications. If 0x195 is not received by the Software Register within the timeout period, the ALERT pin will go active.

INTERNAL REFERENCE

The AD5757/AD5737 contains an integrated +5V voltage reference with initial accuracy of ±2mV max and a temperature drift coefficient of ±5 ppm max. The reference voltage is buffered and externally available for use elsewhere within the system.

EXTERNAL CURRENT SETTING RESISTOR

Referring toFigure 14, R1 is an internal sense resistor as part of the voltage to current conversion circuitry. The stability of the output current value over temperature is dependent on the stability of the value of R1. As a method of improving the stability of the output current over temperature an external 15kΩ low drift resistor can be connected to the R_{SET} pin of the AD5757/AD5737 to be used instead of the internal resistor R1. The external resistor is selected via the DAC Control register. See Table 26.

HART

The AD5757/AD5737 has four CHART pins, one corresponding to each output channels. A HART signal can be coupled into these pins. The HART signal appears on the corresponding current output, if the output is enabled. Table 37 shows the recommended input voltages for the HART signal at the CHART pin. If these voltages are used, the current output should meet the HART amplitude specifications. Figure 20 shows the recommended circuit for attenuating and coupling in the HART signal.

Table 37. CHART input voltage to HART output current

R_{SET}	CHART Input Voltage	Current Output (HART)
Internal R_{SET}	150 mV p-p	1 mA p-p
External R_{SET}	170 mV p-p	1 mA p-p

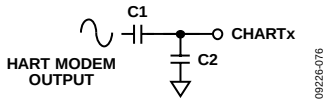


Figure 20. Coupling HART signal

A minimum capacitance of C1 + C2 is required to ensure that the 1.2 kHz and 2.2 kHz HART frequencies are not significantly attenuated at the output. The recommended values are C1 = 22nF, C2 = 47 nF.

Digitally controlling the slew rate of the output is necessary to meet the analog rate of change requirements for HART.

SLEW RATE CONTROL

The Slew Rate Control feature of the AD5757/AD5737 allows the user to control the rate at which the output value changes. This feature is available on both the current and voltage outputs. With the slew rate control feature disabled the output value will change at a rate limited by the output drive circuitry and the attached load. If the user wishes to reduce the slew rate this can be achieved by enabling the slew rate control feature. With the feature enabled via the SREN bit of the Slew Rate Control Register, (See Table 32) the output, instead of slewing directly between two values, will step digitally at a rate defined by two parameters accessible via the Slew Rate Control Register as shown in Table 32. The parameters are SR_CLOCK and SR_STEP. SR_CLOCK defines the rate at which the digital slew will be updated, e.g. if the selected update rate is 8KHz the output will update every 125µs, in conjunction with this the SR_STEP defines by how much the output value will change at each update. Together both parameters define the rate of change of the output value. Table 38 and Table 39 outline the range of values for both the SR_CLOCK and SR_STEP parameters.

Table 38. Slew Rate Update Clock Options

SR_CLOCK	Update Clock Frequency (Hz)*
0000	64K
0001	32K
0010	16K
0011	8k
0100	4k
0101	2k
0110	1k
0111	500
1000	250
1001	125
1010	64
1011	32
1100	16
1101	8
1110	4
1111	0.5Hz

* These clock frequencies are divided down from the 13 MHz internal oscillator.

Table 39. Slew_Rate Step Size Options

SR_STEP	AD5737 **(12 BIT) Step Size (LSBs)**	AD5757 **(16 BIT) Step Size (LSBs)**
000	1/16	1
001	1/8	2
010	1/4	4
011	½	16
100	2	32
101	4	64
110	8	128
111	16	256

The following equation describes the slew rate as a function of the step size, the update clock frequency and the LSB size.

$$Slew\ Time = \frac{Output\ Change}{Step\ Size \times Update\ Clock\ Frequency \times LSB\ Size}$$

Where:

Slew Time is expressed in seconds
Output Change is expressed in Amps
When the slew rate control feature is enabled, all output changes will change at the programmed slew rate, for example if the CLEAR pin is asserted the output will slew to the clear value at the programmed slew rate (assuming that Clear channel is enabled to be cleared). The update clock frequency for any given value will be the same for all output ranges, the step size however will vary across output ranges for a given value of step size as the LSB size will be different for each output range.

POWER DISSIPATION CONTROL

The AD5757/AD5737 contains integrated dynamic power control using a dc-to-dc boost converter circuit, allowing reductions in power consumption from standard designs when using the part in current output mode.

In standard current input module designs, the load resistor values can range from typically 50 Ω to 750 Ω. Output module systems must source enough voltage to meet the compliance voltage requirement across the full range of load resistor values. For example, in a 4 mA to 20 mA loop when driving 20 mA, a compliance voltage of >15 V is required. When driving 20 mA into a 50 Ω load, only 1 V compliance is required.

The AD5757/AD5737 is capable of driving up to 24mA through a 1 kΩ load.

DC-TO-DC CONVERTERS

The AD5757/AD5737 contains four independent dc-to-dc converters. These are used to provide dynamic control of the V_{BOOST} supply voltage for each channel. Figure 21 shows the discreet components needed for the dc-to-dc circuitry, and the following sections describe component selection and operation of this circuitry.

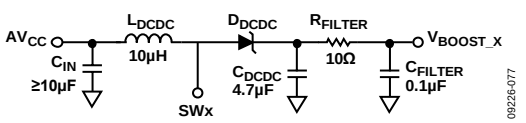


Figure 21. DC-to-DC Circuit

Table 40. Recommended DC-to-DC Components

Symbol	Component	Value	Manufacturer
L_{DCDC}	XAL4040-103	10 µH	Coilcraft
C_{DCDC}	GRM32ER71H475KA88L	4.7 µF	Murata
D_{DCDC}	PMEG3010BEA	0.38V_F	NXP

It is recommended to place a 10 Ω, 100 nF low-pass RC filter after C_{DCDC}. This consumes a small amount of power, but reduces the amount of ripple on the V_{BOOST_x} supply.

DC-to-DC Converter Operation

The on-board dc-to-dc converters use a constant frequency, peak current mode control scheme to step up an AV_{CC} input of 4.5 V to 5.5 V to drive the AD5757/AD5737 output channel. These are designed to operate in discontinuous conduction mode (DCM) with a duty cycle <90% typical. Discontinuous conduction mode refers to a mode of operation where the inductor current goes to zero for an appreciable percentage of the switching cycle. The dc-to-dc converters are nonsynchronous, that is, they require an external Schottky diode.

DC-to-DC Converter Output Voltage

When a channel current output is enabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%) or ($I_{OUT} \times R_{LOAD}$ + Headroom), whichever is greater. In current output mode with the output disabled, the converter regulates the V_{BOOST_x} supply to 7.4 V (±5%).

DC-to-DC Converter Settling Time

The settling time for a step greater than ~1V ($I_{OUT} \times R_{LOAD}$) will be dominated by the settling time of the dc-to-dc converter. The exception to this is when the required voltage at the I_{OUT_X} pin plus the compliance voltage is below 7.4 V (±5%). A typical plot of the output settling time can be found in Figure 7. This plot is for a 1kΩ load. The settling time for smaller loads will be faster, also the settling time for current steps less than 24mA will also be faster.

DC-to-DC Converter V_{MAX} Functionality

The maximum V_{BOOST_x} voltage is set in the dc-to-dc control register (23 V, 24.5 V, 27 V, or 29.5 V; see Table 30)

). On reaching this maximum voltage, the dc-to-dc converter is disabled and the V_{BOOST_x} voltage is allowed to decay by ~0.4 V. After the V_{BOOST_x} voltage has decayed by ~0.4 V, the dc-to-dc converter
is reenabled and the voltage ramps up again to V_{MAX}, if still required. This operation is shown in Figure 22.

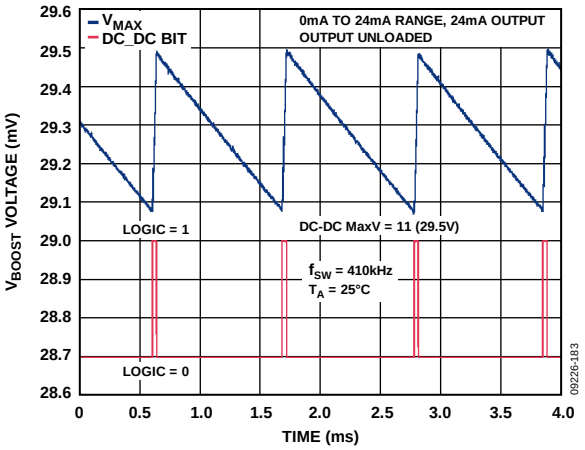


Figure 22. Operation on Reaching V_{MAX}

As can be seen in Figure 22, the DC-DCx bit in the status register asserts when the AD5757/AD5737 is ramping to the V_{MAX} value, but deasserts when the voltage is decaying to V_{MAX} − ~0.4 V.

DC-to-DC Converter On-Board Switch

The AD5757/AD5737 contains a 0.425 Ω internal switch. The switch current is monitored on a pulse by pulse basis and is limited to 0.8 A peak current.

DC-to-DC Converter Switching Frequency and Phase

The AD5757/AD5737 dc-to-dc converter switching frequency can be selected from the dc-to-dc control register. The phasing of the channels can also be adjusted so that the dc-to-dc converter can clock on different edges (seeTable 30). For typical applications, a 410 kHz frequency is recommended. At light loads (low output current and small load resistor), the dc-to-dc converter enters a pulse-skipping mode to minimize switching power dissipation.

DC-to-DC Converter Inductor Selection

For typical 4 mA to 20 mA applications, a 10 µH inductor (such as the XAL4040-103 from Coilcraft) combined with a switching frequency of 410 kHz allows up to 24 mA to be driven into a load resistance of up to 1 kΩ with an AV_{CC} supply of 4.5 V to 5.5 V. It is important to ensure that the inductor is able to handle the peak current without saturating at the maximum ambient temperature. If the inductor were to enter into saturation mode, it would result in a decrease in efficiency. The inductance value would also drop during saturation and may result in the dc-to-dc converter circuit not being able to supply the required output power.

DC-to-DC Converter External Schottky Selection

The AD5757/AD5737 requires an external Schottky for correct operation. Ensure that the Schottky is rated to handle the maximum reverse breakdown expected in operation and that the rectifier maximum junction temperature is not exceeded. The diode average current is approximately equal to the I_{LOAD}

current. Diodes with larger forward voltage drops result in a decrease in efficiency.

DC-to-DC Converter Compensation Capacitors

As the dc-to-dc converter operates in DCM, the uncompensated transfer function is essentially a single-pole transfer function. The pole frequency of the transfer function is determined by the dc-to-dc converter's output capacitance, input and output voltage, and output load. The AD5757/AD5737 uses an external capacitor in conjunction with an internal 150 kΩ resistor to compensate the regulator loop. Alternatively, an external compensation resistor can be used in series with the compensation capacitor, by setting the DC-DC Comp bit in the dc-to-dc control register. In this case, a ~50 kΩ resistor is recommended. A description of the advantages of this can be found in the AICC Supply Requirements—Slewing section. For typical applications, a 10 nF dc-to-dc compensation capacitor is recommended.

DC-to-DC Converter Input and Output Capacitor Selection

The output capacitor affects ripple voltage of the dc-to-dc converter and indirectly limits the maximum slew rate at which the channel output current can rise. The ripple voltage is caused by a combination of the capacitance and equivalent series resistance (ESR) of the capacitor. For the AD5757/AD5737 a ceramic capacitor of 4.7 µF is recommended for typical applications. Larger capacitors or paralleled capacitors improve the ripple at the expense of reduced slew rate. Larger capacitors also impact the AV_{CC} supplies current requirements while slewing (see the AICC Supply Requirements—Slewing section). This capacitance at the output of the dc-to-dc converter should be >3 µF under all operating conditions.

The input capacitor provides much of the dynamic current required for the dc-to-dc converter and should be a low ESR component. For the AD5757/AD5737, a low ESR tantalum or ceramic capacitor of 10 µF is recommended for typical applications. Ceramic capacitors must be chosen carefully because they can exhibit a large sensitivity to dc bias voltages and temperature. X5R or X7R dielectrics are preferred because these capacitors remain stable over wider operating voltage and temperature ranges. Care must be taken if selecting a tantalum capacitor to ensure a low ESR value.

AI_{CC} SUPPLY REQUIREMENTS—STATIC

The dc-dc converter is designed to supply a V_{BOOST} voltage of

$$V_{BOOST} = I_{OUT} \times R_{LOAD} + Headroom \quad (2)$$

This means that, for a fixed load and output voltage, the dc-to-dc converter's output current can be calculated by the following formula:

$$AI_{CC} = \frac{Power\ Out}{Efficiency \times AV_{CC}} = \frac{I_{OUT} \times V_{BOOST}}{\eta_{V_{BOOST}} \times AV_{CC}} \quad (3)$$

where:

I_{OUT} is the output current from I_{OUT_X} in amps.

$\eta_{V_{BOOST}}$ is the efficiency at V_{BOOST} as a fraction (see Figure 8 and **Error! Reference source not found.**).

AI_{CC} SUPPLY REQUIREMENTS—SLEWING

The AI_{CC} current requirement while slewing is greater than in static operation because the output power increases to charge the output capacitance of the dc-to-dc converter. This transient current can be quite large (see Figure 23), although the methods outlined in the Reducing AICC Current Requirements section can reduce the requirements on the AV_{CC} supply. If not enough AI_{CC} current can be provided, the AV_{CC} voltage droops. Due to this AV_{CC} droop, the AI_{CC} current required to slew increases further. This means that the voltage at AV_{CC} drops further (see Equation 3) and the V_{BOOST} voltage, and thus the output voltage, may never reach its intended value. Because this AV_{CC} voltage is common to all channels, this may also affect other channels.

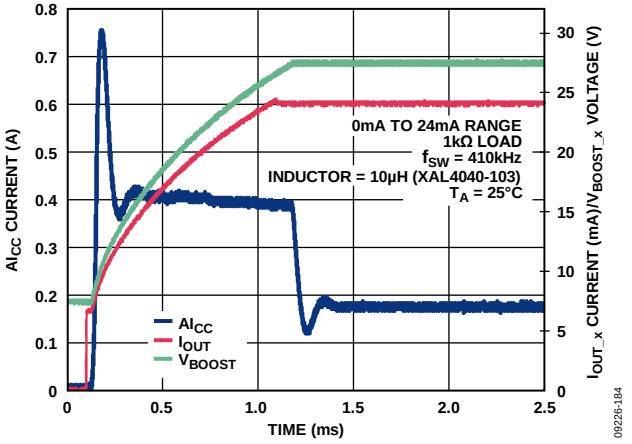


Figure 23. AI_{CC} Current vs. Time for 24 mA Slew with Internal Compensation Resistor

Reducing AI_{CC} Current Requirements

There are two main methods that can be used to reduce the AI_{CC} current requirements. One method is to add an external compensation resistor, and the other is to use slew rate control. Both of these methods can be used in conjunction.

A compensation resistor can be placed at the $COMP_{DCDC\_X}$ pin in series with the 10 nF compensation capacitor. A 51 kΩ external compensation resistor is recommended. This compensation increases the slew time of the current output, but eases the AI_{CC} transient current requirements. Figure 24 shows a plot of AI_{CC} current for a 24 mA step through a 1 kΩ load when using a 51 kΩ compensation resistor. This method eases the current requirements through smaller loads even further, as shown in Figure 25.

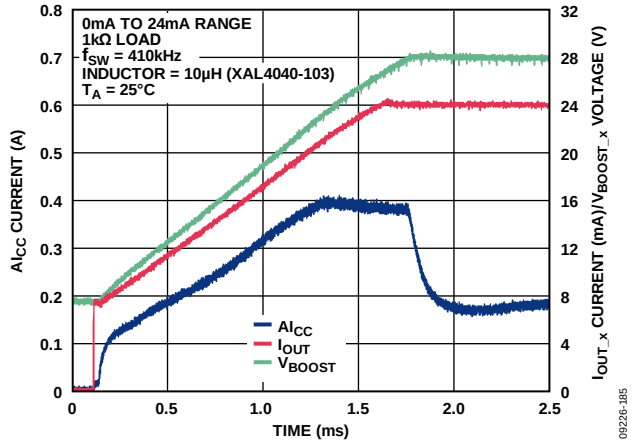


Figure 24. AI_{CC} Current vs. Time for 24 mA Through 1 kΩ Slew with External 51 kΩ Compensation Resistor

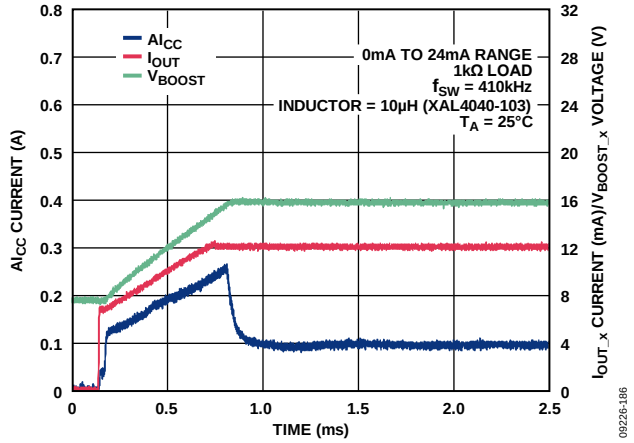


Figure 25. AI_{CC} Current vs. Time for 24 mA Through 500 Ω Slew with External 51 kΩ Compensation Resistor

Using slew rate control can greatly reduce the AV_{CC} supplies current requirements, as shown in Figure 26. When using slew rate control, attention should be paid to the fact that the output cannot slew faster than the dc-to-dc converter. The dc-to-dc converter slews slowest at higher currents through large (for example, 1 kΩ) loads. This slew rate is also dependent on the dc-to-dc converter's configuration. Two examples of the dc-to-dc converter's output slew are shown in Figure 23 and Figure 24 (V_{BOOST} corresponds to the dc-to-dc converter's output voltage).

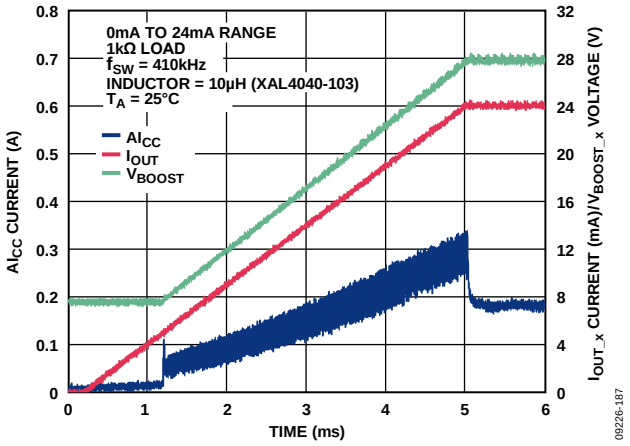


Figure 26. AI_{CC} Current vs. Time for 24 mA Slew with Slew Rate Control

APPLICATIONS INFORMATION

PRECISION VOLTAGE REFERENCE SELECTION

To achieve the optimum performance from the AD5757/AD5737 over its full operating temperature range, a precision voltage reference must be used. Thought should be given to the selection of a precision voltage reference. The voltage applied to the reference inputs is used to provide a buffered reference for the DAC cores. Therefore, any error in the voltage reference is reflected in the outputs of the device.

There are four possible sources of error to consider when choosing a voltage reference for high accuracy applications: initial accuracy, temperature coefficient of the output voltage, long term drift, and output voltage noise.

Initial accuracy error on the output voltage of an external reference can lead to a full-scale error in the DAC. Therefore, to minimize these errors, a reference with low initial accuracy error specification is preferred. Choosing a reference with an output trim adjustment, such as the ADR425, allows a system designer to trim system errors out by setting the reference voltage to a voltage other than the nominal. The trim adjustment can be used at temperature to trim out any error.

Long-term drift is a measure of how much the reference output voltage drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable over its entire lifetime.

The temperature coefficient of a reference's output voltage affects INL, DNL, and TUE. A reference with a tight temperature coefficient specification should be chosen to reduce the dependence of the AD5757/AD5737's output to ambient temperature.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise must be considered. Choosing a reference with as low an output noise voltage as practical for the system resolution required is important. Precision voltage references such as the ADR435 (XFET® design) produce low output noise in the 0.1 Hz to 10 Hz region. However, as the circuit bandwidth increases, filtering the output of the reference may be required to minimize the output noise.

Table 41. Some Recommended Precision References

Part No.	Initial Accuracy (mV Maximum)	Long-Term Drift (ppm Typical)	Temperature Drift (ppm/°C Maximum)	0.1 Hz to 10 Hz Noise (µV p-p Typical)
ADR445	±2	50	3	2.25
ADR02	±3	50	3	10
ADR435	±2	40	3	8
ADR395	±5	50	9	8
AD586	±2.5	15	10	4

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads, a capacitor may be required between I_{OUT_X} and AGND to ensure stability. A 0.01 µF capacitor between I_{OUT_X} and AGND ensures stability of a load of 50 mH. The capacitive component of the load may cause slower settling, although this may be masked by the settling time of the AD5757/AD5737. There is no maximum capacitance limit for the current output of the AD5757/AD5737.

TRANSIENT VOLTAGE PROTECTION

The AD5757/AD5737 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5757/AD5737 from excessively high voltage transients, external power diodes and a surge current limiting resistor are required, as shown in Figure 27. The two protection diodes and resistor must have appropriate power ratings. Further protection can be provided with transient voltage suppressors or transorbs; these are available as both unidirectional suppressors (protect against positive high voltage transients) and bidirectional suppressors (protect against both positive and negative high voltage transients) and are available in a wide range of standoff and breakdown voltage ratings. It is recommended that all field connected nodes be protected.

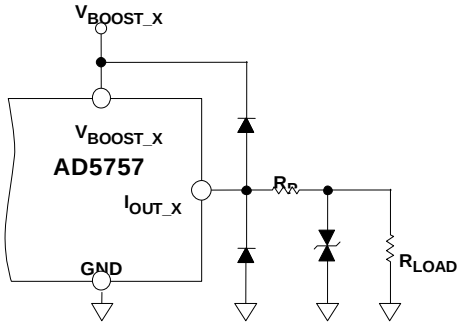


Figure 27. Output Transient Voltage Protection

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5757/AD5737 is via a serial bus that uses a protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire minimum interface consisting of a clock signal, a data signal, and a latch signal. The AD5757/AD5737 require a 24-bit dataword with data valid on the falling edge of SCLK.

The DAC output update is initiated on either the rising edge of $\overline{\text{LDAC}}$ or, if $\overline{\text{LDAC}}$ is held low, on the rising edge of $\overline{\text{SYNC}}$. The contents of the registers can be read using the readback function.

AD5757/AD5737 TO ADSP-BF527 INTERFACE

The AD5757/AD5737 can be connected directly to the SPORT interface of the ADSP-BF527, an Analog Devices, Inc., Blackfin® DSP. Figure 28 shows how the SPORT interface can be connected to control the AD5757/AD5737.

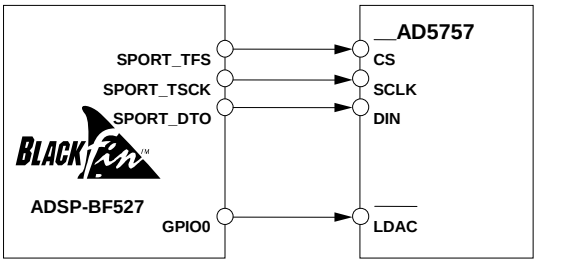


Figure 28. AD5757/AD5737 to ADSP-BF527 SPORT Interface

LAYOUT GUIDELINES

Layout—Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5757/AD5737 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5757/AD5737 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The $GNDSW_x$ and the ground connection for the AV_{CC} supply are referred to as PGND. PGND should be confined to certain areas of the board, and the PGND-to-AGND connection should be made at one point only.

Layout – Supply De-Coupling

The AD5757/AD5737 should have ample supply bypassing of 10 µF
in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

Layout—Traces

The power supply lines of the AD5757/AD5737 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through on the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

Layout—DC to DC Converters

To achieve high efficiency, good regulation, and stability, a well-designed printed circuit board layout is required.

Follow these guidelines when designing printed circuit boards:

- Keep the low ESR input capacitor, C_{IN}, close to AV_{CC} and PGND.
- Keep the high current path from C_{IN} through the inductor, L_{DCDC}, to SW_X and PGND as short as possible.
- Keep the high current path from C_{IN} through L_{DCDC}, the rectifier, D_{DCDC}, and the output capacitor, C_{DCDC}, as short as possible.
- Keep high current traces as short and as wide as possible. The path from C_{IN} through the inductor, L_{DCDC}, to SW_X and PGND should be able to handle a minimum of 1 A.
- Place the compensation components as close as possible to $COMP_{DCDC\_x}$.
- Avoid routing high impedance traces near any node connected to SW or near the inductor to prevent radiated noise injection.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. Isocouplers provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5757/AD5737 makes it ideal for isolated interfaces, because the number of interface lines is kept to a minimum. Figure 29 shows a 4-channel isolated interface to the AD5757/AD5737 using an ADuM1400. For more information, go to www.analog.com.

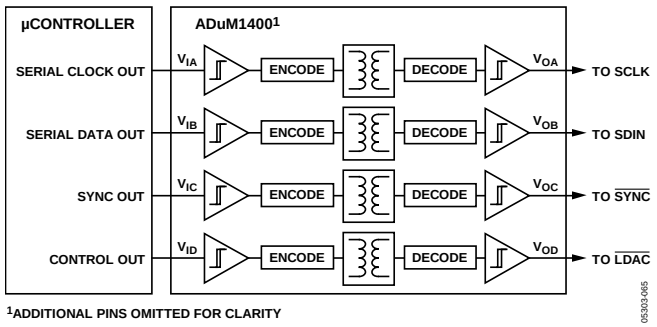
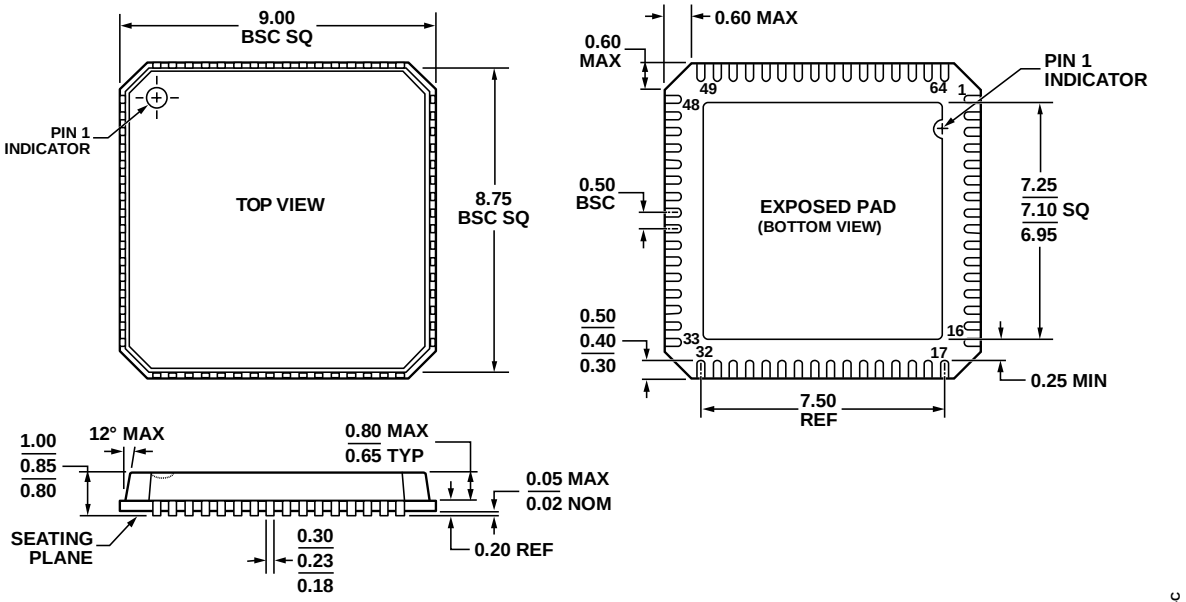


Figure 29. Isolated Interface

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 30. 64-Lead Frame Chip Scale Package, 9x9 Quad. [LFCSP]

Dimensions shown in millimeters

ORDERING GUIDE

Model	Resolution	Temperature Range	Package Description	Package Option
AD5757ACPZ	16-bit	–40°C to +105°C	64-lead LFCSP	CP-64-3
AD5737ACPZ	12-bit	–40°C to +105°C	64-lead LFCSP	CP-64-3