



EN5322QI

2 A Voltage Mode Synchronous Buck PWM DC-DC Converter Evaluation Board

DESCRIPTION

The EN5322 evaluation board is configured to provide a 1.2 V output at up to 2 A from a 2.4 V to 5.5 V input. The output can be set to 7 different voltages through the three VID output voltage select pins.

If using the external divider option, V_{OUT} can be adjusted from 0.6 V up to $V_{IN} - V_{DROPOUT}$, where $V_{DROPOUT} = I_{LOAD} * R_{DROPOUT}$.

The 4 MHz operation allows for the use of tiny MLCC capacitors. It also enables a very wide control loop bandwidth providing excellent transient performance and reduced output impedance. The internal compensation is designed for unconditional stability for all operating conditions. The Power OK signal is available.

FEATURES

- Input Voltage Range: 2.4 V – 5.5 V
- 7 Output Voltage Options via VID Pins
- Adjustable Output Voltage via External Resistor Divider
- 2 A Load Current Guaranteed
- Fully Assembled and Tested

Applications

- Point of Load Regulation for Low Power Processors, Network Processors, DSPs' FPGAs and ASICs
- Replacement of LDOs
- Noise Sensitive Applications such as A/V and RF
- Computing, Computer Peripherals, Storage, Networking, and Instrumentation
- DSL, STB, DVR, DTV, and iPC

EVALUATION BOARD BILL OF MATERIALS

Ref Des	Qty	Description	Manufacturer P/N
C2	1	Ceramic Capacitor, 10 uF, 10 V, X7R, 0805	Murata: GRM21BR71A106KE51L
C3	1	Ceramic Capacitor, 47 uF, 6.3 V, X5R, 1206	Murata: GRM31CR60J476ME19L
C11	1	Ceramic Capacitor, 1 uF, 6.3 V, X7R, 0603	Panasonic: ECJ1VB0J105K
U1	1	2 A PWM Converter	Enpirion: EN5322QI-T
R4 ¹	1	Resistor, 100 kOHM, 5%, 1/8 W, 0805	Digikey: 311-100KACT-ND
C8 ²	1	Electrolytic Capacitor, 150 uF, 10 V	Panasonic: EEVFK1A151P
C10 ²	1	Ceramic Capacitor, 10 uF, 10 V, X7R, 0805	Murata: GRM21BR71A106KE51L
D1 ²	1	TVS Unidirect, 600 W, 6.5 V	Littlefuse: SMBJ6.5A
FB1 ²	1	Multilayer Ferrite Bead, 4000MA, 0805	Würth: 742792012
J1 ²	1	Connector, Custom, Vertical Header	Samtec: ASP12192002
TP5-TP9 ²	5	Connector, Test Point	Keystone: 5016
C1, C4, C5, C6, C9, C12		Not Used	
R1, R2		Not Used	
TP1-TP2		Not Used	

Note 1: R4 is not required if POK is not used.

Note 2: These components are only for demonstration purposes, and are not needed for circuit design.

EVALUATION BOARD CIRCUIT

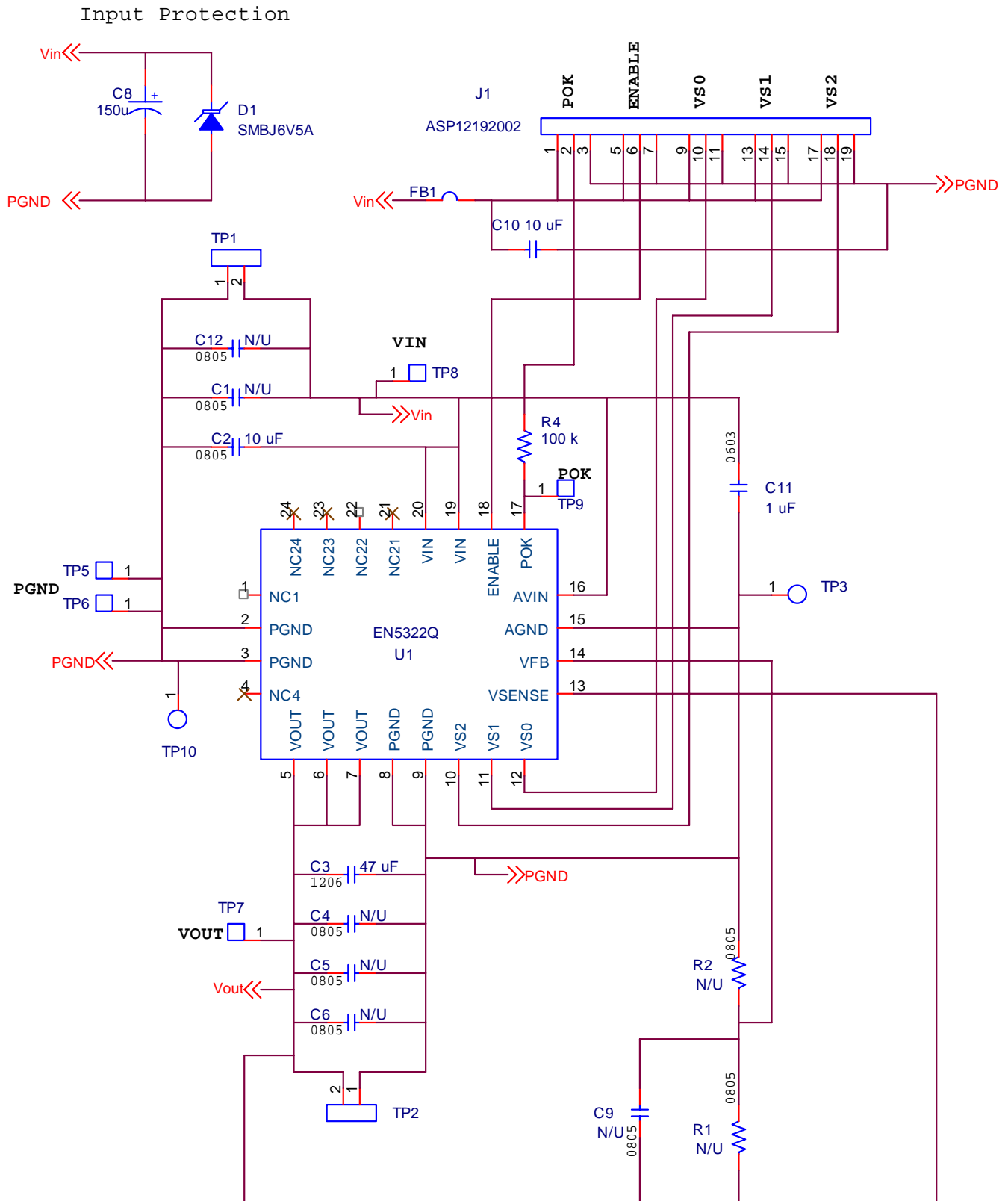


Figure 1. Customer Evaluation Board Schematic

PRINTED CIRCUIT BOARD LAYOUT

Figure 2: Component Placement

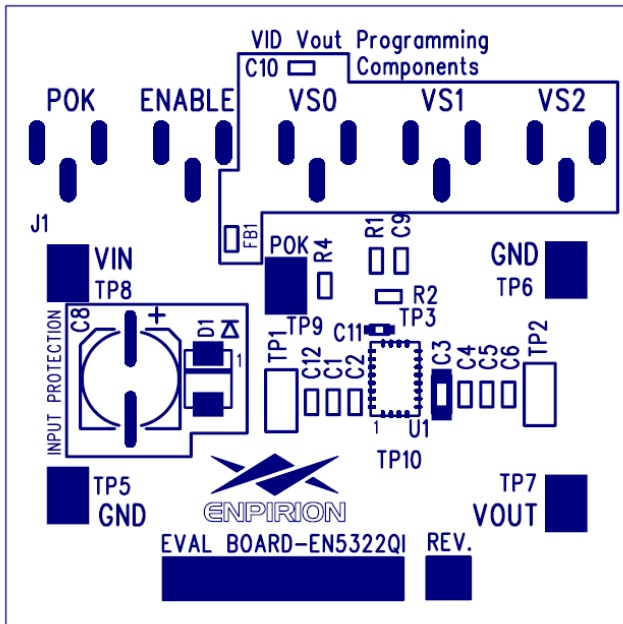


Figure 3: Top Layer Layout

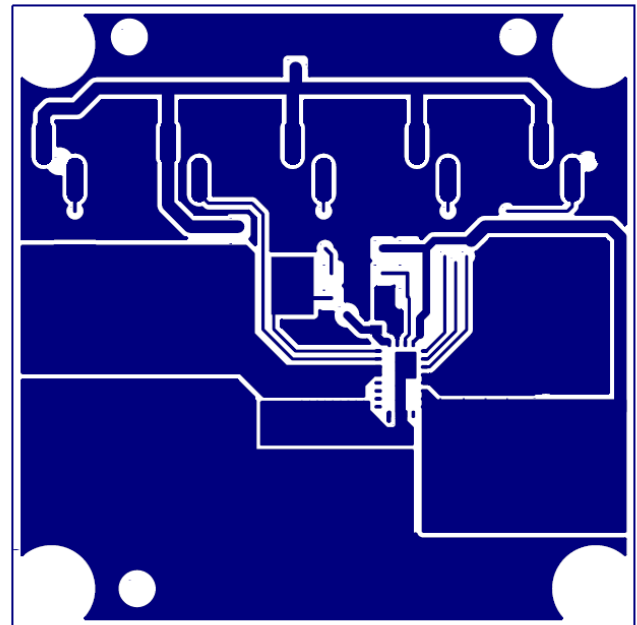


Figure 4: Bottom Layer Layout

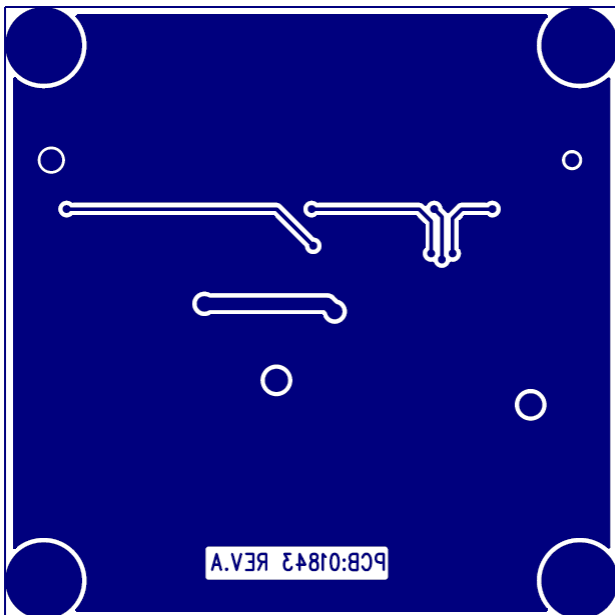
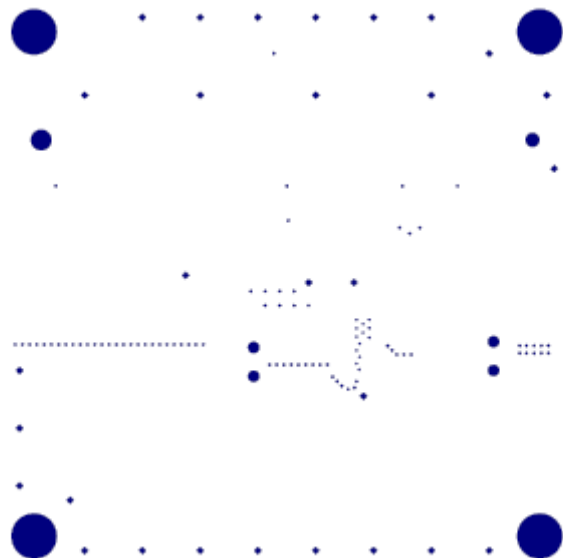


Figure 5: Drills



QUICK START GUIDE

1. Preset power supply to $2.4\text{ V} \leq V_{IN} \leq 5.5\text{ V}$.
2. Turn power supply off.
3. Place jumper ENABLE at the left position to pull the pin high and enable the EN5322. Placing jumper ENABLE at the right position will pull the pin low and disable the EN5322.
4. Place jumper POK at the left position to connect pull up resistor R4 to VIN. Leave the jumper open if the POK function is not used.
5. Place jumpers VS0, VS1, and VS2 according to Table 1 (R: right position; L: left position) to set the desired output voltage.

Table 1: VID Code Setting

VS2	VS1	VS0	Output Voltage
R	R	R	3.3V
R	R	L	2.5V
R	L	R	1.8V
R	L	L	1.5V
L	R	R	1.25V
L	R	L	1.2V
L	L	R	0.8V
L	L	L	External Divider

The output voltage can also be set with an external resistor divider when VS2, VS1 and VS0 are pulled high (left position). Use a $340\text{ k}\Omega$, 1 % or better resistor for R1. Then the value of the bottom resistor R2 is given as:

$$R2 = \frac{204}{V_{OUT} - 0.6} \text{ k}\Omega$$

where V_{OUT} is the output voltage. For example, if the desired output voltage is 1 V, R2 should be a $511\text{ k}\Omega$, 1% or better resistor.

6. Connect input power supply terminals to +VIN (TP8) and GND (TP5).
7. Connect load terminals to +VOUT (TP7) and GND (TP6).
8. Turn on the power supply after making connections.
9. The EN5322 will be enabled. The POK output can be observed at TP9. To observe noise-sensitive waveforms on input / output ripple and NC(SW), use the measurement technique as shown in Figure 6. Wrap bus wire around the GND portion of the bare probe and bring it close to the probe tip. Then solder the bus wire to the nearest GND on the board.

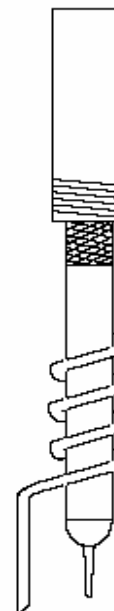


Figure 6: Balanced Impedance Scope Probe for Noise Measurements

Contact Information

Enpirion, Inc.
685 Route 202/206
Suite 305
Bridgewater, NJ 08807
Phone: 908-575-7550
Fax: 908-575-0775

Enpirion reserves the right to make changes in circuit design and/or specifications at any time without notice. Information furnished by Enpirion is believed to be accurate and reliable. Enpirion assumes no responsibility for its use or for infringement of patents or other third party rights, which may result from its use. Enpirion products are not authorized for use in nuclear control systems, as critical components in life support systems or equipment used in hazardous environment without the express written authority from Enpirion..