

# DATA SHEET

## **74LVC574A**

Octal D-type flip-flop with 5 V  
tolerant inputs/outputs; positive  
edge-trigger; 3-state

Product specification  
Supersedes data of 2003 Jun 20

2004 Mar 22

## Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

### 74LVC574A

#### FEATURES

- 5 V tolerant inputs and outputs, for interfacing with 5 V logic
- Supply voltage range from 1.2 to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when  $V_{CC} = 0$  V
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Flow-through pin-out architecture
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

#### DESCRIPTION

The 74LVC574A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC574A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A clock (CP) and an Output Enable ( $\overline{OE}$ ) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When  $\overline{OE}$  is LOW, the contents of the eight flip-flops is available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance off-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The 74LVC574A is functionally identical to the 74LVC374A, but has a different pin arrangement.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay CP to Qn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.2	ns
$f_{max}$	maximum clock frequency		150	MHz
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	15	pF

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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## FUNCTION TABLE

See note 1.

OPERATING MODE	INPUT			INTERNAL FLIP-FLOP	OUTPUT
	$\overline{OE}$	CP	Dn		Qn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

### Note

- H = HIGH voltage level;  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
L = LOW voltage level;  
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;  
↑ = LOW-to-HIGH clock transition;  
Z = high-impedance OFF-state.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC574AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC574ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC574APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC574ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

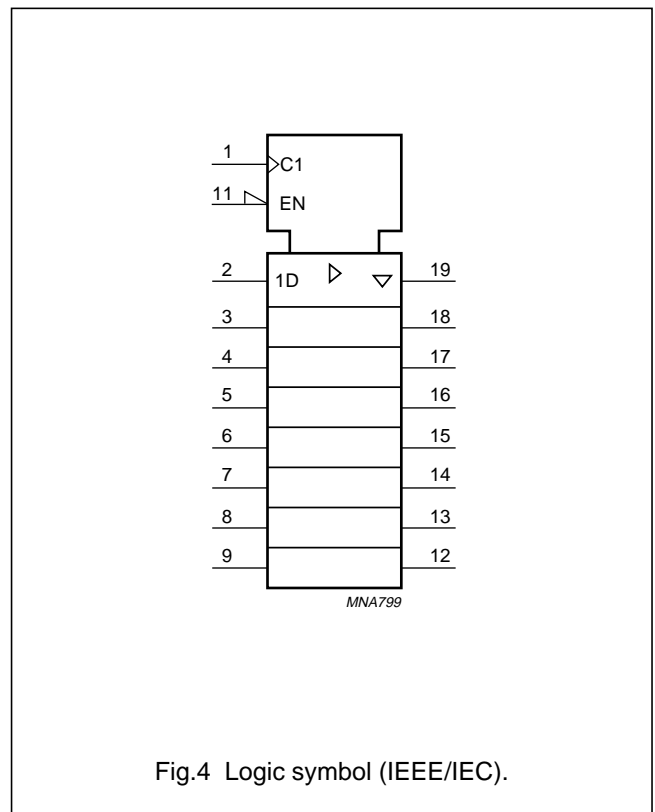
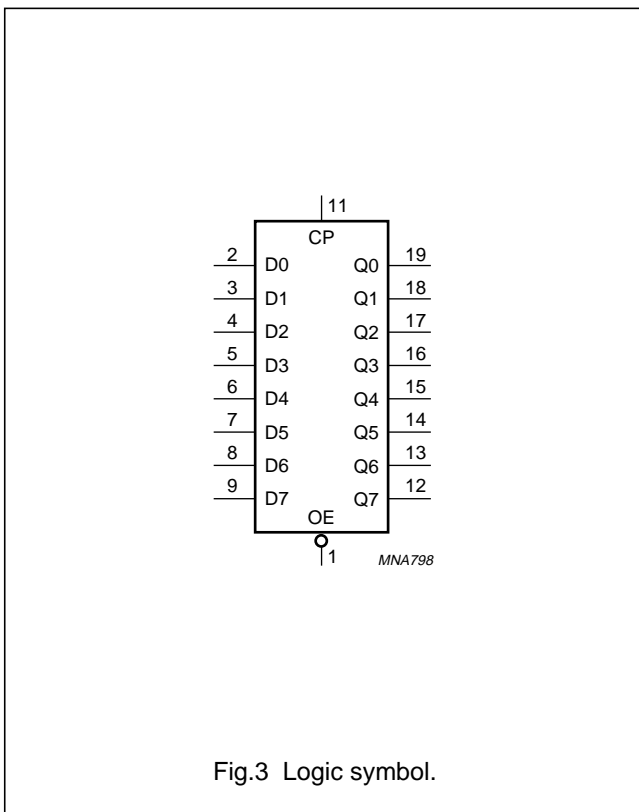
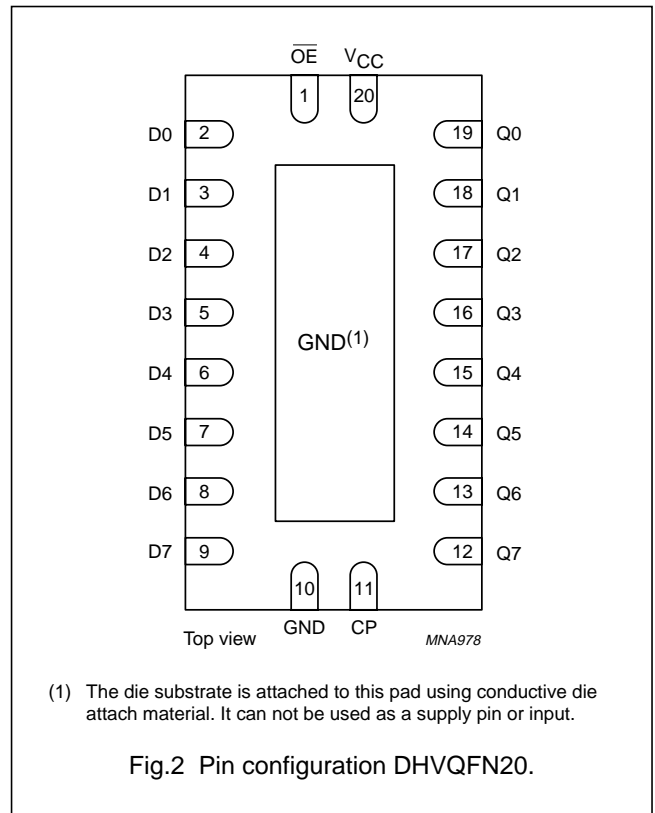
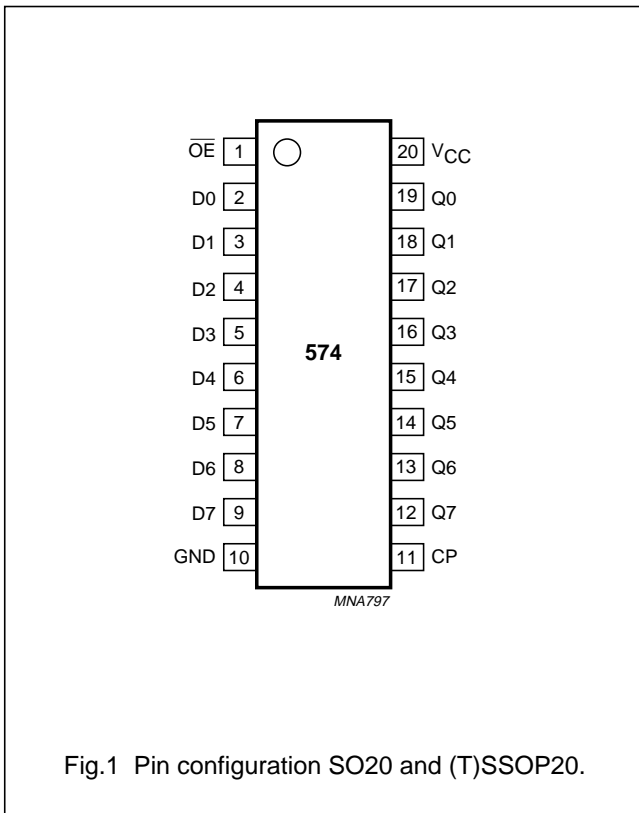
## PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{OE}$	output enable input (active LOW)
2	D0	data input
3	D1	data input
4	D2	data input
5	D3	data input
6	D4	data input
7	D5	data input
8	D6	data input
9	D7	data input
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	CP	clock input (LOW-to-HIGH; edge triggered)
12	Q7	data output
13	Q6	data output
14	Q5	data output
15	Q4	data output
16	Q3	data output
17	Q2	data output
18	Q1	data output
19	Q0	data output
20	V <sub>CC</sub>	supply voltage

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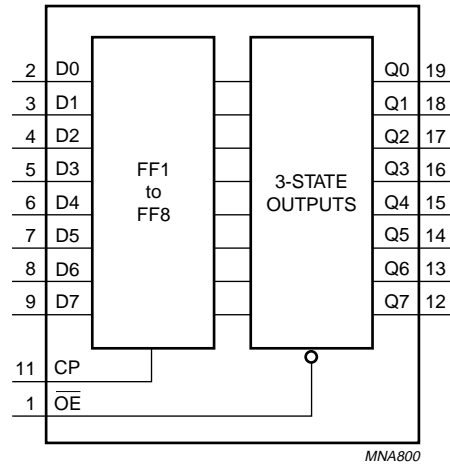


Fig.5 Functional diagram.

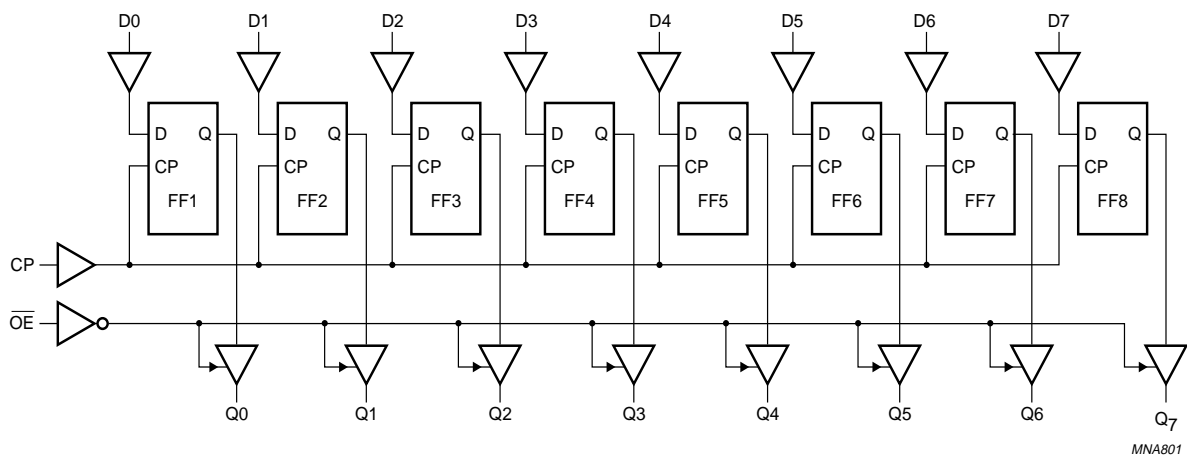


Fig.6 Logic diagram.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.  
For (T)SSOP20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C the value of P<sub>tot</sub> derates linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -100 µA	3.0	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 12 mA	2.7	-	-	0.40	V
		I <sub>O</sub> = 100 µA	3.0	-	GND	0.20	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; note 2	3.6	-	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	0.1	±10	µA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 12 mA	2.7	-	-	0.6	V
		I <sub>O</sub> = 100 μA	2.7 to 3.6	-	-	0.3	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	μA

**Notes**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. The specified overdrive current at the data input forces the data input to the opposite logic input state.



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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500 \Omega$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP to Qn	see Figs 7 and 10	2.7	1.5	3.6	8.0	ns
			3.0 to 3.6	1.5	3.2 <sup>(2)</sup>	7.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Figs 9 and 10	2.7	1.5	4.3	8.5	ns
			3.0 to 3.6	1.5	3.5 <sup>(2)</sup>	7.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Figs 9 and 10	2.7	1.5	2.8	6.5	ns
			3.0 to 3.6	1.5	2.5 <sup>(2)</sup>	6.0	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see Fig.7	2.7	3.3	–	–	ns
			3.0 to 3.6	3.4	1.7 <sup>(2)</sup>	–	ns
t <sub>su</sub>	set-up time Dn to CP	see Fig.8	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0.3 <sup>(2)</sup>	–	ns
t <sub>h</sub>	hold time Dn to CP	see Fig.8	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	-0.2 <sup>(2)</sup>	–	ns
f <sub>max</sub>	maximum clock frequency		2.7	80	–	–	MHz
			3.0 to 3.6	100	150 <sup>(2)</sup>	–	MHz
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay CP to Qn	see Figs 7 and 10	2.7	–	–	10.0	ns
			3.0 to 3.6	–	–	9.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to Qn	see Figs 9 and 10	2.7	–	–	11.0	ns
			3.0 to 3.6	–	–	9.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to Qn	see Figs 9 and 10	2.7	–	–	8.5	ns
			3.0 to 3.6	–	–	7.5	ns
t <sub>W</sub>	clock pulse width HIGH or LOW	see Fig.7	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
t <sub>su</sub>	set-up time Dn to CP	see Fig.8	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
t <sub>h</sub>	hold time Dn to CP	see Fig.8	2.7	–	–	–	ns
			3.0 to 3.6	–	–	–	ns
f <sub>max</sub>	maximum clock frequency		2.7	–	–	–	MHz
			3.0 to 3.6	–	–	–	MHz
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	–	ns

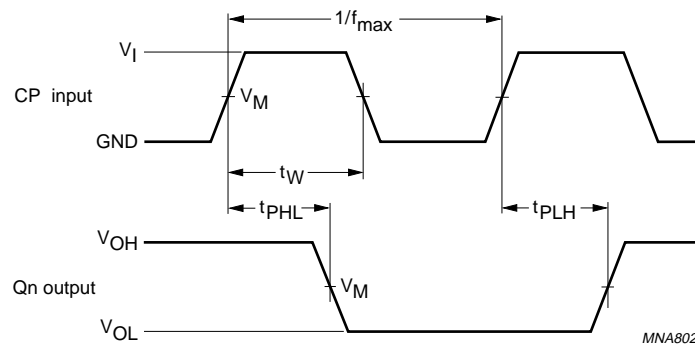
### Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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AC WAVEFORMS

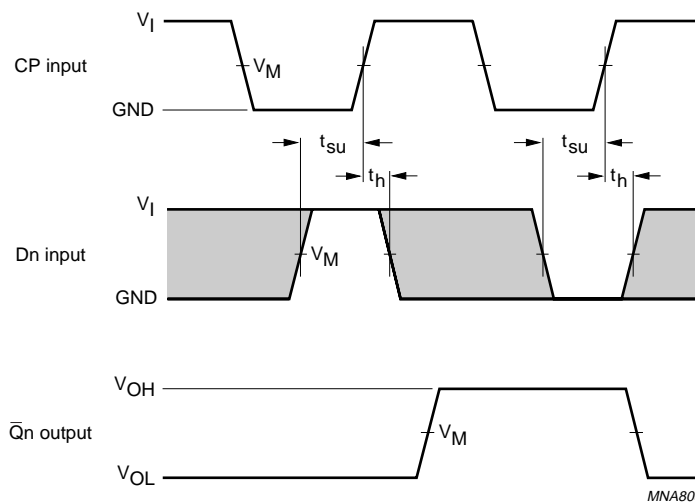


V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V.

V<sub>M</sub> = 0.5 V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

Fig.7 Clock (CP) to output (Qn) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



V<sub>M</sub> = 1.5 V at V<sub>CC</sub> ≥ 2.7 V.

V<sub>M</sub> = 0.5 V<sub>CC</sub> at V<sub>CC</sub> < 2.7 V.

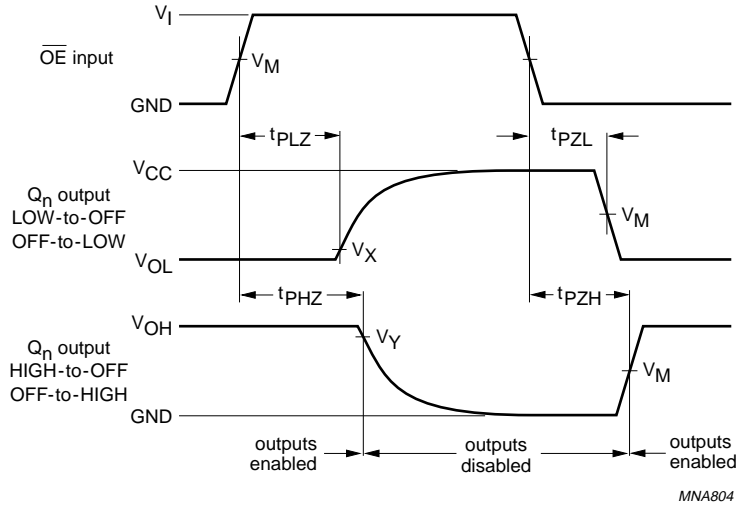
V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.8 Data setup and hold times for the Dn input to the CP input.

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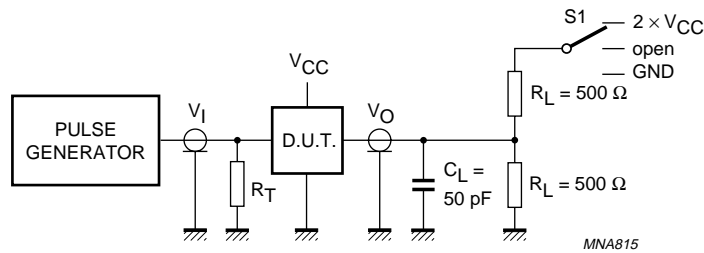
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MNA804

- $V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .
- $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .
- $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.
- $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;
- $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .
- $V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;
- $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .

Fig.9 3-state enable and disable times.



MNA815

TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_I$
$< 2.7\text{ V}$	$V_{CC}$
$2.7\text{ to }3.6\text{ V}$	$2.7\text{ V}$

- Definitions for test circuit:
- $R_L$  = load resistor.
  - $C_L$  = load capacitance includes jig and probe capacitance.
  - $R_T$  = termination resistance should be equal to  $Z_o$  of pulse generators.

Fig.10 Load circuitry for switching times.

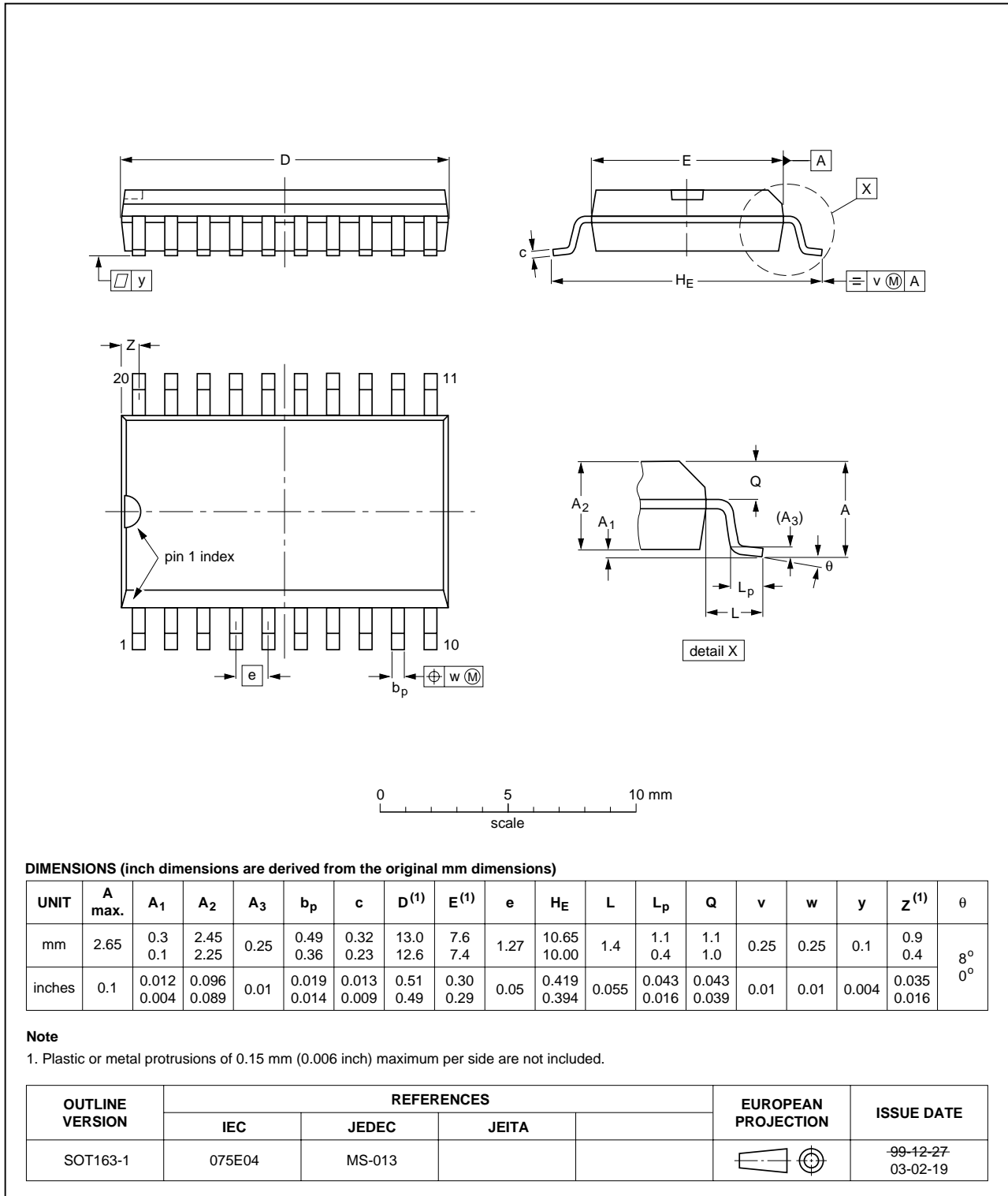
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

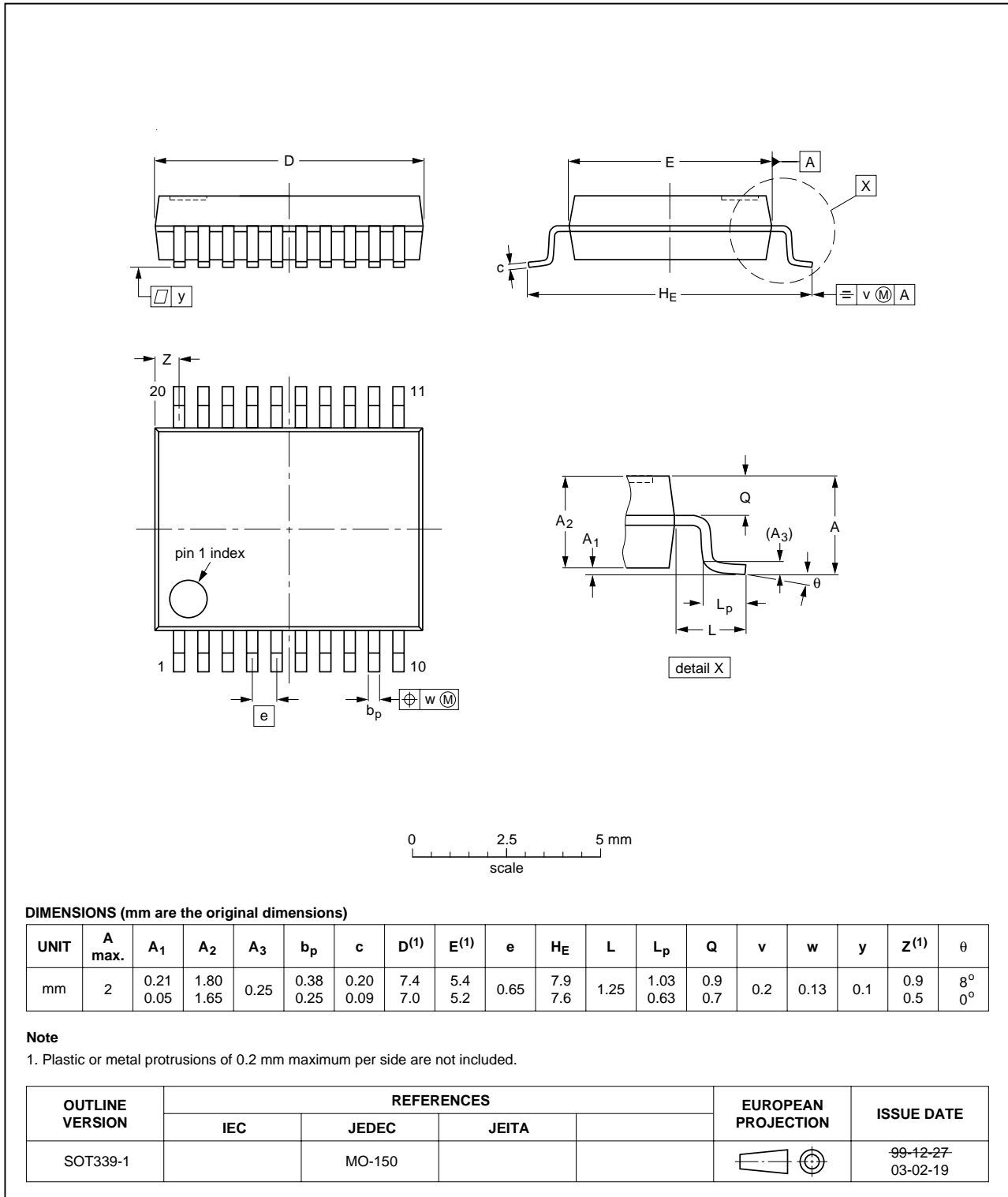


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

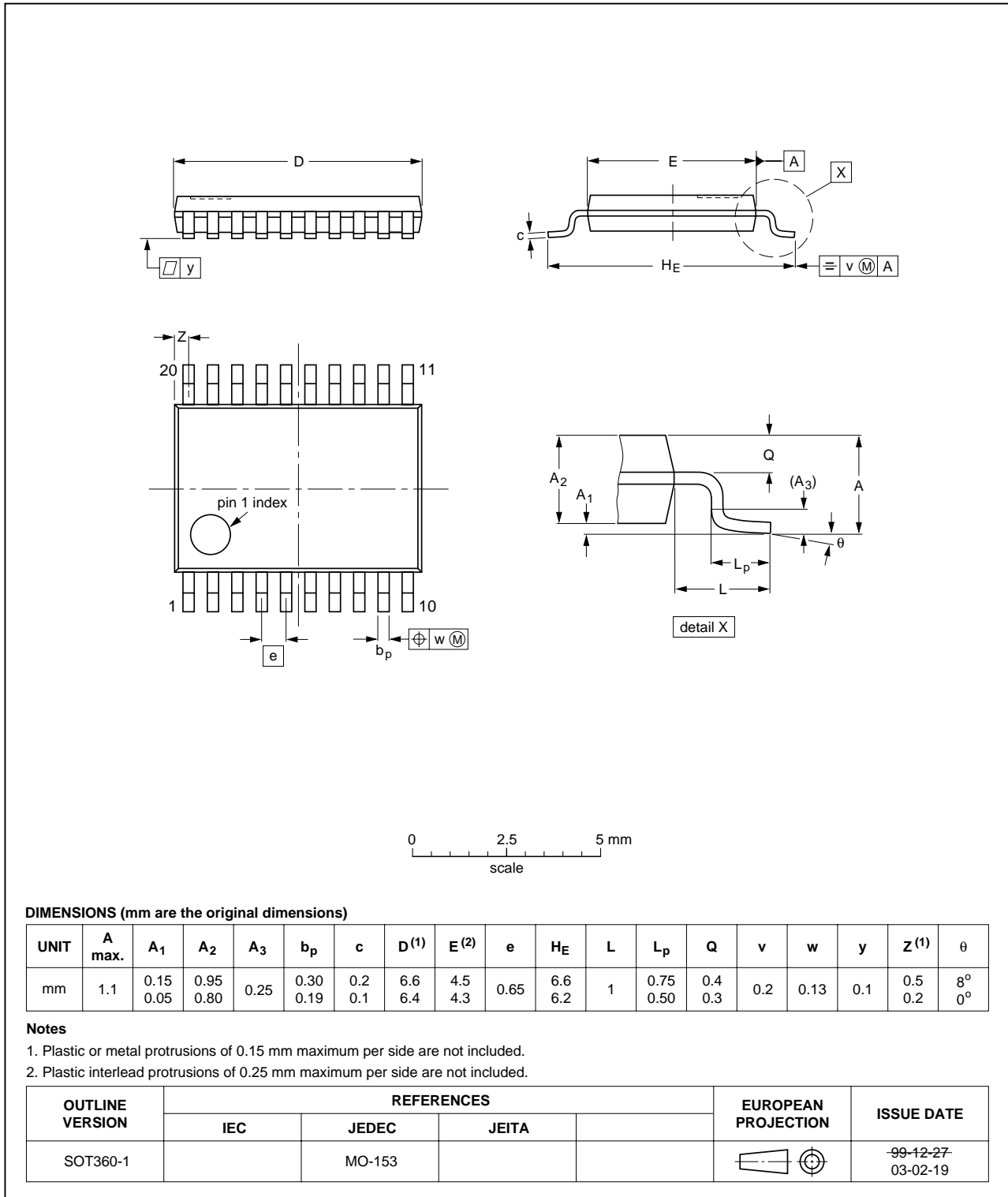


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

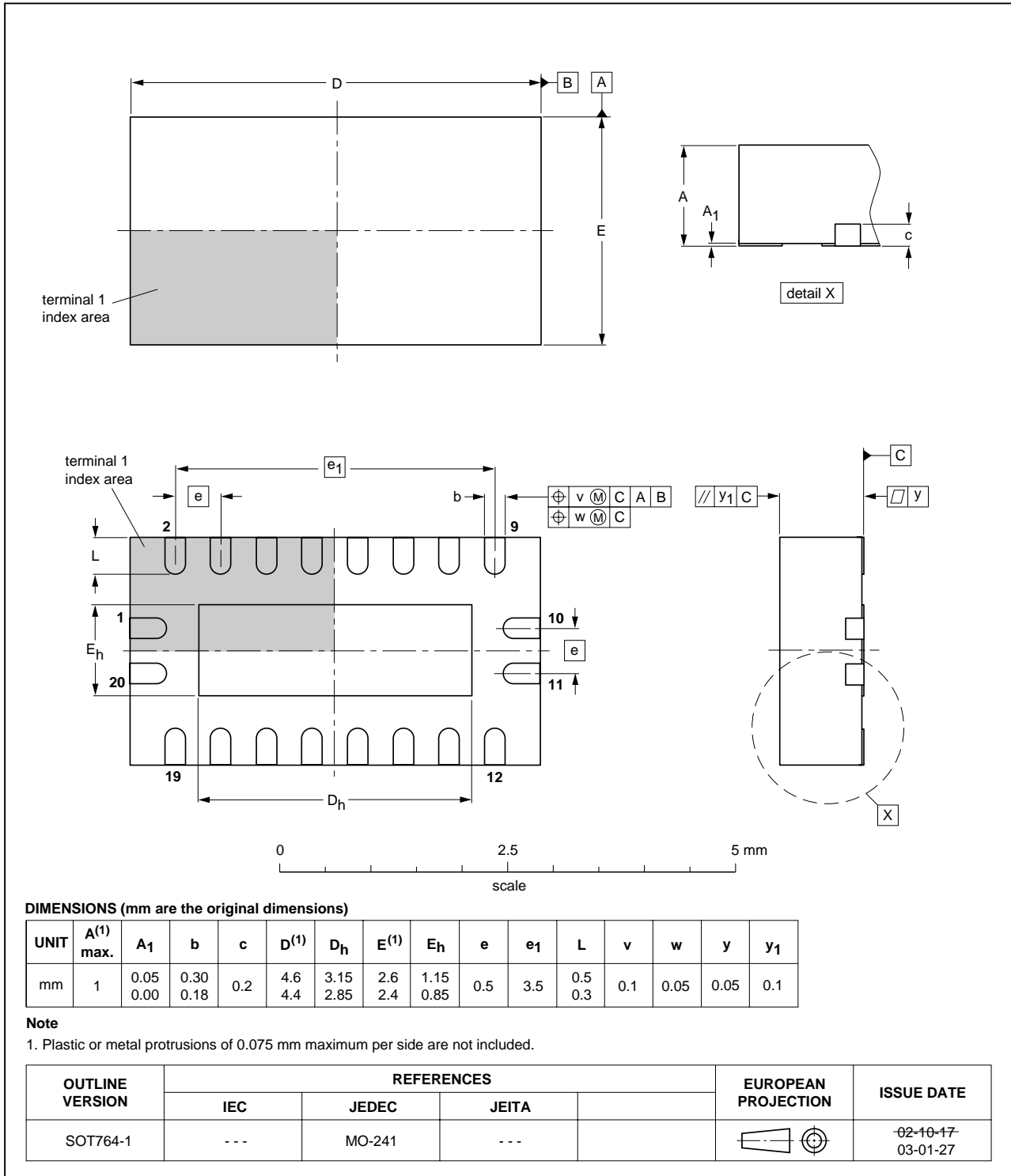


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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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