74LVC1G99

Ultra-configurable multiple function gate; 3-state

Rev. 7 — 22 June 2012 Product data sheet

1. General description

The 74LVC1G99 provides a low voltage, ultra-configurable, multiple function gate with 3-state output. The device can be configured as one of several logic functions including, AND, OR, NAND, NOR, XOR, XNOR, inverter, buffer and MUX. No external components are required to configure the device as all inputs can be connected directly to V_{CC} or GND. The 3-state output is controlled by the output enable input ($\overline{OE}$). A HIGH level at $\overline{OE}$ causes the output (Y) to assume a high-impedance OFF-state. When $\overline{OE}$ is LOW, the output state is determined by the signals applied to the Schmitt trigger inputs (A, B, C and D).

Due to the use of Schmitt trigger inputs the device is tolerant of slowly changing input signals, transforming them into sharply defined, jitter free output signals. By eliminating leakage current paths to V_{CC} and GND, the inputs and disabled output are also over-voltage tolerant, making the device suitable for mixed-voltage applications.

This device is fully specified for partial power-down applications using I_{OFF}.
The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G99 is fully specified over the supply range from 1.65 V to 5.5 V.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G99DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC1G99GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC1G99GF	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC1G99GD	–40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74LVC1G99GM	–40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
74LVC1G99GN	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC1G99GS	–40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC1G99DP	V99
74LVC1G99GT	V99
74LVC1G99GF	YF
74LVC1G99GD	V99
74LVC1G99GM	V99
74LVC1G99GN	YF
74LVC1G99GS	YF

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

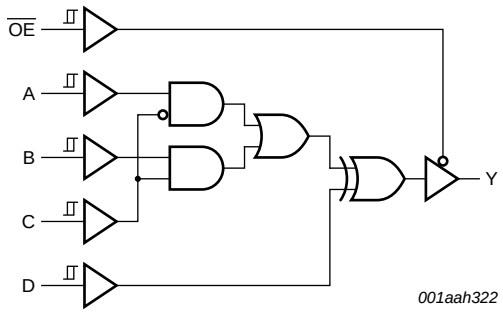


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning

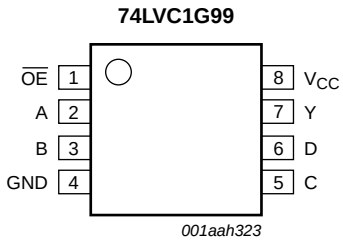
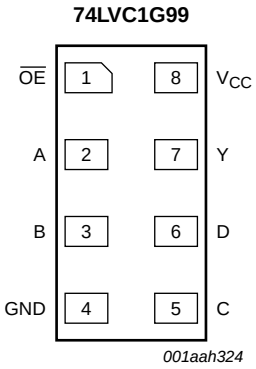
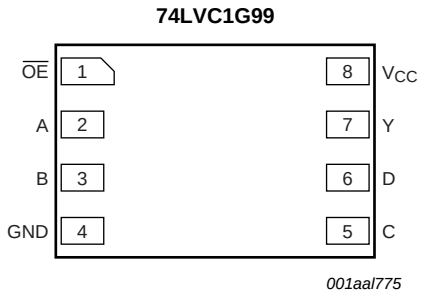


Fig 2. Pin configuration SOT505-2



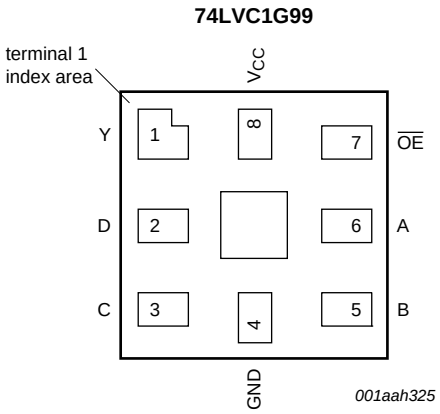
Transparent top view

Fig 3. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203



Transparent top view

Fig 4. Pin configuration SOT996-2



Transparent top view

Fig 5. Pin configuration SOT902-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT996-2	SOT902-2	
$\overline{OE}$	1	7	output enable input $\overline{OE}$ (active LOW)
A	2	6	data input
B	3	5	data input
GND	4	4	ground (0 V)
C	5	3	data input
D	6	2	data input
Y	7	1	data output
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input					Output
$\overline{OE}$	D	C	B	A	Y
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	X	X	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7.1 Logic configurations

Table 5. Function selection table

Primary function	Complementary function
3-state buffer	
3-state inverter	
3-state 2-input multiplexer	
3-state 2-input multiplexer with inverting output	
3-state 2-input AND	3-state 2-input NOR with two inverting inputs
3-state 2-input AND with one inverting input	3-state 2-input NOR with one inverting input
3-state 2-input AND with two inverting inputs	3-state 2-input NOR
3-state 2-input NAND	3-state 2-input OR with two inverting inputs
3-state 2-input NAND with one inverting input	3-state 2-input OR with one inverting input
3-state 2-input NAND with two inverting inputs	3-state 2-input OR
3-state 2-input XOR	
3-state 2-input XNOR	3-state 2-input XOR with one inverting input

7.2 3-state buffer functions available

Table 6. Function table[1]

See Figure 6.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state buffer	L	input	H or L	L	L
	L	H or L	input	H	L
	L	L	H	input	L
	L	H	L	input	H
	L	H	H or L	L	input
	L	H or L	L	H	input
	L	L	L	H or L	input

[1] H = HIGH voltage level;
L = LOW voltage level.

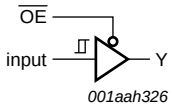


Fig 6. 3-state buffer function

7.3 3-state inverter functions available

Table 7. Function table[1]

See Figure 7.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state inverter	L	input	H or L	L	H
	L	X	input	H	H
	L	L	H	input	H
	L	H	L	input	L
	L	H	H or L	L	input
	L	H or L	H	H	input
	L	H	H	H or L	input

[1] H = HIGH voltage level;
L = LOW voltage level.
X = don't care.

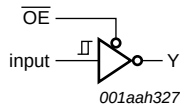


Fig 7. 3-state inverter function

7.4 3-state multiplexer functions available

Table 8. Function table[1]

See Figure 8.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state 2-input multiplexer	L	input 1	input 2	$\overline{\text{input 1}}$ or input 2	L
	L	input 2	input 1	$\overline{\text{input 2}}$ or input 1	L
	L	input 1	input 2	$\overline{\text{input 1}}$ or input 2	H
	L	input 2	input 1	$\overline{\text{input 2}}$ or input 1	H

[1] H = HIGH voltage level;
L = LOW voltage level.

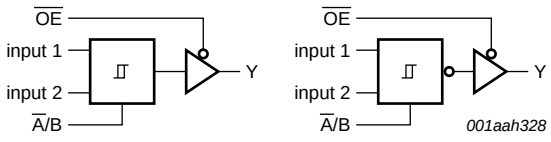


Fig 8. 3-state 2-input multiplexer function

7.5 3-state AND/NOR functions available

Table 9. Function table[1]

See Figure 9.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state AND	3-state NOR	L	L	input 1	input 2	L
2	3-state AND	3-state NOR	L	L	input 2	input 1	L

[1] H = HIGH voltage level;
L = LOW voltage level.

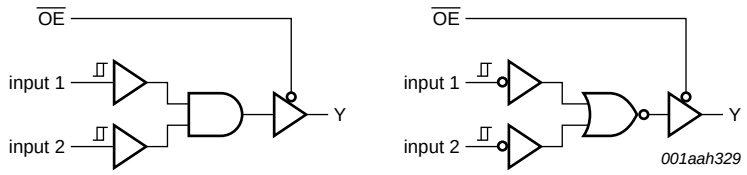


Fig 9. 3-state AND/NOR function

Table 10. Function table[1]

See Figure 10.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state AND	3-state NOR	L	input 2	L	input 1	L
2	3-state AND	3-state NOR	L	H	input 1	input 2	H

[1] H = HIGH voltage level;
L = LOW voltage level.

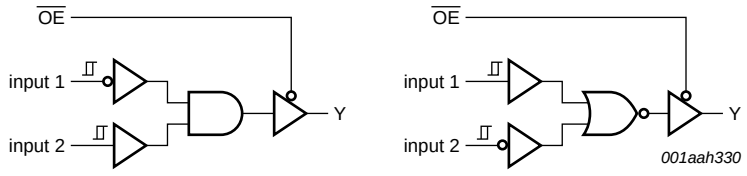


Fig 10. 3-state AND/NOR function

Table 11. Function table[1]

See Figure 11.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state AND	3-state NOR	L	input 1	L	input 2	L
2	3-state AND	3-state NOR	L	H	input 2	input 1	H

[1] H = HIGH voltage level;
L = LOW voltage level.

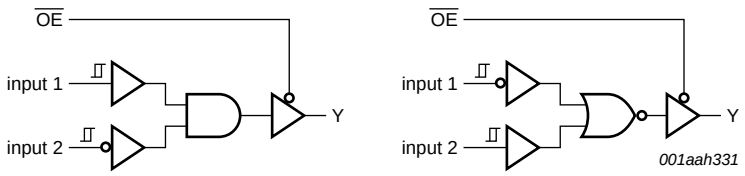


Fig 11. 3-state AND/NOR function

Table 12. Function table[1]

See Figure 12.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state AND	3-state NOR	L	input 1	H	input 2	L
2	3-state AND	3-state NOR	L	input 2	H	input 1	L

[1] H = HIGH voltage level;
L = LOW voltage level.

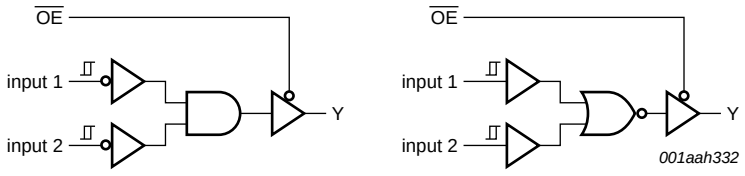


Fig 12. 3-state AND/NOR function

7.6 3-state NAND/OR functions available

Table 13. Function table[1]

See Figure 13.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state NAND	3-state OR	L	L	input 1	input 2	H
2	3-state NAND	3-state OR	L	L	input 2	input 1	H

[1] H = HIGH voltage level;
L = LOW voltage level.

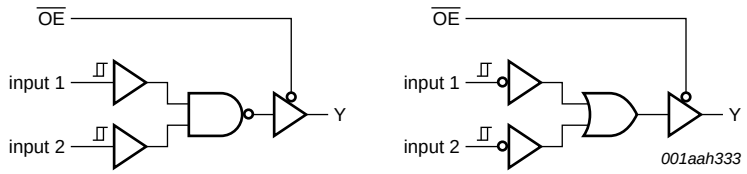


Fig 13. 3-state NAND/OR function

Table 14. Function table[1]

See Figure 14.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state NAND	3-state OR	L	input 2	L	input 1	H
2	3-state NAND	3-state OR	L	H	input 1	input 2	L

[1] H = HIGH voltage level;
L = LOW voltage level.

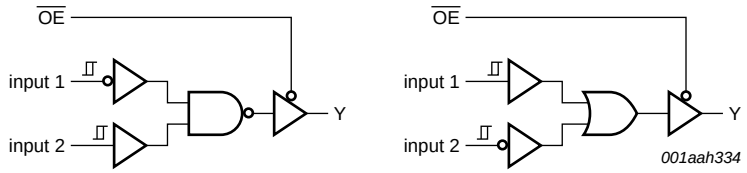


Fig 14. 3-state NAND/OR function

Table 15. Function table[1]

See Figure 15.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state NAND	3-state OR	L	input 1	L	input 2	H
2	3-state NAND	3-state OR	L	H	input 2	input 1	L

[1] H = HIGH voltage level;
L = LOW voltage level.

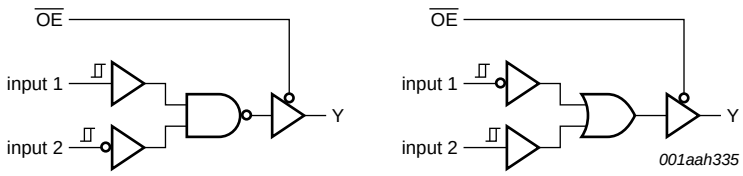


Fig 15. 3-state AND/NOR function

Table 16. Function table[1]

See Figure 16.

Number of inputs	Function		Input				
	AND/NAND	OR/NOR	$\overline{OE}$	A	B	C	D
2	3-state NAND	3-state OR	L	input 1	H	input 2	L
2	3-state NAND	3-state OR	L	input 2	H	input 1	L

[1] H = HIGH voltage level;
L = LOW voltage level.

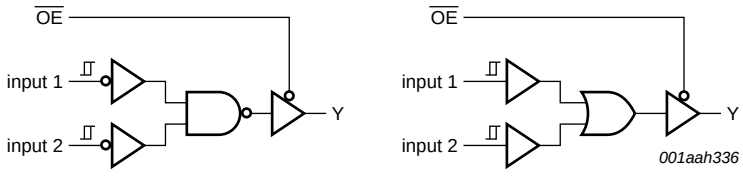


Fig 16. 3-state AND/NOR function

7.7 3-state XOR/XNOR functions available

Table 17. Function table[1]

See Figure 17.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state XOR	L	input 1	H or L	L	input 2
	L	input 2	H or L	L	input 1
	L	H or L	input 1	H	input 2
	L	H or L	input 2	H	input 1
	L	L	H	input 1	input 2
	L	L	H	input 2	input 1

[1] H = HIGH voltage level;
L = LOW voltage level.

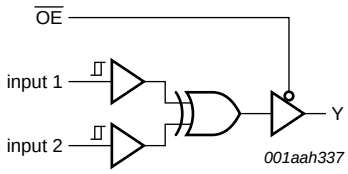


Fig 17. 3-state XOR function

Table 18. Function table[1]

See Figure 18.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state XOR	L	H	L	input 1	input 2

[1] H = HIGH voltage level;
L = LOW voltage level.

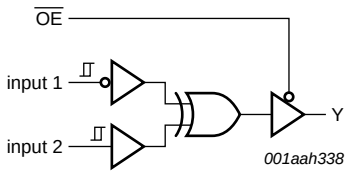


Fig 18. 3-state XOR function

Table 19. Function table[1]

See Figure 19.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state XOR	L	H	L	input 1	input 2

[1] H = HIGH voltage level;
L = LOW voltage level.

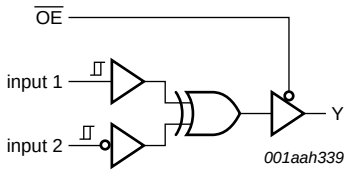


Fig 19. 3-state XOR function

Table 20. Function table[1]

See Figure 20.

Function	Input				
	$\overline{OE}$	A	B	C	D
3-state XNOR	L	H	L	input 1	input 2
	L	H	L	input 2	input 1

[1] H = HIGH voltage level;
L = LOW voltage level.

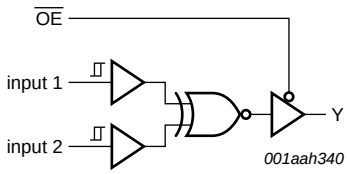


Fig 20. 3-state XNOR function

8. Limiting values

Table 21. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1][2]	–0.5	V_{CC} + 0.5	V
		Power-down mode	[1][2]	–0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			–100	-	mA
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	-	250	mW
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

[3] For TSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8, XSON8U and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 22. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 4.5 V	-	10	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	5	ns/V

10. Static characteristics

Table 23. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	1.2	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	2.2	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.3	-	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	V
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND	-	±0.1	±10	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±10	µA
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; V_I = 5.5 V or GND; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	2.5	-	pF
T_{amb} = –40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = –100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} – 0.1	-	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	0.95	-	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	1.7	-	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	1.9	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	2.0	-	-	V
		I_O = –32 mA; V_{CC} = 4.5 V	3.4	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V

Table 23. Static characteristics *…continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_I	input leakage current	V_{CC} = 0 V to 5.5 V; V_I = 5.5 V or GND	-	-	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND	-	-	±200	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	-	±200	µA
I_{CC}	supply current	V_{CC} = 1.65 V to 5.5 V; V_I = 5.5 V or GND; I_O = 0 A	-	-	200	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} − 0.6 V; I_O = 0 A	-	-	5000	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 24. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 23.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{pd}	propagation delay	A to Y; see Figure 21 [2]							
		V_{CC} = 1.65 V to 1.95 V	-	7.5	-	2.8	30.8	38.5	ns
		V_{CC} = 2.3 V to 2.7 V	-	5.0	-	2.0	11.7	14.6	ns
		V_{CC} = 2.7 V	-	5.4	-	2.0	9.0	11.3	ns
		V_{CC} = 3.0 V to 3.6 V	-	4.5	-	1.8	8.4	10.5	ns
		V_{CC} = 4.5 V to 5.5 V	-	3.8	-	1.8	5.5	6.9	ns
		B to Y; see Figure 21 [2]							
		V_{CC} = 1.65 V to 1.95 V	-	7.5	-	2.8	28.9	36.2	ns
		V_{CC} = 2.3 V to 2.7 V	-	5.0	-	2.0	11.3	14.2	ns
		V_{CC} = 2.7 V	-	5.4	-	2.0	9.0	11.3	ns
		V_{CC} = 3.0 V to 3.6 V	-	4.5	-	1.8	8.2	10.3	ns
		V_{CC} = 4.5 V to 5.5 V	-	3.8	-	1.8	5.4	6.8	ns
		C to Y; see Figure 21 [2]							
		V_{CC} = 1.65 V to 1.95 V	-	7.8	-	3.2	29.8	37.3	ns
		V_{CC} = 2.3 V to 2.7 V	-	5.2	-	2.3	12.3	15.4	ns
		V_{CC} = 2.7 V	-	5.3	-	2.3	9.6	12.0	ns
		V_{CC} = 3.0 V to 3.6 V	-	4.6	-	2.3	8.6	10.8	ns
		V_{CC} = 4.5 V to 5.5 V	-	3.8	-	1.8	5.7	7.2	ns
		D to Y; see Figure 21 [2]							
		V_{CC} = 1.65 V to 1.95 V	-	7.0	-	2.8	25.7	32.2	ns
		V_{CC} = 2.3 V to 2.7 V	-	4.6	-	2.0	10.7	13.4	ns
		V_{CC} = 2.7 V	-	4.8	-	2.0	9.2	11.5	ns
		V_{CC} = 3.0 V to 3.6 V	-	4.1	-	1.8	7.6	9.5	ns
		V_{CC} = 4.5 V to 5.5 V	-	3.4	-	1.6	5.2	6.5	ns

Table 24. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 23.

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C			Unit
			Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
t_{en}	enable time	$\overline{OE}$ to Y; see Figure 22 [3]							
		V_{CC} = 1.65 V to 1.95 V	-	5.7	-	2.0	25.2	32.0	ns
		V_{CC} = 2.3 V to 2.7 V	-	3.8	-	1.4	11.3	14.0	ns
		V_{CC} = 2.7 V	-	4.2	-	1.4	8.6	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	-	3.5	-	1.4	7.0	9.0	ns
		V_{CC} = 4.5 V to 5.5 V	-	2.7	-	1.4	4.7	6.0	ns
t_{dis}	disable time	$\overline{OE}$ to Y; see Figure 22 [4]							
		V_{CC} = 1.65 V to 1.95 V	-	5.7	-	3.0	15.0	19.0	ns
		V_{CC} = 2.3 V to 2.7 V	-	3.6	-	2.0	5.8	7.3	ns
		V_{CC} = 2.7 V	-	4.5	-	2.0	6.6	8.2	ns
		V_{CC} = 3.0 V to 3.6 V	-	4.5	-	2.1	5.9	7.4	ns
		V_{CC} = 4.5 V to 5.5 V	-	3.4	-	1.0	4.5	5.6	ns
C_{PD}	power dissipation capacitance	per buffer (output enabled); f_i = 10 MHz; C_L = 50 pF; V_I = GND to V_{CC} [5]							
		V_{CC} = 1.65 V to 1.95 V	-	14	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	16	-	-	-	-	pF
		V_{CC} = 2.7 V	-	18	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	25	-	-	-	-	pF
		V_{CC} = 4.5 V to 5.5 V	-	30	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

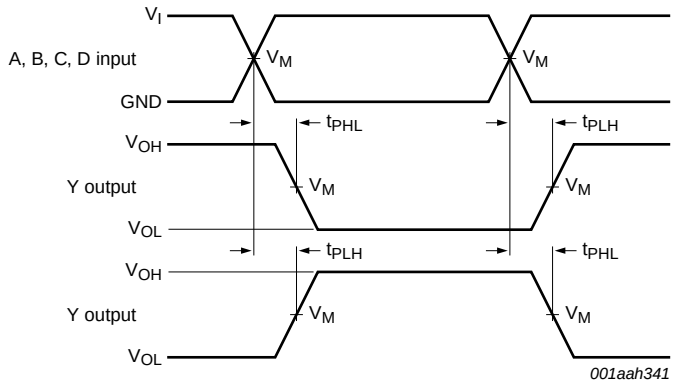
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

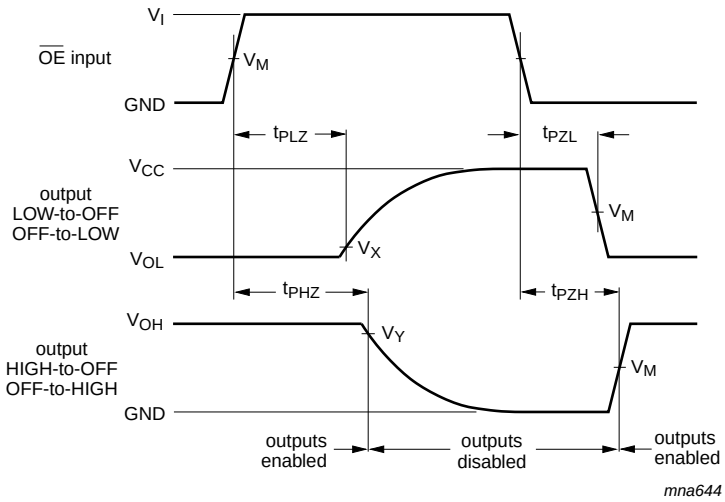
12. Waveforms



Measurement points are given in Table 25.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 21. The data input (A, B, C, D) to output (Y) propagation delays



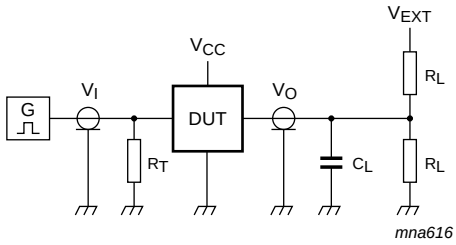
Measurement points are given in Table 25.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 22. 3-state enable and disable times

Table 25. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} – 0.15 V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} – 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Test data is given in Table 26.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 23. Test circuit for measuring switching times

Table 26. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

13. Transfer characteristics

Table 27. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 23

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Figure 24, Figure 25, Figure 26, Figure 27 and Figure 28						
		V_{CC} = 1.8 V	0.70	1.02	1.20	0.67	1.20	V
		V_{CC} = 2.3 V	1.11	1.42	1.60	1.08	1.60	V
		V_{CC} = 3.0 V	1.50	1.79	2.00	1.47	2.00	V
		V_{CC} = 4.5 V	2.16	2.52	2.74	2.13	2.74	V
		V_{CC} = 5.5 V	2.61	2.99	3.33	2.58	3.33	V

Table 27. Transfer characteristics *…continued*

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 23

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{T-}	negative-going threshold voltage	see Figure 24, Figure 25, Figure 26, Figure 27 and Figure 28						
		V_{CC} = 1.8 V	0.30	0.53	0.72	0.30	0.75	V
		V_{CC} = 2.3 V	0.58	0.77	1.00	0.58	1.03	V
		V_{CC} = 3.0 V	0.80	1.04	1.30	0.80	1.33	V
		V_{CC} = 4.5 V	1.21	1.55	1.90	1.21	1.93	V
		V_{CC} = 5.5 V	1.45	1.86	2.29	1.45	2.32	V
V_H	hysteresis voltage	($V_{T+} - V_{T-}$); see Figure 24, Figure 25, Figure 26, Figure 27 and Figure 28						
		V_{CC} = 1.8 V	0.30	0.48	0.62	0.23	0.62	V
		V_{CC} = 2.3 V	0.40	0.64	0.80	0.34	0.80	V
		V_{CC} = 3.0 V	0.50	0.75	1.00	0.44	1.00	V
		V_{CC} = 4.5 V	0.71	0.97	1.20	0.65	1.20	V
		V_{CC} = 5.5 V	0.71	1.13	1.40	0.65	1.40	V

[1] All typical values are measured at T_{amb} = 25 °C

14. Waveforms transfer characteristics

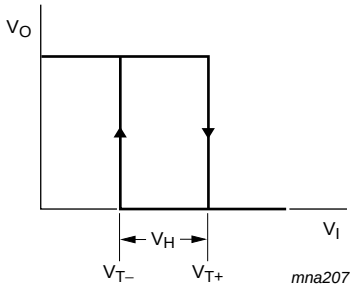


Fig 24. Transfer characteristic

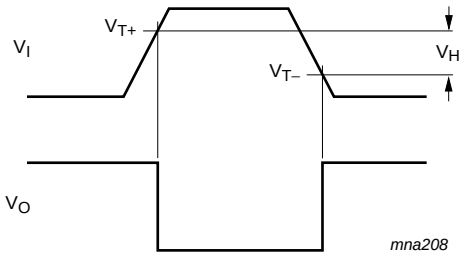


Fig 25. Definition of V_{T+}, V_{T-} and V_H

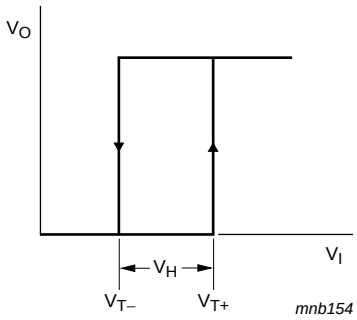


Fig 26. Transfer characteristic

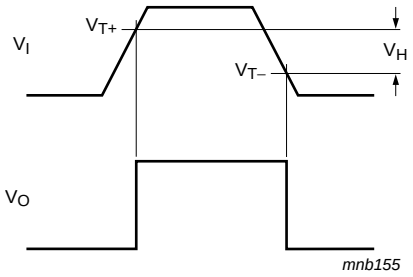


Fig 27. Definition of V_{T+}, V_{T-} and V_H

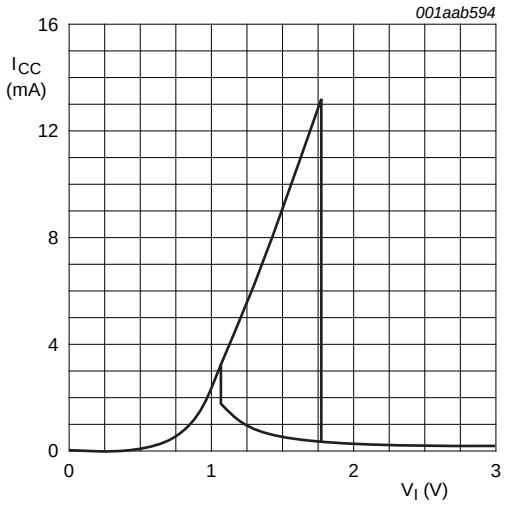
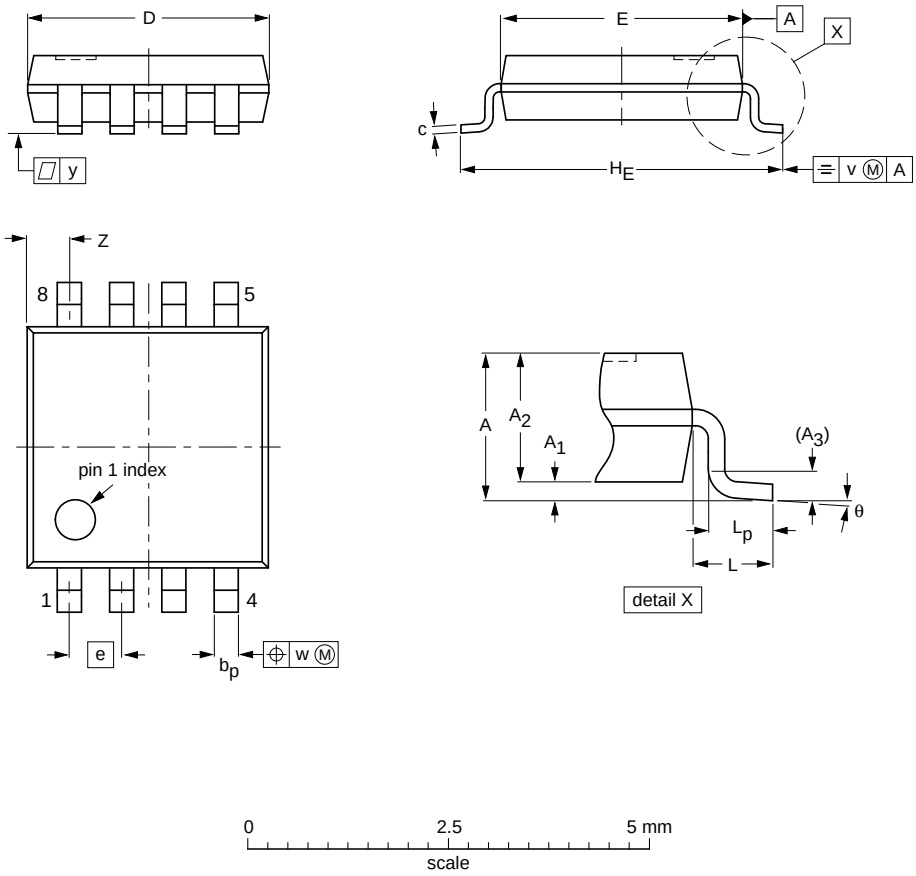


Fig 28. Typical 74LVC1G99 transfer characteristic; V_{CC} = 3.0 V

15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

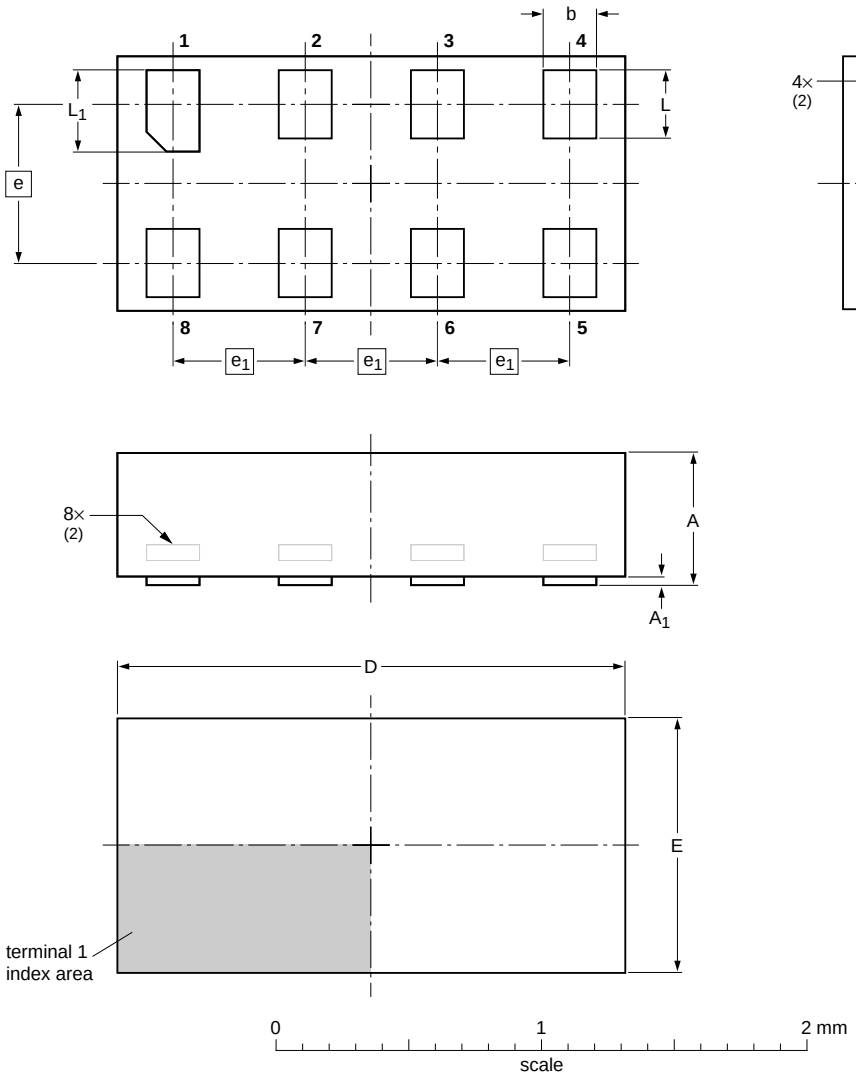
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 29. Package outline SOT505-2 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

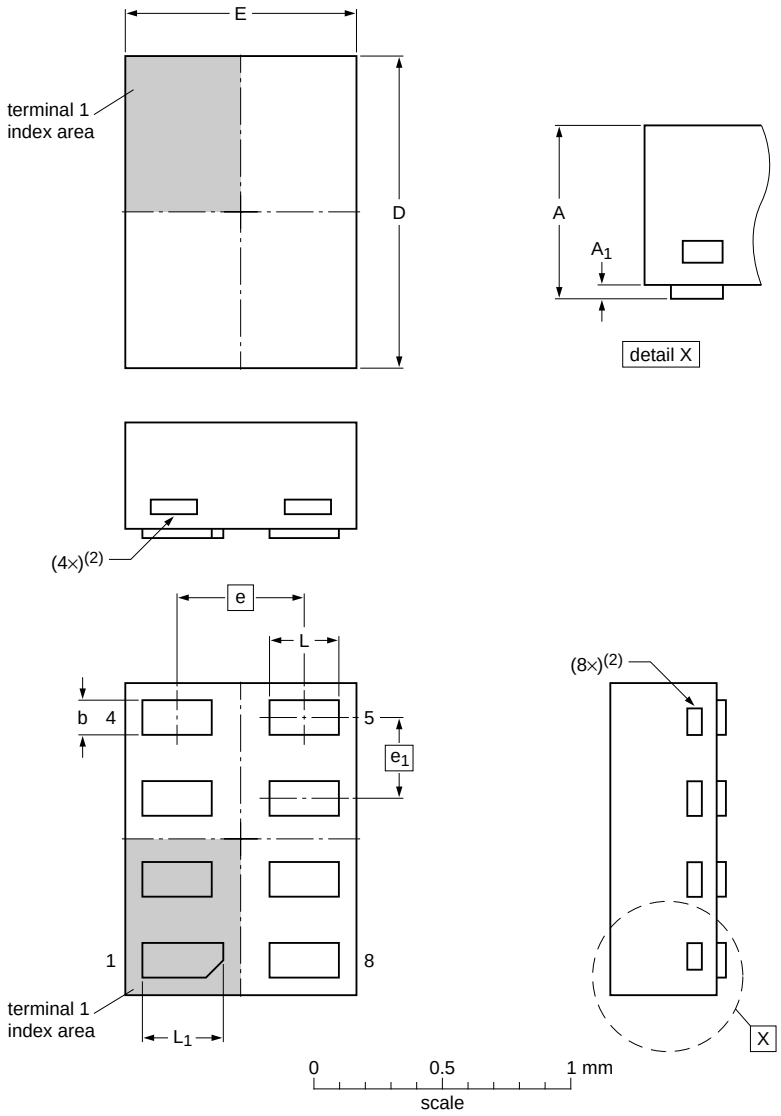
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 30. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
mm	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

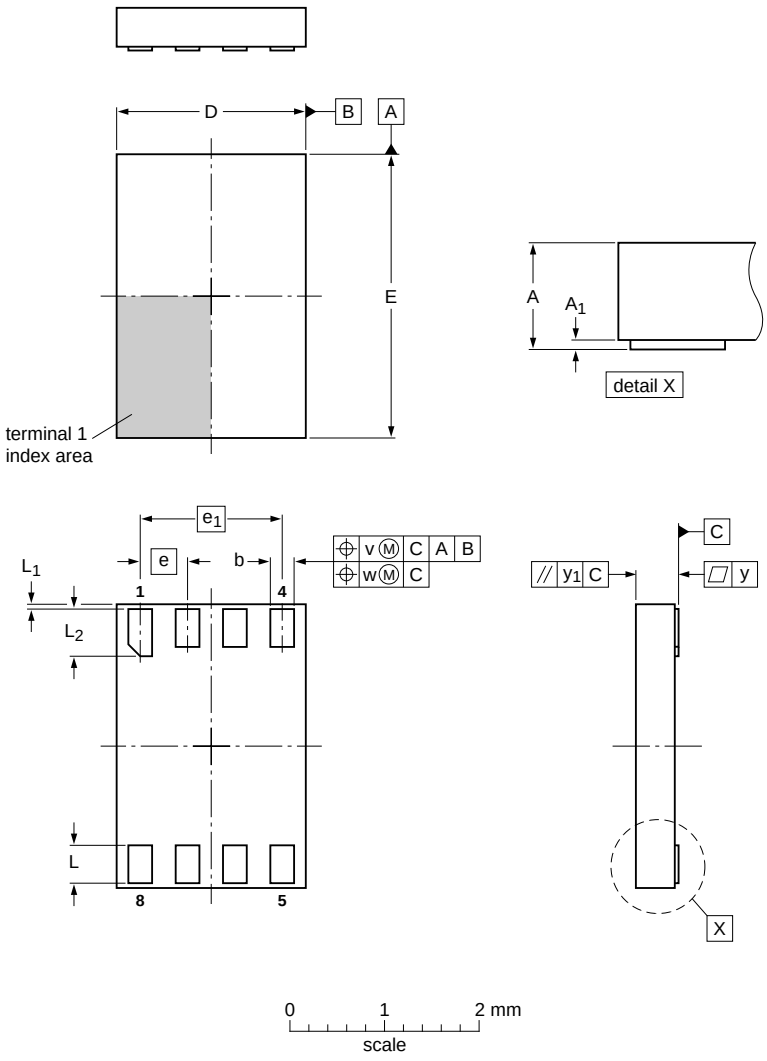
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig 31. Package outline SOT1089 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm **SOT996-2**



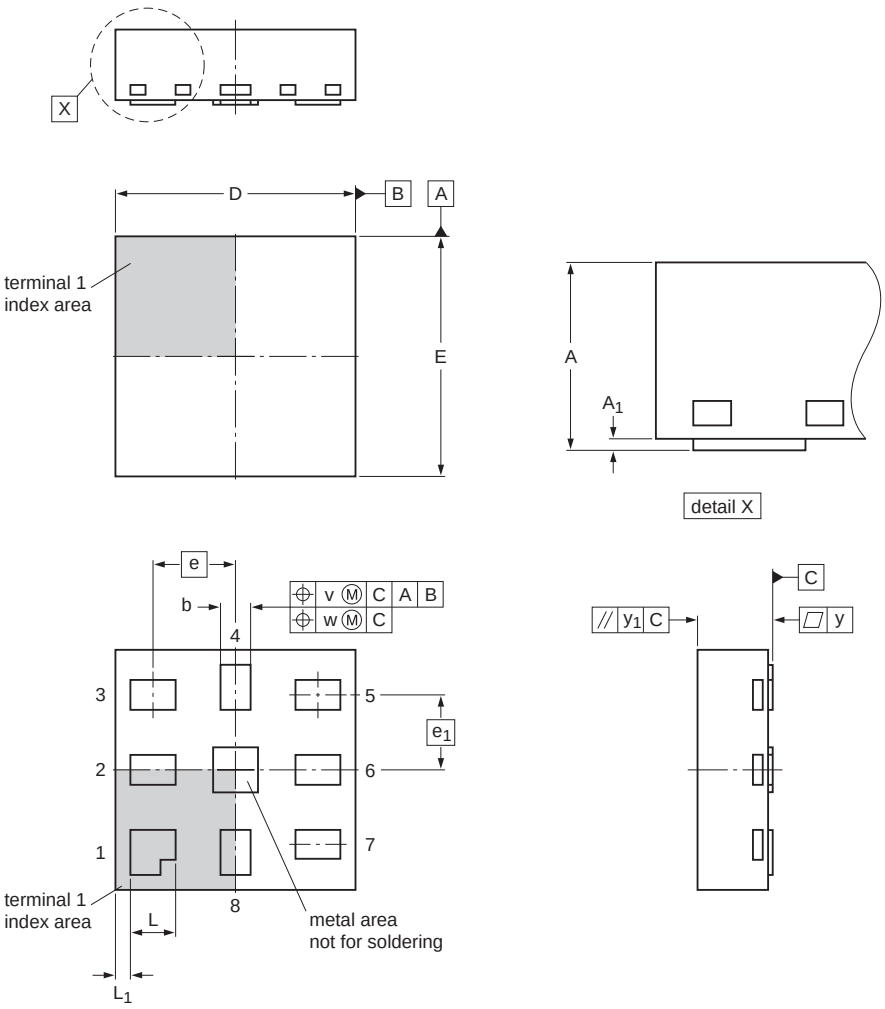
DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT996-2	- - -		- - -			~~07-12-18~~ 07-12-21

Fig 32. Package outline SOT996-2 (XSON8U)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65	0.55	0.5	0.35	0.15	0.1	0.05	0.05	0.05
	nom			0.20	1.60	1.60			0.30	0.10				
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note

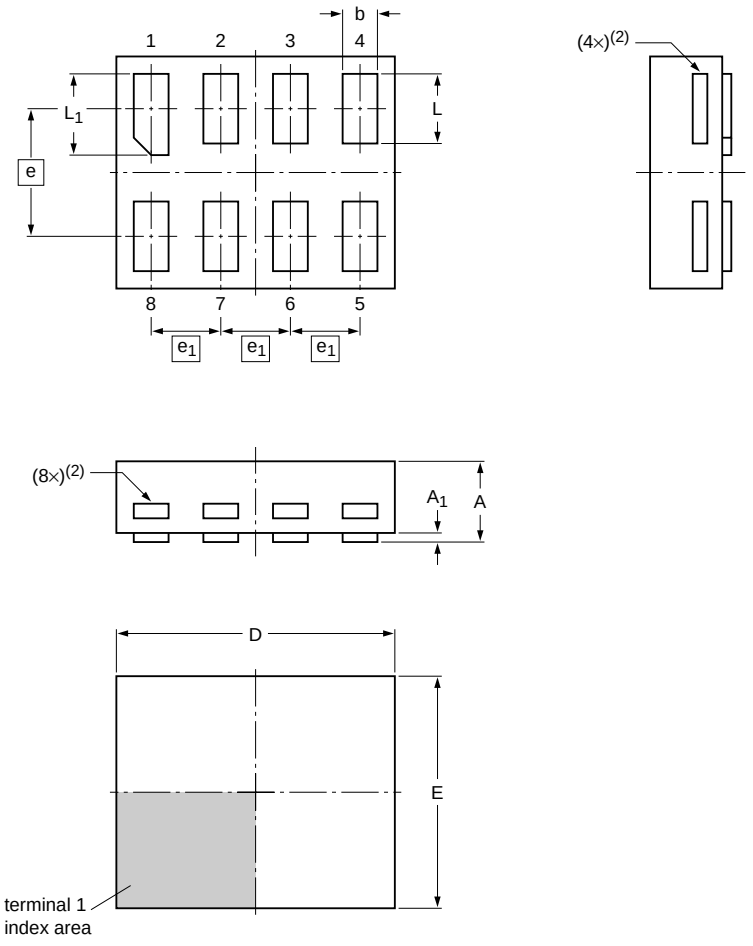
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 33. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

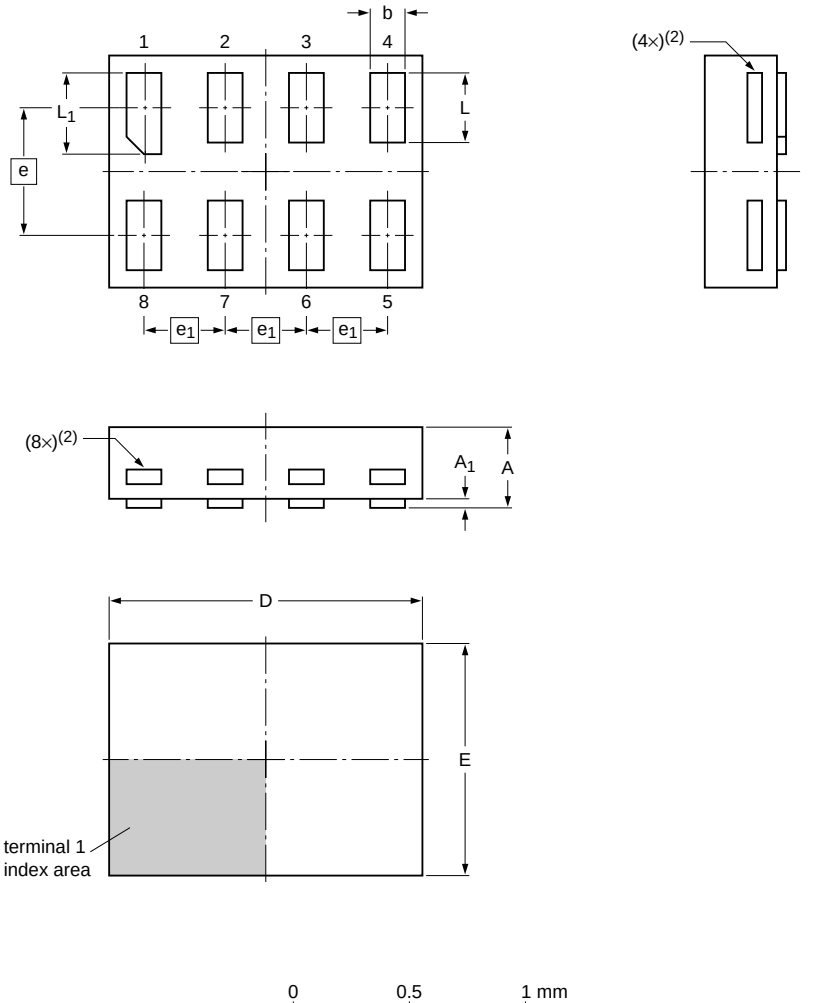
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07

Fig 34. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig 35. Package outline SOT1203 (XSON8)

16. Abbreviations

Table 28. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

17. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G99 v.7	20120622	Product data sheet	-	74LVC1G99 v.6
Modifications:	• For type number 74LVC1G99GM the SOT code has changed to SOT902-2.			
74LVC1G99 v.6	20111201	Product data sheet	-	74LVC1G99 v.5
Modifications:	• Legal pages updated.			
74LVC1G99 v.5	20101021	Product data sheet	-	74LVC1G99 v.4
74LVC1G99 v.4	20100416	Product data sheet	-	74LVC1G99 v.3
74LVC1G99 v.3	20091203	Product data sheet	-	74LVC1G99 v.2
74LVC1G99 v.2	20080208	Product data sheet	-	74LVC1G99 v.1
74LVC1G99 v.1	20080103	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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