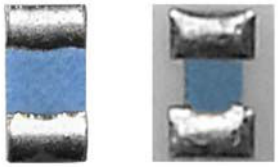
High Frequency 50 GHz Thin Film Chip Resistor



FEATURES

- Operating frequency 50 GHz
- Thin film microwave resistors
- SMD wraparound or flip chip resistor
- Small size, down to 20 mils by 16 mils
- Edged trimmed block resistors
- Pure alumina substrate (99.5 %)
- Ohmic range: 10R to 500R
- Design kits available
- Small internal reactance (LC down to 1×10^{-24})
- Tolerance 1 %, 2 %, 5 %, 10 %
- TCR: 100 ppm/°C in (- 55 °C, + 155 °C) temperature range
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

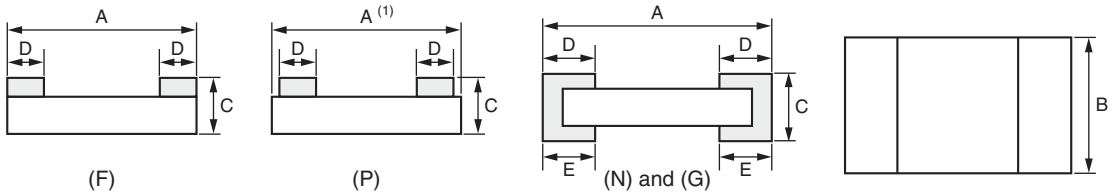
GREEN (5-2008)

Those miniaturized components are designed in such a way that their internal reactance is very small. When correctly mounted and utilized, they function as almost pure resistors on a very large range of frequency, up to 50 GHz.

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	RESISTANCE RANGE Ω	RATED POWER Pn W	LIMITING ELEMENT VOLTAGE V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
CH02016	02016	10 to 500	0.030	30	1, 2, 5, 10	100
CH0402	0402	10 to 500	0.050	37	1, 2, 5, 10	100
CH0603	0603	10 to 500	0.125	50	1, 2, 5, 10	100

DIMENSIONS in millimeters (inches)



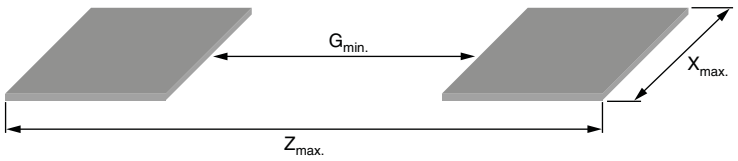
CASE SIZE MAX. TOL. + 0.1 (+ 0.004) MIN. TOL. - 0.1 (- 0.004)	DIMENSIONS				
	A (1)	B	C	D/E	
	MAX. TOL. + 0.1 (+ 0.004) MIN. TOL. - 0.1 (- 0.004)	MAX. TOL. + 0.1 (+ 0.004) MIN. TOL. - 0.1 (- 0.004)	MAX. TOL. + 0.127 (+ 0.005) MIN. TOL. - 0.127 (- 0.005)	MIN.	MAX.
02016	0.48 (0.020)	0.39 (0.016)	0.42 (0.02) (2)	0.11 (0.004)	0.15 (0.008)
0402	1.00 (0.040)	0.6 (0.023)	0.5 (0.02)	0.15 (0.006)	0.35 (0.014)
0603	1.52 (0.060)	0.75 (0.030)	0.5 (0.02)	0.25 (0.010)	0.51 (0.020)

Notes

(1) For CH0402 and CH0603 with P termination, A dimension is increased by 0.2 mm

(2) + or - 0.07 mm

LAND PATTERN FLIP CHIP TERMINATIONS in millimeters



CHIP SIZE	$Z_{max.}$	$X_{max.}$	$G_{min.}$
02016	0.53	0.44	0.15
0402	1.4	0.650	0.4
0603	1.71	0.9	0.760

Note

- Suggested land pattern: According to IPC-7351

Dimension and tolerance of land pattern shall be defined by PCB designer; PCB can be designed according to IPC-7351A “Generic Requirements for Surface Mount Design and Land Pattern Standard”

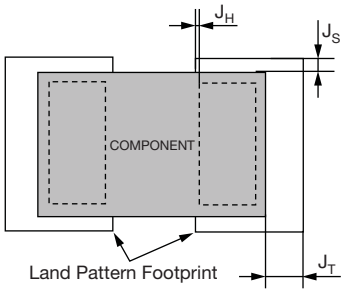
Example of land pattern: Fabrication allowance, assembly location and min. or max. level density board are not included in the exemple bellow.

According to IPC-7351A “Generic Requirements for Surface Mount Design and Land Pattern Standard”:

$Z_{max.} = A_{min.} + 2J_T + \sqrt{(C_A^2 + F^2 + P^2)}$ with C: “Unilateral profile tolerance for the component”;

$G_{min.} = F_{max.} + 2J_H - \sqrt{(C_F^2 + F^2 + P^2)}$ F: ”Unilateral profile tolerance for the board land pattern”;

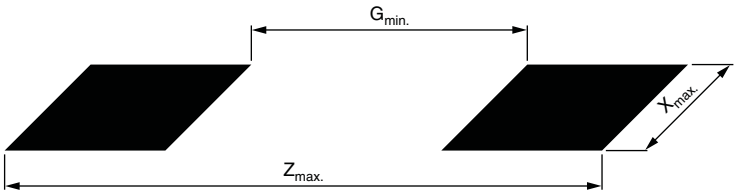
$X_{max.} = B_{min.} + 2J_S + \sqrt{(C_B^2 + F^2 + P^2)}$ and P: “Diameter of true position placement accuracy to the center of land pattern”.



For rectangular component Flip-Chip mounting, we suggest:

JT (TOE)	0 mm
JH (HELL)	0 mm
JS (SDE)	0 mm

WRAPAROUND TERMINATIONS in millimeters



CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0402	1.55	0.15	0.73
0603	2.37	0.35	0.98

TOLERANCE VS. OHMIC VALUES

Ohmic range	10 Ω ≤ *R* < 50 Ω	50 Ω ≤ *R* < 100 Ω	100 Ω ≤ *R* ≤ 500 Ω (1)
Tolerance	5 %, 10 %	2 %, 5 %, 10 %	1 %, 2 %, 5 %, 10 %

Note

(1) Best tolerance for 100 Ω to 500 Ω in 02016 is 2 %

PREFERRED MODELS AND VALUES

Vishay Sfernice highly recommend to use the smallest sizes and flip chip version to get the best performances.

Recommended Values:

10R/18R/25R/50R/75R/100R/150R/180R/200R/250R/330R/500R
Those values are available with a **MOQ of 100 pieces.**
Other values can be ordered upon request, but higher MOQ will apply: 1000 pieces for CH02016, 500 pieces for CH0402, 250 pieces for CH0603.

Recommended terminations:

F

Recommended tolerance:

2 %

Design kits are available Ex Stock in CH02016 and CH0402 sizes. There are 20 pieces per recommended value. F termination. 5 % tolerance.
Those kits are packaged in pieces of tape and delivered in ESD bags.

PACKAGING

Standard packaging is waffle pack for sizes 0402 and 0603. Plastic tape and reel (low conductivity) for size 02016.
Plastic tape and reel is available for 0402 and 0603 (low conductivity) or paper tape under request for all sizes.
Depending on the type of terminations, parts will be packed differently:

One face:

- Gold terminations: Active face up
- Tin/silver termination: Active face down

Note

- Please refer to Vishay Sfernice Application Note "Guidelines for Vishay Sfernice Resistive and Inductive Products" for soldering recommendation (document number 52029, 3. Guidelines for Surface Mounting Components (SMD), profile number 3 applies

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" X 2"	TAPE AND REEL		
			Min.	Max.	
02016	See MOQ mentioned on preferred models and values	484	100	5000	8 mm
0402		100			
0603		100			

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover. To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided. When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code.

GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: CH0402-50RJF (preferred part number format)

C	H	0	4	0	2	-	5	0	R	J	F	T

GLOBAL MODEL	SIZE	OHMIC VALUE	TOLERANCE	TERMINATION (1)	PACKAGING (2)
CH	**02016** **0402** **0603**	**10R to 500R**	**F** = 1 % **G** = 2 % **J** = 5 % **K** = 10 %	**F** (Flip Chip): SnAg over nickel barrier **N** (W/A): SnAg over nickel barrier (except 02016) **P** (one face): (3) Gold bonding pads **G** (W/A): Gold (except 02016)	**T** = Tape and reel **PT** = Paper tape Leave blank for waffle pack

Historical Part Number example: CH 0402 50R 5 % P e2 (will continue to be accepted)

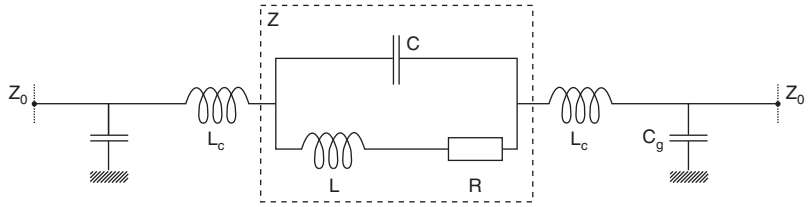
CH	0402	50R	5 %	P	e2
HISTORICAL MODEL	SIZE	OHMIC VALUE	TOLERANCE	TERMINATION	LEAD (Pb)-FREE VERSION **e2**: Tin/silver **e4**: Gold

Global Part Number Ordering design kits:
CHKIT-02016
CHKIT-0402

Notes

(1) 02016 not available with N and G termination
(2) 02016 paper tape only available
(3) Gold termination for application in hermetic package

TYPICAL HIGH FREQUENCY PERFORMANCE ELECTRICAL MODEL



C	Internal shunt capacitance
L	Internal inductance
R	Resistance
Z	Internal impedance (R, L, C)
L_c	External connection inductance
C_g	External capacitance to ground

The complex impedance of the chip resistor is given by the following equations:

$$Z = \frac{R + j\omega(L - R^2C - L^2C\omega^2)}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]}$$

$$\frac{[Z]}{R} = \frac{1}{1 + C[(R^2C - 2L)\omega^2 + L^2C\omega^4]} \times \sqrt{1 + \left[\frac{\omega(L - R^2C - L^2C\omega^2)}{R}\right]^2}$$

$$\theta = \tan^{-1}\frac{\omega(L - R^2C - L^2C\omega^2)}{R}$$

Notes

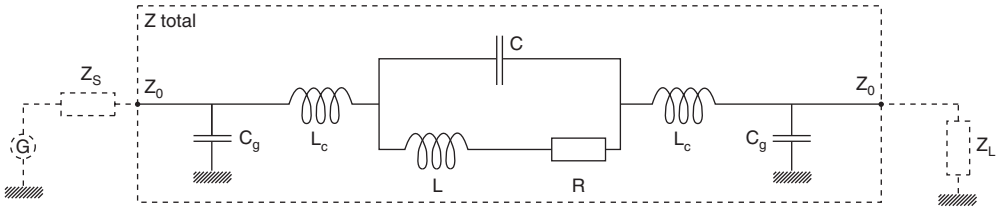
- $\omega = 2 \times \pi \times f$
- f: Frequency

The chip resistor itself is purely resistive when $R = \sqrt{\frac{L}{C}}$. The smaller the L x C product the greater the frequency range over which the resistor looks approximately resistive.
This can be seen on the graphs showing the ratio $\frac{[Z]}{R}$ versus frequency.
R, L and C are relevant to the chip resistor itself.
L_c and C_g also depends on the way the chip resistor is mounted.
It is important to notice that after assembly the external reactance of L_c and C_g will be combined to internal reactance of L and C. This combination can upgrade or downgrade the HF behaviour of the component.
This is why we are displaying two sets of data:

- $\frac{[Z]}{R}$ versus frequency curves which aims to show at a glance the intrinsic HF performance of a given chip resistor
- S-parameters versus frequency curves relevant to chip resistor when assembled on ideal Z0 impedance transmission line

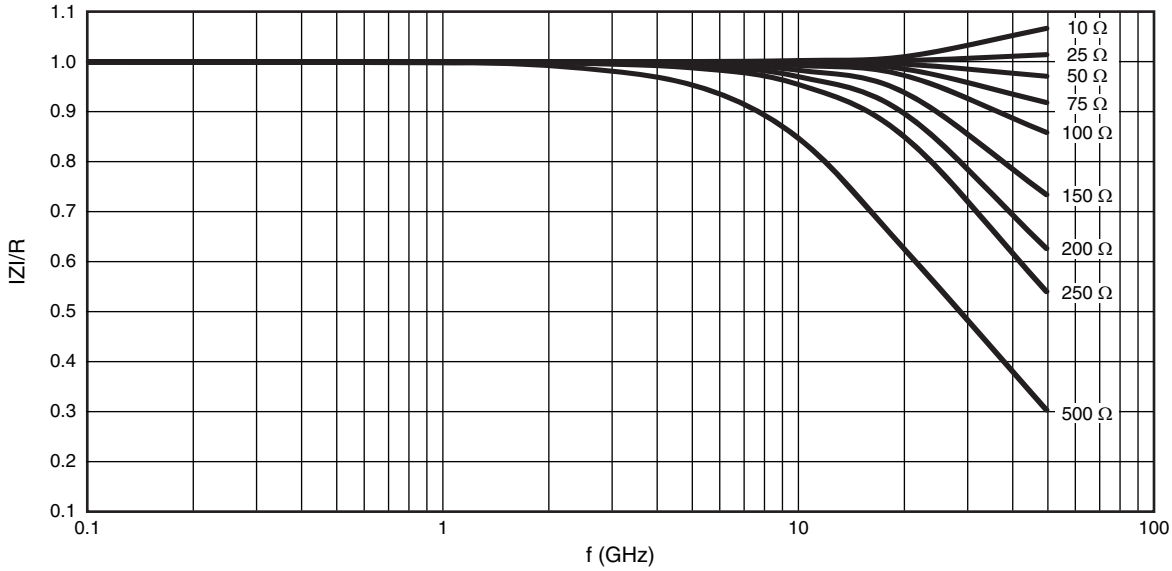
These lines are terminated with adapted source and load impedance respectively Z_s and Z_l with $Z_0 = Z_L = Z_s$ (for others configurations please consult us).

Equivalent circuit for S-parameters:

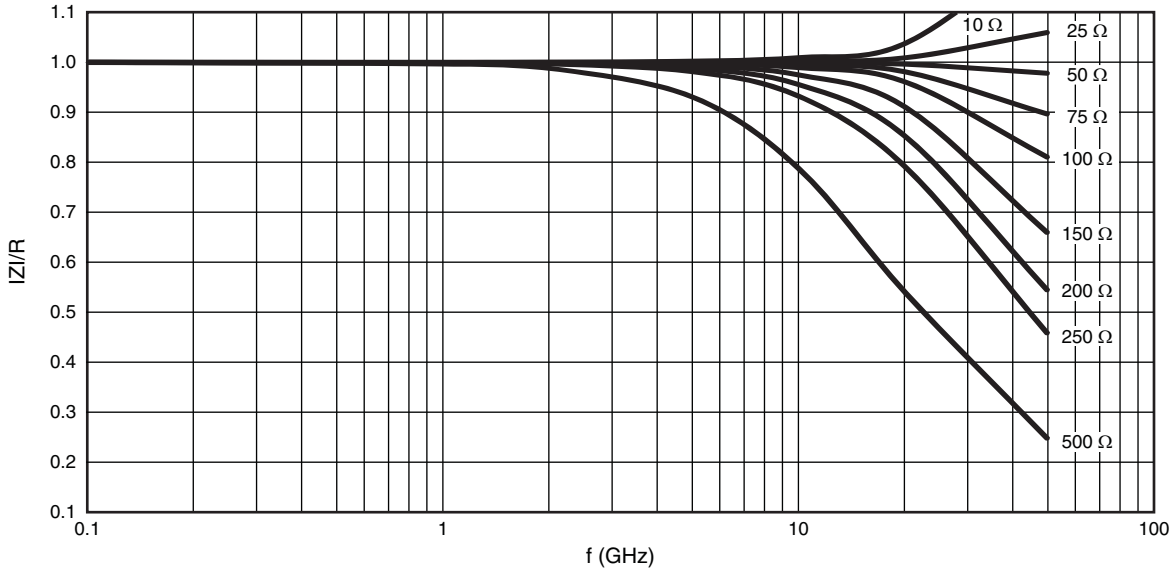


S-parameters are computed taking into account all the resistive, inductive and capacitive elements (Z total) and $Z_0 = Z_L = Z_s = R$.

INTERNAL IMPEDANCE CURVES

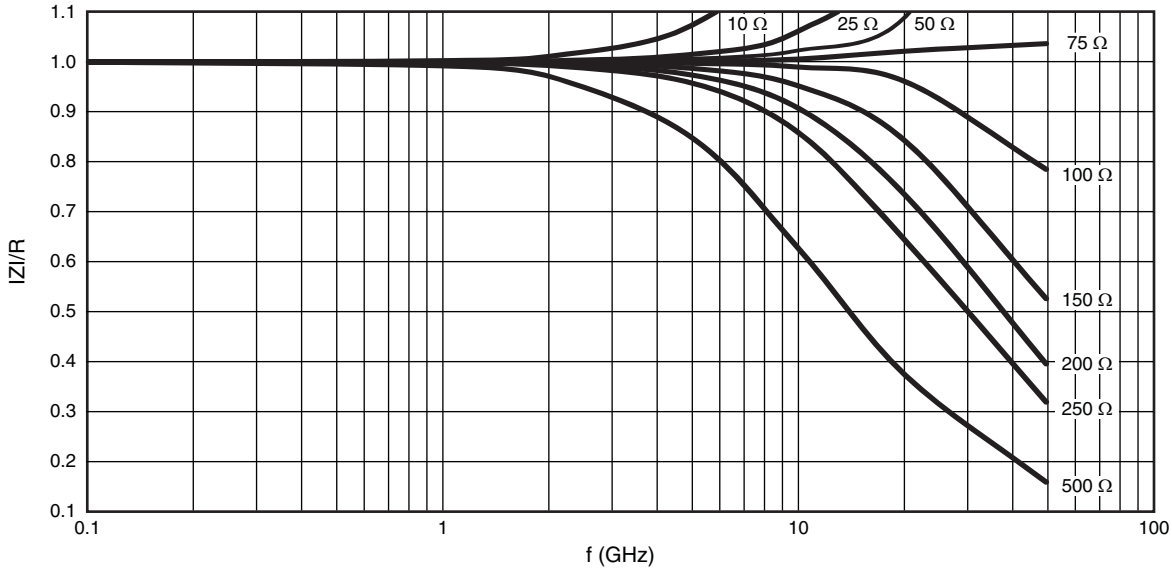


Internal impedance curve for 02016 size (F and P terminations)

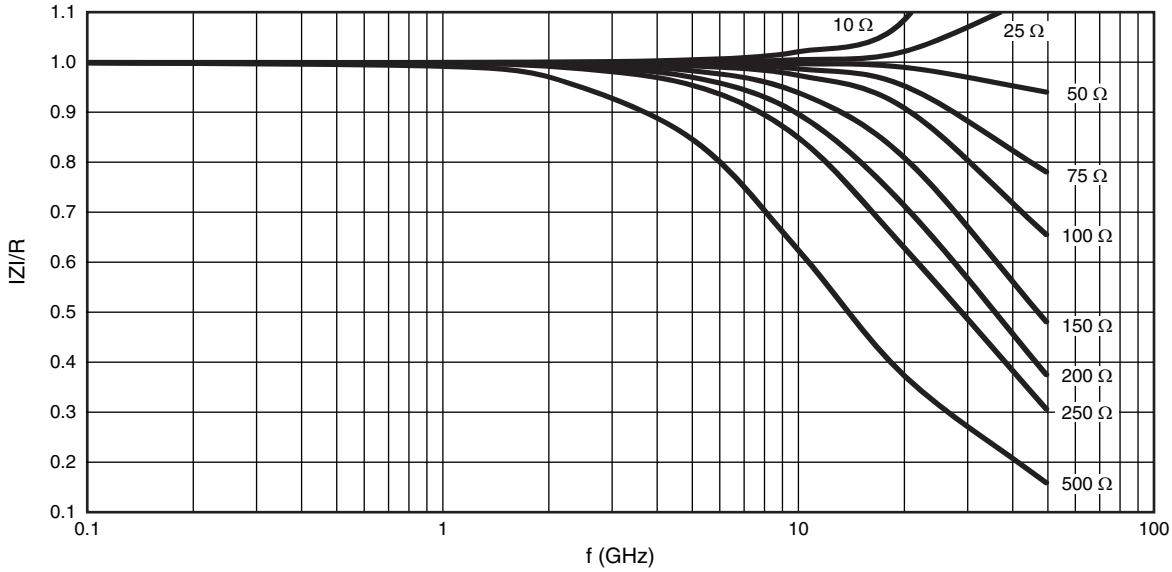


Internal impedance curve for 0402 size (F and P terminations)

INTERNAL IMPEDANCE CURVES

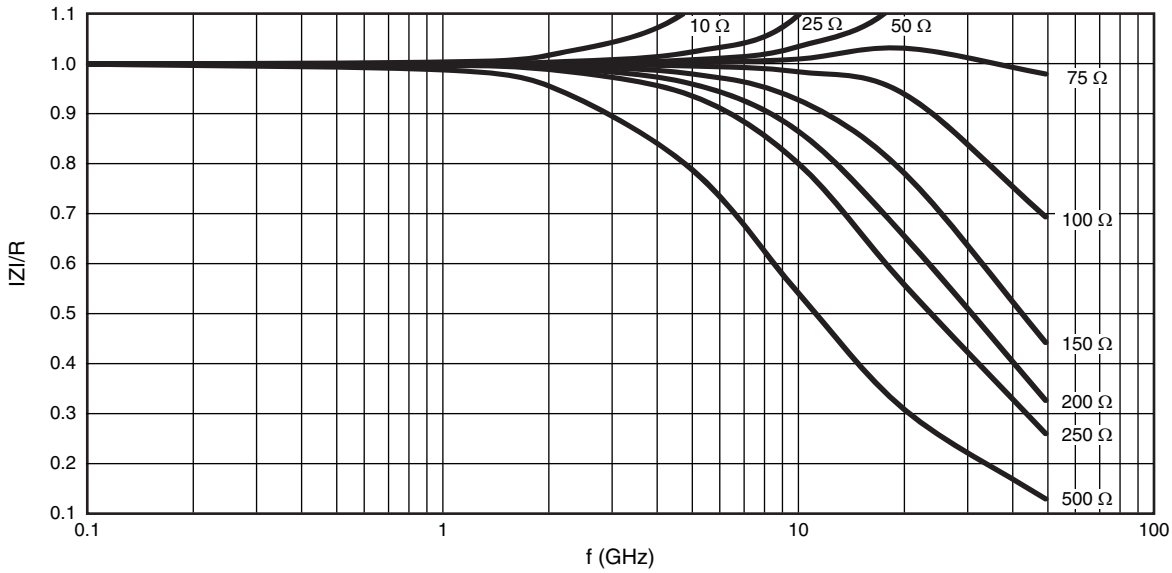


Internal impedance curve for 0402 size (N and G terminations)



Internal impedance curve for 0603 size (F and P terminations)

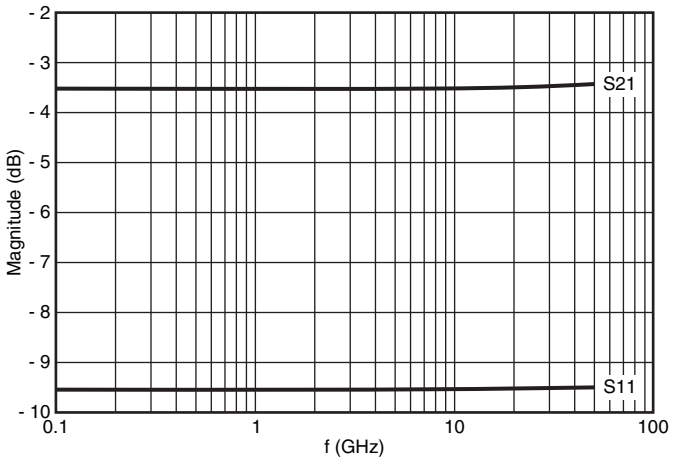
INTERNAL IMPEDANCE CURVES



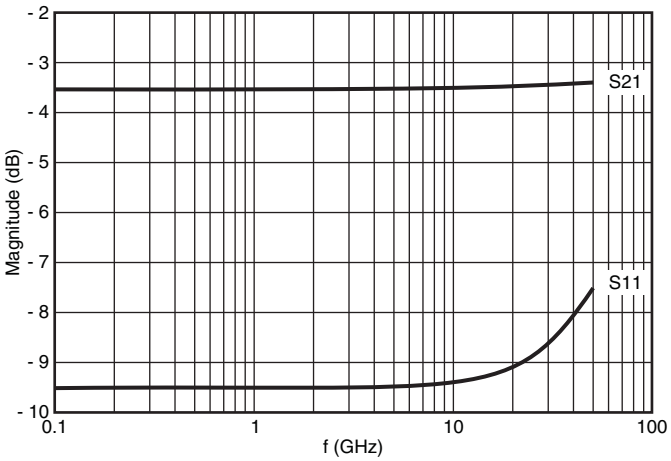
Internal impedance curve for 0603 size (N and G terminations)

S-PARAMETER

CH02016 (F and P Terminations)



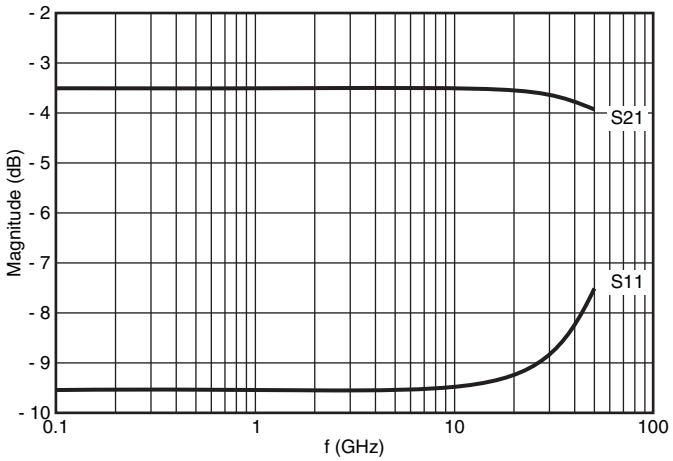
CH02016 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



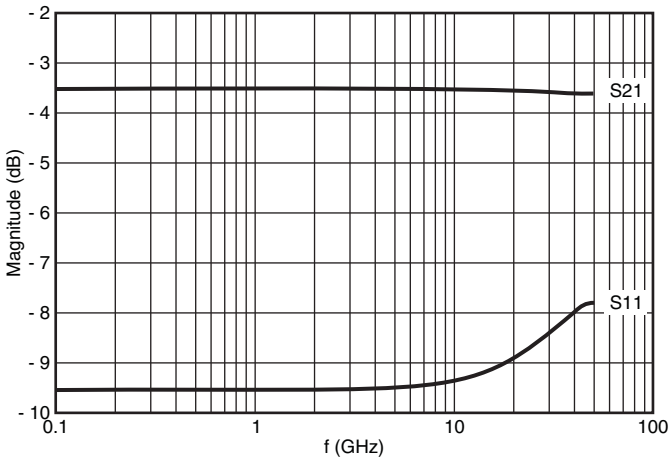
CH02016 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

S-PARAMETER

CH0402 (F and P Terminations)

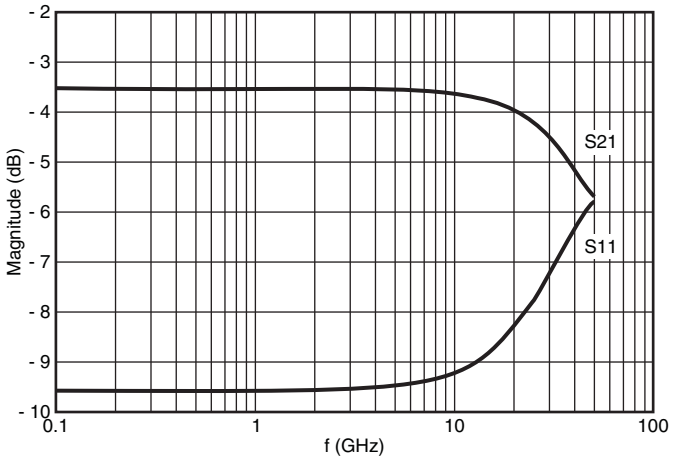


CH0402 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

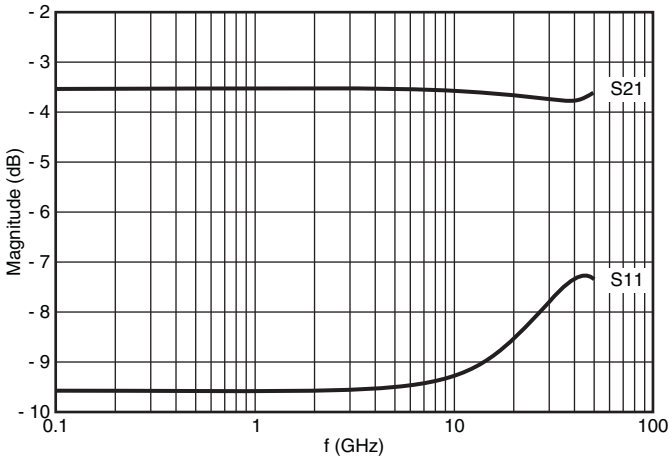


CH0402 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CH0402 (N and G Terminations)

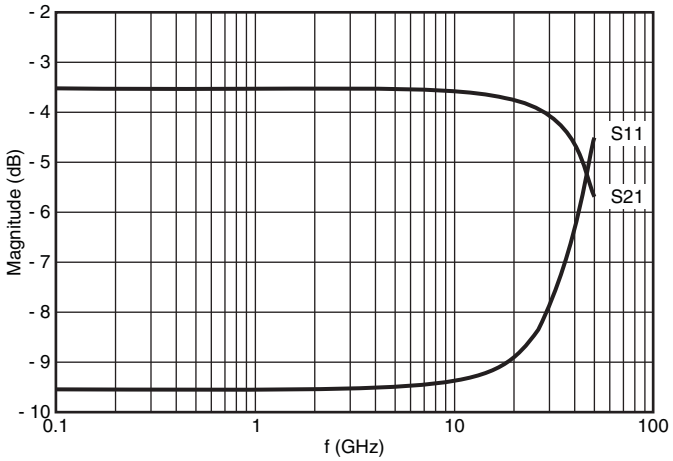


CH0402 wraparound ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)

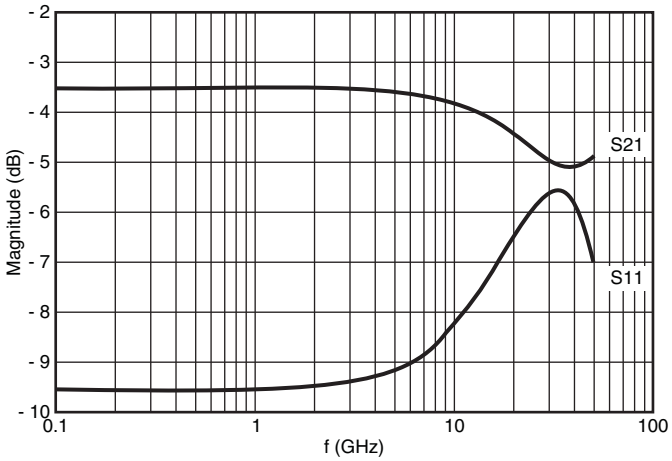


CH0402 wraparound ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

CH0603 (F and P Terminations)



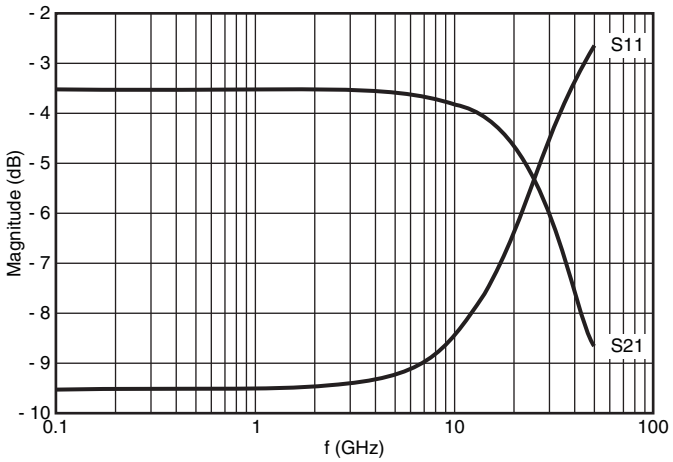
CH0603 flip chip ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



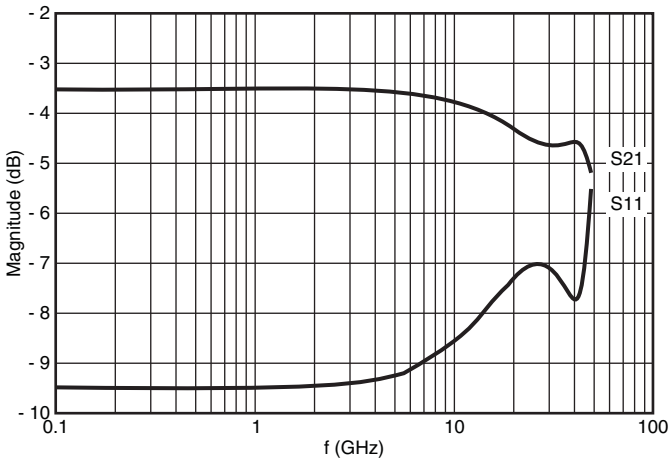
CH0603 flip chip ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)

S-PARAMETER

CH0603 (N and G Terminations)



CH0603 wraparound ($Z_0 = Z_l = Z_s = R = 50\ \Omega$)



CH0603 wraparound ($Z_0 = Z_l = Z_s = R = 100\ \Omega$)