



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

ATP104 — P-Channel Silicon MOSFET General-Purpose Switching Device Applications

Features

- Low ON-resistance
- Slim package
- Halogen free compliance
- Large current
- 4.5V drive
- Protection diode in

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V _{DSS}		-30	V
Gate-to-Source Voltage	V _{GSS}		±20	V
Drain Current (DC)	I _D		-75	A
Drain Current (PW≤10μs)	I _{DP}	PW≤10μs, duty cycle≤1%	-225	A
Allowable Power Dissipation	P _D	Tc=25°C	60	W
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C
Avalanche Energy (Single Pulse) *1	E _{AS}		130	mJ
Avalanche Current *2	I _{AV}		38	A

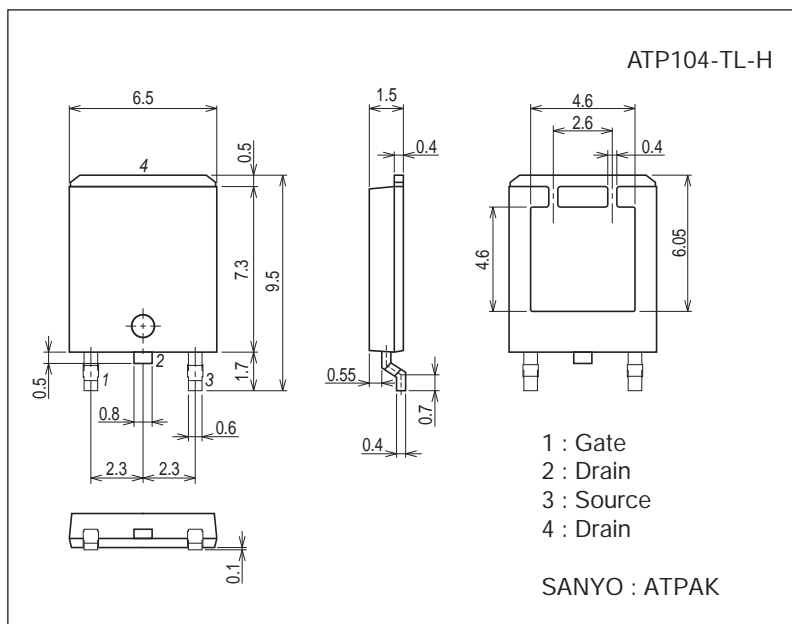
Note : *1 V_{DD}=15V, L=100μH, I_{AV}=38A

*2 L≤100μH, Single pulse

Package Dimensions

unit : mm (typ)

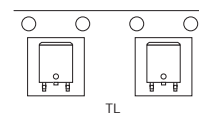
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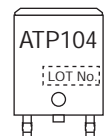
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

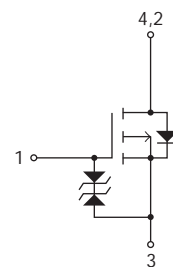
Packing Type: TL



Marking



Electrical Connection

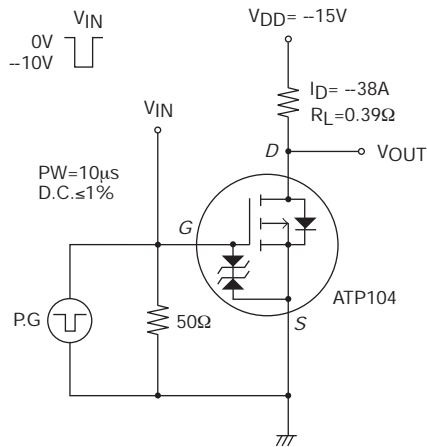


ATP104

Electrical Characteristics at $T_a=25^\circ\text{C}$

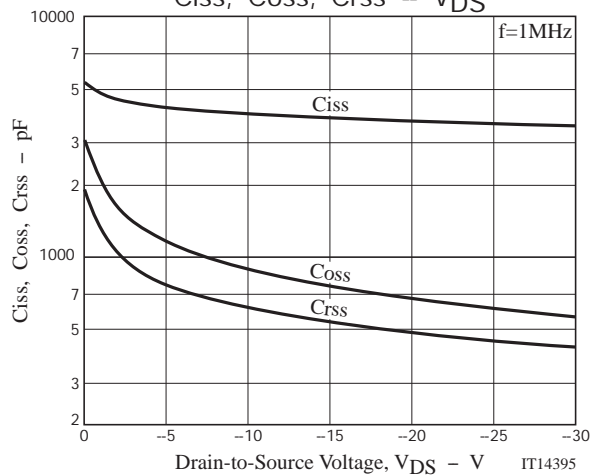
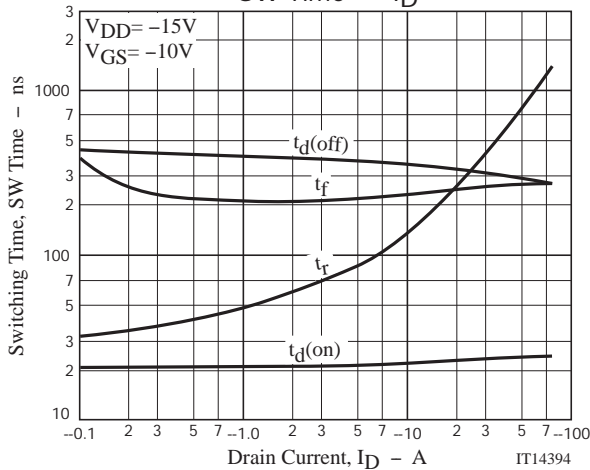
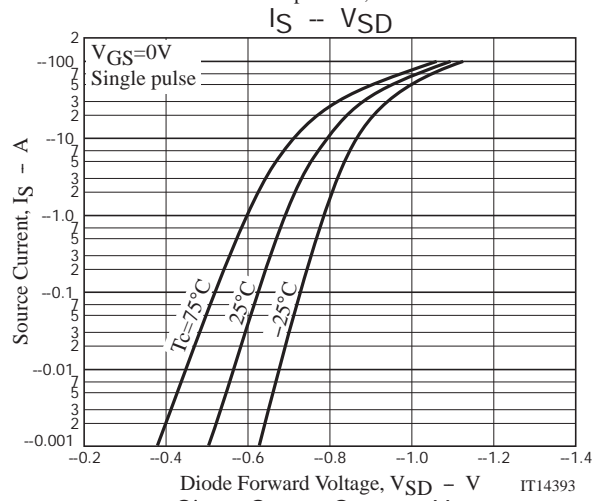
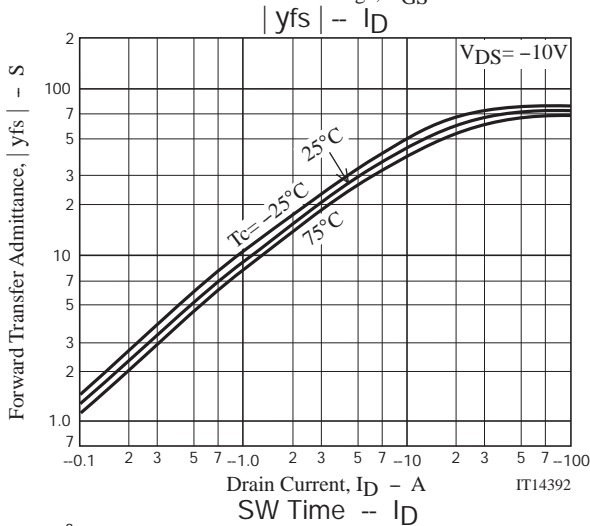
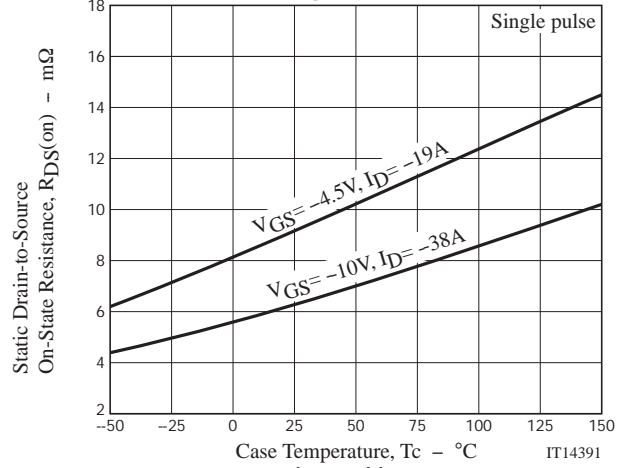
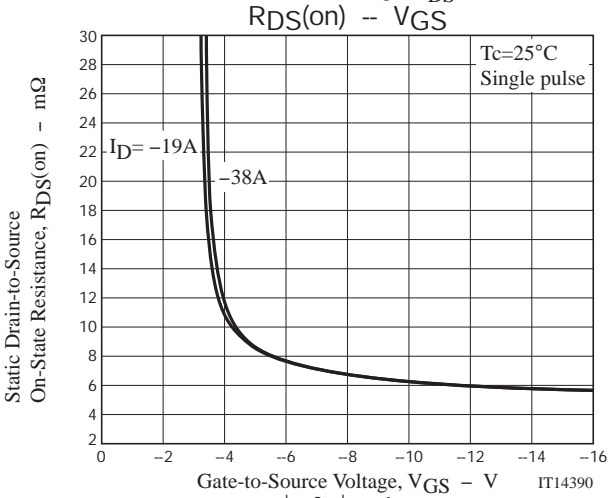
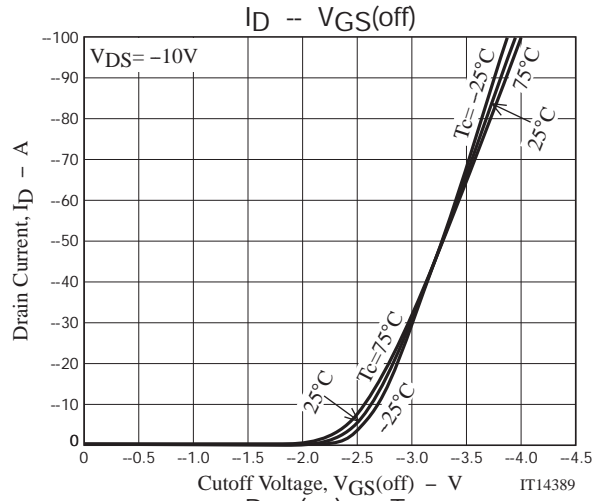
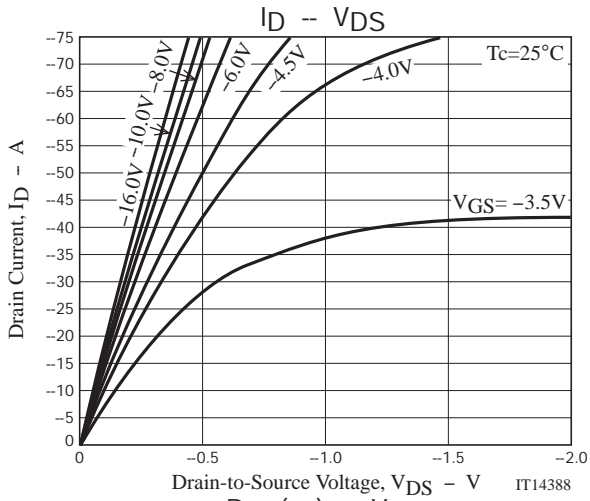
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D=-1\text{mA}, V_{GS}=0\text{V}$	-30			V
Zero-Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30\text{V}, V_{GS}=0\text{V}$			-1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 16\text{V}, V_{DS}=0\text{V}$			± 10	μA
Cutoff Voltage	$V_{GS(off)}$	$V_{DS}=-10\text{V}, I_D=-1\text{mA}$	-1.2		-2.6	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS}=-10\text{V}, I_D=-38\text{A}$		70		S
Static Drain-to-Source On-State Resistance	$R_{DS(on)1}$	$I_D=-38\text{A}, V_{GS}=-10\text{V}$		6.4	8.4	$\text{m}\Omega$
	$R_{DS(on)2}$	$I_D=-19\text{A}, V_{GS}=-4.5\text{V}$		9.6	13.5	$\text{m}\Omega$
Input Capacitance	C_{iss}			3950		pF
Output Capacitance	C_{oss}	$V_{DS}=-10\text{V}, f=1\text{MHz}$		880		pF
Reverse Transfer Capacitance	C_{rss}			610		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit.		24		ns
Rise Time	t_r			520		ns
Turn-OFF Delay Time	$t_{d(off)}$			290		ns
Fall Time	t_f			260		ns
Total Gate Charge	Q_g				76	
Gate-to-Source Charge	Q_{gs}	$V_{DS}=-15\text{V}, V_{GS}=-10\text{V}, I_D=-75\text{A}$		18		nC
Gate-to-Drain "Miller" Charge	Q_{gd}			13		nC
Diode Forward Voltage	V_{SD}	$I_S=-75\text{A}, V_{GS}=0\text{V}$		-1.02	-1.5	V

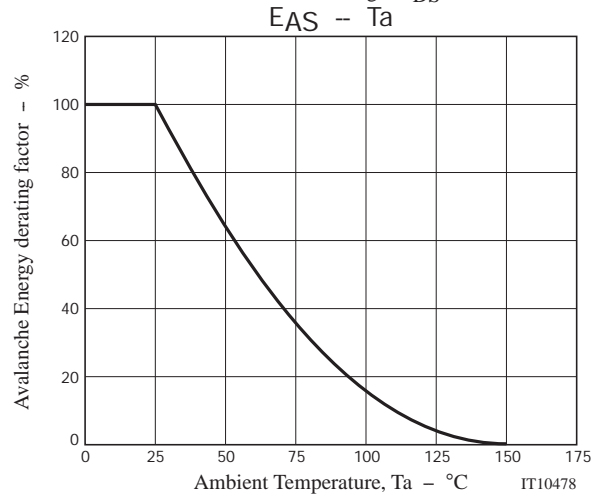
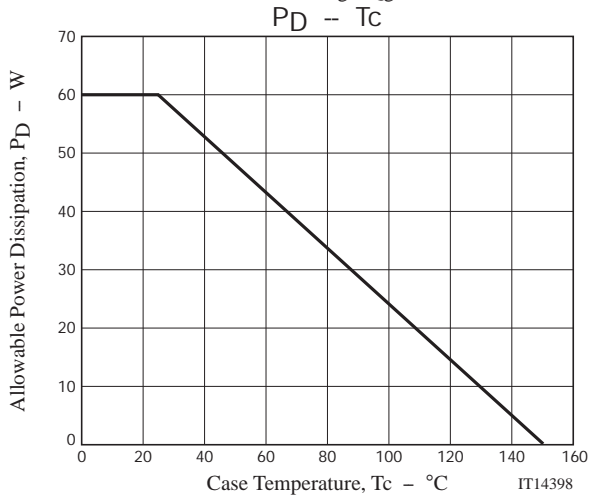
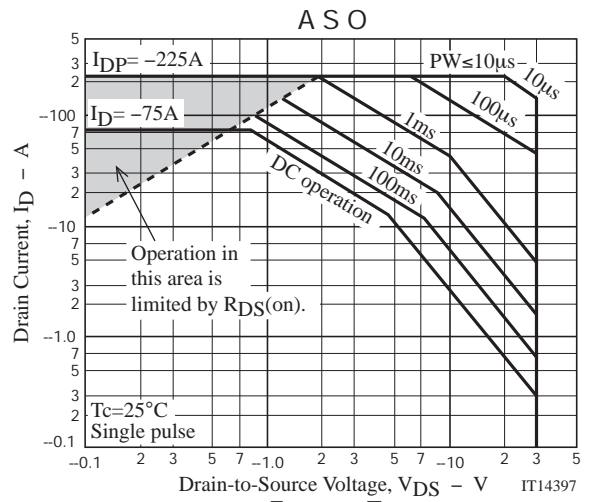
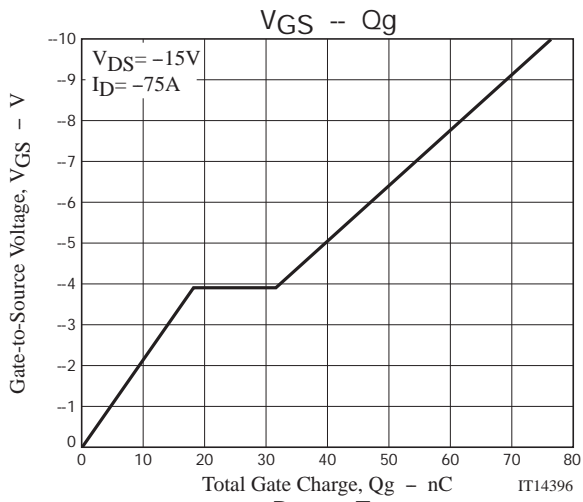
Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
ATP104-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free





Taping Specification

ATP104-TL-H

1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

Packing method



Reel label

Reel label, Inner box label
(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



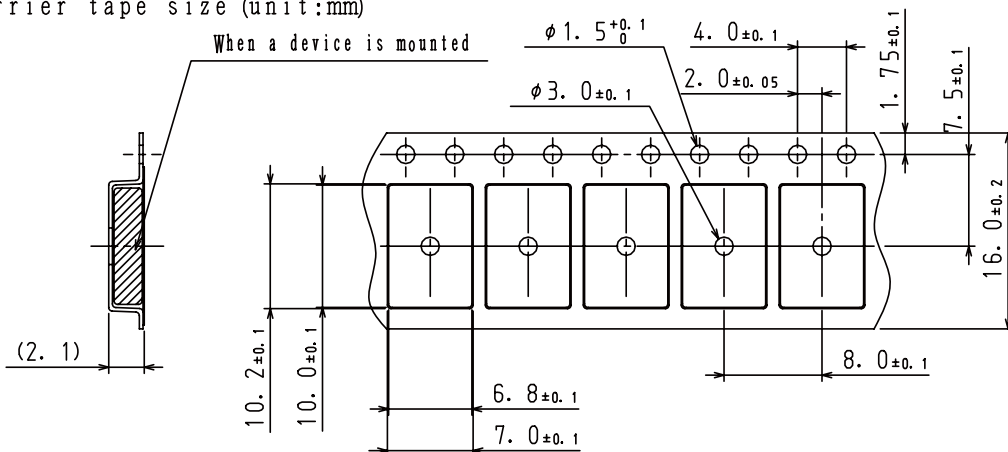
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction Reel



The one electrode terminals on feed hole side...TL

ATP104

Outline Drawing

ATP104-TL-H



Land Pattern Example



Note on usage : Since the ATP104 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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