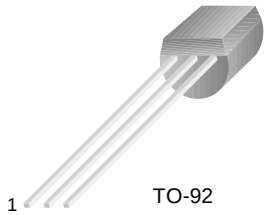
FAIRCHILD
SEMICONDUCTOR®

BC337/338

Switching and Amplifier Applications

- Suitable for AF-Driver stages and low power output stages
- Complement to BC327/BC328



TO-92

1. Collector 2. Base 3. Emitter

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CES}	Collector-Emitter Voltage		
	: BC337	50	V
	: BC338	30	V
V_{CEO}	Collector-Emitter Voltage		
	: BC337	45	V
	: BC338	25	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	800	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C=10mA, I_B=0				
	: BC337		45			V
	: BC338		25			V
BV_{CES}	Collector-Emitter Breakdown Voltage	I_C=0.1mA, V_{BE}=0				
	: BC337		50			V
	: BC338		30			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=0.1mA, I_C=0	5			V
I_{CES}	Collector Cut-off Current					
	: BC337	V_{CE}=45V, I_B=0		2	100	nA
	: BC338	V_{CE}=25V, I_B=0		2	100	nA
h_{FE1}	DC Current Gain	V_{CE}=1V, I_C=100mA	100		630	
h_{FE2}		V_{CE}=1V, I_C=300mA	60			
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C=500mA, I_B=50mA			0.7	V
V_{BE} (on)	Base Emitter On Voltage	V_{CE}=1V, I_C=300mA			1.2	V
f_T	Current Gain Bandwidth Product	V_{CE}=5V, I_C=10mA, f=50MHz		100		MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz		12		pF

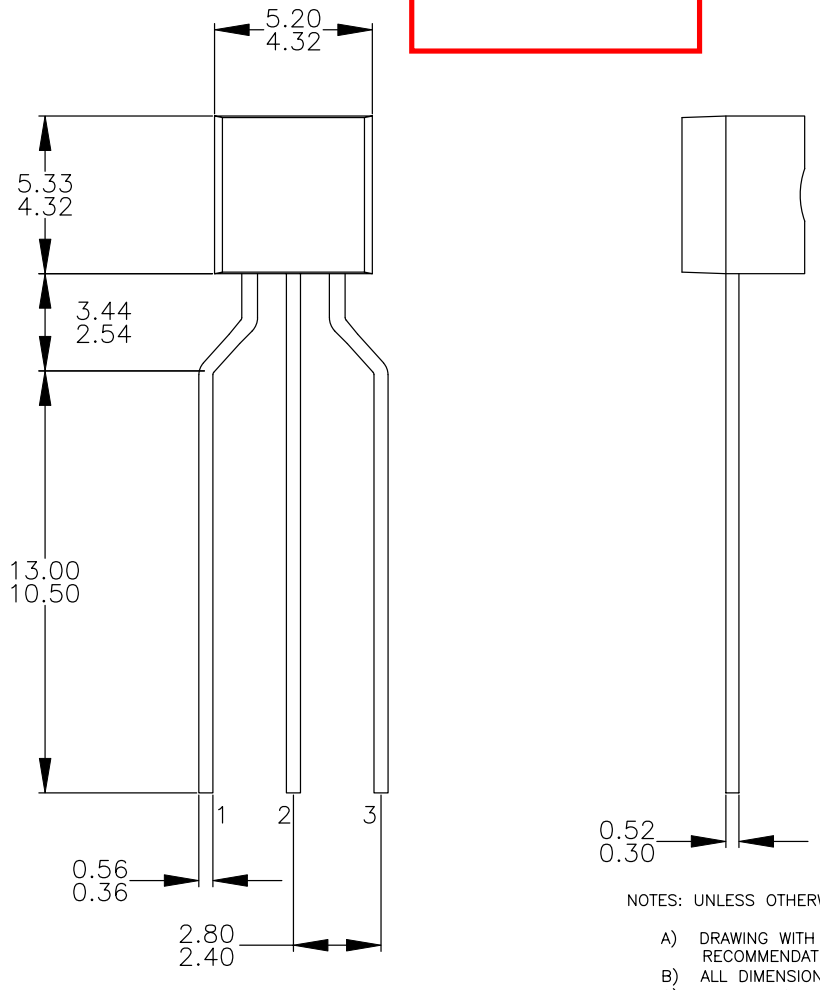
h_{FE} Classification

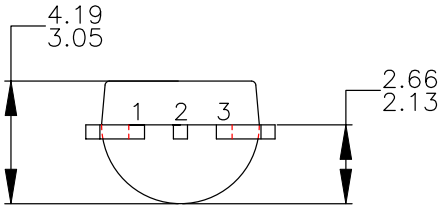
Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60-	100-	170-

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JUL.5'96	JT/CB
2	RDRW FR NATIONAL TEMPLATE TO STD FSC MKT DWG TEMPLATE; CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 2.667 2.413 TO 2.60 2.40; CHG STRAIGHT LD LEN FR 13.97 12.70 TO 13.00 10.50; CHG MOLD BODY HT FR 4.826 4.318 TO 5.33 4.32; CHG MOLD BODY WD FR 4.826 4.318 TO 5.20 4.32; ADD PKG THICKNESS DIM; CHG PKG BOT TO LD SURF DIM FR 3.175 2.413 TO 3.44 2.54; REMOVE LD SURFACE TO MOLDED SURFACE DIM; REMOVE LAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD BENDED LD OVERALL LEN DIM 44; CHG LD WD FR 0.508 0.356 TO 0.56 0.36; CHG LD THICKNESS FR 0.483 0.304 TO 0.52 0.30; ADD NOTES SECTION.	26MAR2008	JC/FSCP

APPROVED
July-14-2008





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03FREV2.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	01APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO-92,MOLDED
0.200 IN LINE SPACING
LD FORM(J61Z OPTION)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT-ZA03F	2

FORMERLY: N/A SHEET : 1 OF 1