Title	***Reference Design Report for a 1.1 W Power Factor Corrected LED Driver (Non-Isolated) Using LinkSwitch™-PL LNK454DG***
Specification	85 VAC – 265 VAC, >0.85 PF Input; 2.5 V – 3.5 V, 366 mA ±10% Output
Application	LED Driver for Candelabra Lamp Replacement
Author	Applications Engineering Department
Document Number	RDR-268
Date	April 4, 2011
Revision	1.2

Summary and Features

- Single stage power factor correction and accurate constant current (CC) output
- Low cost, low component count and small PCB footprint solution
- Superior performance and end user experience
    - Clean monotonic start-up – no output blinking
    - Fast start-up (<300 ms) – no perceptible delay
- Universal input
- Integrated protection and reliability features
    - Output open-circuit protected / output short-circuit protected with auto-recovery
    - Auto-recovering thermal shutdown with large hysteresis protects both components and printed circuit board
    - No damage during brown out conditions
    - Extended pin creepage distance between device DRAIN pin and other pins for reliable operation in high pollution and humid environments
- Surge protected for high reliability
    - Meets IEC ringwave and differential mode surge
- Meets EN55015 conducted EMI
- PF >0.9 at 115 VAC and PF>0.85 at 230 VAC
- %ATHD <15% at 115 VAC and <25% at 230 VAC
- Meets EN61000-3-2 harmonic current requirements

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Important Note:
This board is designed for non-isolated application and the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a non-isolated LED driver (power supply) utilizing a LNK454DG from the LinkSwitch™-PL family of devices. It contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

The RD-268 provides a single constant current output of 366 mA with a nominal LED voltage of 3 V.

The board was optimized to operate over a universal AC input voltage range (85 VAC to 265 VAC, 47 Hz to 63 Hz) but suffers no damage over an input range of 0 VAC to 300 VAC. This increases field reliability and lifetime during line sags and swells.

Key benefits of this design are the very high power factor (>0.85), low THD (<25%) and low harmonic content (a significant challenge due to the low output power) and the ability to fit inside the limited space of a candelabra size lamp base.

High PF is a requirement or desire in many commercial applications, for example large chandeliers in hotel foyers. Here a large number of lamps (25 to >200) are connected in parallel however by using individual lamps that have PFC allows the overall fixture to meet PFC and THD requirements with the large energy savings that come from using LEDs vs. incandescent lamps.

The form factor of the board was chosen to meet the requirements for standard candelabra shaped LED replacement lamps. The output is non-isolated and requires the mechanical design of the enclosure to isolate the output of the supply and the LED load from the user.

Figure 1 – RD-268 (Top View).

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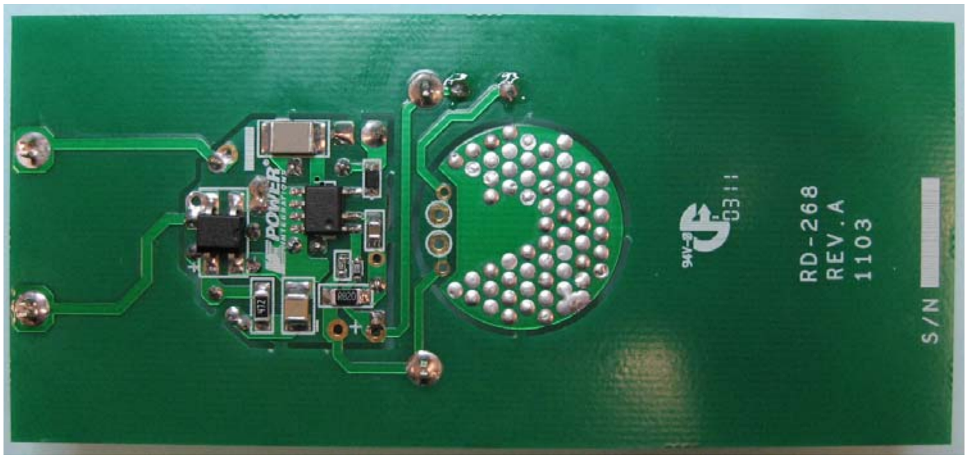

Figure 2 – RD-268 (Bottom View).

The board is provided with break out locations that allow the driver board to be removed and inserted into a candelabra base as show in Figure 3.

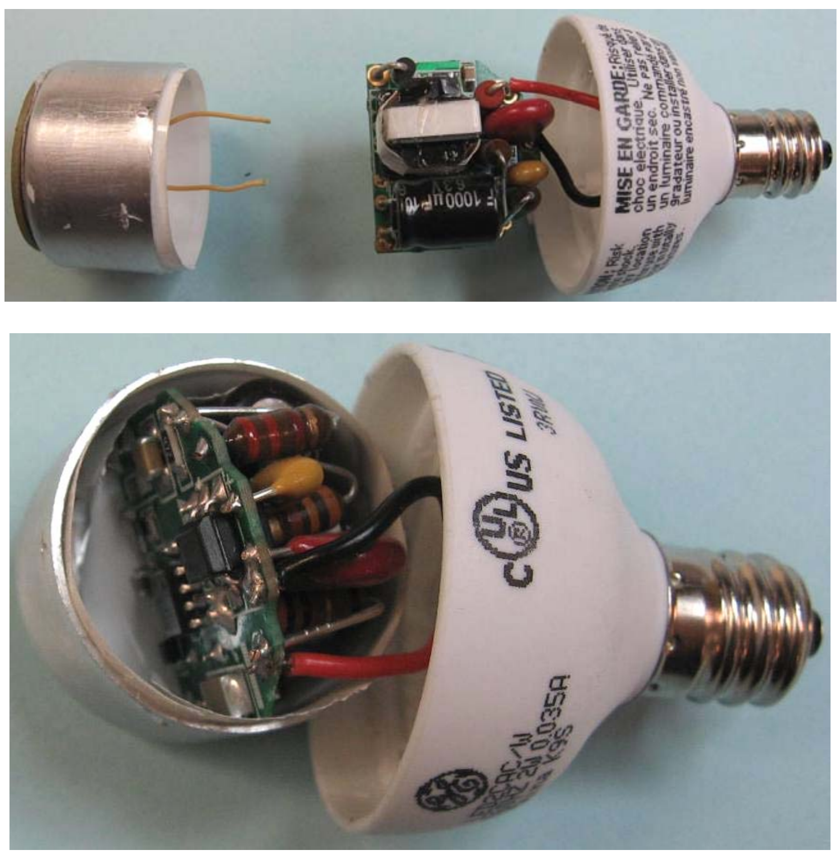

Figure 3 – RD-268 Driver Board Removed and Inserted into a Typical Candelabra Base (Metal Part Forms LED Heat Sink).

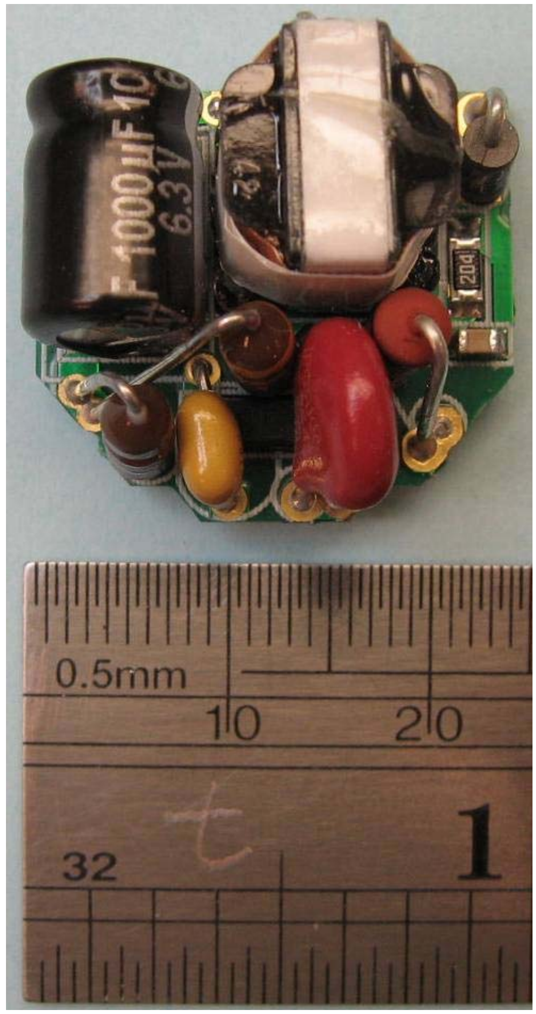

Figure 4 – Size Comparison of RD-268 Used in a Candelabra LED Replacement Lamp.

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2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$V_{IN(NOM)}$		115/230		VAC	Nominal line voltages
	$V_{IN(EXT)}$	85		265	VAC	Normal operating range
	$V_{IN(ND)}$	0		300	VAC	Voltage range over which no damage to the supply shall occur
THD	A_{THD}			25	%	
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output Voltage	V_{OUT}	2.5	3	3.5	V	Thermal results were verified with 3 V LED string
Output Current	$I_{OUT(N)}$	336	366	395	mA	(±8%) Nominal 115 VAC / 230 VAC input, after reaching thermal equilibrium
	$I_{OUT(E)}$	336	366	395	mA	(±10%) Extended 90 VAC-265 VAC Input, -20 °C to 80 °C
Output Power	P_{OUT}		1.1		W	
Efficiency						
	η		50		%	Measured at P_{OUT} 25 °C
Environmental						
Conducted EMI		Meets CISPR22B / EN55015				Mounted into candelabra metal finned enclosure and measured on ground plane (to simulate end application)
Safety		Non-isolated				
Line Surge Differential Mode (L1-L2)				500	V	1.2/50 µs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: N/A
Ring Wave (100 kHz) Differential Mode (L1-L2)				2500	V	200 A short-circuit Series Impedance: Differential Mode: 12.5 Ω Common Mode: N/A
Dimensions						23 x 21 mm
Board Level Ambient Temperature	T_{AMB}	-20		80	°C	Free convection, sea level

3 Schematic

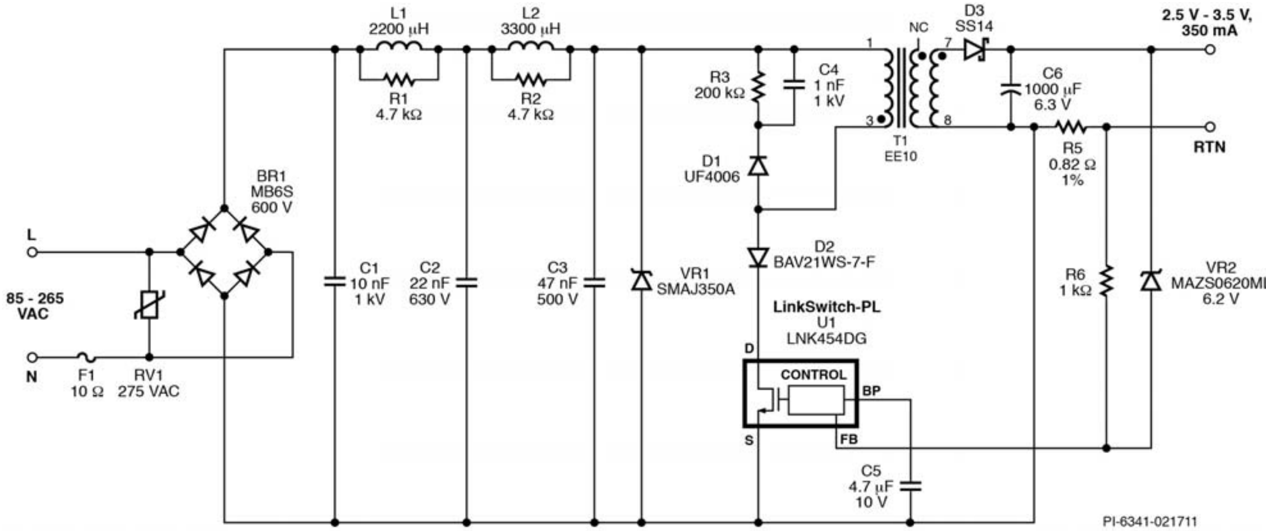

Figure 5 – Schematic.

Notes:

- Replace fusible resistor F1 with a slow blow 2 A fuse for differential line surge withstand levels above 500 V.
- The PCB has optional location for secondary rectifier RC snubber (R4 and C7). Populate if increased radiated EMI margin is required.

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4 Circuit Description

This circuit is configured as non-isolated discontinuous flyback converter designed to drive LED strings at voltages of 2.5 V to 3.5 V with an output current of 366 mA. The driver is guaranteed to operate across a wide range input voltage range and provide high power factor. The circuit meets both line surge and EMI requirements and the low component count allows board dimensions required for LED candelabra bulb replacement applications.

4.1 Input EMI Filtering and Input Rectification

The EMI filter was optimized to meet high power factor and low THD. Fuse (F1) provides protection from component failure that causes excessive input current. A 10 Ω, 2 W rated fusible resistor was selected. Film types (vs. wirewound) are acceptable in this design due to the lower instantaneous resistor dissipation when AC is applied and the small input capacitance charges. For ring wave surge withstand >2 kV or differential surge >500 V a fuse should be substituted as the increased instantaneous dissipation in the resistor causes it to fail open circuit.

Two differential pi (π) filter EMI stages are used with C1, R1, L1 and C2 forming one stage and C2, L2, R2 and C3 the second.

The incoming AC is rectified by BR1 and filtered by C1, C2 and C3. The total effective input capacitance, the sum of C1, C2 and C3, was selected to assure correct zero crossing detection of the AC input by the LinkSwitch-PL device and to meet high power factor and low THD.

Due to the limited input capacitance (to meet PF) RV1 and VR1 are used to limit component voltage stress during line surges.

4.2 LinkSwitch-PL Primary

The LNK454DG device (U1) incorporates the power switching device, oscillator, output constant current control, start-up, and protection functions. The integrated 725 V MOSFET provides extended voltage margin and ensures high reliability even during line surge events. The device is powered from the BYPASS pin via the decoupling capacitor C5. During start-up and normal operation C5 is supplied via the DRAIN pin. This self powered operation simplifies the design and reduces component count.

The rectified and filtered input voltage is applied to one end of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated MOSFET in U1. The leakage inductance generated drain voltage spike is limited by an RCD clamp consisting of D1, R3, and C4.

Diode D2 is used to protect the IC from negative ringing (drain voltage ringing below source voltage) when the MOSFET is off due to the reflected output voltage exceeding the DC bus voltage, the result of minimal input capacitance to give high power factor.

4.3 Output Rectification

The secondary of the transformer is rectified by D3 and filtered by C6. A Schottky barrier type was selected for higher efficiency. As C6 provides energy storage during AC zero crossings its value determines the magnitude of the line frequency output ripple (2 x f_L due to full wave rectification). The value may therefore be adjusted based on the desired output ripple. The value of 1000 μF chosen provided good regulation and acceptable output current ripple. Lower values may be used providing the resultant LED current ripple is acceptable. Provision is made on the PCB for optional snubber components R4 and C7. These damp high frequency ringing and improve conducted and radiated EMI margin.

4.4 Output Feedback

The output current is directly sensed via R5. The average output current (constant current operation) is determined by the value of R5 and the threshold voltage of the FEEDBACK (FB) pin of U1 (290 mV). Disconnected load (output overvoltage protection) is provided by VR2. Under this condition the output voltage is regulated at a value equal to the FB pin voltage and the voltage rating of VR2.

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5 PCB Layout

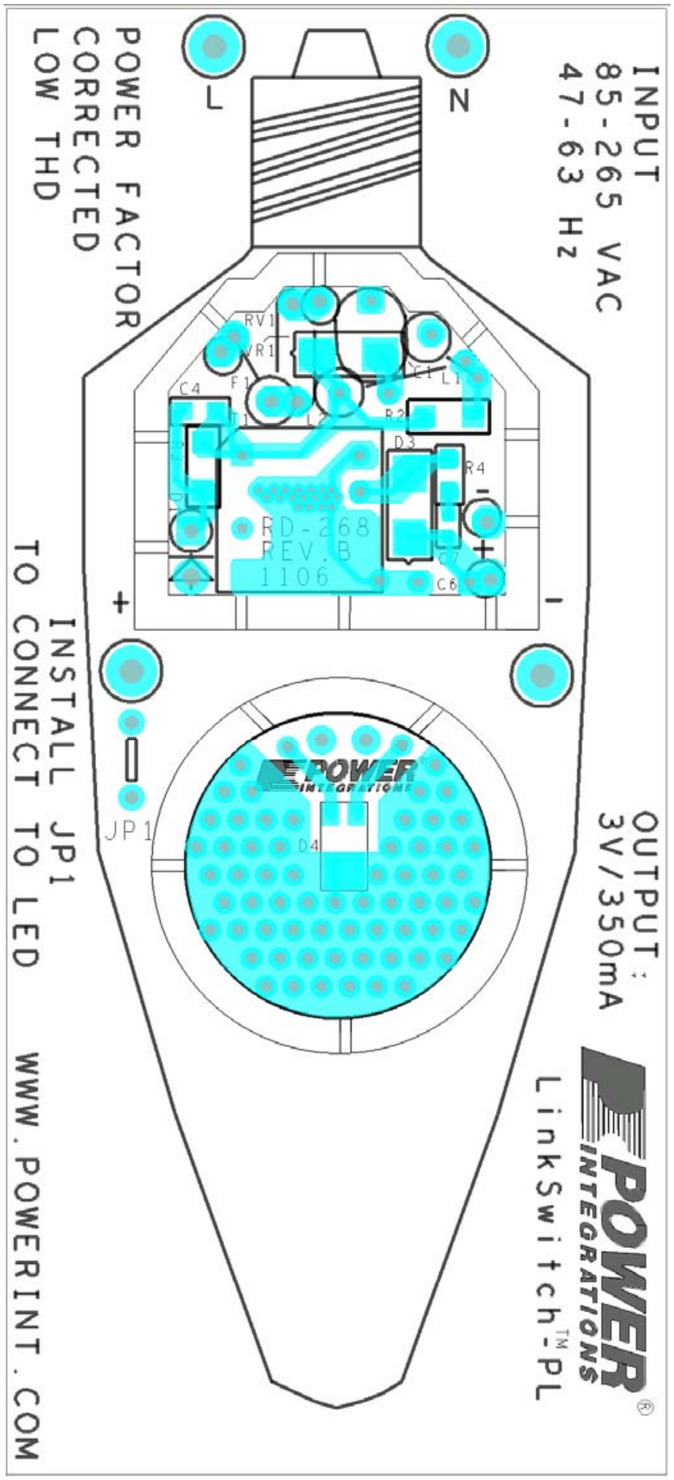

Figure 6 – Top Printed Circuit Layout (3.94” x 1.77”).

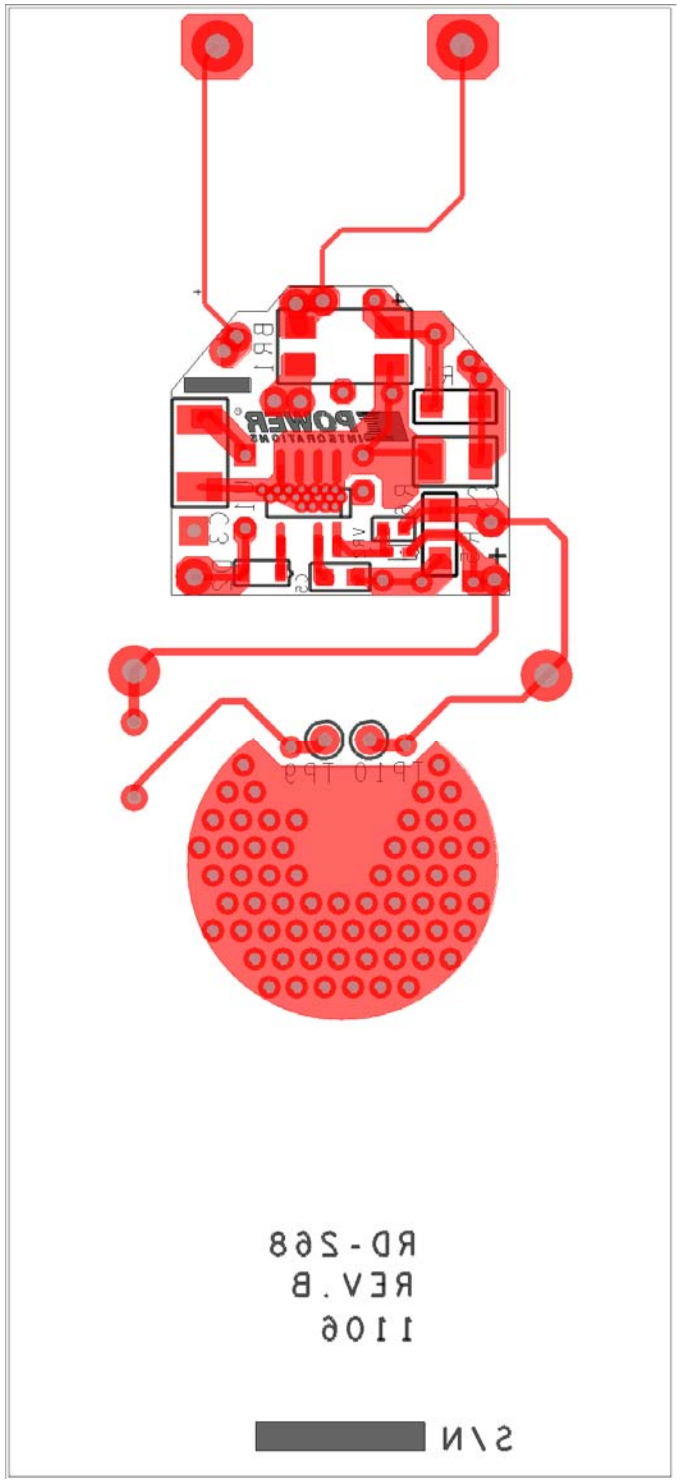

Figure 7 – Bottom Printed Circuit Layout.

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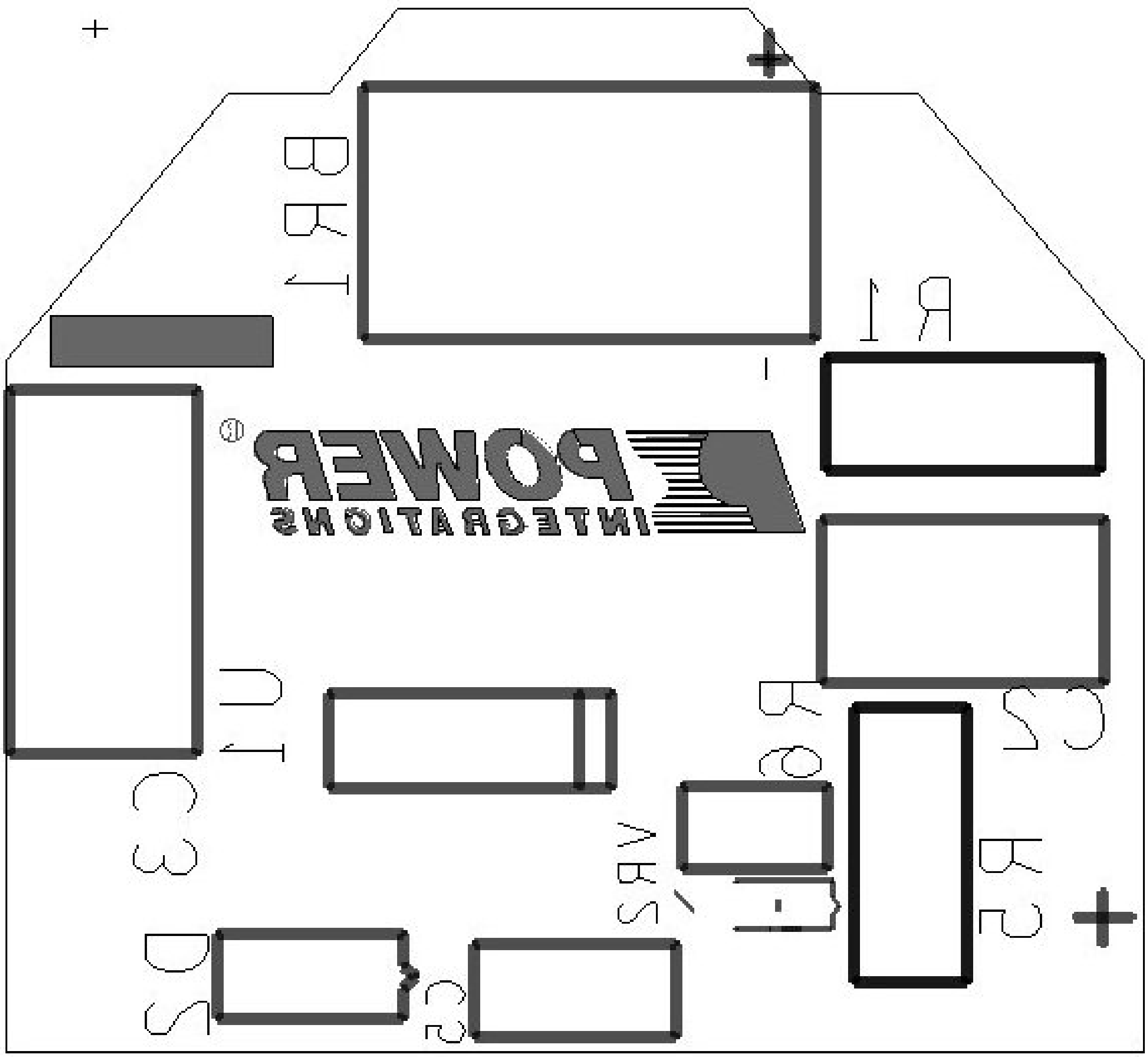

Figure 8 – Bottom Silkscreen.

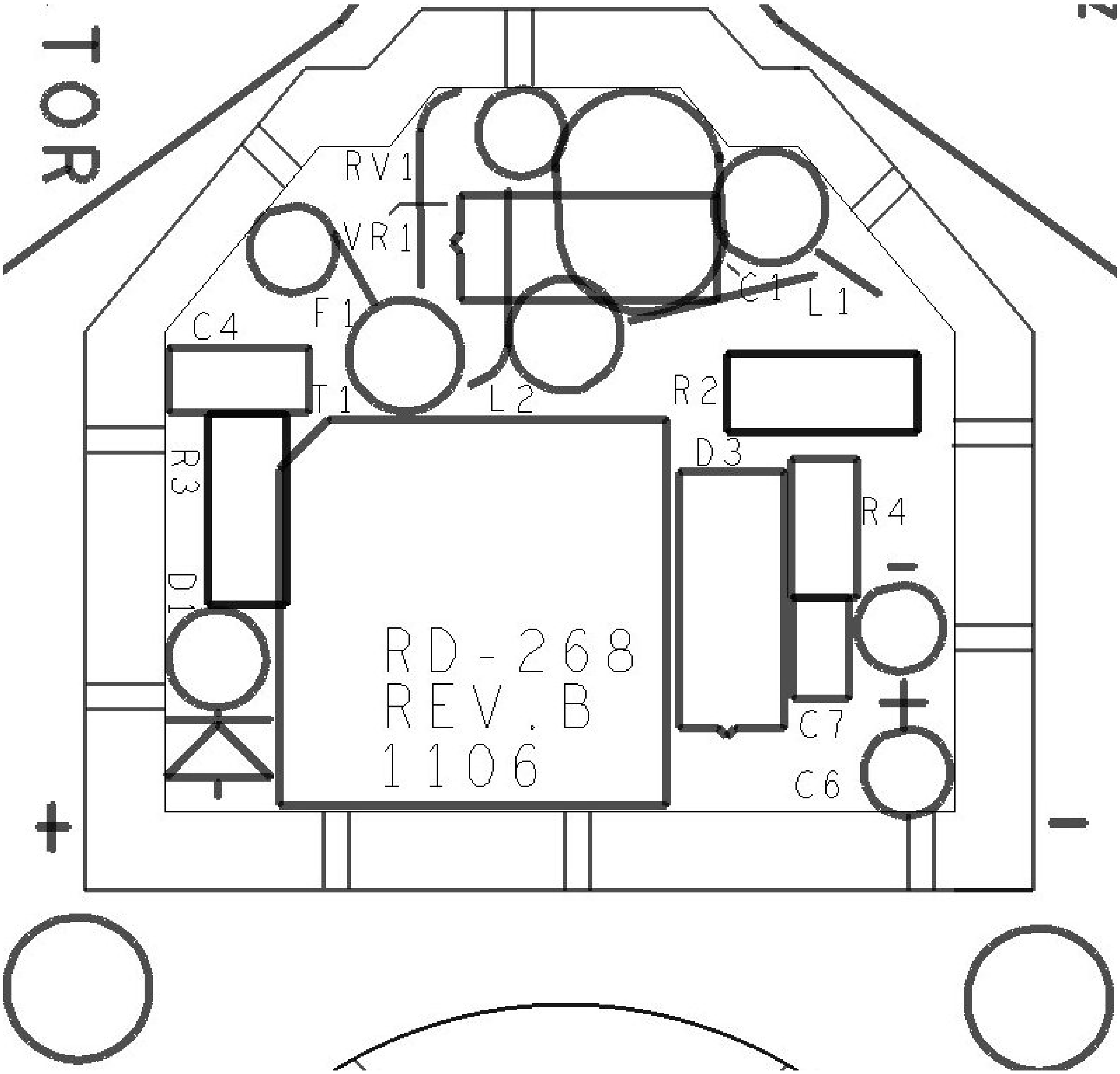

Figure 9 – Top Silkscreen.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Manufacturer P/N	Manufacturer
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	10 nF, 1 kV, Disc Ceramic, X7R	SV01AC103KAR	AVX
3	1	C2	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
4	1	C3	47 nF, 500 V, Ceramic, X7R, 1812	VJ1812Y473KXEAT	Vishay
5	1	C4	1 nF, 1000 V, Ceramic, X7R, 0805	C0805C102KDRACTU	Kemet
6	1	C5	4.7 μF, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
7	1	C6	1000 μF, 6.3 V, Electrolytic, Gen Purpose, (8 x 11.5)	ECA-0JHG102	Panasonic
8	1	D1	800 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4006-E3	Vishay
9	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
10	1	D3	40 V, 1 A, Schottky, DO-214AC	SS14	Vishay
11	1	F1	10 Ω, 5%, 2 W, Metal Film, Fusible	NFR0200001009JR500	Vishay
12	1	L1	2200 μH, 80 mA, 34.7 Ohm, Axial Ferrite Inductor	B78108S1225J	Epcos
13	1	L2	3300 μH, 62 mA, 59.5 Ohm, Axial Ferrite Inductor	B78108S1335J	Epcos
14	2	R1 R2	4.7 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ472V	Panasonic
15	1	R3	200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
16	1	R5	0.82 Ω, 1%, 1/2 W, Thick Film, 1206	RL1632R-R820-F	Susumu
17	1	R6	1 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
18	1	RV1	275 V, 23 J, 7 mm, RADIAL	V275LA4P	Littlefuse
19	1	T1	Bobbin, EE10, Vertical, 8 pins	SNX R1568	Santronics
20	1	U1	LinkSwitch-PL, SO-8C	LNK454DG	Power Integrations
21	1	VR1	350 V, 400 W, 5%, DO214AC (SMA)	SMAJ350A	LittlelFuse
22	1	VR2	6.2 V, 5%, 150 mW, SSMINI2	DZ2S06200L	Panasonic-SSG
23	1	D4	LED, SMD, Luxeon Rebel, Neutral-White	LXML-PWN1-0100	Luxeon
24	2	TP5 TP8	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
25	1	TP6	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
26	1	TP7	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone

7 Transformer Design Spreadsheet

ACDC_LinkSwitch-PL-Flb_101210; Rev.2.0; Copyright Power Integrations 2010	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-PL_Flb_101210; LinkSwitch-PL Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					***Reference Design Report for a 1.2 W Non-Dimmable Power Factor Corrected LED Driver (Non-Isolated) Using LinkSwitch™-PL LNK454DG***
VACMIN	85		85	V	Minimum AC input voltage
VACMAX	265		265	V	Maximum AC input voltage
FL	47		47	Hz	Minimum line frequency
VO	3.50		3.50	V	Nominal Output Voltage
VO_MIN			3.5	V	Minimum output voltage tolerance
VO_MAX			3.50	V	Maximum output voltage tolerance
IO	0.35		0.350	A	Average output current
n			0.7	%/100	Total power supply efficiency
Z			0.5		Loss allocation factor.
Enclosure	Retrofit Lamp		Retrofit Lamp		Enclosure selections determines thermal conditions and maximum power
Dimming Application	No		No		Dimming applications generally require lower flux density to avoid audible noise problems
PO			1.23	W	Average output power
VD			0.5	V	Output diode forward voltage drop
LinkSwitch-PL DESIGN VARIABLES					
Device	LNK454		LNK454		Chose device PO max in Open Frame: 2.46W, PO Max in Retrofit Lamp: 1.54 W.
VOR			104.0	V	Reflected output voltage
Turns Ratio			26.0		Primary to secondary turns ratio
TON			2.61	us	Expected on-time of MOSFET at low line and PO
FSW			122.1	kHz	Expected switching frequency at low line and PO
Duty Cycle			31.9	%	Expected operating duty cycle at low line and PO
VDRAIN			572	V	Estimated worst case drain voltage at VACMAX and VO_MAX
IRMS			0.031	A	Worst case primary RMS current at VO
IPK			0.253	A	Worst case peak primary current at VO
ILIM_MAX			0.325	A	Device peak current
KDP			1.85		Ratio between off-time of switch and reset time of core at VACMIN
LinkSwitch-PL EXTERNAL COMPONENT CALCULATIONS					
RSENSE			0.829	Ohms	Output current sense resistor
Standard RSENSE			0.83	Ohms	Closest 1% value for RSENSE
PSENSE			0.102	W	Power dissipated by RSENSE
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE10		EE10		Core Type
Core Part Number			#N/A		Core Part Number (if Available)
Bobbin Part Number			#N/A		Bobbin Part Number (if available)
AE	12.10		12.10	mm^2	Core Effective Cross Sectional Area
LE	26.10		26.10	mm	Core Effective Path Length
AL	850		850	nH/T^2	Ungapped Core Effective Inductance
BW	6.00		6	mm	Bobbin Physical Winding Width
L	3.00		3		Number of primary winding layers
NS			7	Turns	Number of Secondary Turns
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2.000	mH	Primary Inductance
LP Tolerance			10	%	Tolerance of Primary Inductance
NP			180	Turns	Primary Winding Number of Turns
ALG			62	nH/T^2	Gapped Core Effective Inductance
BM			2325	Gauss	Operating Flux Density
BAC			1163	Gauss	Worst case AC Flux Density for Core Loss

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					Curves (0.5 X Peak to Peak)
BP			3283	Gauss	Calculated Worst Case Peak Flux Density (BP < 3600 G)
LG			0.246	mm	Gap Length (Lg > 0.1 mm)
BWE			18	mm	Effective Bobbin Width
OD			0.10	mm	Maximum Primary Wire Diameter including insulation
INS			0.02	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.08	mm	Bare conductor diameter
AWG			41	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			8	Cmils	Bare conductor effective area in circular mils
CMA			261	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
Primary Current Density (J)			7.71	A/mm^2	Primary Winding Current density (3.8 < J < 9.75 A/mm^2)
SECONDARY DESIGN PARAMETERS					
ISP			6.51	A	Worst Case Peak Secondary Current
ISRMS			1.18	A	Worst Case Secondary RMS current
IO			0.35	A	Output Current
PIVS			17.9	V	Peak Inverse Voltage at VO_MAX on output diode
CMS1			235	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS			26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.41	mm	Minimum Bare Conductor Diameter
ODS			2.57	mm	Maximum Outside Diameter for Wire

8 Transformer Specification

8.1 Electrical Diagram

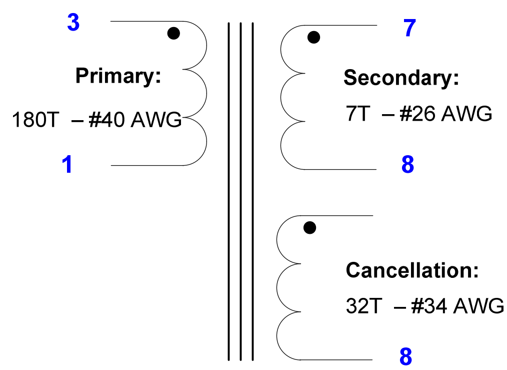

Figure 10 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength		500 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	2 mH ±10%
Resonant Frequency	Pins 1-2, all other windings open	1.2 MHz
Primary Leakage Inductance	Pins 1-2, with pins 7-9 shorted, measured at 100 kHz, 0.4 VRMS	270 μH (Max.)

8.3 Materials

Item	Description
[1]	Core: EE10/PC40
[2]	Bobbin: EE10, Vertical, 8 pins, (4/4)
[3]	Magnet Wire: #34 AWG.
[4]	Magnet Wire: #40 AWG
[5]	Magnet Wire #26 AWG
[6]	Tape: 3M 1298 Polyester Film, 6.5 mm wide.
[7]	Copper Foil Tape, 6.5 mm
[8]	Bus Wire: #24 AWG
[9]	Varnish.

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8.4 Transformer Build Diagram

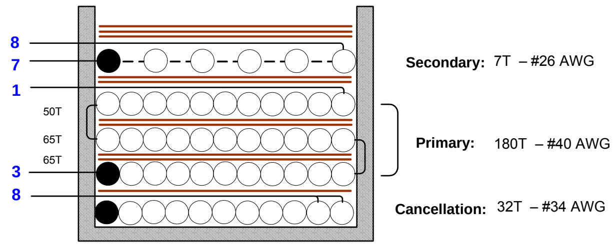
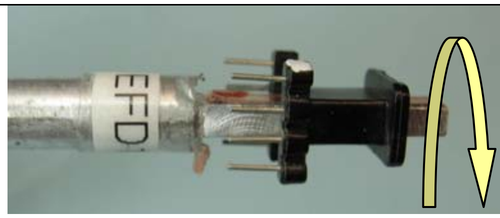
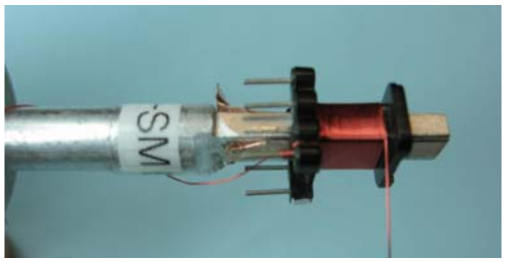
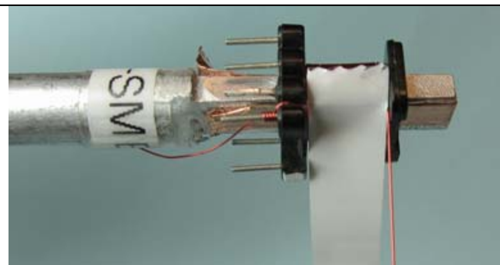
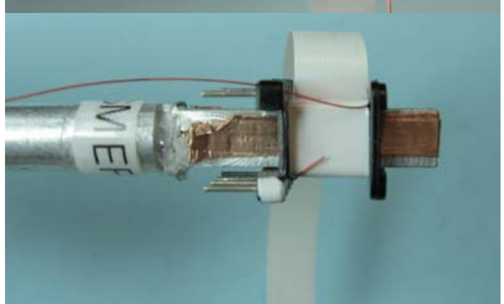
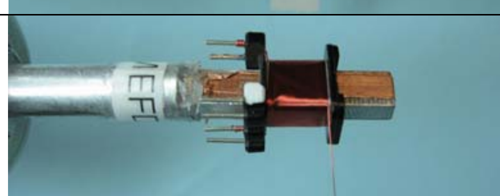
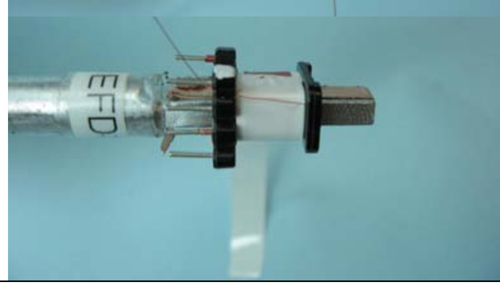


Figure 11 – Transformer Build Diagram.

8.5 Transformer Construction

Winding Preparation	Place bobbin on the mandrel such that primary on the left and secondary on the right. Winding direction is clock-wise direction.
General Note	For the purpose of these instructions, Bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is clockwise.
WD1	Start on a temporary pin on secondary side, wind 32 turns of #34 AWG item [3] from left to right one layer. Finish at pin 8.
Insulation	1 layers of tape item [6] for insulation.
WD2	Start at pin 3, wind 180 turns of #40 AWG [4] wire from left to right three layers 65T + 65T + 50T. Use 2 layers of tape item [6] between each layer. Finish at pin 1.
Insulation	2 layers of tape [6] for insulation.
WD3	Start at pin 7, wind 7 turns of #26 AWG [5] from left to right one layer. Finish at pin 8.
Insulation	3 layers of tape [6] for insulation.
Core Assembly	Grind and assemble core.
Copper Shielding	1 turn of 6.5 mm copper foil tape [7] around assembly and solder the tape seal. Solder #24 AWG buss wire [8] to the copper shield and terminate at pin 8
Finish	2 layers of tape item [6] for insulation over copper shield and varnish using item [9].

8.6 Winding Illustrations

Bobbin Preparation		For the purpose of these instructions, Bobbin is oriented on winder such that pin 1 side is on the left side (see illustration). Winding direction as shown is clockwise.
WD1		Start on a temporary pin on the secondary side and wind 32 turns of #34 AWG item [3] from left to right one layer. Finish at pin 8. Remove wire from temporary pin and cut off excess leaving on a small portion to be terminated under the insulation tape.
Insulation		1 Layers of tape item [6] for insulation.
WD2		Start at pin 3, wind 180 turns of #40 AWG item [4] in 3 layers: 65T + 65T + 50T, place 2 layers of tape item [6] between layers. Finish at pin 1.

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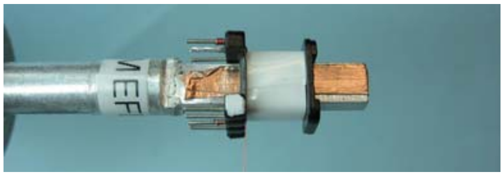
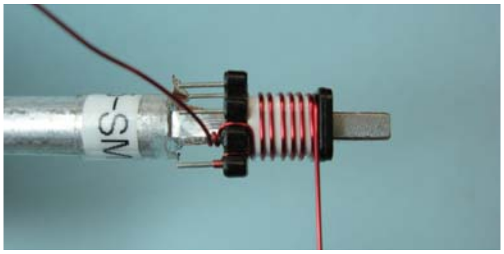
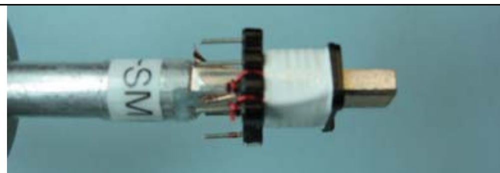
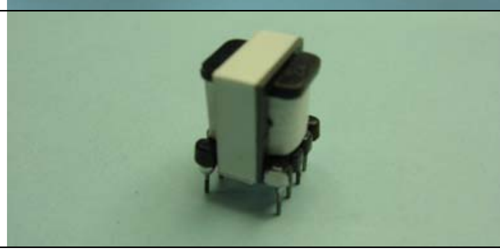
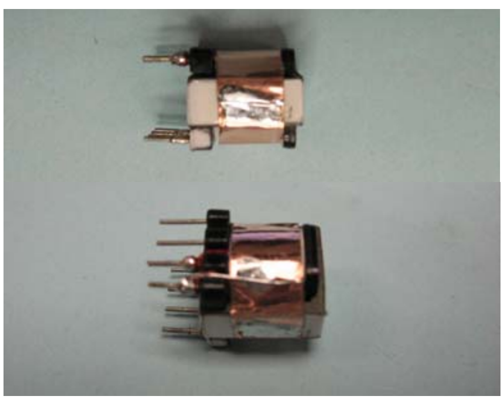
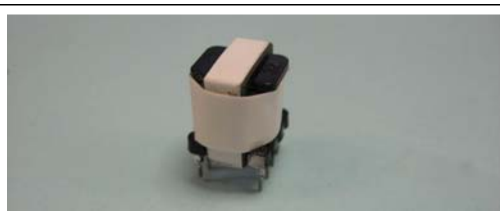
Insulation		2 layers of tape item [6] for insulation.
WD3		Start at pin 7, wind 7 turns of #26 AWG item [5] from left to right one layer. Finish at pin 8.
Insulation		3 layers of tape item [6] for insulation.
Core Assembly		Grind core halves to get 2 mH, between cores, refer to section 1.3 for electrical specifications, and assemble with tape.
Copper Shielding		Wind 1 turn of 6.5 mm copper foil tape item [7] around the core assembly. Solder the tape seal. Solder #24 AWG buss wire item [8] to the copper shield and terminate at pin 8
Finish		Add 2 Layers of tape item [6] over copper shield and varnish with item [9].

Figure 12 – Transformer Construction.

9 Performance Data

All measurements performed at room temperature otherwise specified.

9.1 Active Mode Efficiency

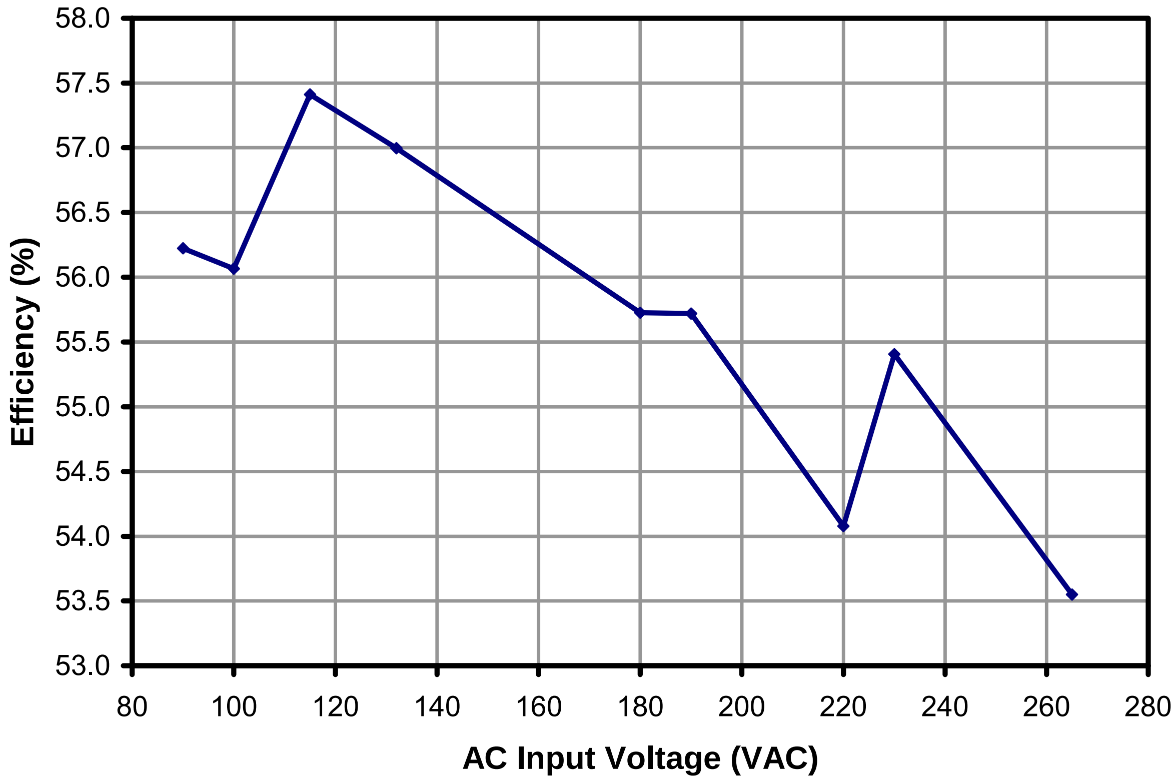


Figure 13 – Nominal Load (3 V, 366 mA) Efficiency with Respect to Line Input Voltage.

Input		Input Measurement				Load Measurement			Efficiency (%)
VAC (V_{RMS})	Freq (Hz)	I_{IN} (mA_{RMS})	P_{IN} (W)	PF	%THD	V_O (V_{DC})	I_O (mA_{DC})	Po (W)	
90	47	21.61	1.93	0.99	6.15	2.86	371.80	1.08	56.22
100	60	19.48	1.92	0.98	8.04	2.85	370.50	1.07	56.07
115	60	17.40	1.95	0.97	10.52	2.86	385.30	1.12	57.41
132	60	14.43	1.82	0.95	14.58	2.85	358.10	1.04	57.00
180	50	11.80	1.98	0.93	15.09	2.85	379.00	1.10	55.73
190	50	10.90	1.90	0.92	17.51	2.85	365.60	1.06	55.72
220	50	10.03	2.00	0.90	20.26	2.85	372.40	1.08	54.08
230	50	9.68	2.01	0.90	21.1	2.85	383.30	1.11	55.41
265	50	9.02	2.04	0.85	25.59	2.85	376.30	1.09	53.55

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9.2 *Harmonics*

Meets EN61000-3-2 Harmonics content limits.

Order	Input Current Harmonics (mA)				EN 61000-3-2
	Measured		Limits		
	115 V	230 V	115 V	230 V	
1	17.71	9.60			
3	0.43	0.84	13.5728	6.9360	P
5	1.18	1.02	7.5848	3.8760	P
7	0.61	0.87	3.9920	2.0400	P
9	0.51	0.64	1.9960	1.0200	P
11	0.49	0.43	1.3972	0.7140	P
13	0.54	0.34	1.1822	0.6042	P
15	0.33	0.36	1.0246	0.5236	P
17	0.16	0.36	0.9041	0.4620	P
19	0.17	0.33	0.8089	0.4134	P
21	0.18	0.26	0.7319	0.3740	P
23	0.27	0.24	0.6682	0.3415	P
25	0.18	0.24	0.6148	0.3142	P
27	0.17	0.23	0.5692	0.2909	P
29	0.12	0.21	0.5300	0.2708	P
31	0.17	0.21	0.4958	0.2534	P
33	0.12	0.18	0.4657	0.2380	P
35	0.15	0.17	0.4391	0.2244	P
37	0.20	0.17	0.4154	0.2123	P
39	0.14	0.15	0.3941	0.2014	P
41	0.07	0.13			
43	0.10	0.14			
45	0.07	0.12			
47	0.04	0.12			
49	0.08	0.16			

P: Pass

Table 1 – Measured Harmonic Input Current.

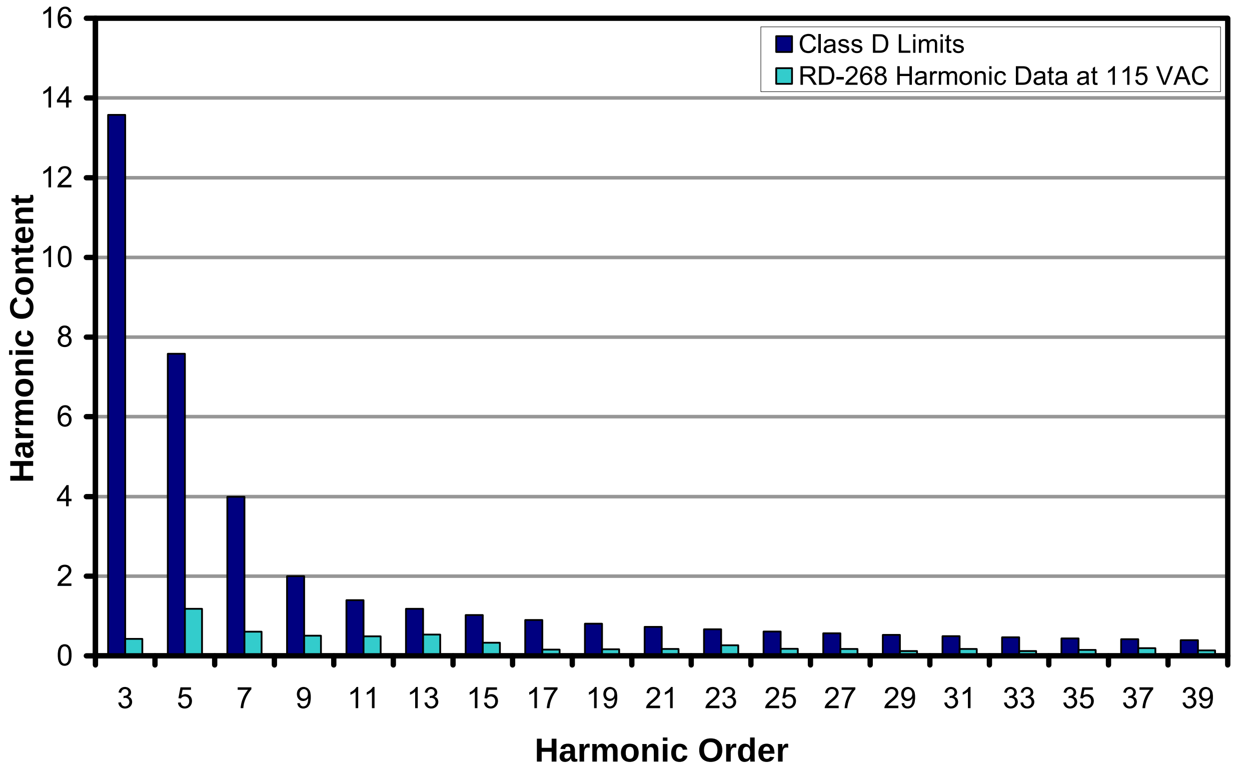

Figure 14 – 115 V UUT Harmonic Content**.**

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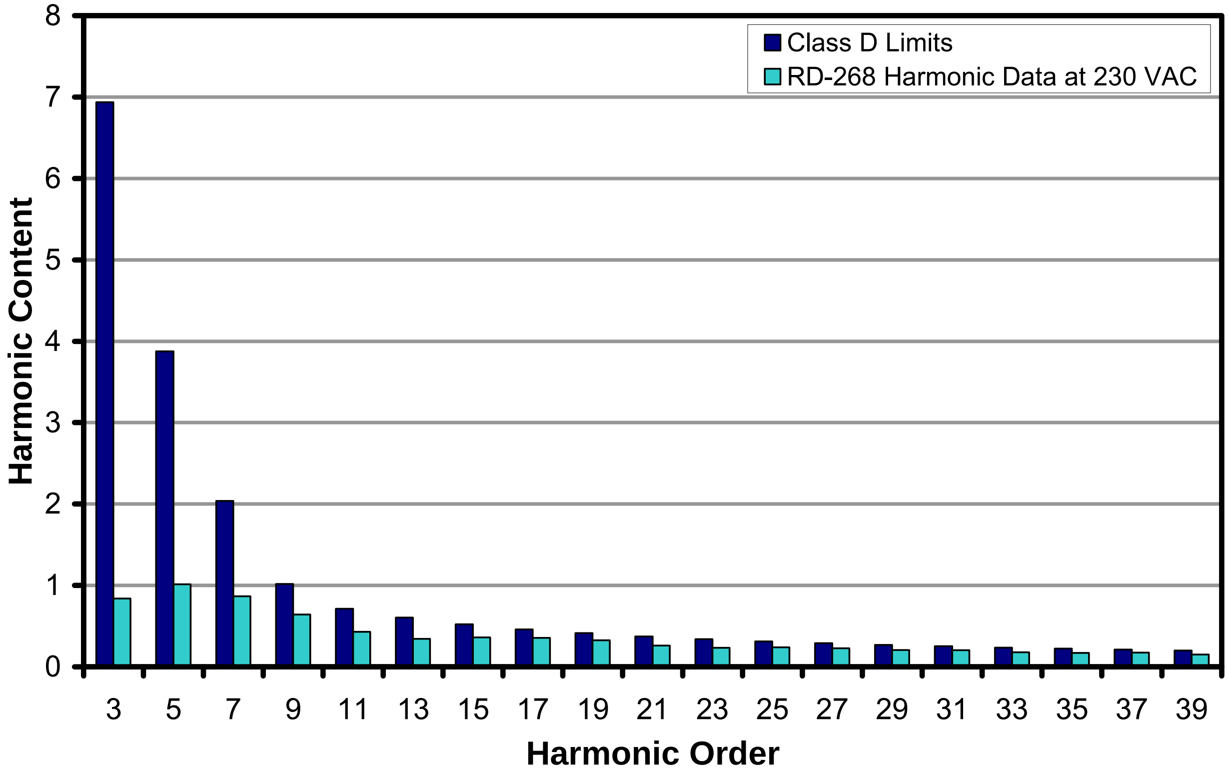

Figure 15 – 230 V UUT Harmonic Content.

9.3 Power Factor

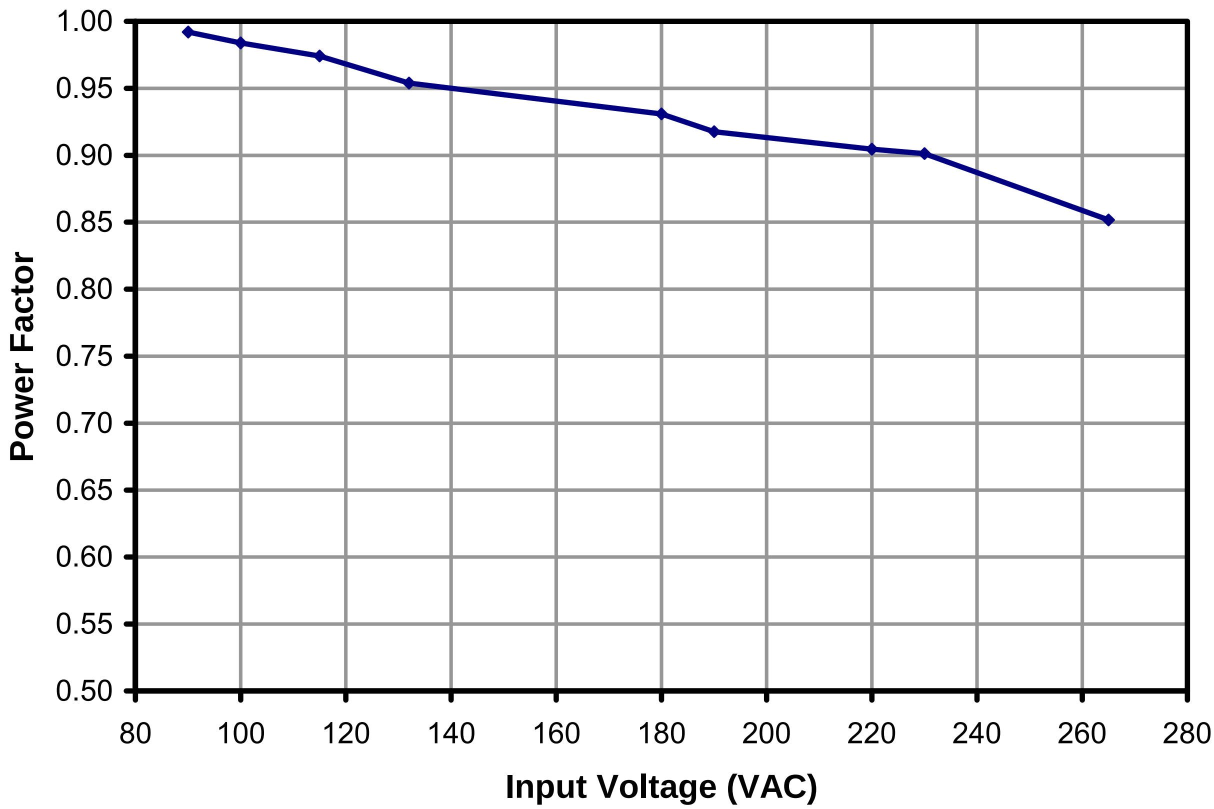

Figure 16 – Power Factor with Respect to AC Input at Full Load.

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9.4 Line Regulation

Output current vs. line voltage measurements were taken by directly applying the AC input at the line voltages indicated, removing the AC power, adjusting the AC voltage (via an AC source) and reapplying AC at the new voltage. This approach was taken to ensure repeatability as variations in the operating state of the LinkSwitch-PL can occur when the AC input voltage is swept.

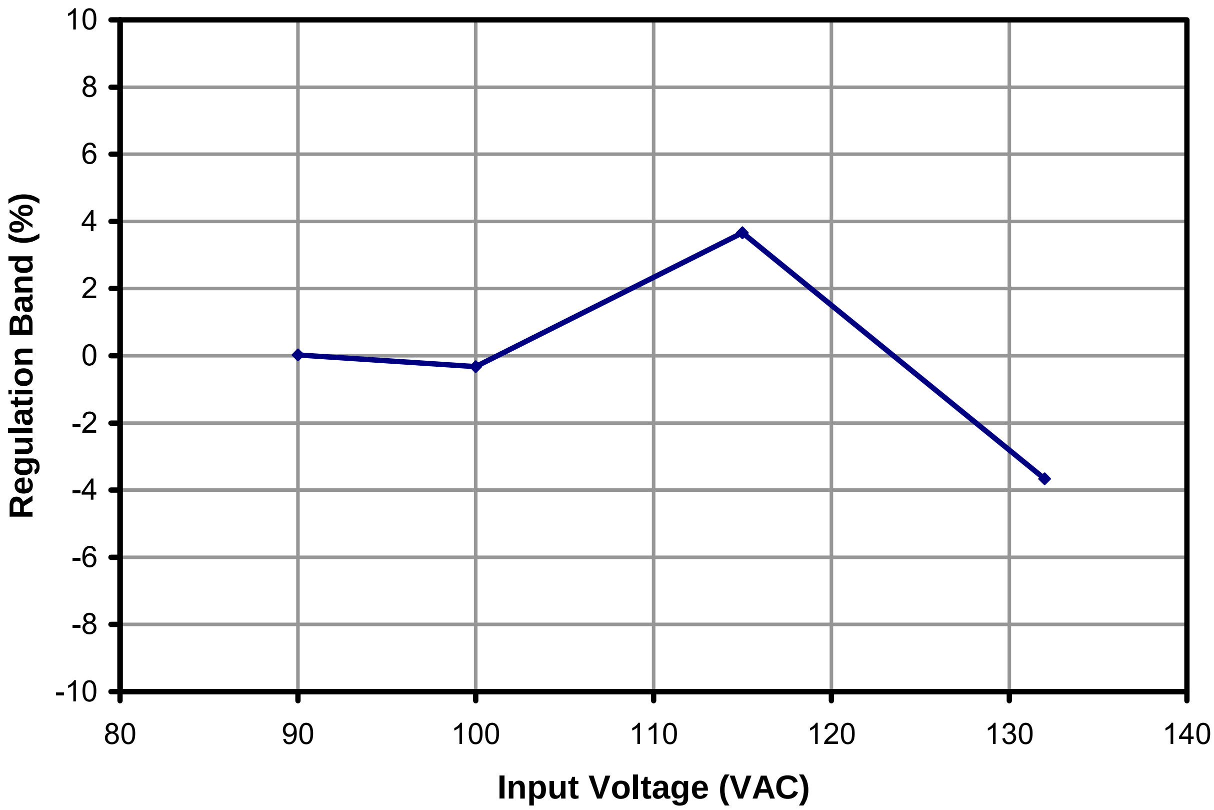

Figure 17 – Low Line Regulation Band, Room Temperature, Full Load.

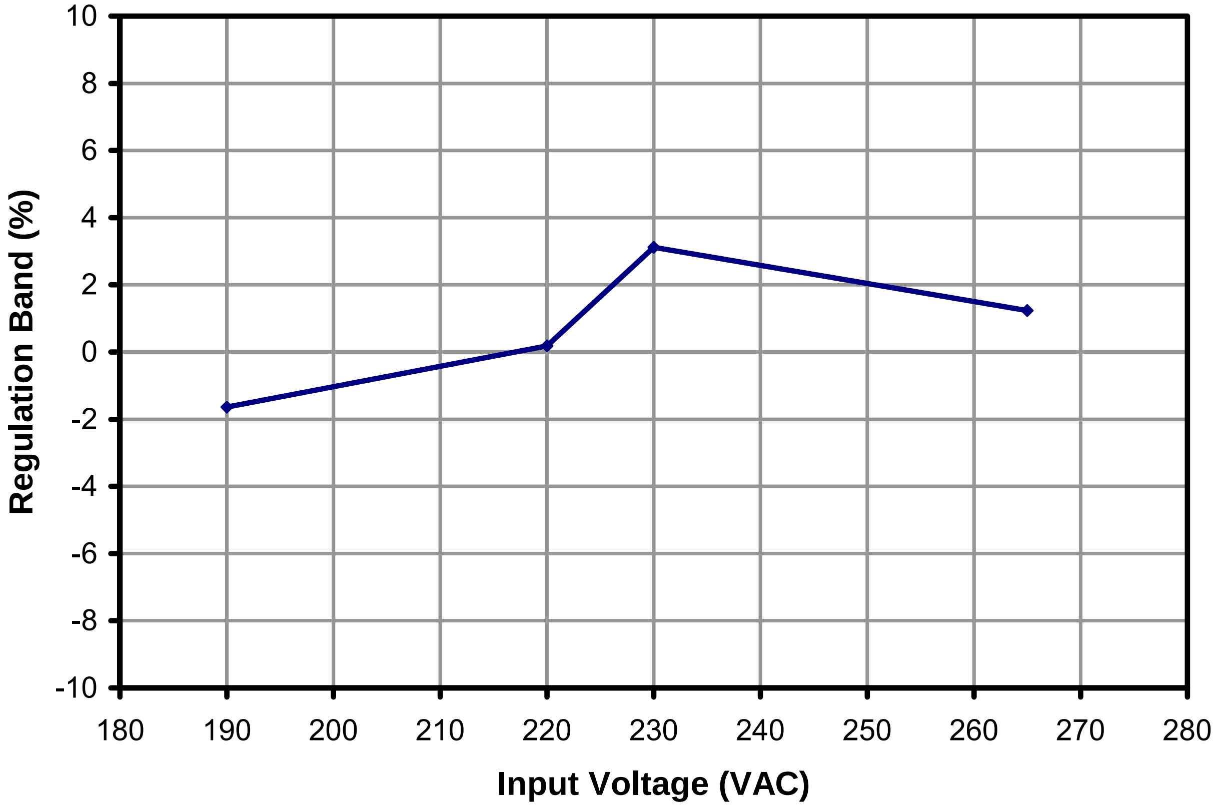

Figure 18 – High Line Regulation Band, Room Temperature, Full Load.

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10 Thermal Performance

10.1 Thermal Set-up

The unit was verified inside a cardboard box to avoid the influence of circulating air inside the thermal chamber.

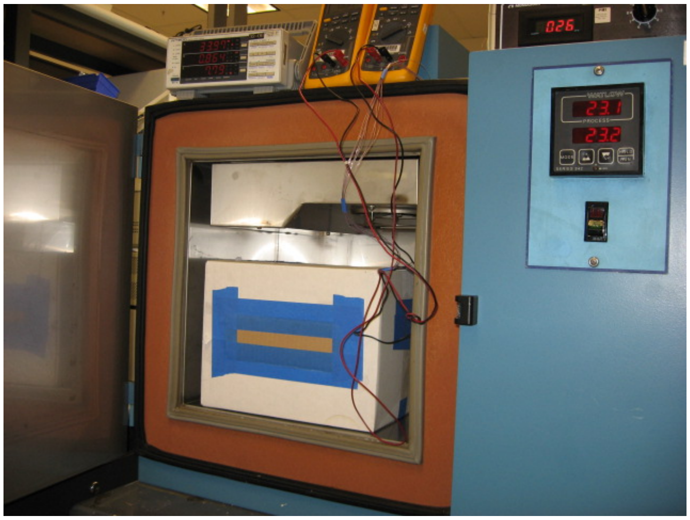

Figure 19 – Thermal Chamber Set-up Showing Box Used to Prevent Airflow Over UUT.

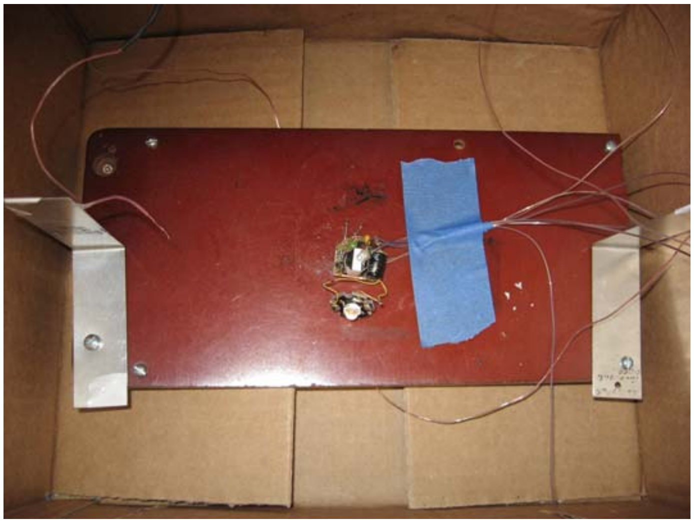

Figure 20 – UUT Within Box.

10.2 Equipment Used

Chamber: Tenney Environmental Chamber
Model No: TJR-17 942

AC Source: Chroma Programmable AC Source
Model No: 6415

Wattmeter: Yokogawa Power Meter
Model No: WT2000

Data Logger: Monogram
SN:1290492

10.3 Thermal Result

Load: 3 V / 366 mA LED load.

10.3.1 Startup at Low Temperatures

Unit was soaked at -30°C with no AC applied. AC was then applied and supply correctly started up and operated.

10.3.2 Operation at Maximum Ambient

Operation at an ambient of 80°C was verified. This simulates operation inside sealed candelabra enclosure.

Component	90 V / 50 Hz Input	265 / 63 Hz Input
	Device Temperature (ºC)	Device Temperature (ºC)
Ambient (ºC)	80	80
Bridge Pin (BR1)	97	102
Input Inductor (L1)	96	100
LNK454DG SOURCE Pin (U1)	106	109
Transformer Core (T1)	100	105
Output Diode (D3)	110	109
Output Case Capacitor (C6)	98	103

Table 2 – Thermal Measurement at 80ºC Ambient (Board Temperature).

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10.4 Thermal Scan

10.4.1 Load: 3 V / 366 mA

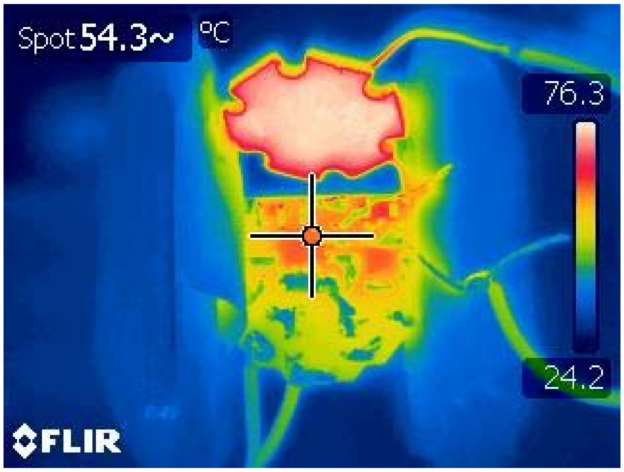

Figure 21 – LNK454DG Device Temperature at 25ºC Open Air.

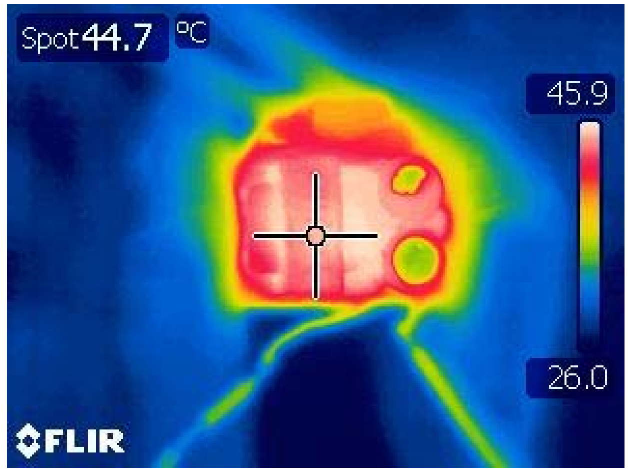

Figure 22 – Transformer (T1) Temperature at 25ºC Open Air.

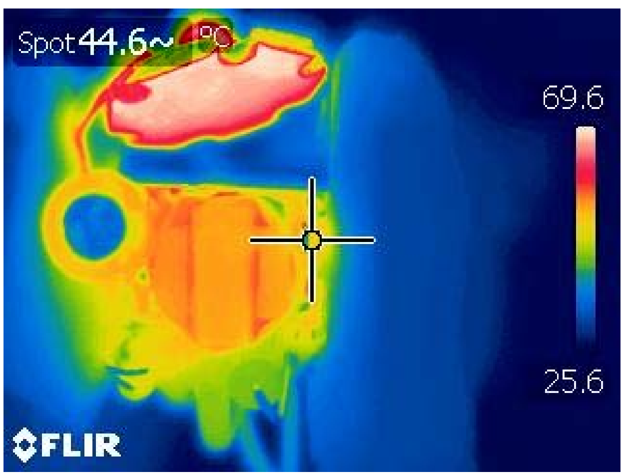

Figure 23 – Clamp Diode (D1) Temperature at 25ºC Open Air.

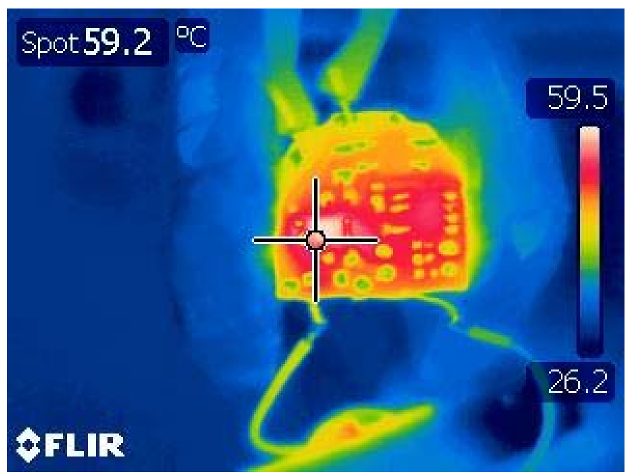

Figure 24 – Output Diode D3 Temperature at 25ºC Open Air.

11 Waveforms

11.1 Drain Voltage and Current

11.1.1 Normal Steady-State Operation

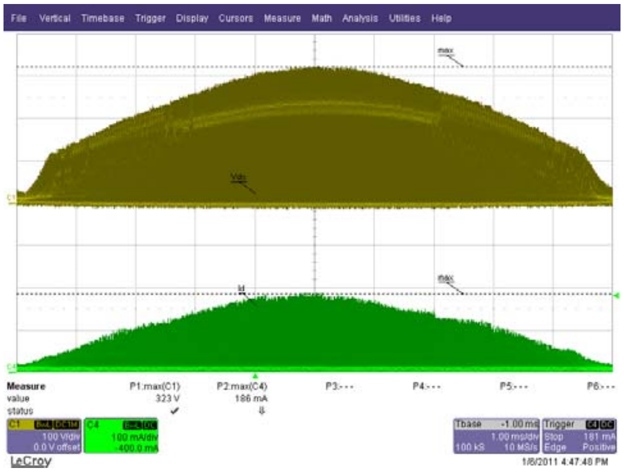

Figure 25 – 90 VAC / 50 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 100 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.1 A / div.

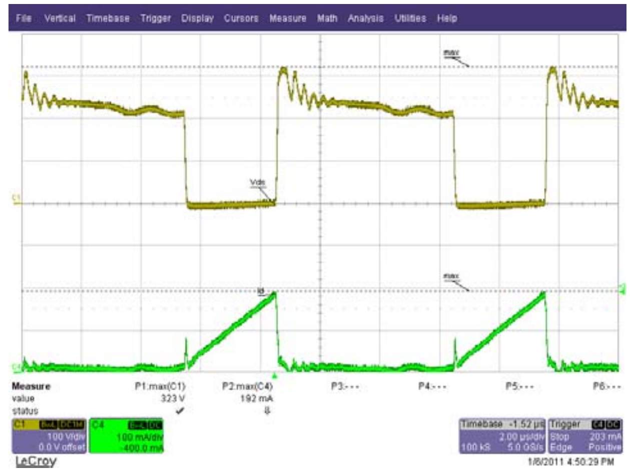

Figure 26 – 90 VAC / 50 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 100 V / div., 2 µs / div.
Lower: I_{DRAIN}, 0.1 A / div.

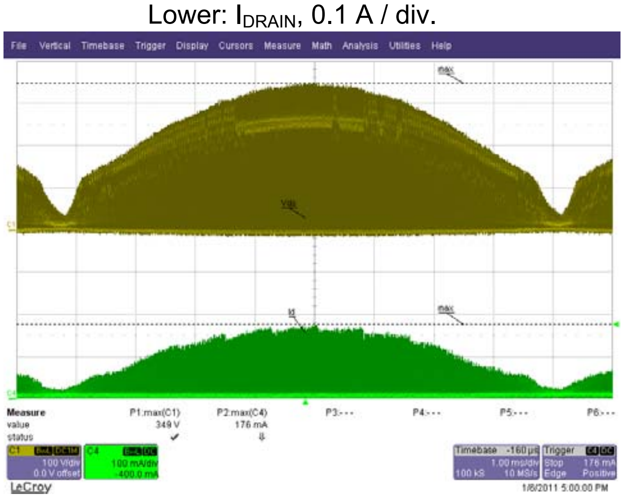

Figure 27 – 115 VAC / 60 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 100 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.1 A / div.

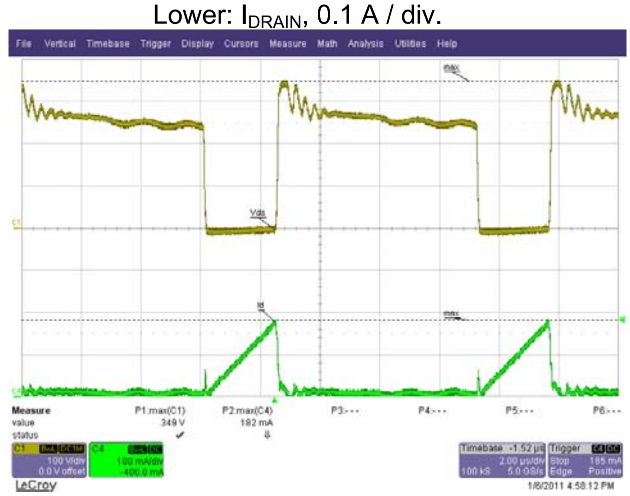

Figure 28 – 115 VAC / 60 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 100 V / div., 2 µs / div.
Lower: I_{DRAIN}, 0.1 A / div.

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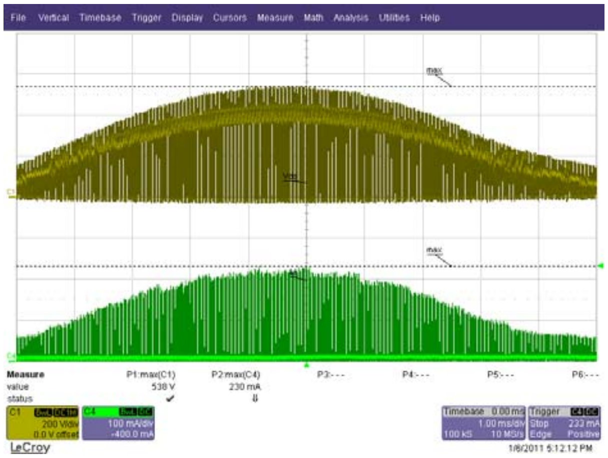

Figure 29 – 230 VAC / 50 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 200 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.1 A / div.

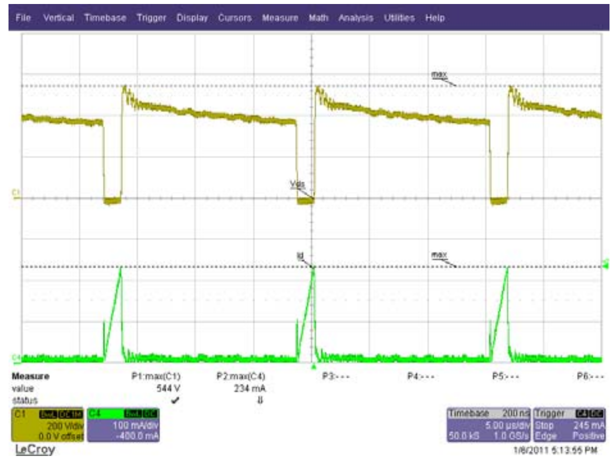

Figure 30 – 230 VAC / 50 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 200 V / div., 5 μs / div.
Lower: I_{DRAIN}, 0.1 A / div.

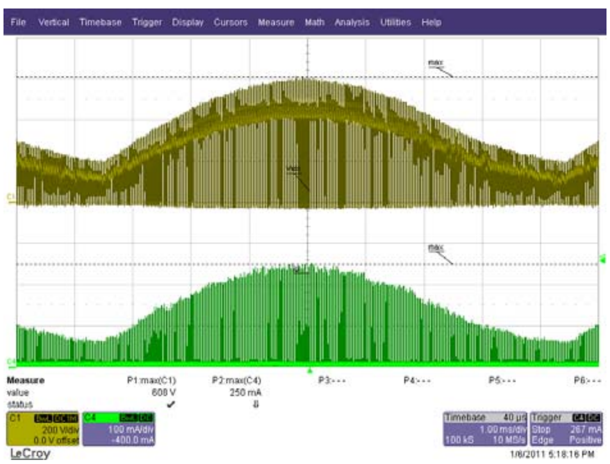

Figure 31 – 265 VAC / 63 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 200 V / div., 1 ms / div.
Lower: I_{DRAIN}, 0.1 A / div.

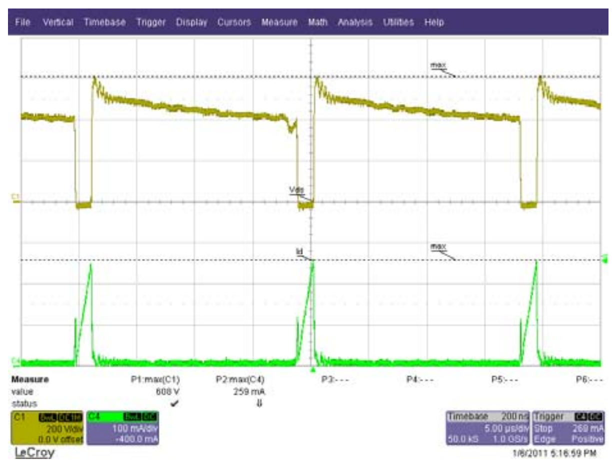

Figure 32 – 265 VAC / 63 Hz,
LED = 3 V / 366 mA.
Upper: V_{DRAIN}, 200 V / div., 5 μs / div.
Lower: I_{DRAIN}, 0.1 A / div.

11.1.2 AC Start-up

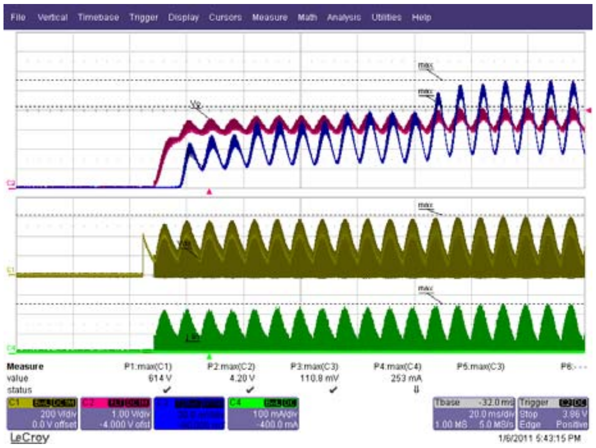

Figure 33 – 265 VAC / 63 Hz,
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_O, 1 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 100 mA / div.
Time Scale: 20 ms / div.

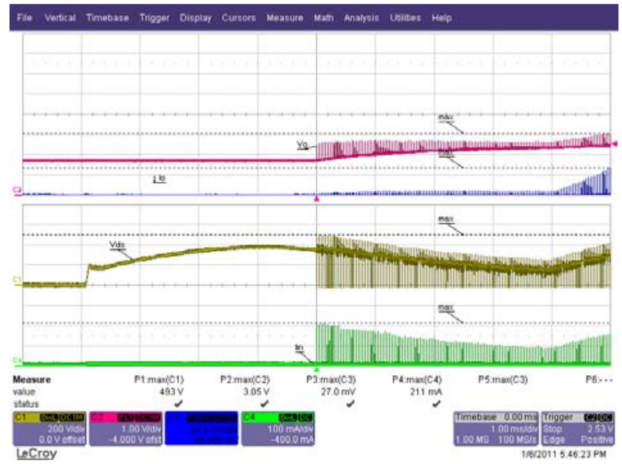

Figure 34 – 265 VAC / 63 Hz,
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_O, 1 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 100 mA / div.
Time Scale: 1 ms / div.

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11.1.3 Fault Conditions (Output Shorted / Open Circuit)

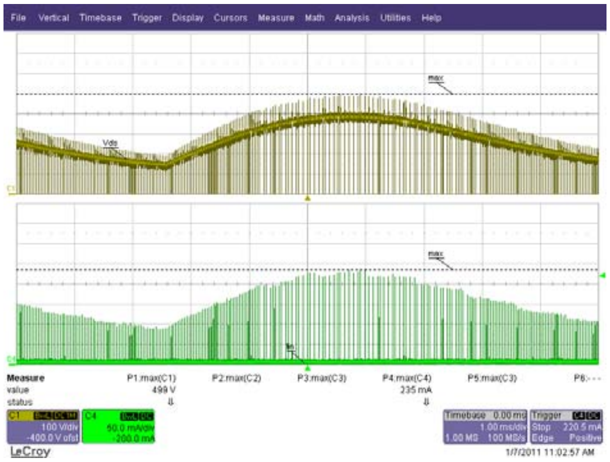

Figure 35 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 50 m A / div., 1 ms / div.

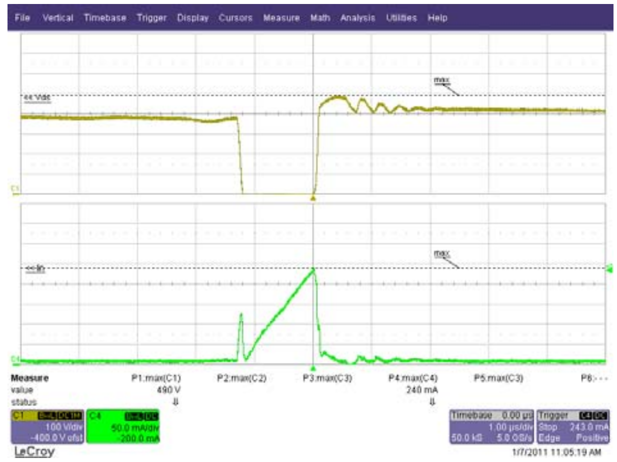

Figure 36 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 50 mA / div., 1 μs / div.

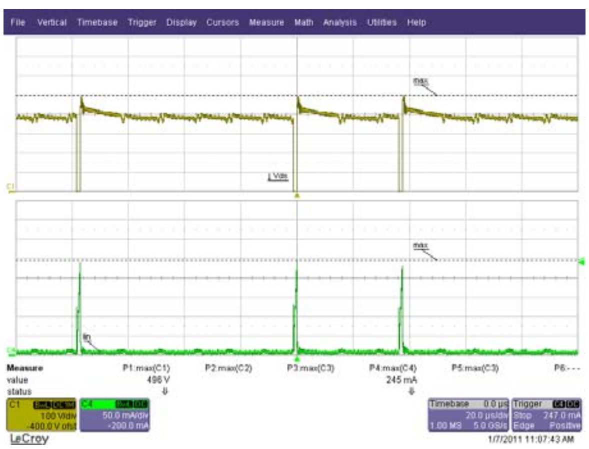

Figure 37 – 265 VAC.
Load Shorted.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 50 mA / div., 20 μs / div.

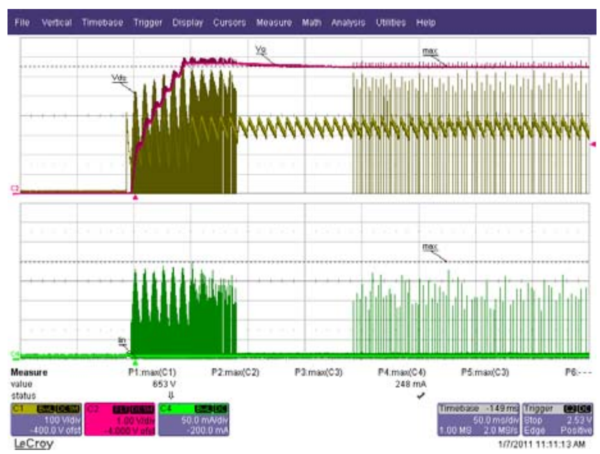

Figure 38 – 265 VAC.
Load Open.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_O, 1 V / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

11.2 Output Current Start-up Profile

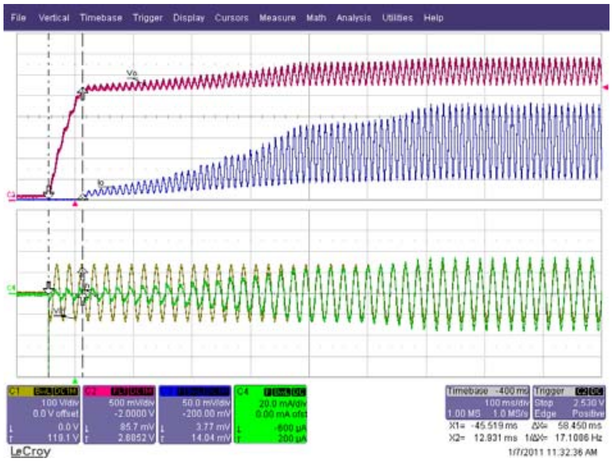

Figure 39 – 90 VAC / 47 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 20 mA / div.
Time Scale:100 ms / div.

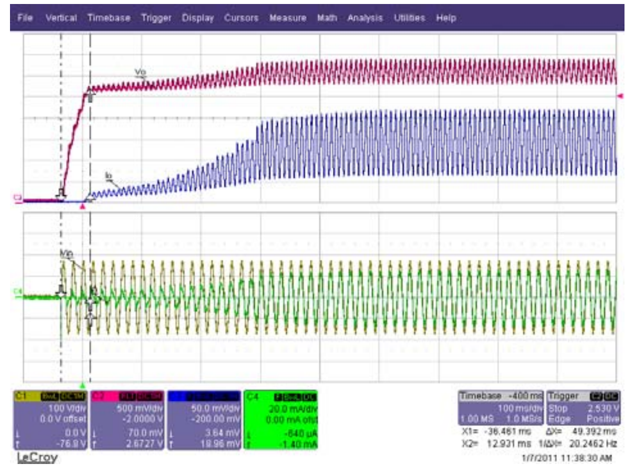

Figure 40 – 115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 20 mA / div.
Time Scale:100 ms / div.

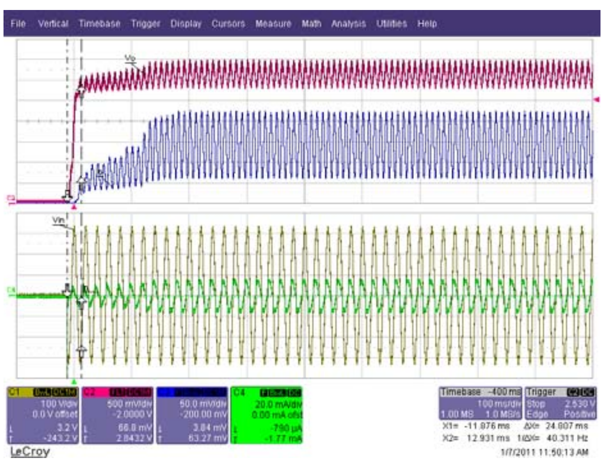

Figure 41 – 230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 20 mA / div.
Time Scale:100 ms / div.

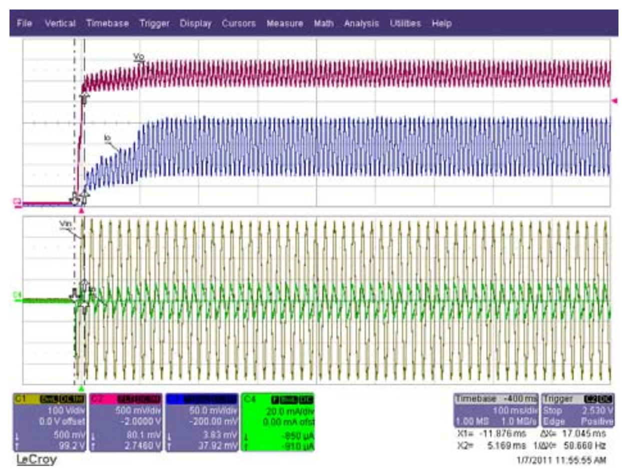

Figure 42 – 265 VAC / 63 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 20 mA / div.
Time Scale:100 ms / div.

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11.3 Input and Output Waveforms

11.3.1 Normal Operation (V_{IN}, I_{IN}, V_O and I_O)

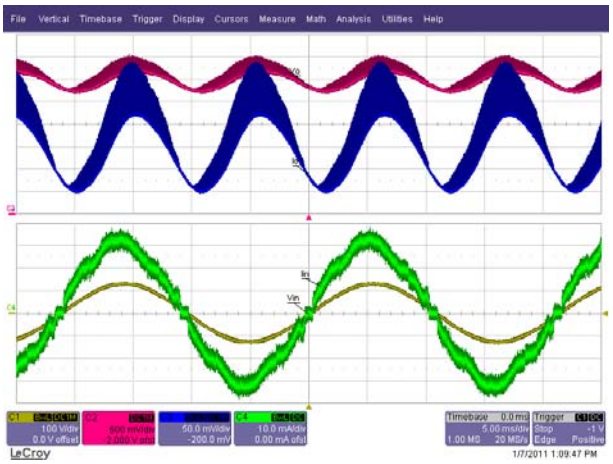

Figure 43 – 90 VAC / 47 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 10 mA / div., 5 ms / div.

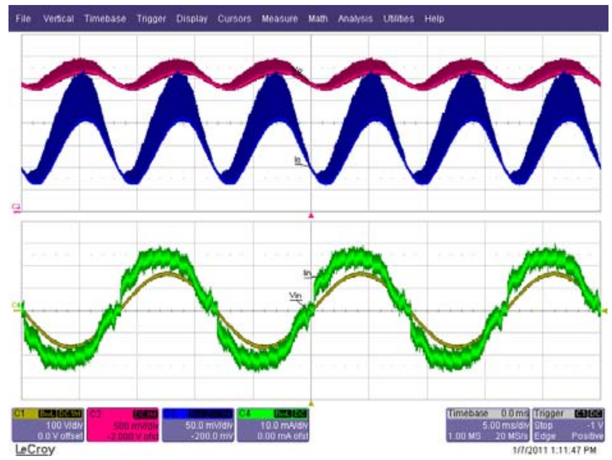

Figure 44 – 115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 10 mA / div., 5 ms / div.

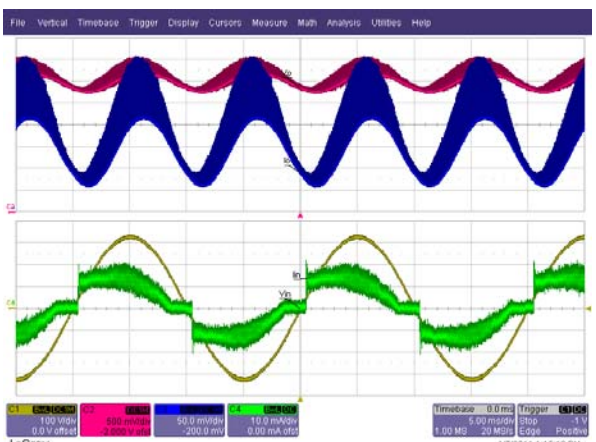

Figure 45 – 230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 10 mA / div., 5 ms / div.

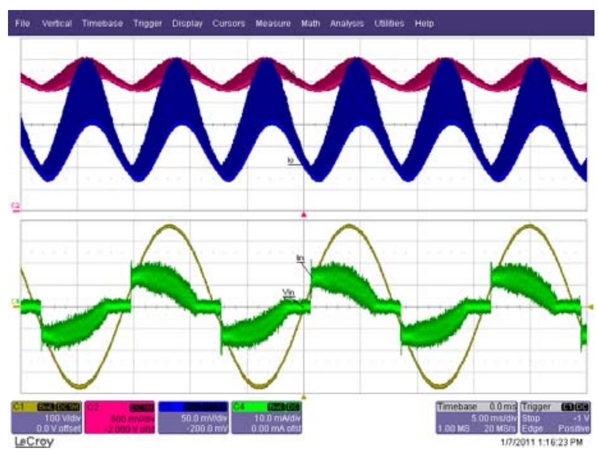

Figure 46 – 265 VAC / 63 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 100 V / div.
Ch2(Red): V_O, 500 mV / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{IN}, 10 mA / div., 5 ms / div.

11.4 Line Transient Response

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

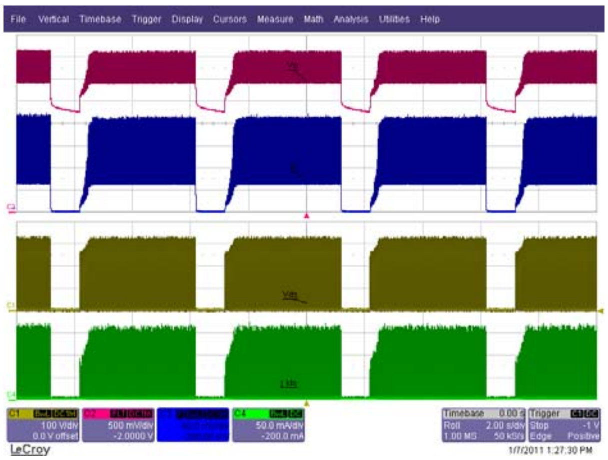

Figure 47 – 115-0-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 2 s / div.

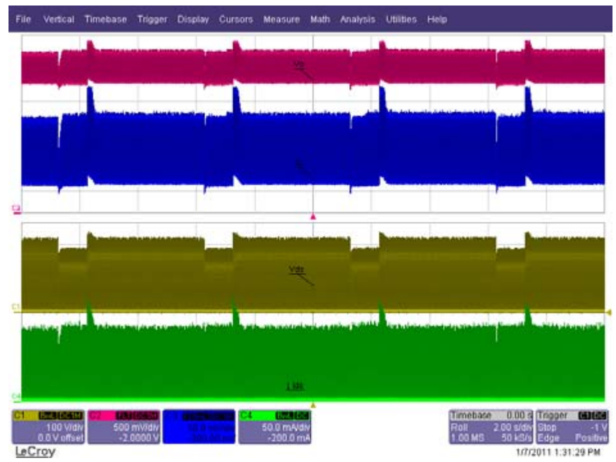

Figure 48 – 115-85-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 2 s / div.

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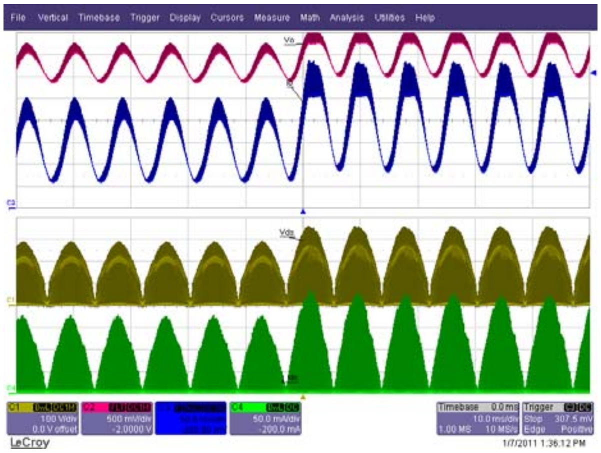

Figure 49 – 115-85-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 10 ms / div.

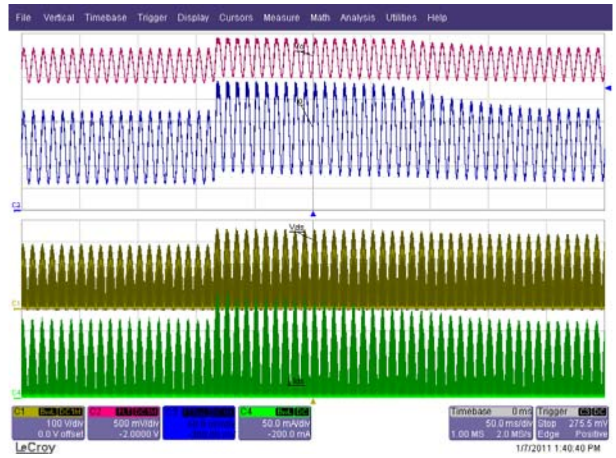

Figure 50 – 115-85-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

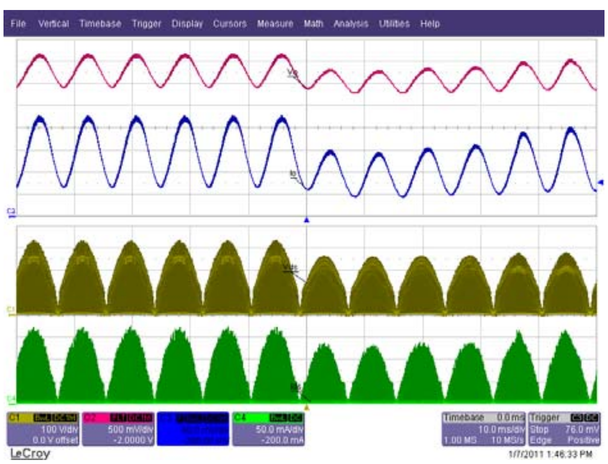

Figure 51 – 115-85-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 10 ms / div.

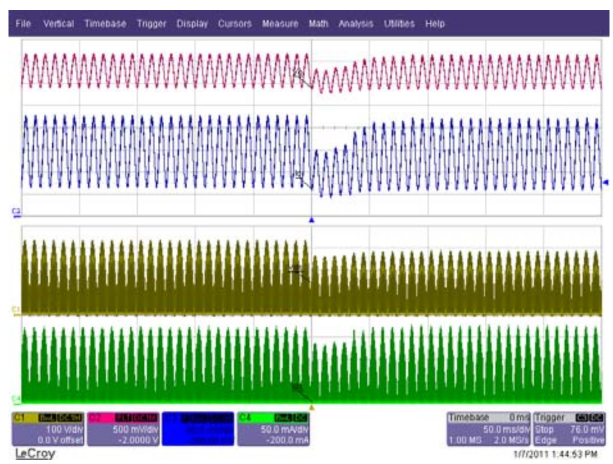

Figure 52 – 115-85-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

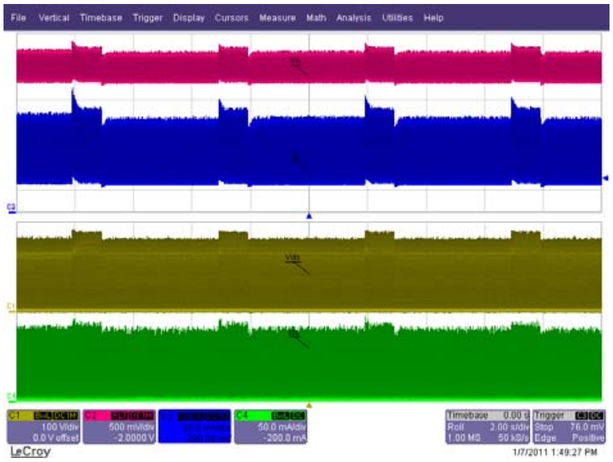

Figure 53 – 115-132-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 2 s / div.

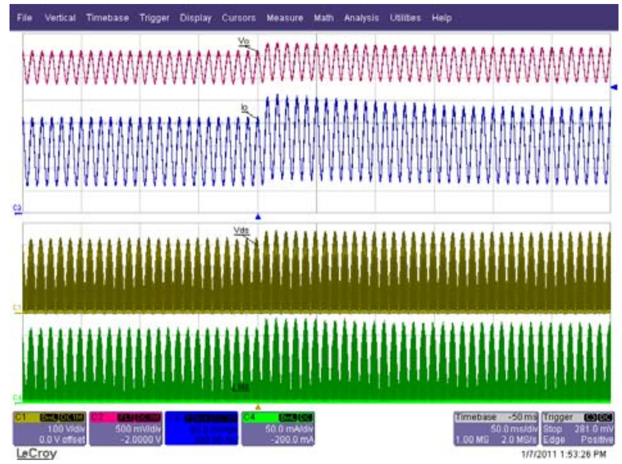

Figure 54 – 115-132-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

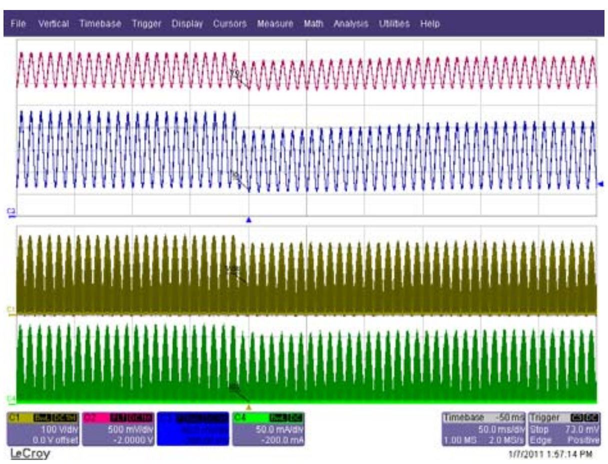

Figure 55 – 115-132-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

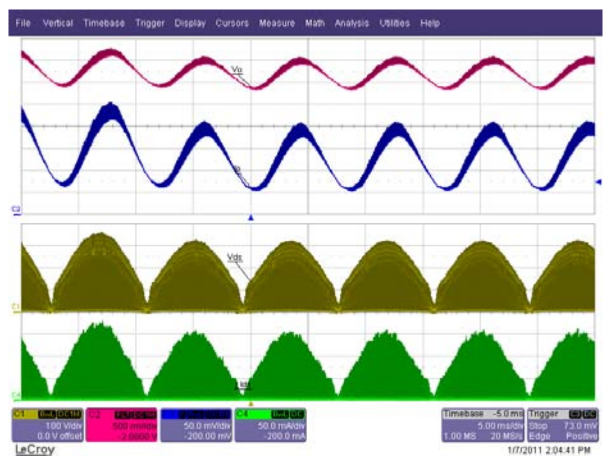

Figure 56 – 115-132-115 VAC / 60 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 100 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 5 ms / div.

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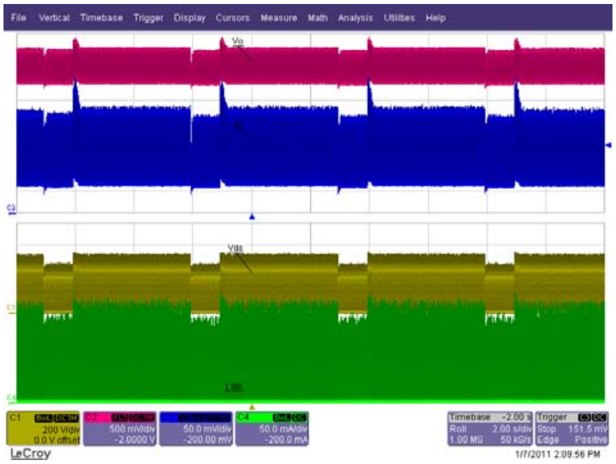

Figure 57 – 230-180-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 2 s / div.

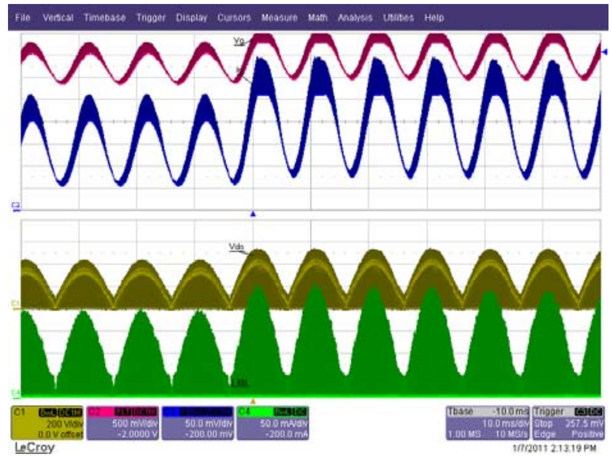

Figure 58 – 230-180-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 10 ms / div.

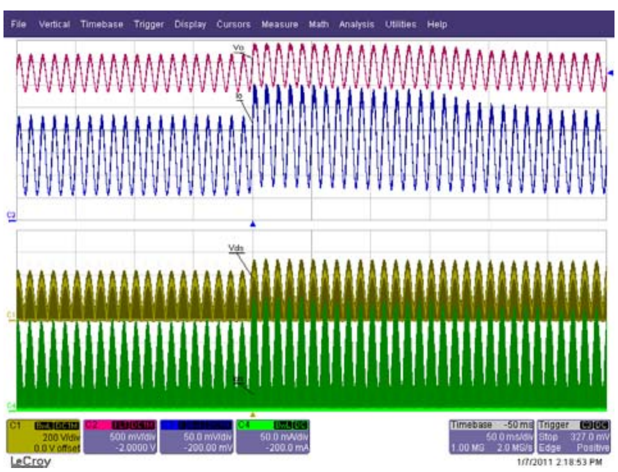

Figure 59 – 230-180-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

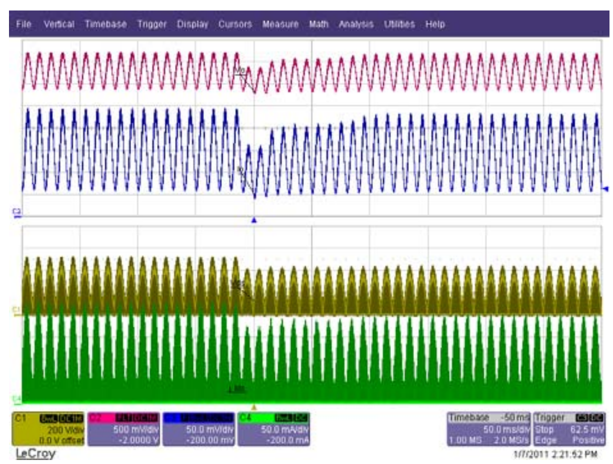

Figure 60 – 230-180-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

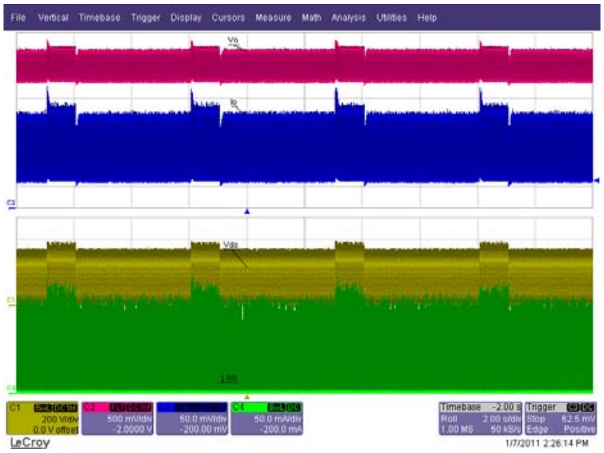

Figure 61 – 230-265-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 2 s / div.

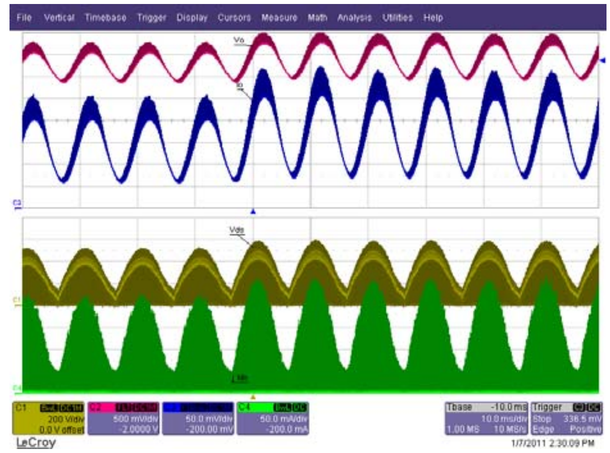

Figure 62 – 230-265-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 10 ms / div.

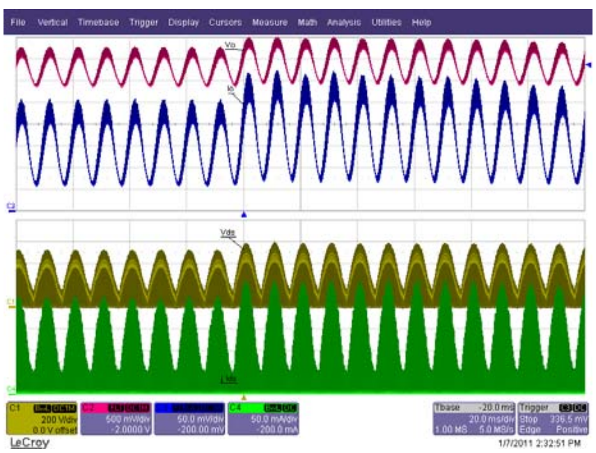

Figure 63 – 230-265-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

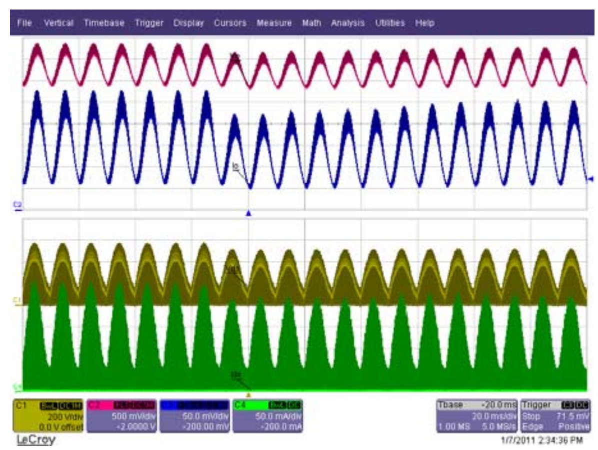

Figure 64 – 230-265-230 VAC / 50 Hz.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{DS}, 200 V / div.
Ch2(Red): V_{IN}, 0.5 V / div.
Ch3(Blue): I_O, 100 mA / div.
Ch4(Green): I_{DS}, 50 mA / div., 50 ms / div.

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11.5 Brown-Out

AC input voltage is ramp up and ramp down slowly in a rate of 0.1 V / s to verify that no damage (e.g. overheating) or component failure occurs during this abnormal condition. Unit was not expected to operate normally below 85 VAC, turning off, low output current and flicker at extremely low input voltage is acceptable. Normal operation was verified once the AC input voltage was returned to specified range.

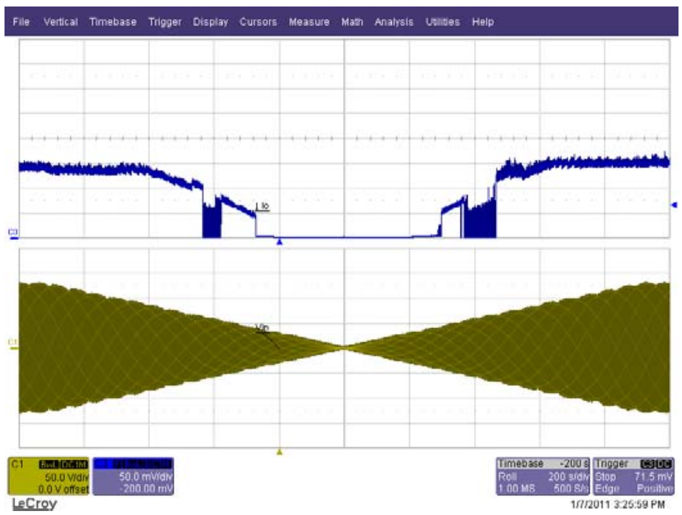

Figure 65 – 90-0-90 VAC / 50 Hz at 0.1 V / s Slew Rate.
LED = 3 V / 366 mA.
Ch1(Yellow): V_{IN}, 50 V / div.
Ch3(Blue): I_O, 100 mA / div.
Time Scale: 200 s / div.

12 Line Surge

Differential input line 1.2 / 50 μs surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded with 3 V / 366 mA and operation was verified following each surge event.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Surge Type	Test Result (Pass/Fail)
+500	230	L1 to L2	90	Line	Pass
+500	230	L1 to L2	0	Line	Pass
-500	230	L1 to L2	90	Line	Pass
-500	230	L1 to L2	0	Line	Pass
+2500	230	L1 to L2	90	Ring Wave	Pass
+2500	230	L1 to L2	0	Ring Wave	Pass
-2500	230	L1 to L2	90	Ring Wave	Pass
-2500	230	L1 to L2	90	Ring Wave	Pass

Unit passed all test conditions.

12.1 Line Surge Drain Voltage waveforms.

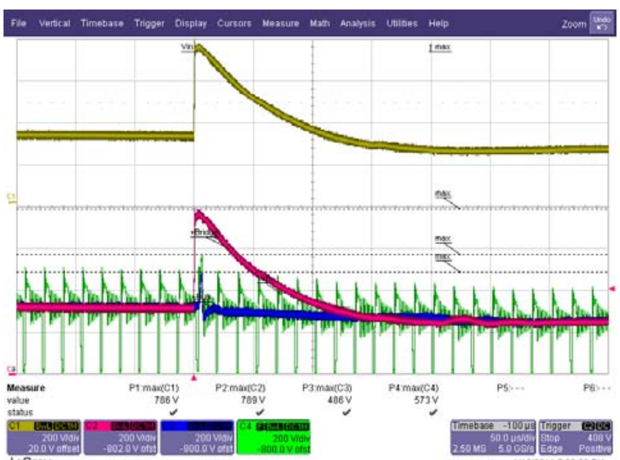

Figure 66 – 500 V Differential Line Surge at 230 VAC / 60 Hz.
LED = 3 V / 366 mA. Peak V_{DS} = 573 V.
Ch1(Yellow): V_{IN}, 200 V / div.
Ch2(Red): V_{BRIDGE}, 200 V / div.
Ch3(Blue): V_{BULK}, 2000 V / div.
Ch4(Green): V_{DS}, 200 V / div., 50 μs / div.

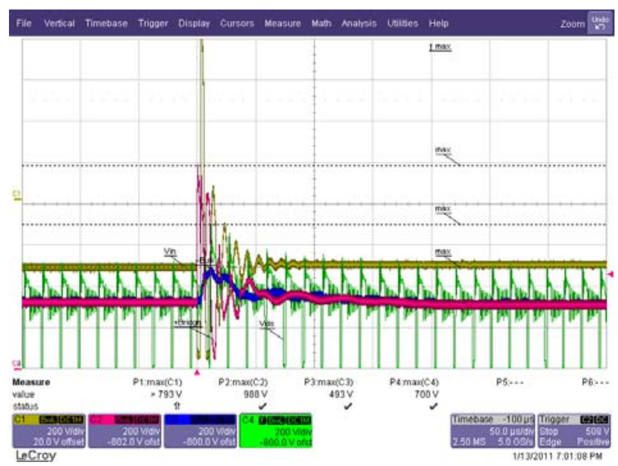

Figure 67 – 2.5 kV Ring Surge at 230 VAC / 60 Hz.
LED = 3 V / 366 mA; Peak V_{DS} = 700 V.
Ch1(Yellow): V_{IN}, 200 V / div.
Ch2(Red): V_{BRIDGE}, 200 V / div.
Ch3(Blue): V_{BULK}, 2000 V / div.
Ch4(Green): V_{DS}, 200 V / div., 50 μs / div.

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12.2 Conducted EMI

12.3 Equipment:

Receiver:

Rohde and Schwarz
ESPI - Test Receiver (9 kHz – 3 GHz)
Model No: ESPI3

LISN:

Rohde and Scharrz
Two-Line-V-Network
Model No: ENV216

12.4 EMI Test Set-up

LED driver was placed within a candelabra base (Figure 3) with LED load and placed in a conical metal housing (for self-ballasted lamps; CISPR15 Edition 7.2).

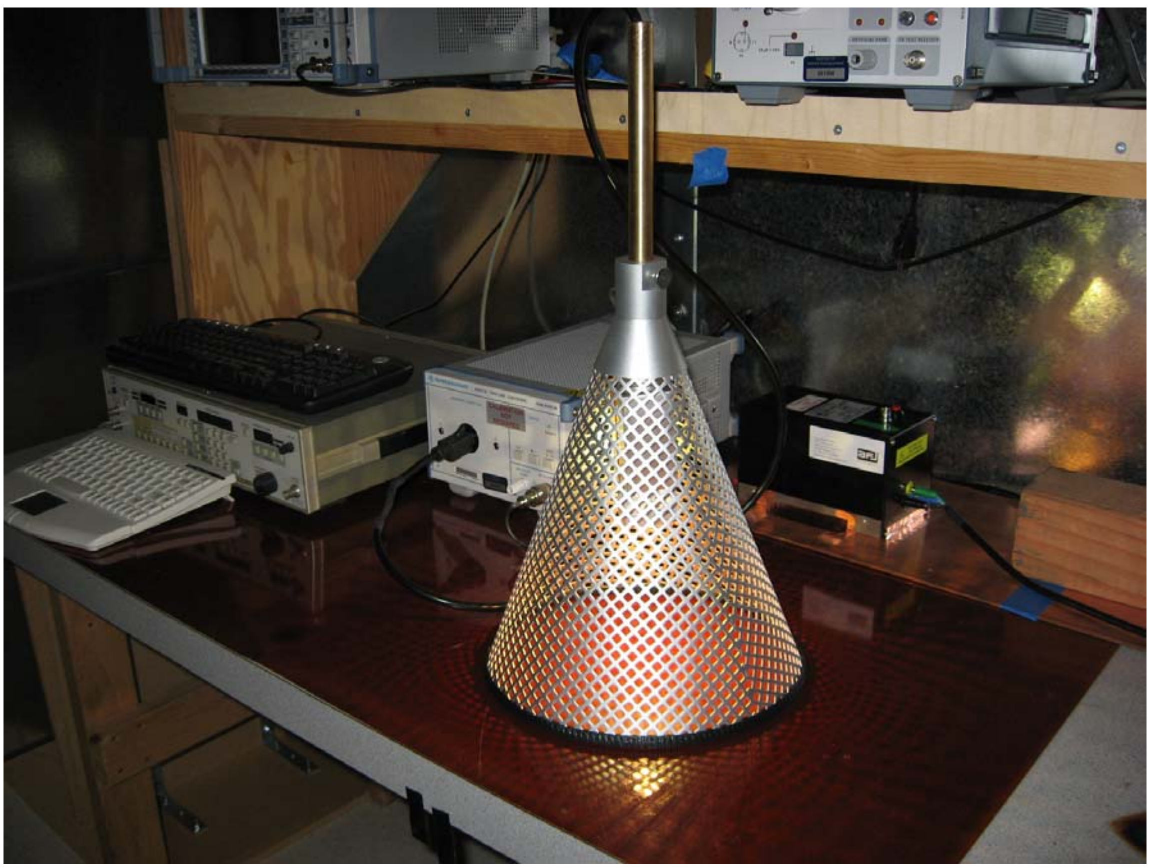

Figure 68 – Conducted Emissions Measurement Set-up
Showing Conical Ground Plane Inside which UUT was Mounted.

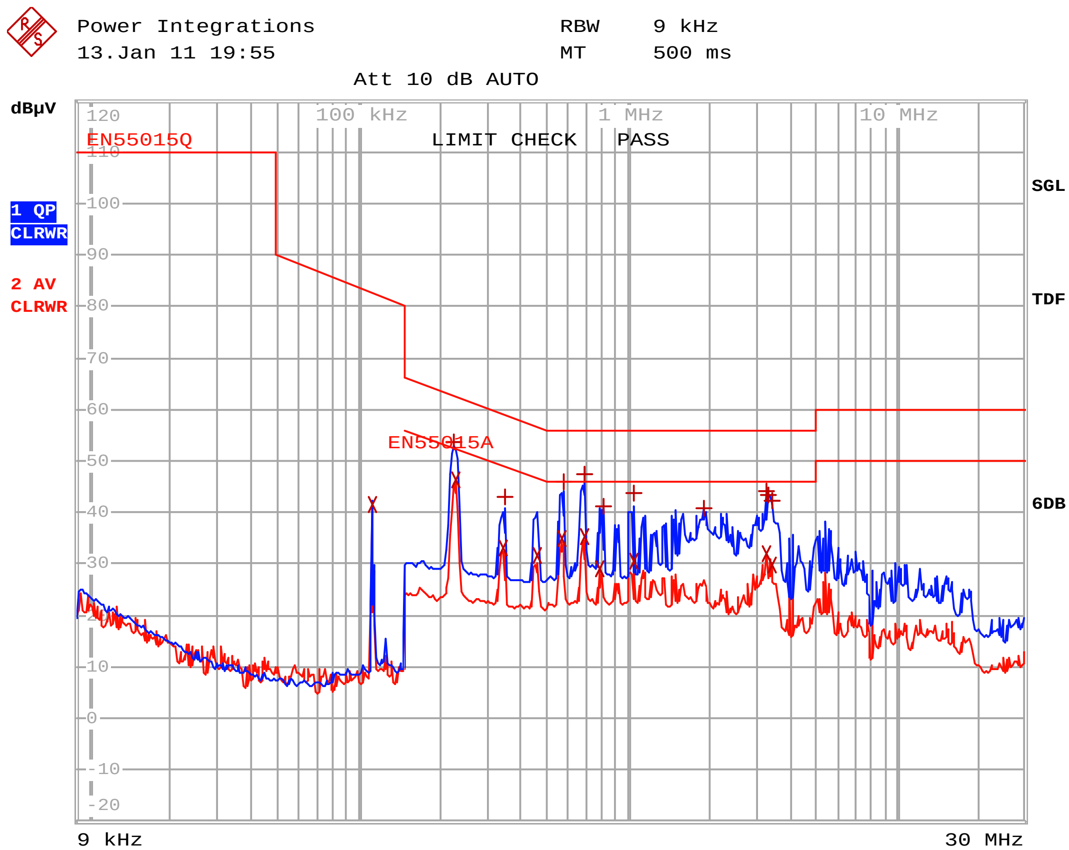

Figure 69 – Pre-scan Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 Limits. Note Blue Line is Peak Result vs. QP Limit Line – Refer to Table for QP Margin.

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EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	112.686385873 kHz	41.60	L1 gnd	
1	Quasi Peak	223.329560038 kHz	53.71	L1 gnd	-8.97
2	Average	227.818484195 kHz	46.44	L1 gnd	-6.08
2	Average	342.582585749 kHz	33.21	L1 gnd	-15.92
1	Quasi Peak	346.008411606 kHz	43.16	L1 gnd	-15.89
2	Average	461.749566613 kHz	31.79	L1 gnd	-14.86
2	Average	563.422222132 kHz	34.91	L1 gnd	-11.08
1	Quasi Peak	580.494478884 kHz	45.93	L1 gnd	-10.06
2	Average	687.48218373 kHz	35.17	L1 gnd	-10.82
1	Quasi Peak	694.357005568 kHz	47.40	L1 gnd	-8.59
2	Average	790.243042258 kHz	29.00	L1 gnd	-16.99
1	Quasi Peak	814.188196682 kHz	41.27	L1 gnd	-14.72
1	Quasi Peak	1.04414099339 MHz	43.78	L1 gnd	-12.21
2	Average	1.04414099339 MHz	30.42	L1 gnd	-15.58
1	Quasi Peak	1.91585637048 MHz	40.94	N gnd	-15.05
1	Quasi Peak	3.24635311795 MHz	44.14	L1 gnd	-11.85
2	Average	3.24635311795 MHz	32.10	L1 gnd	-13.89
1	Quasi Peak	3.31160481562 MHz	43.42	N gnd	-12.57
1	Quasi Peak	3.44606925067 MHz	42.44	N gnd	-13.55
2	Average	3.44606925067 MHz	29.81	N gnd	-16.18

Table 3 – Conducted EMI, Maximum Steady State Load, 115 VAC, 60 Hz, and EN55015 Margin.

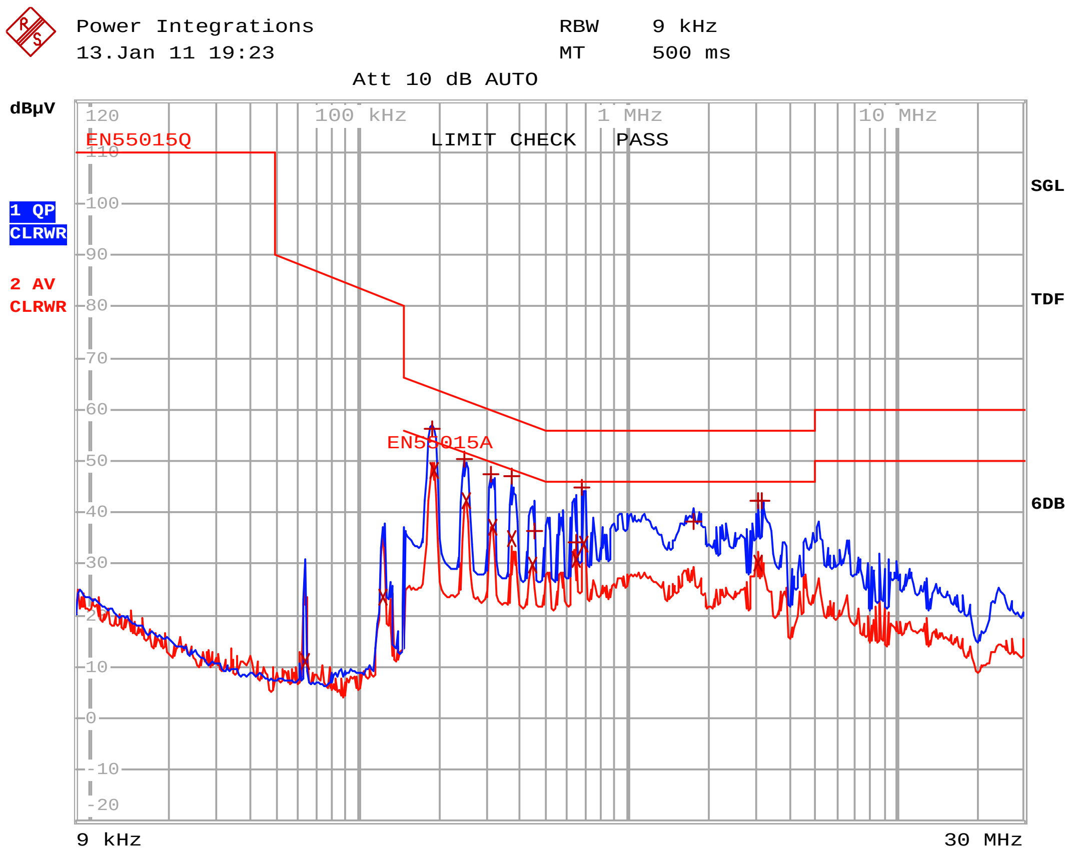

Figure 70 – Pre-scan Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 Limits. Note Blue Line is Peak Result vs. QP Limit Line – Refer to Table for QP Margin.

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EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55015Q
Trace2: EN55015A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV		DELTA LIMIT dB
2	Average	63.2749441994 kHz	11.22	N gnd	
2	Average	123.243440661 kHz	23.41	N gnd	
1	Quasi Peak	186.707378963 kHz	56.35	L1 gnd	-7.82
2	Average	190.46019728 kHz	48.09	L1 gnd	-5.92
1	Quasi Peak	249.161721009 kHz	50.27	L1 gnd	-11.51
2	Average	251.653338219 kHz	42.25	L1 gnd	-9.45
1	Quasi Peak	310.135545783 kHz	47.46	L1 gnd	-12.50
2	Average	316.369270253 kHz	37.10	L1 gnd	-12.70
1	Quasi Peak	370.967850209 kHz	47.19	L1 gnd	-11.28
2	Average	374.677528711 kHz	35.01	L1 gnd	-13.38
2	Average	448.169580165 kHz	29.85	L1 gnd	-17.05
1	Quasi Peak	452.651275966 kHz	36.42	L1 gnd	-20.40
2	Average	641.227045055 kHz	30.88	L1 gnd	-15.11
1	Quasi Peak	647.639315505 kHz	34.20	L1 gnd	-21.79
1	Quasi Peak	680.675429436 kHz	44.78	N gnd	-11.21
2	Average	687.48218373 kHz	33.65	N gnd	-12.34
1	Quasi Peak	1.75174377706 MHz	38.26	N gnd	-17.73
1	Quasi Peak	3.08879360159 MHz	42.28	L1 gnd	-13.71
2	Average	3.08879360159 MHz	30.28	L1 gnd	-15.71
1	Quasi Peak	3.15087835298 MHz	42.36	N gnd	-13.63

Table 4 – Conducted EMI, Maximum Steady State Load, 230 VAC, 60 Hz, and EN55015 Margin.

13 Output Current Production Distribution

Figure 71 shows the production distribution of output current for 22 randomly selected RD-268 boards. The data was gathered using a NH Research 5600 series power supply test system, commonly used in the power supply industry for production testing of power supplies. The data is also summarized in Table 5.

Measurements were made at room temperature, with a CV+CC load representing the characteristics of the included Luxeon Rebel LED. Measurements were after directly applying voltages of 115 VAC and 230 VAC. These distributions includes variations not only from the LinkSwitch-PL devices but also all the components of the driver.

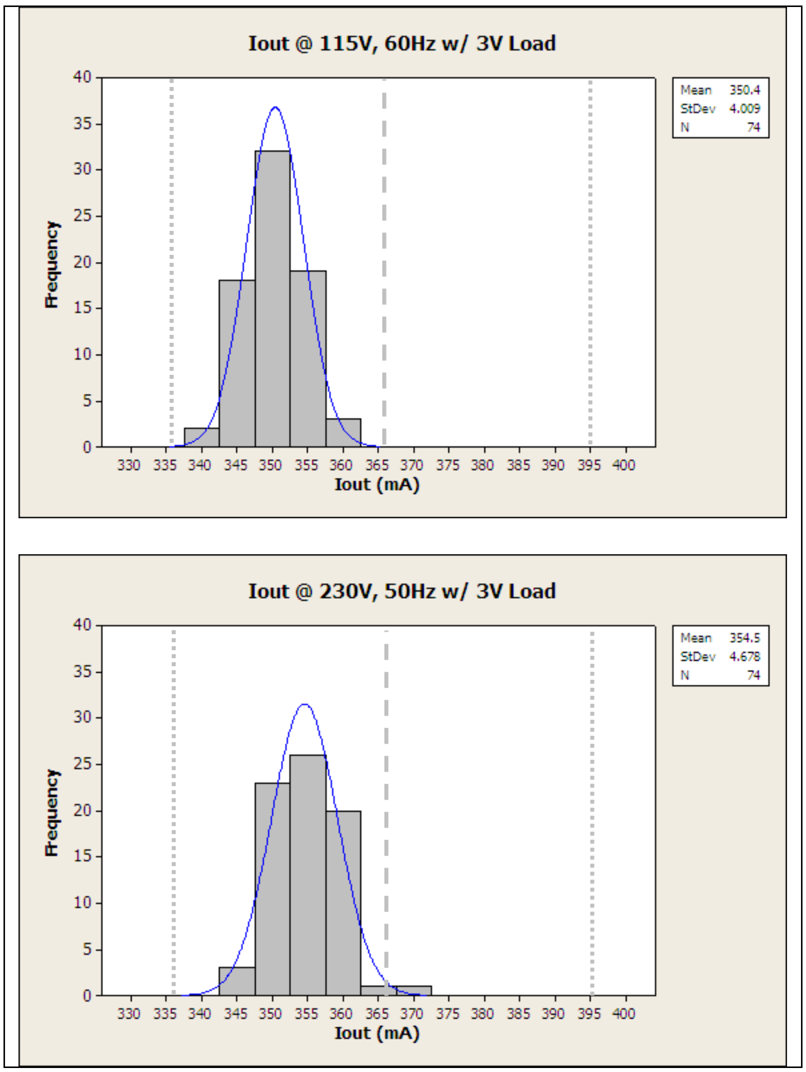

Figure 71 – Output Current Distribution Plot for RD-268 (Line Represents Nominal, Minimum and Maximum I_O Specification)

From the data it can be seen that the output current is not centered. This could be corrected by adjusting the output current sense resistor value, reducing it by 6% to

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increase the output current by 6%. Therefore to correctly demonstrate the achievable tolerance of the design, C_P values were calculated versus C_{PK}. C_P provides process capability when the distribution is centered (C_P=C_{PK} for a centered process) such as would be the case if the sense resistor were adjusted.

Output current tolerance values are given based on C_P of 1.33, 1.5, and 1.67. A value of 1.33 is typical for high volume production. A value of 1.5 is generally considered to indicate a 6 sigma process (allowing for a 1.5 sigma drift from the mean with a C_P of 2).

For reference Table 7 shows the expected PPM fallout rate for a given C_P/C_{PK} value.

Input Voltage (VAC)	Mean (mA)	σ (mA)	I_O Tolerance for Given C_P Value		
			C_P=1.33	C_P=1.5	C_P=1.67
115	351.2	4.0	±4.1%	±4.%	±5.9%
230	354.6	4.68	±4.1%	±4.7%	±8%
115 - 230	352.9	4.16			

Table 5 – Output Current Tolerance vs. C_P Value.

C_{PK}	Sigma	PPM
1	3	2700
1.33	4	64
1.5	4.5	7
1.67	5	1

Table 6 – PPM Fallout Rate vs. C_{PK} Value.

The data in Table 6 shows that the design meets the ±7% target specification with a C_P of >1.33. In additional the design is capable of meeting a tolerance specification of < ±5% at low line.

14 Revision History

Date	Author	Revision	Description & changes	Reviewed
28-Feb-11	JDC	1.0	Initial Release	Apps & Mktg
04-Mar-11	PV	1.1	Added Production I_O Data	
04-Apr-11	KM	1.2	Updated Figures 39 to 65	

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