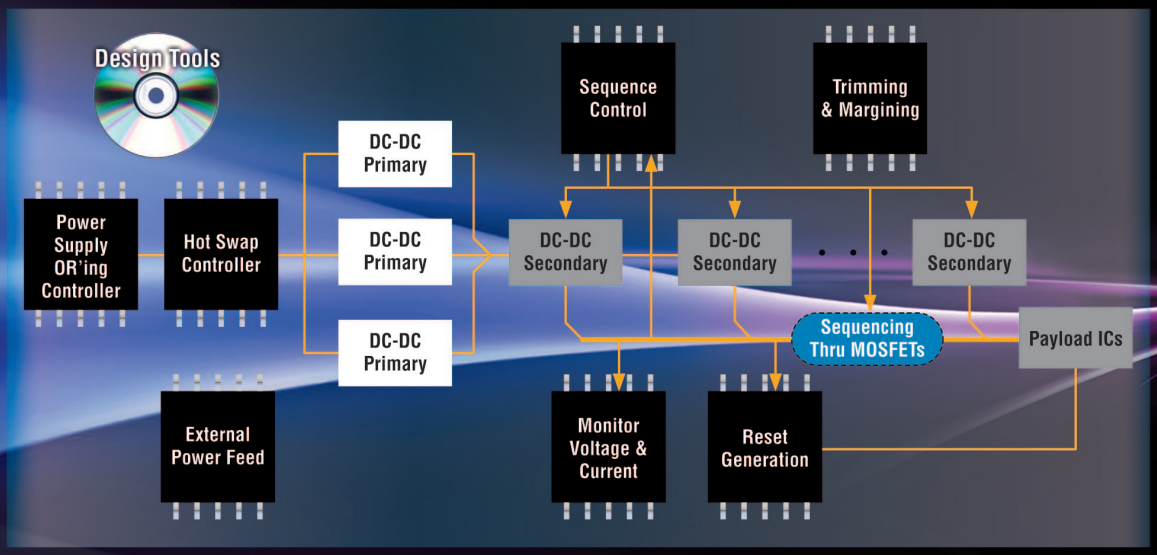
Power 2 You

A Guide to Power Supply Management and Control



Board Power Management Functions

LEARN HOW TO:

» Reduce Power Management Costs
» Increase System Reliability
» Reduce the Risk of Circuit Board Respins

Shyam Chandra

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Introduction

1.1 Power 2 You

This book provides technical details and design considerations for implementing the common circuit board power management functions shown as 3-D blocks in Figure 1-1 and Figure 1-2. This book also provides generalized cost effective solutions for each of these functions that can be customized to meet a circuit board's specific voltage, current and control environment.

For readers viewing this document in .pdf format, the 3-D blocks in Figure 1-1 and Figure 1-2 are hyperlinked to the appropriate section of Chapter 2, where multiple circuit options are provided for that particular power management function. Each of the circuit options hyperlink to a detailed description in the relevant chapters.

If you are already familiar with Lattice Semiconductor Power Manager II devices and need to find a solution for a power management function:

1. Click on the required power management block in Figure 1-1.
2. You will automatically navigate to the section of Chapter 2 that provides multiple circuit options for the selected power management function.
3. Click on the relevant circuit option.
4. You will automatically navigate to the detailed description of that circuit diagram.

If you wish to read about the general board power management blocks, the design criteria and circuit options, read this chapter. After reading this chapter, you can skip Chapter 2 - "Solutions Summary" on page 2-1 and continue with Chapter 3 - "Reset Generators & Supervisors" on page 3-1.

What is Power Management?

Every circuit board is powered from one or more sources called the input, or primary, power supplies. And, every circuit board performs one or more functions using a number of ICs, such as ASICs, CPUs, FPGAs, and so on. These ICs are called the payload ICs. The circuit board generates multiple power rails from the input supplies to power these payload ICs, using board

mounted supplies called primary and secondary supplies. The term ‘Power Management’ in this book includes all power rail control functions implemented in a circuit board. Typically, input power rails are controlled by power management functions such as hot-swap control and redundant power rail control. On the payload side, power management functions include sequencing, monitoring, supervisory signal generation, trimming and margining.

Typical Board Power Supply Architectures

Circuit boards can be broadly classified into two types:

1. Boards that derive input power supply from a backplane with its power always on and the boards plugged into or extracted from the backplane without turning the power off – these are called hot-swappable boards, shown in Figure 1-1.

2. Boards that derive power from an external power supply that is turned on after the board is connected and is turned off before the board is disconnected – these are called non hot-swappable boards.

There are solutions to implement all of the critical power supply control functions. Advanced power supply designers can click on any of the hyperlinked functions to see the solution. To learn the background of all these functions, continue reading this chapter.

Figure 1-1. Power Management in a Hot-Swappable Circuit Board. (If viewing this document in .pdf format, click on any of the 3-D blocks to jump to implementation details.)

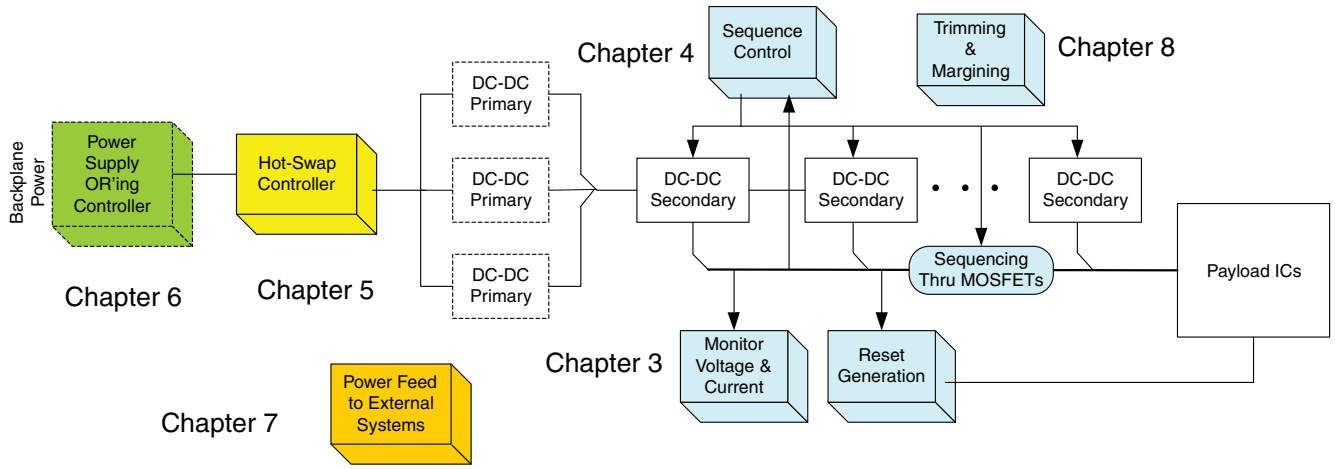


Figure 1-1 illustrates the power supply architecture of a circuit board with the common power management blocks shown in 3-D. A hot-swappable board derives its power from one or more supplies from the backplane. There can be more than one set of supplies sourced from the backplane, so these boards are operational even when one of the supplies fails. The backplane supplies in Figure 1-1 are also called the primary supplies.

In systems that require high availability, such as telecom / datacom systems, backplanes provide redundant supplies called on-line and standby power. The **Power Supply OR’ing Controller, also called the redundant power supply controller,** selects between the online and standby supplies to derive the power to the board. (Refer to “2.4 Redundant Supply Management” on page 2-14.)

In order to extract and reinsert the boards from the backplane without disturbing the other boards plugged into the same backplane, a **hot-swap controller** function is implemented on each of these circuit boards.

(Refer to "2.3 Hot-Swap Controllers" on page 2-6.) In some cases, the supply rail output from the hot-swap controller feeds one or more DC-DC converters, shown in Figure 1-1 as 'DC-DC Primary' supplies.

Primary supplies are used to derive one or more main payload supply rails, which are also called secondary supply rails and are shown in Figure 1-1 as the 'DC-DC Secondary' supplies. These secondary supplies may have to be sequenced either through the DC-DC converter enable signals or through **MOSFETs**. Sequencing of these supplies is controlled by the **sequence controller**. (Refer to "2.2 Power Supply Sequencing" on page 2-3.) After all supplies are sequenced, the **reset generator** starts the board's normal operation by releasing the reset signal to the CPU. (Refer to "2.1 N-Supply Supervisor, Reset Generator and Watchdog Timer" on page 2-1.) The **voltage and current are monitored** for faults and board shut down or reset generation functions are initiated as a result. (Refer to "2.1 N-Supply Supervisor, Reset Generator and Watchdog Timer" on page 2-1.) In addition, monitoring these lower voltages for faults should take into consideration, and compensate for, other error sources such as the ground voltage difference between the supply and the monitoring device. For example, the fault level of 1.2V is 1.2V * 5% = ±60mV. The ground voltage difference between different points in the circuit board can be be as much as 20mV to 30mV. To compensate for the error, differential sensing, as shown in Figure 3-9 on page 9, is used.

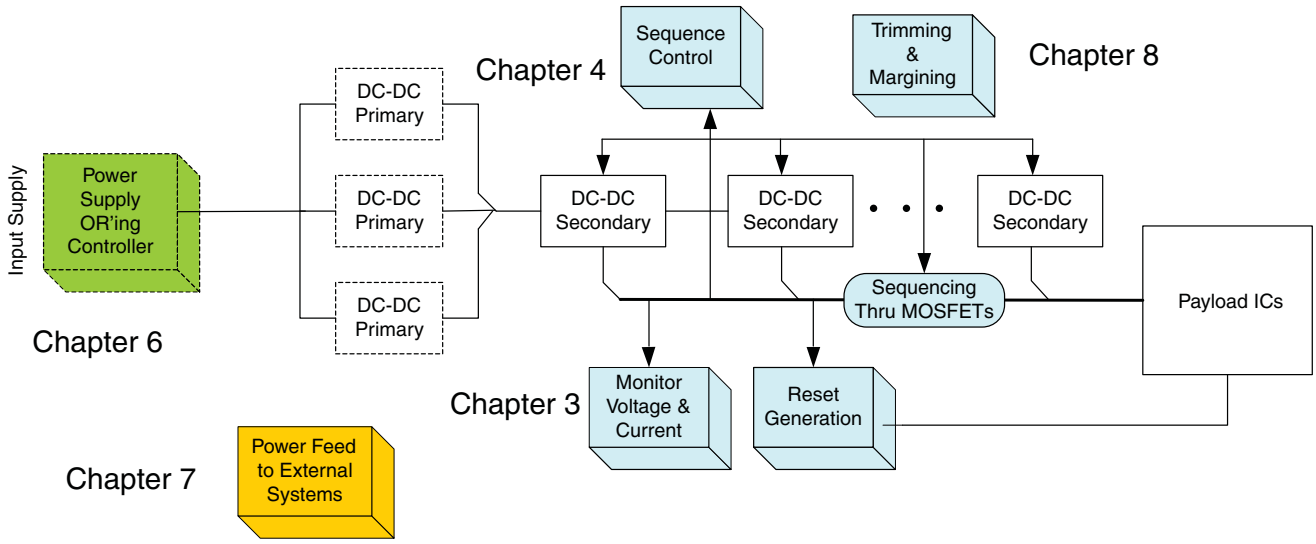
Modern ICs require lower core voltages (1.2V or lower) with high current capacity (10A or higher) with reduced voltage tolerance. To meet these stringent supply requirements, a power supply **trimming controller** is often required. (Refer to "2.6 Trimming and Margining" on page 2-23.)

For quality assurance purposes, four-corner testing of boards (voltage and temperature) frequently requires margining of supplies. These boards use **margining controllers**. (Refer to "2.6 Trimming and Margining" on page 2-23.)

In some applications, such as GSM basestation boards, microwave boards and boards supporting hot-pluggable mezzanine cards, it may be necessary to power an external unit, such as a remote radio head or an outdoor antenna, or supply power to an AMC. To support these functions, the **power feed controller** is required. (Refer to "2.5 Power Feed Controllers" on page 2-19.)

Figure 1-2 shows the power management requirements in a non hot-swappable circuit board. These boards require primary and secondary power management controllers, as shown in Figure 1-2. The only primary power management function that is not relevant in these non-hot-swappable boards is the hot-swap controller. Systems that typically require non-hot-swappable boards include routers in "pizza-box" form factor, personal computers and medical ultrasound systems.

Figure 1-2. Power Management in a Non-Hot-Swappable Circuit Board. (If viewing this document in .pdf format, click on any of the 3-D blocks to jump to implementation details.)



Typical Power Management Implementations and Their Drawbacks

The power rails in a board currently are managed by simple, single function integrated circuits (ICs) on both the primary and secondary sides. On the input side, each function shown in Figure 1-1 requires different ICs, depending on the rail voltage, board power and other control specifications.

Modern circuit boards with complex payload ICs typically require five or more secondary power rails. Monitoring, sequencing and the generation of resets in these boards require multiple single function ICs.

Together, the power management section requires multiple types of single function power management ICs in a given system. This results in a larger bill of materials (BOM), higher cost of inventory and assembly, as well as reduced reliability.

The cost of the power management portion in a circuit board increases with the number of rails, and the number of power management functions. Lower cost single function power management ICs are usually less accurate in monitoring for faults, resulting in reduced board reliability.

In order to reduce the number of secondary power management ICs, some designs use microcontrollers with an Analog-to-Digital (ADC) converter to monitor power supplies and use software to adapt to board-specific requirements. These microcontrollers are too slow to respond to power supply faults (5 to 10ms) and are unreliable, as they use hundreds of lines of code to perform power management functions and require a watchdog timer to monitor software flow. Microcontrollers are also used because the changes to power management can be met simply by changing software, as opposed to modifying the circuit board layout. However, modifications to software are almost always avoided, as most companies have strict control over software releases.

The ideal power management solution is the one that has the following characteristics:

1. Lower cost and reduced bill of material, and flexibility to meet individual board power management needs.

2. Increased board reliability through increased supply fault monitoring accuracy.

3. Reduced risk of circuit board re-layout to board power management through programmability.

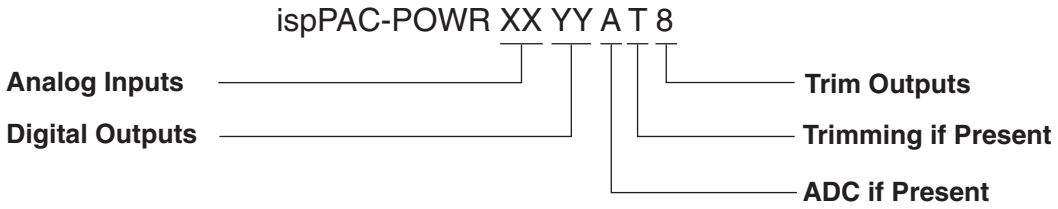
This book details how a Lattice Power Manager II device can integrate all of these functions. Because these devices are in-system programmable, each device can be programmed to meet a wide variety of circuit board functions.

1.2 Lattice Power Manager II IC Family

There are five members in the Power Manager II family of devices: ispPAC®-POWR1220AT8, ispPAC-POWR1014A, ispPAC-POWR1014, ispPAC-POWR607 and ProcessorPM™-POWR605.

Figure 1-3 shows the part numbering convention of the Lattice Power Manager II product family.

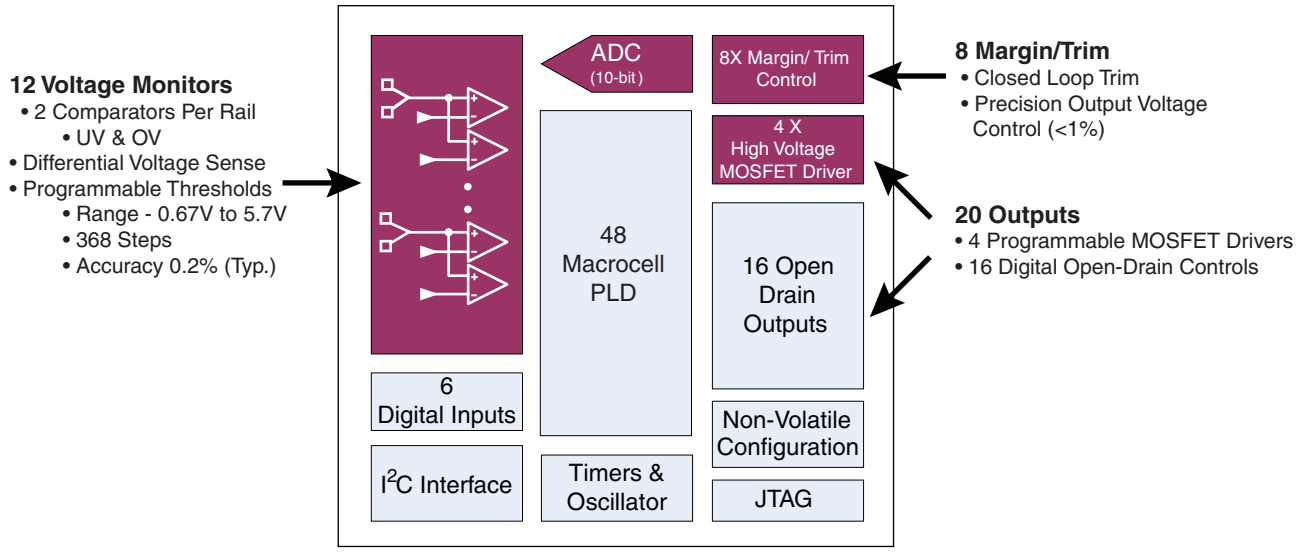
Figure 1-3. Lattice Power Manager II Family Part Numbers Indicate I/O Resources



While the largest device, the ispPAC-POWR1220AT8, can be used to implement complex power management functions, the smallest device, the ProcessorPM-POWR605, can be used to implement power management functions for a wide variety of microprocessors and DSPs. All Power Manager II devices can be programmed in-system through the JTAG interface. The power management algorithm can be designed using the PAC-Designer® software tool that can be downloaded from the Lattice website free of charge.

Figure 1-4 shows the architecture of the largest member of the family, the ispPAC-POWR1220AT8.

Figure 1-4. ispPAC-POWR1220AT8 Device Block Diagram



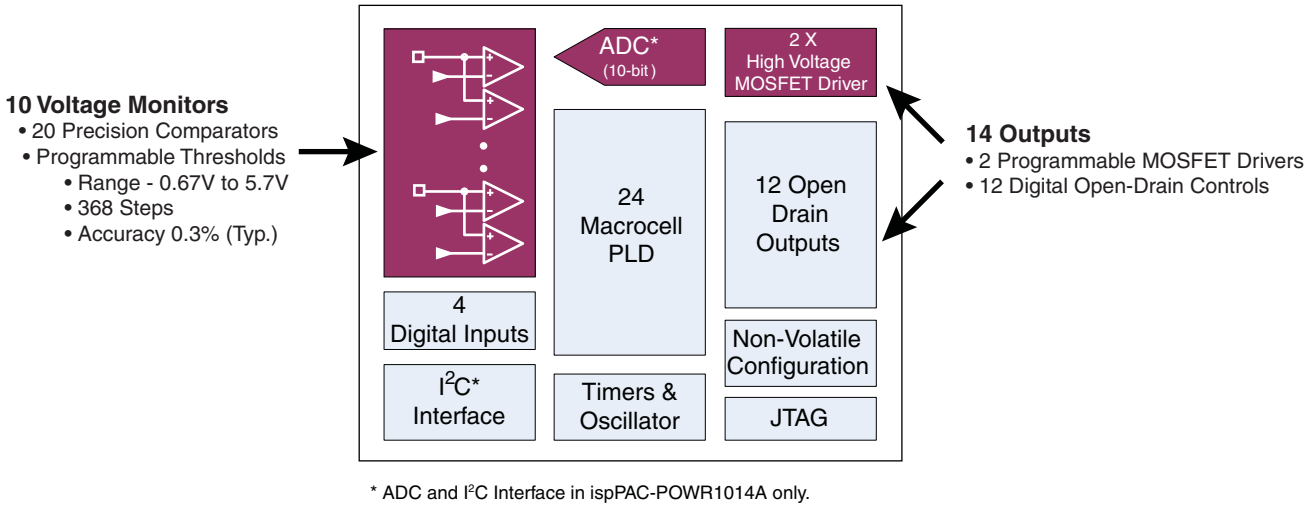
This device can manage up to 12 supply rails and generate 20 outputs (including four programmable MOSFET drive outputs) using its on-chip 48-macrocell ruggedized CPLD. All supply voltages can be measured using the on-chip 10-bit ADC device via the I^2C interface. This device also supports trimming and margining of up to eight DC-DC converters. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

The ispPAC-POWR1220AT8 device can integrate the following power management functions:

- Power supply OR'ing
- Positive rail power feed to external system
- Hot-swap controller for positive voltage rail
- Sequencing
- Voltage and current monitoring
- Reset generation
- Trimming and margining
- Watchdog timer

Figure 1-5 is a block diagram of the next members of the Lattice Power Manager II family, the ispPAC-POWR1014 and ispPAC-POWR1014A.

Figure 1-5. Block Diagram of ispPAC-POWR1014 & ispPAC-POWR1014A Devices



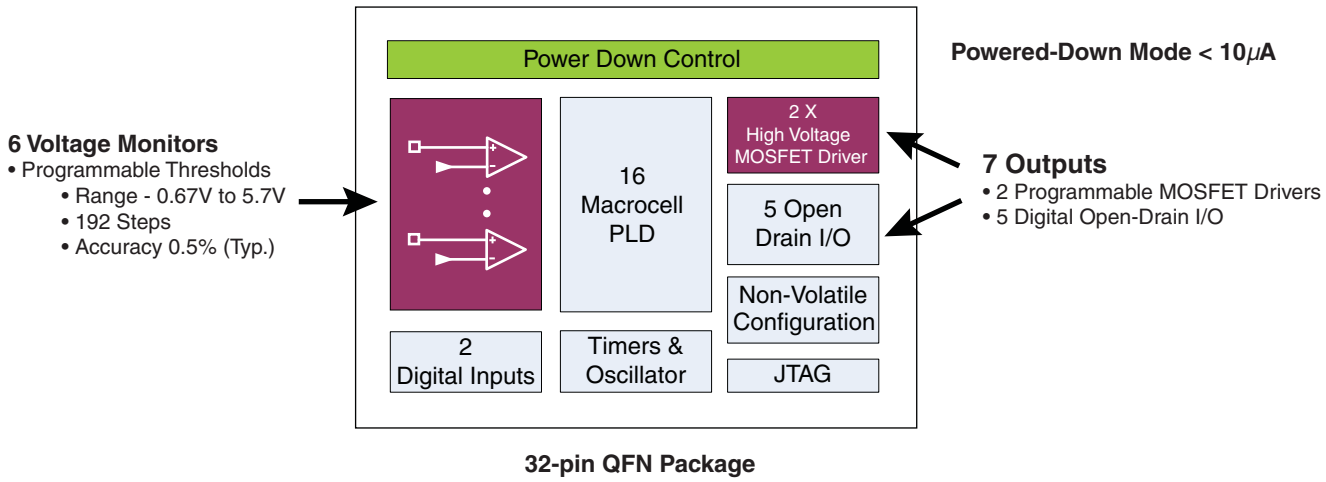
These devices can monitor up to 10 supply rails and generate 14 power management control outputs (including two programmable MOSFET drivers) using an on-chip 24-macrocell PLD block. The ispPAC-POWR1014A device provides a 10-bit ADC and an I^2C interface to measure all supply voltages. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

The ispPAC-POWR1014/A devices can integrate the following power management functions:

- Power Supply OR'ing
- Hot-swap controller for positive voltage rail
- Positive or negative power feed controller
- Sequencing
- Voltage and current monitoring
- Reset generation, sequencing
- Watchdog timer

The ispPAC-POWR607 device shown in Figure 1-6 can monitor up to six supplies and supports seven outputs (including two MOSFET drivers) that are controlled by the on-chip 16-macrocell PLD. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

Figure 1-6. Block Diagram of an ispPAC-POWR607 Device

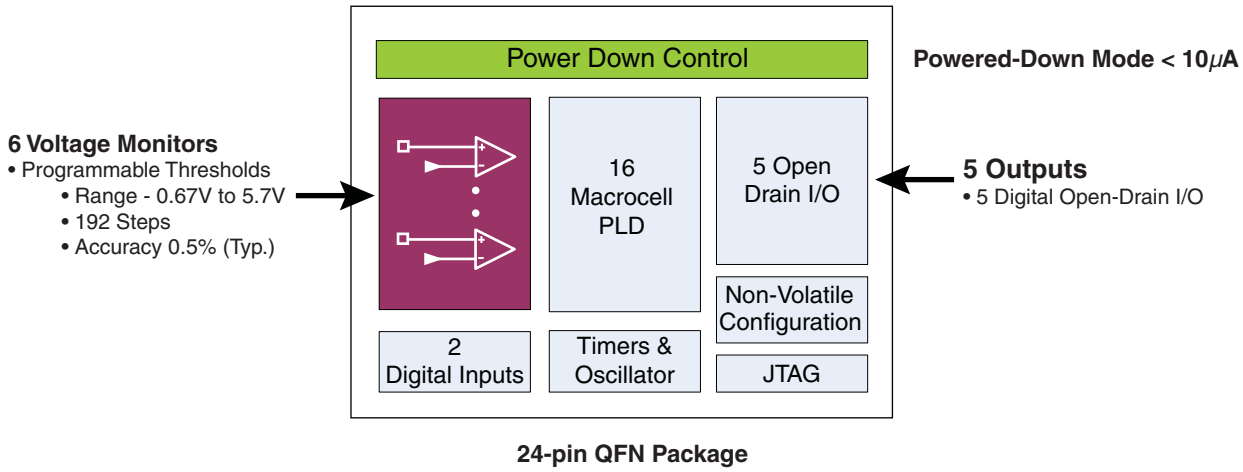


This device can be powered down using a digital signal. The ispPAC-POWR607 device can be used for the following functions:

- Power Supply OR'ing
- Hot-swap controller for positive voltage rail
- Hot-swap controller for negative voltage rail
- Positive or negative power feed controller sequencing
- Reset generation
- Watchdog timer

Figure 1-7 shows the ProcessorPM-POWR605 device, which is ideal for implementing power management functions for any processor or DSP. This device can monitor up to six supplies and generate five outputs that are controlled by the on-chip 16-macrocell PLD. Various time delays used in the power management algorithm can be realized by four on-chip programmable hardware timers.

Figure 1-7. Architecture of the ProcessorPM-POWR605 Device



The ProcessorPM-POWR605 device can be used to integrate the following functions:

- Voltage supervision
- Reset generation
- Watchdog timer

1.3 PAC-Designer Software

Board-specific power management is implemented using the PAC-Designer software: an intuitive, user-friendly software tool set. The PAC-Designer software enables the following:

1. Configure voltage monitoring thresholds for a given voltage rail.
2. Configure MOSFET driver characteristics to meet turn on and off ramp rates.
3. Implement power management functions such as hot-swap controller, sequencer, reset generator through LogiBuilder (simple configurable sequencer steps and logic equations).
4. Simulate the power management algorithm using either high-end tools such as Aldec® Active-HDL™ or Mentor Graphics® ModelSim™, or use the waveform simulator built into the software.
5. Calculate the resistor values to be connected between the Power Manager II devices and the DC-DC converters for implementing Trimming and Margining functions.
6. Generate JEDEC files and SVF files for programming the device using standard programming methods.

1.4 Summary of Chapters

This book has nine chapters. Chapter 3 to Chapter 8 each cover a power management function in detail.

Chapter 1 - “Introduction” on page 1-1 – summarizes the power management functions, explains drawbacks of traditional power management solutions, and provides a brief introduction to Lattice Power Manager II products.

Chapter 2 - "Solutions Summary" on page 2-1 – is a summary of all of the solutions provided for each of the power management functions shown in Figure 1-1.

Chapter 3 - "Reset Generators & Supervisors" on page 3-1 – describes reset generator supervisor and watchdog timer and identifies some of the common pitfalls to avoid in voltage supervision and reset generation in circuit boards with multiple power supplies.

Chapter 4 - "Power Supply Sequencing" on page 4-1 – shows how a flexible power supply sequencing arrangement provides a solution. This section also describes software-based sequencing methodology.

Chapter 5 - "Hot-Swap Controllers" on page 5-1 – describes design considerations for implementing hot-swap controllers and selecting MOSFETs. This chapter also provides hot-swap controller solutions for positive rail, negative rail, and multiple backplane rails.

Chapter 6 - "Power Supply OR'ing Controllers" on page 6-1 – describes the design considerations and provides N-rail positive and negative rail OR'ing solutions.

Chapter 7 - "Power Feed Controllers" on page 7-1 – provides design considerations for implementing power feed controllers and selecting MOSFETs. N-supply positive and negative rail power feed, and MicroTCA power module design, are also discussed.

Chapter 8 - "Margining and Trimming" on page 8-1 – describes the need for trimming and margining of supplies, provides trimming and margining solutions, and describes how to implement these designs using software.

Chapter 9 - "Design Tools for Power Manager II" on page 9-1 – describes the software flow, provides a description of each of the steps, and describes software implementation of complex power management designs.

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