LM3478,LM3488

Application Note 1204 LM3478/LM3488 Evaluation Board

Literature Number: SNVA042A

LM3478/LM3488 Evaluation Board

National Semiconductor
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Introduction

The LM3478 and LM3488 are current mode, low side N channel FET controllers. They can utilized in numerous configurations including a Boost, Flyback or SEPIC (Single Ended Primary Inductor Converter). This evaluation board demonstrates the flexibility of the LM3478 in a boost topology. The operating conditions for the evaluation board are listed below:

$4.5V \le V_{IN} \le 5.5V$

$V_{OUT} = 12V$

$0A \le I_{OUT} \le 1.5A$

The circuit and bill of materials for this design are given below:

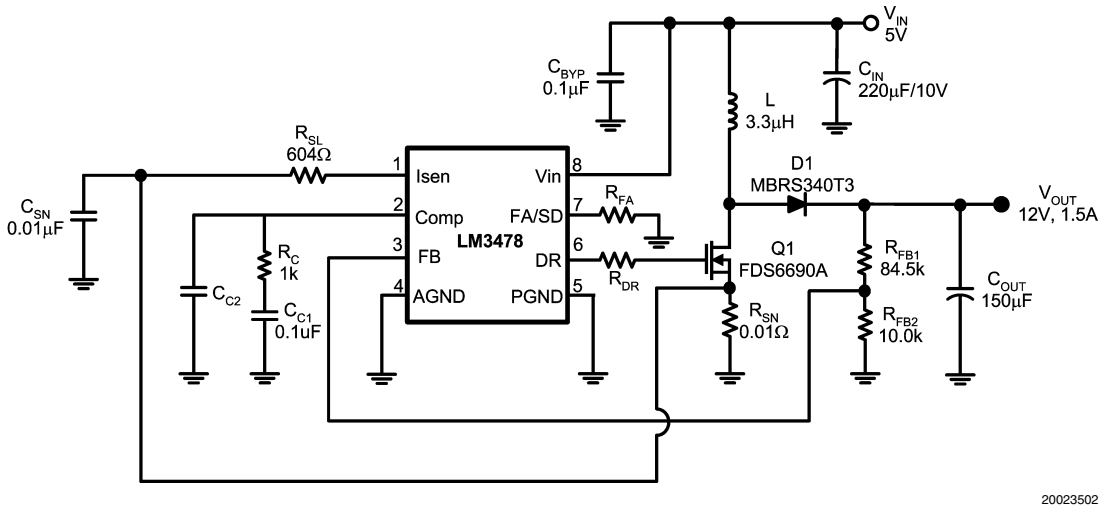

FIGURE 1. Circuit Diagram

TABLE 1. Bill of Materials

Component	Value	Model Number
U1		LM3478
L1	3.3µH	DO3316P-332 (Coilcraft)
Q1	30V/11A	FDS6690A (Fairchild)
D1	100V/3A	MBRS340T3 (Motorola)
C_{IN}	Tantalum, 220µF/10V	595D227X9010R2 (Sprague)
C_{OUT}	Tantalum, 150µF/16V	595D157X9016R2 (Sprague)
C_{OUT1}	No Connect	
C_{C1}	0.1µF/25V	VJ0805Y104KXXA (Vitramon)
C_{C2}	No Connect	
C_{BYP}	0.1µF/25V	VJ0805Y104KXXA (Vitramon)
C_{SEN}	0.01µF/25V	VJ0805Y103KXXA (Vitramon)
R_{FB1}	84.5kΩ	CRCW08058452 (Vitramon)
R_{FB2}	10kΩ	CRCW08051002 (Vitramon)
R_C	1kΩ	CRCW08051001 (Vitramon)
R_{SEN}	0.010Ω	(Dale, 1%, 1W, R01F, 2512)
R_{DR}	0Ω	CRCW0805600R0 (Vitramon)
R_{S1}	604Ω	CRCW08056040 (Vitramon)
R_{FA}	40.2kΩ	CRCW08054022 (Vitramon)

Performance

Benchmark data has been taken from the evaluation board using the LM3478. *Figure 2* shows an efficiency measurement taken at the maximum load of 1.5A with Vin at 5V.

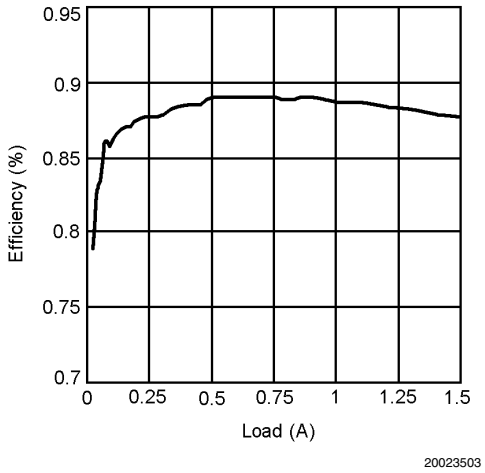

FIGURE 2. Efficiency vs Load

The open loop frequency response was also measured using the evaluation board as specified in the bill of materials. The bode plot can be seen below in *Figure 3*.

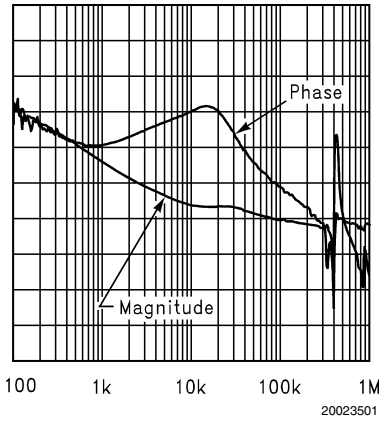

FIGURE 3. Frequency Response

The advantage of the evaluation board is the ability to examine performance tradeoffs through substitution of parts. By careful selection of the components used, it is possible to optimize the application circuit for a given parameter. For instance, the FET footprint has been designed to accommodate either a SO-8 or SOT23-6 package. The selection of FET would then be determined by the design constraints. An example would be that a lower system cost could be obtained by selection of a FET with a higher $R_{DS(ON)}$, although performance would be sacrificed through reduced efficiency.

Current Limit

The purpose of the R_{SL} resistor is to provide flexibility in the selection of the slope compensation needed for the required application. The amount of slope compensation directly determines the minimum inductance required for stability. (Please see the LM3478 or LM3488 datasheet for adjustment of slope compensation). In addition to slope compensation R_{SL} also provides assistance in the adjustment of current limit. Current limit is usually solely determined by the value of the sense resistor Rsn. But in the LM3478 and LM3488 an increase in R_{SL} causes the current limit to decrease by a slight amount. This can be advantageous in several situations. Common sense resistor values are typically separated by large intervals, making the task of accurately setting the current limit in any application difficult. As a result current limit is often ignored during the design phase, which can cause the application to suffer. An excessively high current limit can result in startup problems if the cycle-by-cycle current limit does not engage, limiting the effect of the soft start feature. Or worse, current limit could be set to low causing the output voltage to drop at the maximum load. This is where the R_{SL} resistor can be used to avoid these issues. By selecting a common value sense resistor, current limit can be accurately set by calculating the R_{SL} size needed. This eliminates the need to choose custom sense resistors that can be cost prohibitive and cause production issues because of the difficulty in obtaining an adequate supply. For a complete discussion on how to calculate the R_{SL} value needed, refer to the current limit section in the LM3478 or LM3488 datasheet.

Layout Fundamentals

Good layout for DC-DC converters can be implemented by following a few simple design guidelines:

1. Place the power components (catch diode, inductor, and filter capacitors) close together. Make the traces between them as short and wide as possible.
2. Use wide traces between the power components and for power connections to the DC-DC converter circuit.
3. Connect the ground pins of the input and output filter capacitors and catch diode as close as possible using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground plane through several vias.
4. Arrange the power components so that the switching loops curl in the same direction.
5. Separate noise sensitive traces, such as the voltage feedback path, from noisy traces associated with the power components.
6. Ensure a good low-impedance ground for the converter IC.
7. Place the supporting components for the converter IC, such as compensation and frequency selection components as close to the converter IC as possible, but away from noisy traces and the power components. Make their connections to the converter IC and its pseudo-ground plane as short as possible.
8. Place noise sensitive circuitry such as radio or modem blocks away from the DC-DC converter.

Layout Fundamentals (Continued)

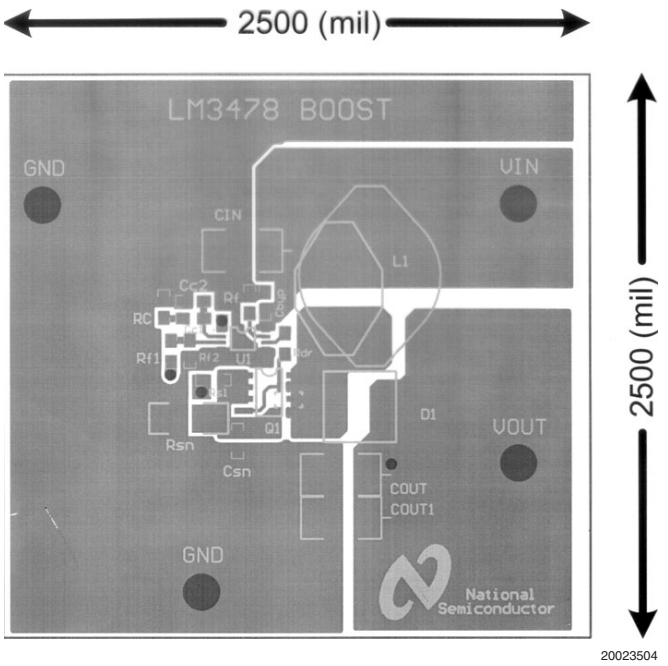

FIGURE 4. Front Side

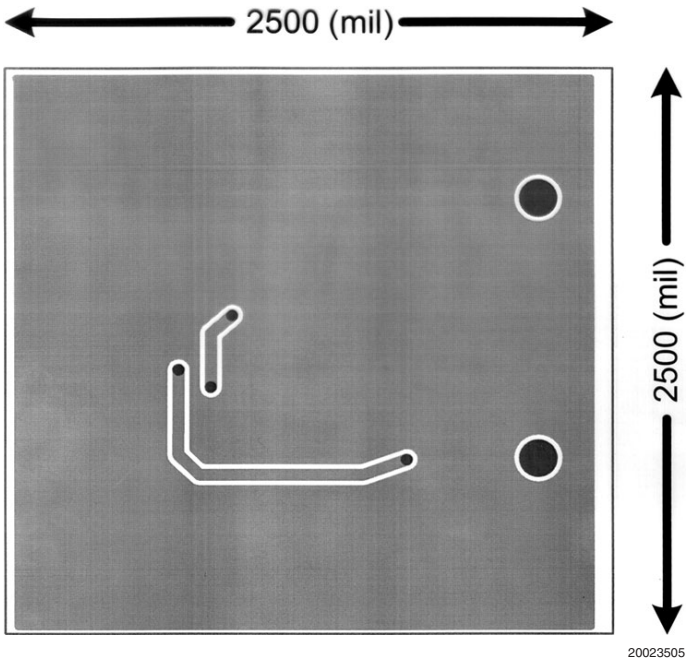

FIGURE 5. Back Side

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