Address: Midas Displays, Electra House, 32 Southtown Road, Great Yarmouth, Norfolk, NR31 0DU
Telephone: +44 (0)1493 602602
Fax: +44 (0)1493 665111
Email: sales@midasdisplays.com
Website: www.midasdisplays.com

Specification

MCOT096096AZ-RGBM

Address: Midas Displays, Electra House, 32 Southtown Road, Great Yarmouth, Norfolk, NR31 0DU
Telephone: +44 (0)1493 602602
Fax: +44 (0)1493 665111
Email: sales@midasdisplays.com
Website: www.midasdisplays.com

Midas Displays OLED Part Number System

MCO	B	21605	A	*	V	-	E	W	I	*
1	2	3	4	5	6		7	8	9	10

1	=	**MCO:**	Midas Displays OLED
2	=	**Blank:**	**B**: COB (Chip on Board) **T**: TAB (Taped Automated Bonding)
3	=	**No of dots:**	**(**e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)
4	=	**Series**	A to Z
5	=	**Series Variant:**	A to Z and 1 to 9 **– see addendum**
6	=	**Operating Temp Range:**	**B:** -40+70° C **V:** -40+80° C **Y:** -40 +70° C **Z:** -30+70° C
7	=	**Character Set:**	**Blank**: Not Applicable **E:** Multi European Font Set (English/Japanese – Western European (K) – Cyrillic (R))
8	=	**Colour:**	**Y:** Yellow **W:** White **B:** Blue **R:** Red **G:** Green **RGB**: Full Colour
9	=	**Interface:**	**P:** Parallel **I:** I²C **S:** SPI **M:** Multi
10	=	**Voltage Variant:**	e.g. **3** = 3v

Contents

MIDAS DISPLAYS

1. Basic Specifications

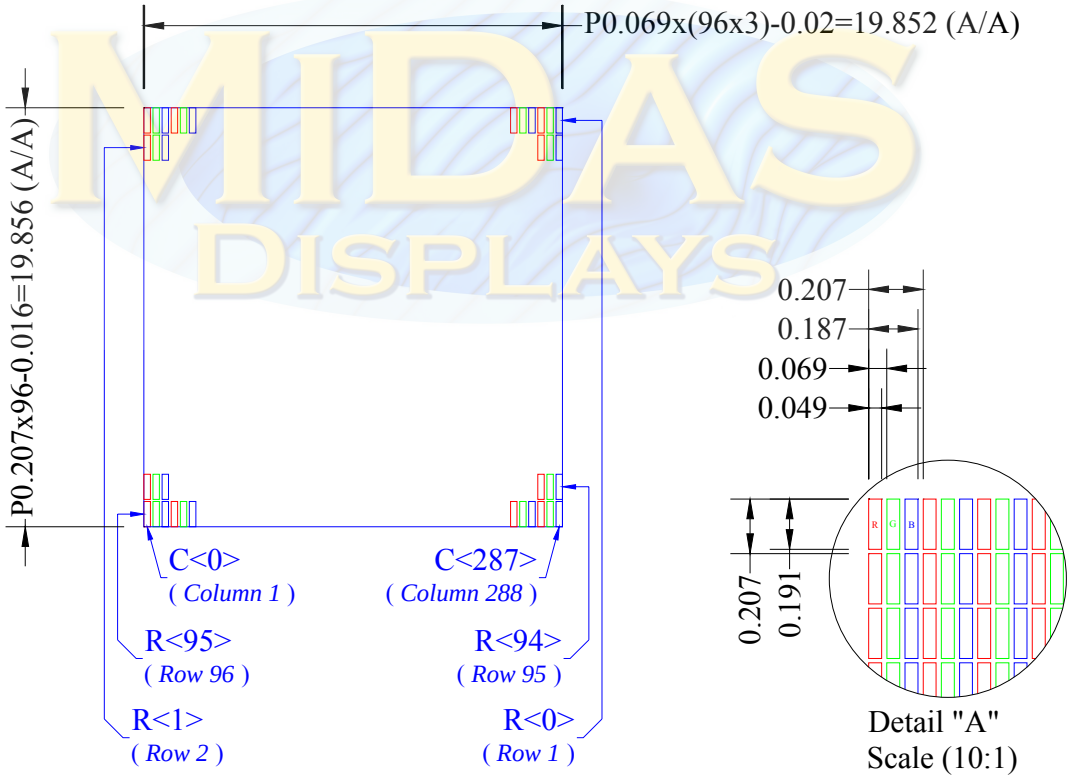
1.1 Display Specifications

1)	Display Mode:	Passive Matrix
2)	Display Color:	65,536 Colors (Maximum)
3)	Drive Duty:	1/96 Duty

1.2 Mechanical Specifications

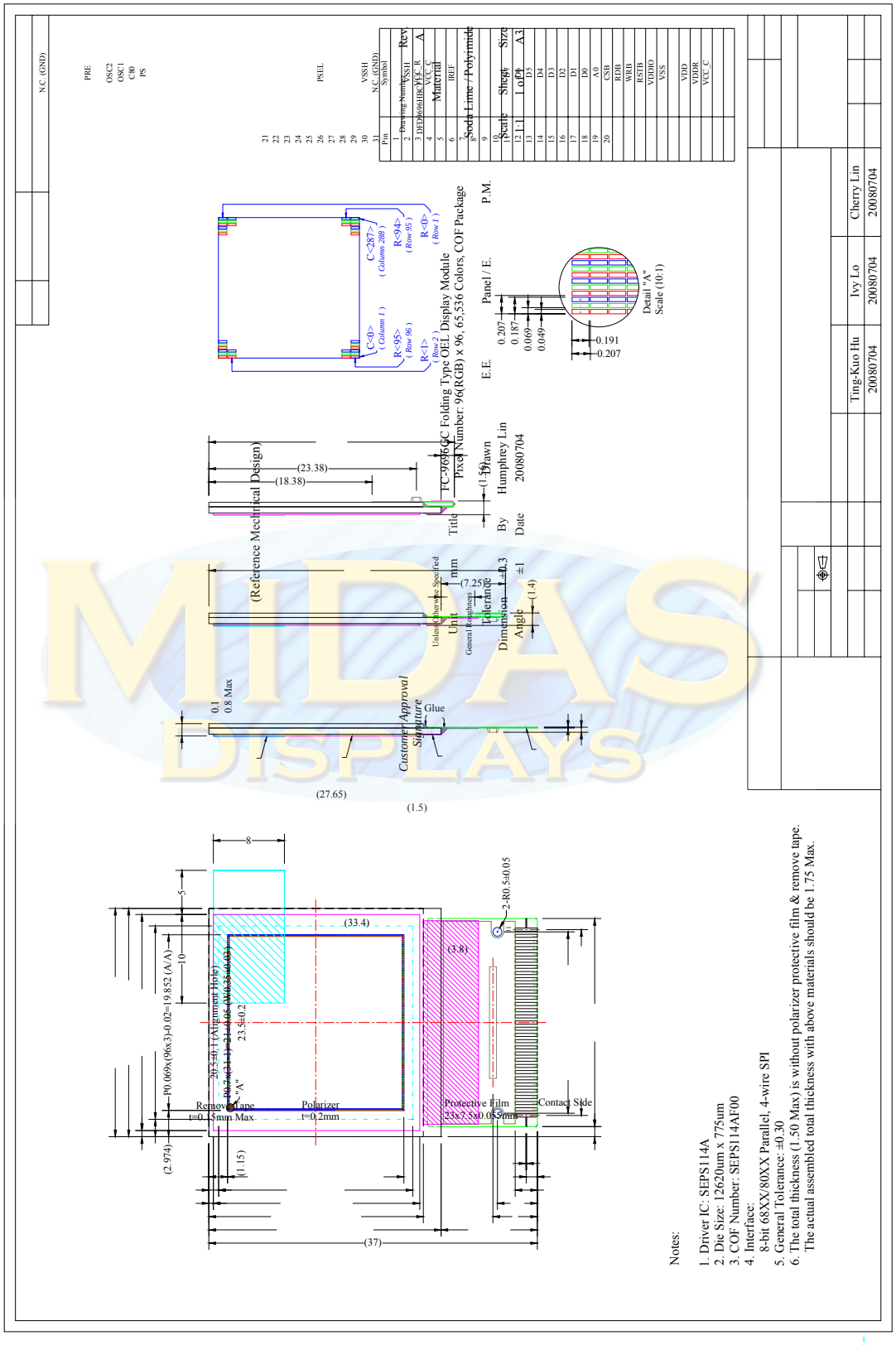
1)	Outline Drawing:	According to the annexed outline drawing
2)	Number of Pixels:	96 (RGB) × 96
3)	Panel Size:	25.80 × 26.15 × 1.40 (mm)
4)	Active Area:	19.852 × 19.856 (mm)
5)	Pixel Pitch:	0.069 × 0.207 (mm)
6)	Pixel Size:	0.049 × 0.191 (mm)
7)	Weight:	1.95 (g)

1.3 Active Area & Pixel Construction



MIDAS DISPLAYS

1.4 Mechanical Drawing



MIDAS DISPLAYS

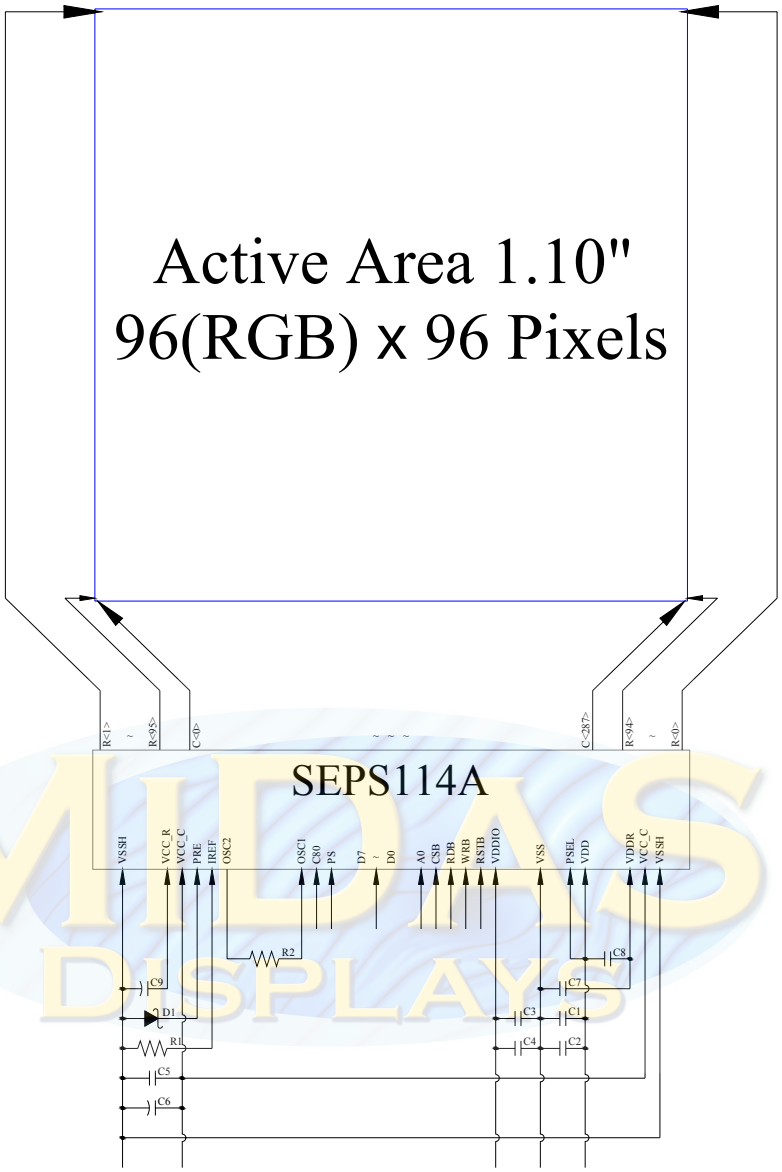
1.5 Pin Definition

Pin Number	Symbol	Type	Function
Power Supply			
27	VDD	P	*Power Supply for Operation* This is a voltage supply pin. It must be connected to external source.
28	VDDR	P	*Power Supply for Core Logic Circuit* This is a voltage supply pin. It can be supplied externally or regulated internally from VDD. A capacitor should be connected between this pin & VSS under all circumstances.
24	VDDIO	P	*Power Supply for I/O Pin* This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signal should have VIH reference to VDDIO. When I/O signal pins (C80, PS, D0~D7, control signals…) pull high, they should be connected to VDDIO.
25	VSS	P	*Ground of Logic Circuit* A reference for the logic pins. It must be connected to external ground.
4, 29	VCC_C	P	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. It must be connected to external source.
2, 30	VSSH	P	*Ground of OEL Panel* This is the ground pins for analog circuits. It must be connected to external ground.
Driver			
5	PRE	I/O	*External Voltage Reference for Pre-charge Signal* This is the precharge driving voltages for OEL driving segment pins respectively. A zener diode should be connected between this pin and VSS.
6	IREF	I/O	*Current Reference for Brightness Adjustment* This is the current reference pin to generate precharge and driving current. A 39kΩ resistor should be connected between this pin and VSS.
3	VCC_R	P	*Voltage Output High Level for Scan Signal* This is the scan driver power supply pin. A tantalum capacitor should be connected between this pin and VSS.
Clock			
8 7	OSC1 OSC2	I O	*Fine Adjustment for Oscillation* The frequency is controlled by external 27kΩ resistor between OSC1 and OSC2. The oscillator signal is used for system clock generation. When the external clock mode is selected, OSC1 is used external clock input.
Configuration			
26	PSEL	I	*Regulator Enable/Disable for Logic Power Supply* This pin is the regulator enable/disable input of VDDR. If it is connected to VDD, the internal regulator is used. Otherwise, an external voltage supplier should be used.

1.5 Pin Definition (Continued)

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>Type</th><th>Function</th></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>9</td><td>C80</td><td>I</td><td>Select the CPU Type
Low: 80XX-Series MCU
High: 68XX-Series MCU.</td></tr>
<tr><td>10</td><td>PS</td><td>I</td><td>Select Parallel/Serial Interface Type
Low: Serial Interface
High: Parallel Interface</td></tr>
<tr><td>23</td><td>RSTB</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>20</td><td>CSB</td><td>I</td><td>Chip Select
Low: SEPS114A is selected and can be accessed.
High: SEPS114A is not selected and cannot be accessed.</td></tr>
<tr><td>19</td><td>A0</td><td>I</td><td>Data/Command Control
Low: Command
High: Parameter/Data</td></tr>
<tr><td>21</td><td>RDB</td><td>I</td><td>Read or Read/Write Enable
68XX Parallel Interface: Bus Enabled Strobe (Active High)
80XX Parallel Interface: Read Strobe Signal (Active Low)
While using SPI, it must be connected to VDD or VSS.</td></tr>
<tr><td>22</td><td>WRB</td><td>I</td><td>Write or Read/Write Select
68XX Parallel Interface: Read (Low)/Write (High) Select
80XX Parallel Interface: Write Strobe Signal (Active Low)
While using SPI, it must be connected to VDD or VSS.</td></tr>
<tr><td>11~18</td><td>D7~D0</td><td>I/O</td><td>Host Data Input/Output Bus
These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus.
<table>
<tr><th>PS</th><th>Description</th></tr>
<tr><td>0</td><td>D[0] SCL: Synchronous Clock Input
D[1] SDI: Serial Data Input
D[2] SDO: Serial Data Output
D[3] R/W: Serial Read (High)/Write (Low)</td></tr>
<tr><td>1</td><td>8-bit Bus: D[7:0]</td></tr>
</table>
While using SPI, the unused pins must be connected to VSS.</td></tr>
<tr><td colspan="4">Reserve</td></tr>
<tr><td>1, 31</td><td>N.C. (GND)</td><td>-</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
</table>

1.6 Block Diagram



MCU Interface Selection: C80, PS
Pins connected to MCU interface: D7~D0, A0, CSB, RDB, WRB, and RSTB

C1, C3, C5: 0.1µF
C2, C4, C8: 4.7µF
C6, C9: 4.7µF / 25V Tantalum Capacitor
C7: 2.2µF
R1: 39kΩ
R2: 27kΩ
D1: 2.7V, 0.5W Zener Diode

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Operation	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for I/O Pins	V_{DDIO}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC_C}	-0.3	16	V	1, 2
Operating Temperature	T_{OP}	-30	70	°C	-
Storage Temperature	T_{STG}	-40	80	°C	-

Note 1: All the above voltages are on the basis of "VSS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

MIDAS DISPLAYS

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	With Polarizer	0.26 0.29	0.30 0.33	0.34 0.37	
C.I.E. (Red)	(x) (y)	With Polarizer	0.60 0.30	0.64 0.34	0.68 0.38	
C.I.E. (Green)	(x) (y)	With Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	
C.I.E. (Blue)	(x) (y)	With Polarizer	0.10 0.12	0.14 0.16	0.18 0.20	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC_C} = 13V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{DD}		2.4	2.8	3.3	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	2.8	V_{DD}	V
Supply Voltage for Display	V_{CC_C}	Note 3	12.5	13	13.5	V
High Level Input	V_{IH}		$0.8\times V_{DDIO}$	-	V_{DDIO}	V
Low Level Input	V_{IL}		0	-	0.4	V
High Level Output	V_{OH}	I_{OH} = -0.1mA	V_{DDIO}-0.4	-		V
Low Level Output	V_{OL}	I_{OL} = -0.1mA		-	0.4	V
Operating Current for V_{DD}	I_{DD}		-	2.5	3.5	mA
Operating Current for V_{CC_C}	I_{CC_C}	Note 4	-	12.1	15.2	mA
		Note 5	-	20.2	25.3	mA

Note 3: Brightness (L_{br}) and Supply Voltage for Display (V_{CC_C}) are subject to the change of the panel characteristics and the customer's request.
Note 4: V_{DD} = 2.8V, V_{CC_C} = 13V, 50% Display Area Turn on.
Note 5: V_{DD} = 2.8V, V_{CC_C} = 13V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

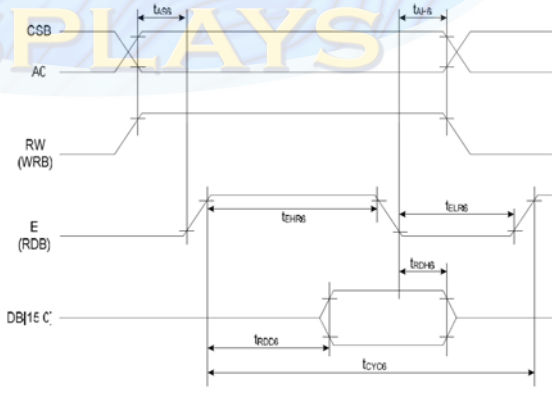
3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

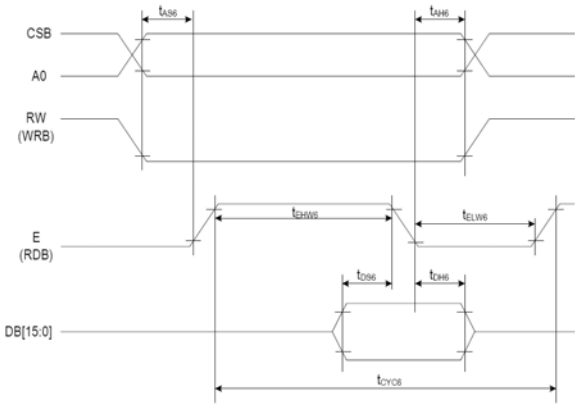
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description		Min	Max	Unit	Port
t_{AH6}	Address Setup Timing	(Read)	10	-	ns	CSB RS
		(Write)	5	-	ns	
t_{AS6}	Address Hold Timing	(Read)	10	-	ns	
		(Write)	5	-	ns	
t_{CYC6}	System Cycle Timing		200	-	ns	E
t_{ELR6}	Read "L" Pulse Width		90	-	ns	
t_{EHR6}	Read "H" Pulse Width		90	-	ns	
t_{CYC6}	System Cycle Timing		100	-	ns	
t_{ELW6}	Write "L" Pulse Width		45	-	ns	
t_{EHW6}	Write "H" Pulse Width		45	-	ns	
t_{RDD6}	Read Data Output Delay Time * CL = 15pF		0	70	ns	D[17:9]
t_{RDH6}	Data Hold Timing		0	70	ns	
t_{DS6}	Data Setup Timing		40	-	ns	
t_{DH6}	Data Hold Timing		10	-	ns	

* All the timing reference is 10% and 90% of V_{DD}.



(Read Timing)



(Write Timing)

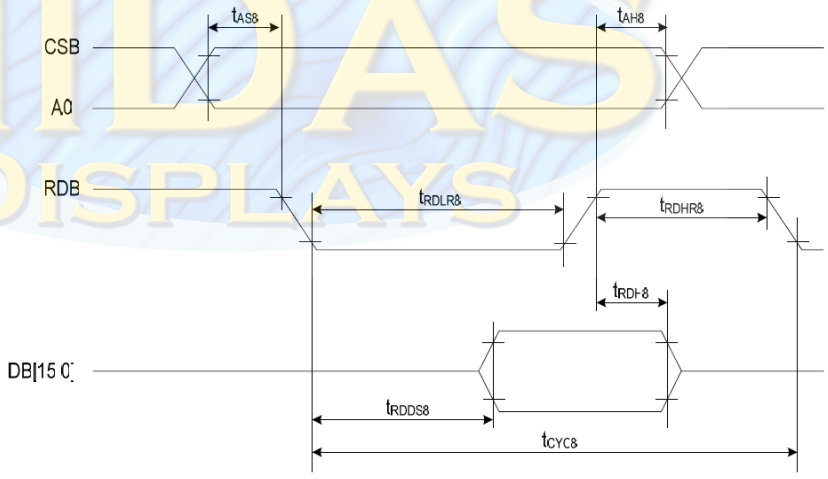
MIDAS DISPLAYS

3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

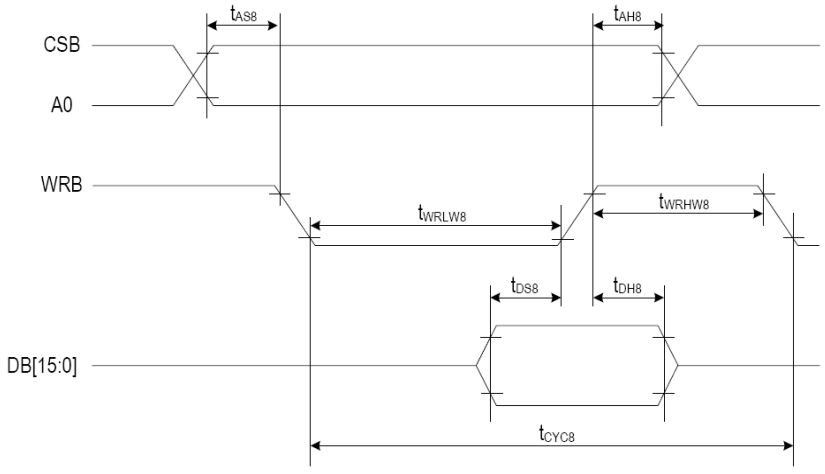
(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Description	Min	Max	Unit	Port
t_{AS8}	Address Setup Timing	5	-	ns	CSB A0
t_{AH8}	Address Hold Timing	5	-	ns	
t_{CYC8}	System Cycle Timing	200	-	ns	RDB
t_{RDLR8}	Read "L" Pulse Width	90	-	ns	
t_{RDHR8}	Read "H" Pulse Width	90	-	ns	
t_{CYC8}	System Cycle Timing	100	-	ns	WRB
t_{WRLW8}	Write "L" Pulse Width	45	-	ns	
t_{WRHW8}	Write "H" Pulse Width	45	-	ns	
t_{RDD8}	Read Data Output Delay Time * CL = 15pF	-	60	ns	D[7:0]
t_{RDH8}	Data Hold Timing	0	60	ns	
t_{DS8}	Data Setup Timing	30	-	ns	
t_{DH8}	Data Hold Timing	10	-	ns	

* All the timing reference is 10% and 90% of V_{DD}.



(Read Timing)



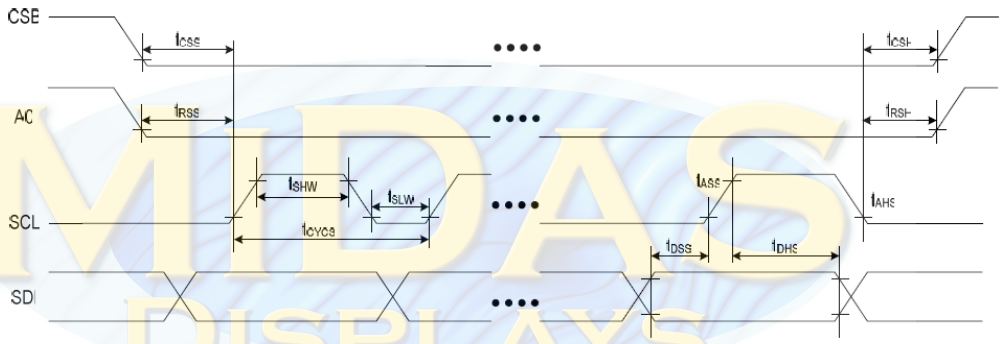
(Write Timing)

3.3.3 Serial Interface Timing Characteristics:

(V_{DD} = 2.8V, T_a = 25°C)

Symbol	Item	Min	Max	Unit	Port
t_{CYCS}	Serial Clock Cycle	200	-	ns	SCL
t_{SLW}	SCL "L" Pulse Width	90	-	ns	
t_{SHW}	SCL "H" Pulse Width	90	-	ns	
t_{DSS}	Data Setup Timing	25	-	ns	SDI
t_{DHS}	Data Hold Timing	25	-	ns	
t_{CSS}	CSB-SCL Timing	25	-	ns	CSB
t_{CSH}	CSB-Hold Timing	25	-	ns	
t_{RSS}	RS-SCL Timing	25	-	ns	A0
t_{RSH}	RS-Hold Timing	25	-	ns	

* All the timing reference is 10% and 90% of V_{DD}.



MIDAS DISPLAYS

4. Functional Specification

4.1. Commands

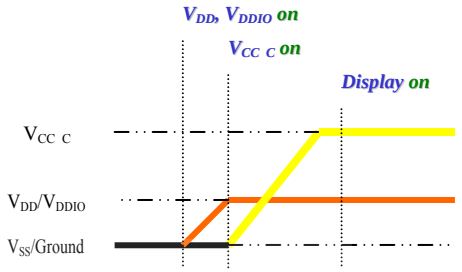
Refer to the Technical Manual for the SEPS114A

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

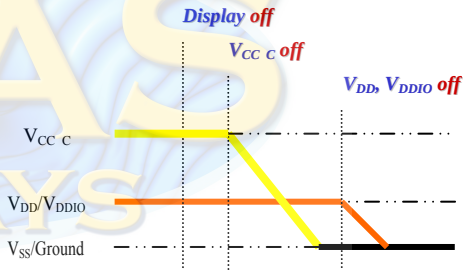
4.2.1 Power up Sequence:

1. Power up V_{DD} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC_C}
6. Delay 100ms
   (when V_{CC_C} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC_C}
3. Delay 100ms
   (when V_{CC_C} is reach 0 and panel is completely discharges)
4. Power down V_{DD} & V_{DDIO}



4.3 Reset Circuit

When RSTB input is low, the chip is initialized with the following status:

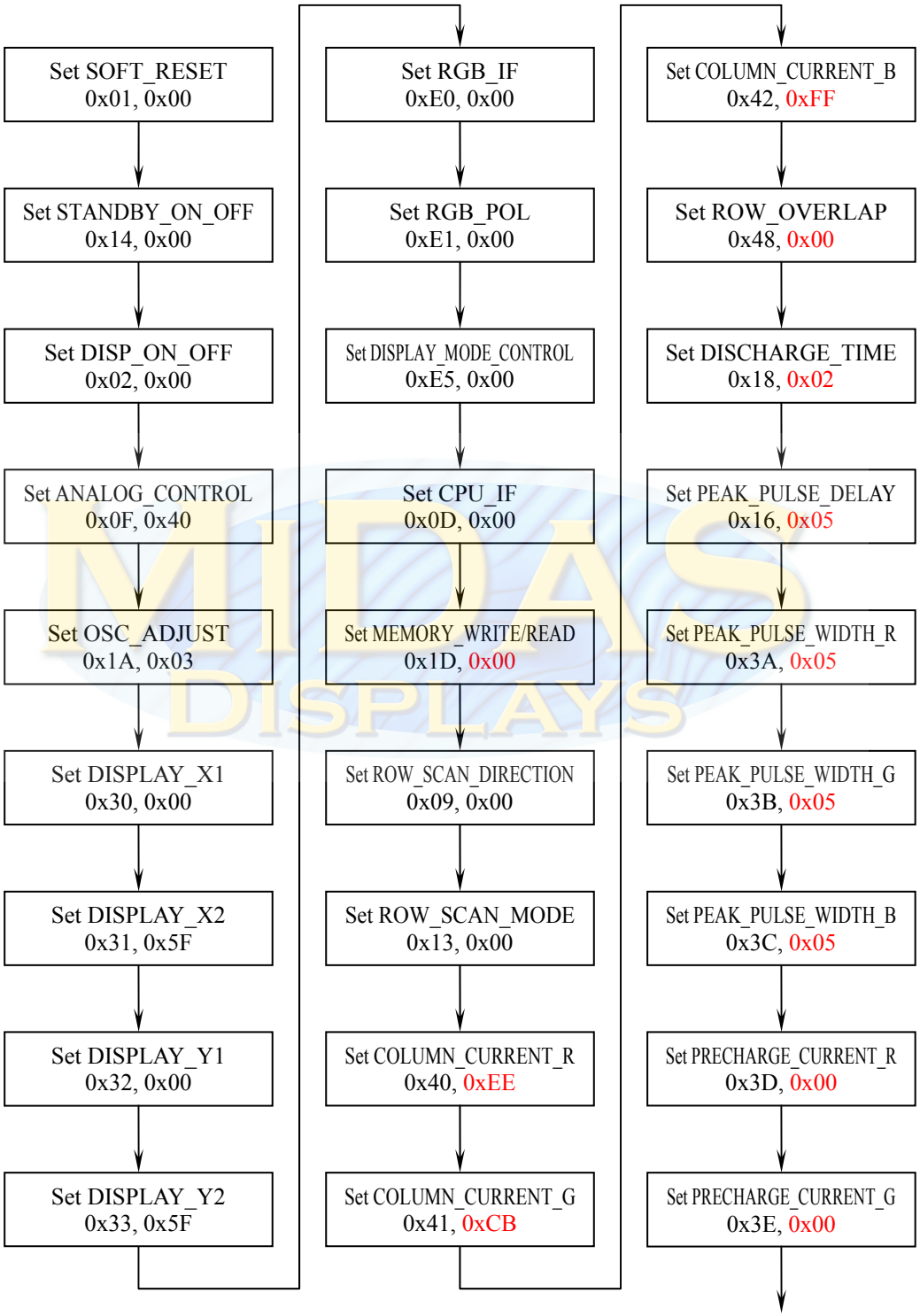
1. Standby Mode: On
2. Frame Frequency: 95Hz
3. Oscillation: Internal Oscillator Off
4. DDRAM Write Horizontal Address: XS = 0x00, XE = 0x5F
5. DDRAM Write Vertical Address: YS = 0x00, YE = 0x5F
6. Display Data RAM Write: MDIR1 = 0, MDIR0 = 0, VH = 0
7. Row Scan Shift Direction: R0, R1, … , R94, R95
8. Column Data Shift Direction: C0, C1, … , C286, C287
9. Display On/Off: Off
10. Panel Display Size: FX = 0x00, TX = 0x5F, FY = 0x00, TY = 0x5F
11. Display Data RAM Read Column/Row Address: DX = 0x00, DY = 0x00
12. Discharge Time: 8 Clock
13. Peak Pulse Delay: 5 Clock
14. Peak Pulse Width Time (R/G/B): 5 Clock
15. Precharge Current (R/G/B): 0µA

16. Driving Current (R/G/B): 0μA

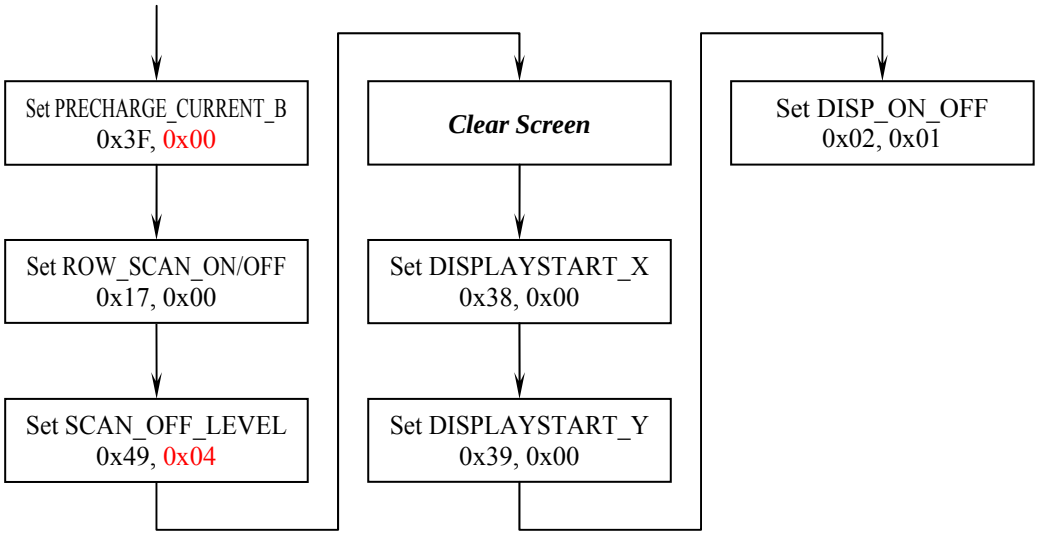
4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization>



MIDAS DISPLAYS



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

MIDAS DISPLAYS

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-30°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

Lifetime 65 cd/m^2, 30,000 hours(TYP) Note6.

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. *Outgoing Quality Control Specifications*

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

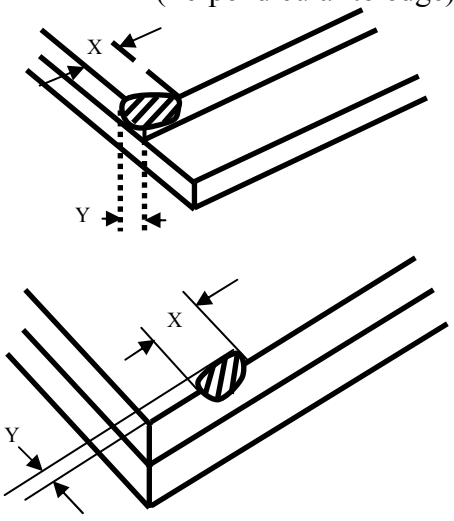
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

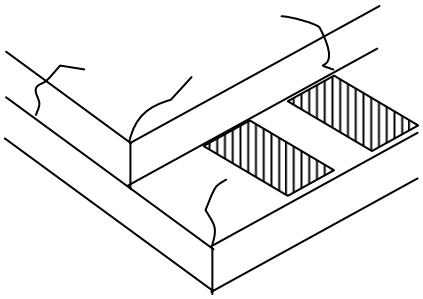
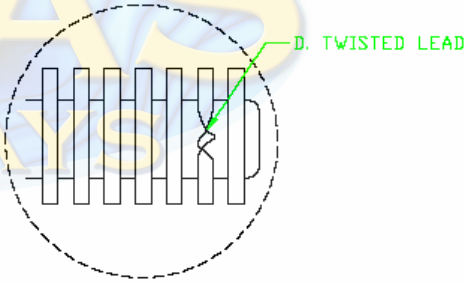
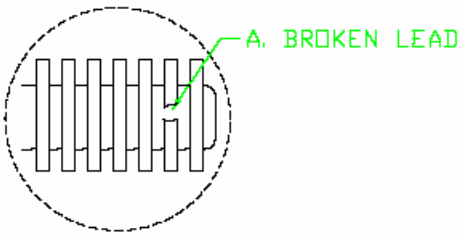
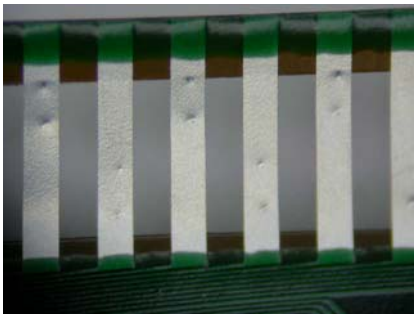
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

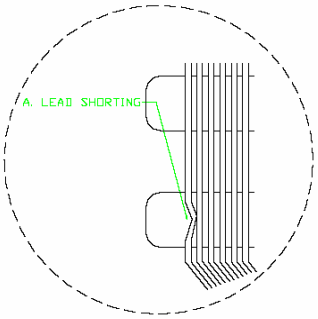
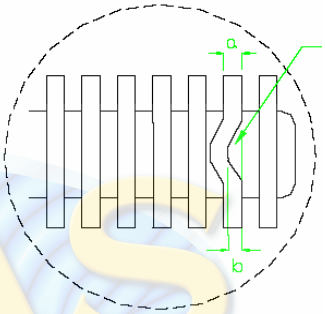
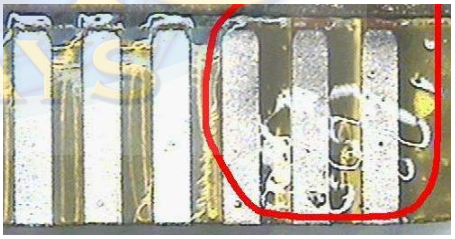
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

MIDAS DISPLAYS

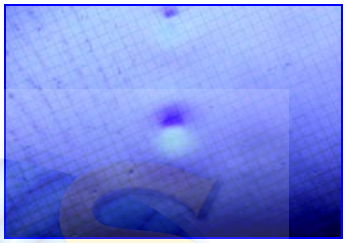
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

MIDAS DISPLAYS

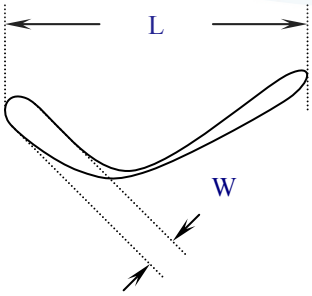
6.3.2 Cosmetic Check (Display Off) in Active Area

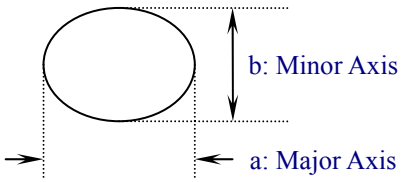
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1, L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.25 n ≤ 1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

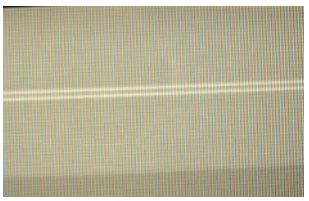
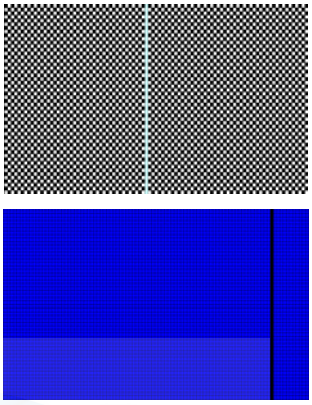
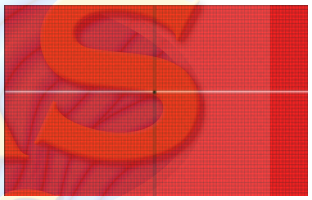
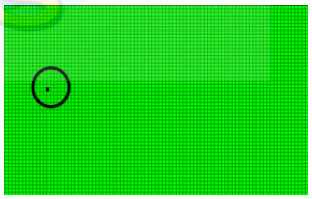
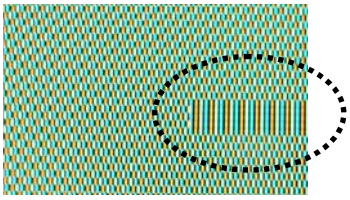
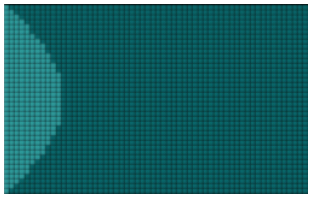
** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





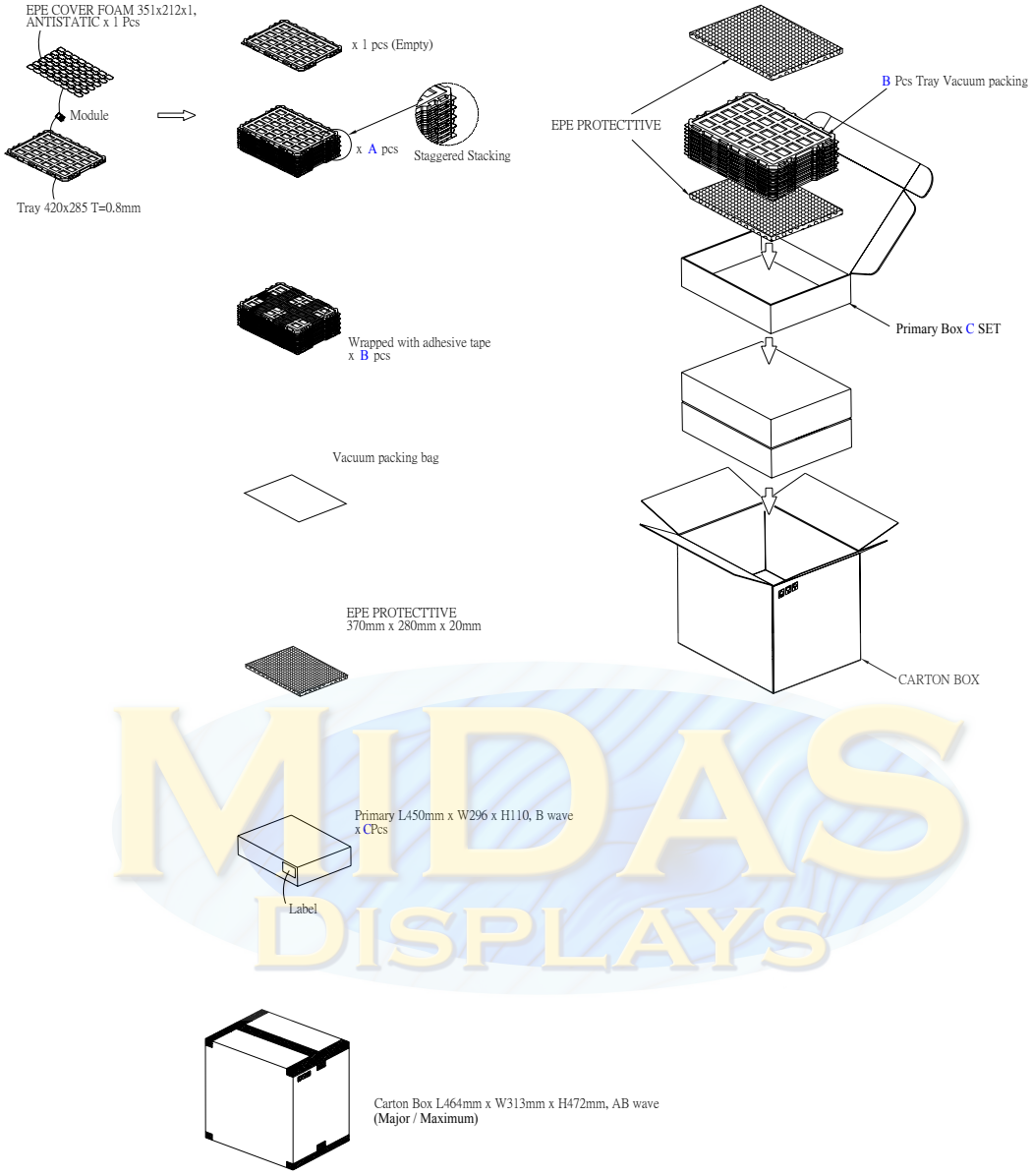
MIDAS DISPLAYS

6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	Not allowable
Bright Line	Major	
Missed Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-Uniform (Luminance Variation within a Display)	Major	

MIDAS DISPLAYS

7. Package Specifications



Item		Quantity	
Holding Trays	(A)	15	per Primary Box
Total Trays	(B)	16	per Primary Box (Including 1 Empty Tray)
Primary Box	(C)	1~4	per Carton (4 as Major / Maximum)

MIDAS DISPLAYS

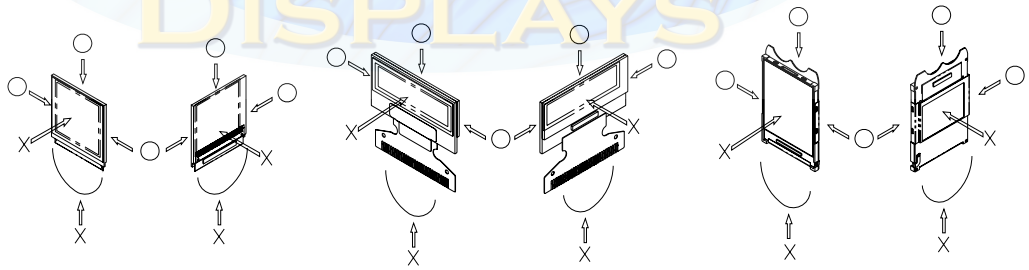
8. *Precautions When Using These OEL Display Modules*

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold the OEL display module very carefully when placing the OEL display module onto/into any device. Do not apply excessive stress or pressure to the OEL module. And, do not over bend the film with electrode layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes

the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Midas Displays. At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SEPS114A
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.