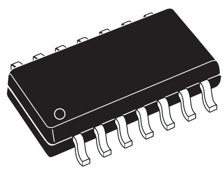
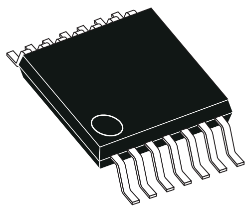
LM224A, LM324A

Low power quad operational amplifiers

Datasheet - production data



D
SO14
(plastic micropackage)



P
TSSOP14
(thin shrink small outline package)

Features

- Wide gain bandwidth: 1.3 MHz
- Input common mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current/amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset voltage: 3 mV max.
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: +3 V to +30 V
  - Dual supplies: ±1.5 V to ±15 V

Description

These circuits consist of four independent, high gain operational amplifiers with frequency compensation implemented internally. They operate from a single power supply over a wide range of voltages.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
LM224ADT	-40 °C to 105 °C	SO14	Tape and reel
LM224APT		TSSOP14	
LM324ADT	0 °C to 70 °C	SO14	
LM324APT		TSSOP14	

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1 Pin connections and schematic diagram

Figure 1. Pin connections (top view)

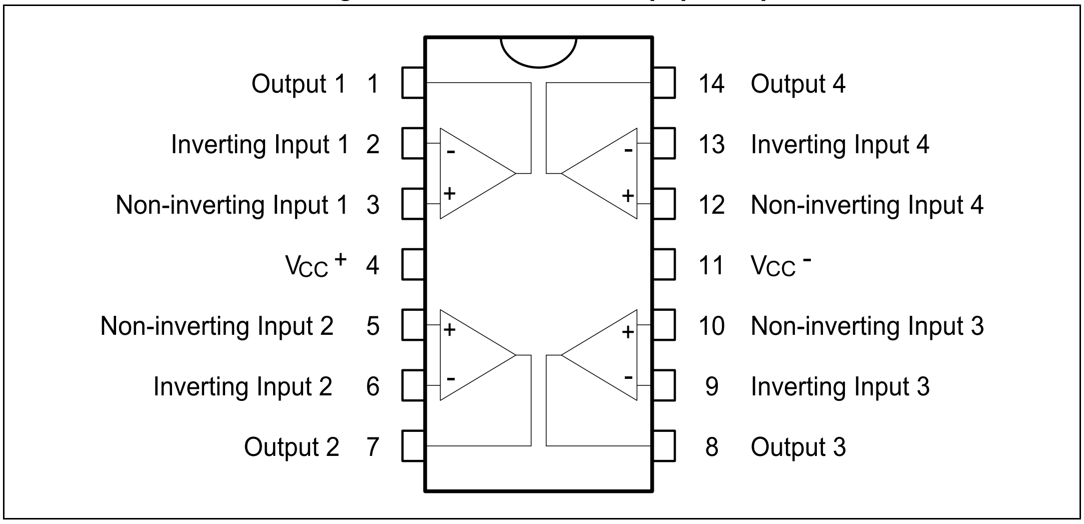
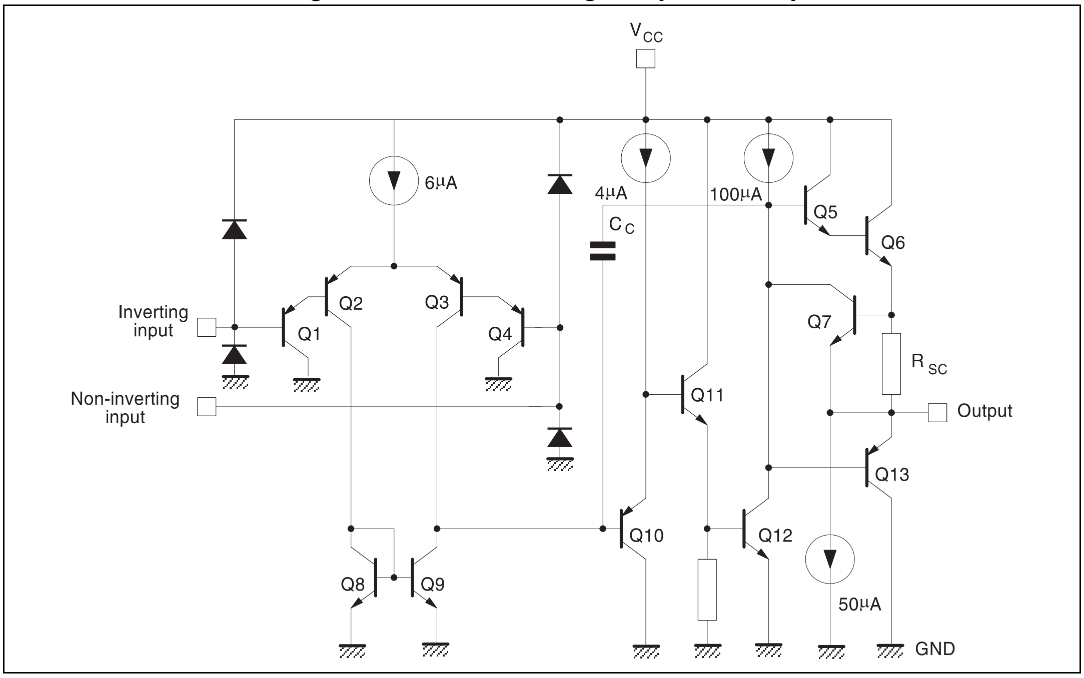


Figure 2. Schematic diagram (1/4 LM124)



2 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	LM224A	LM324A	Unit
V_{CC}	Supply voltage	±16 or 32		V
V_i	Input voltage	-0.3 to V_{CC} + 0.3		V
V_{id}	Differential input voltage (1)	32		V
P_{tot}	Power dissipation: D suffix	400		mW
	Output short-circuit duration (2)	Infinite		
I_{in}	Input current (3)	50		mA
T_{oper}	Operating free-air temperature range	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150		°C
T_j	Maximum junction temperature	150		°C
R_{thja}	Thermal resistance junction to ambient(4): SO14 TSSOP14	103 100		°C/W
R_{thjc}	Thermal resistance junction to case: SO14 TSSOP14	31 32		°C/W
ESD	HBM: human body model(5)	700		V
ESD	MM: machine model(6)	150		V
ESD	CDM: charged device model	1500		V

1. Neither of the input voltages must exceed the magnitude of V_{CC}^+ or V_{CC}^-.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP which is a two-layer board).
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

3 Electrical characteristics

Table 3. V_{CC}^+ = +5 V, V_{CC}^-= Ground, V_o = 1.4 V, T_{amb} = +25 °C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage(1): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		2	3 5	mV
I_{io}	Input offset current: T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		2	20 40	nA
I_{ib}	Input bias current(2): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$		20	100 200	nA
A_{vd}	Large signal voltage gain: V_{CC}^+ = +15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \leq$ 10 kΩ): V_{CC}^+ = 5 V to 30 V T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	65 65	110		dB
I_{CC}	Supply current, all Amp, no load: – T_{amb} = +25° C V_{CC} = +5V V_{CC} = +30 V – $T_{min} \leq T_{amb} \leq T_{max}$ V_{CC} = +5 V V_{CC} = +30 V		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input common mode voltage range: V_{CC} = +30 V (3) T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common mode rejection ratio ($R_s \leq$10 kΩ): T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	70 60	80		dB
I_{source}	Output current source (V_{id} = +1 V): V_{CC} = +15 V, V_o = +2 V	20	40	70	mA
I_{sink}	Output sink current (V_{id} = -1 V): V_{CC} = +15 V, V_o = +2 V V_{CC} = +15 V, V_o = +0.2 V	10 12	20 50		mA µA

Table 3. V_{CC}^+ = +5 V, V_{CC}^-= Ground, V_o = 1.4 V, T_{amb} = +25 °C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage V_{CC} = +30 V, R_L = 2 kΩ T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 26 26	 27		V
	V_{CC} = +30 V, R_L = 10 kΩ T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 27 27	 28		
	V_{CC} = +5 V, R_L = 2 kΩ T_{amb} = +25° C $T_{min} \leq T_{amb} \leq T_{max}$	 3.5 3			
V_{OL}	Low level output voltage (R_L = 10kΩ): T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		 5	 20 20	mV
SR	Slew rate: V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.4		V/µs
GBP	Gain bandwidth product: V_{CC} = 30 V, f =100 kHz, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100pF		1.3		MHz
THD	Total harmonic distortion: f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_{CC} = 30V		0.015		%
e_n	Equivalent input noise voltage: f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel separation(4) - 1kHz ≤ f ≤ 20 kHZ		120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no load change on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of external components, ensure that there is no coupling originating from stray capacitance between these external parts. Typically, this can be detected at higher frequencies because this type of capacitance increases.

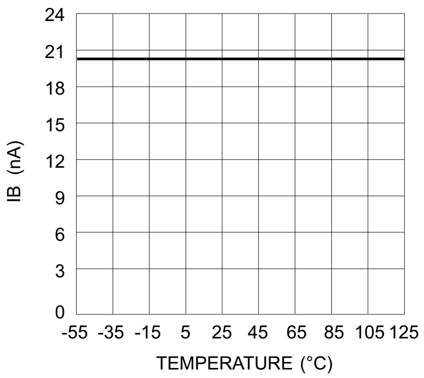


Figure 3. Input bias current vs. temperature

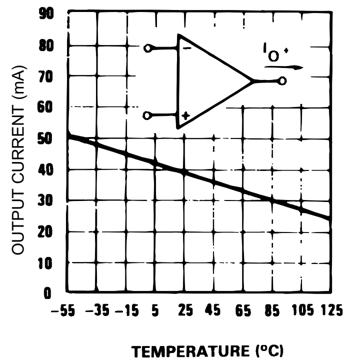


Figure 4. Output current limitation

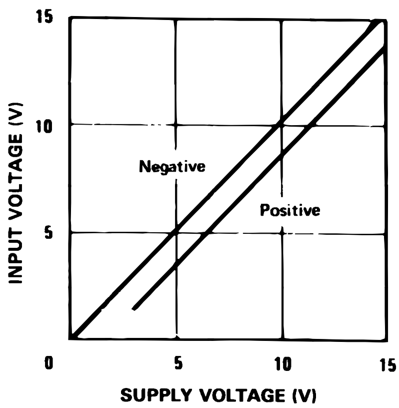


Figure 5. Input voltage range

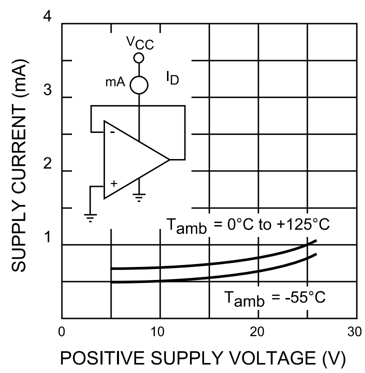


Figure 6. Supply current vs. supply voltage

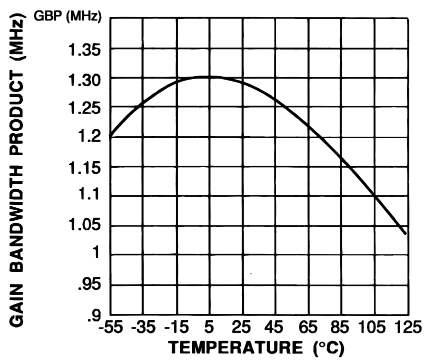


Figure 7. Gain bandwidth product vs. temperature

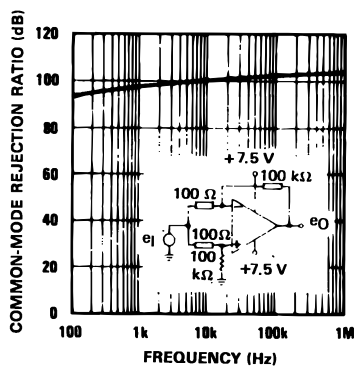


Figure 8. Common mode rejection ratio

Figure 9. Open loop frequency response

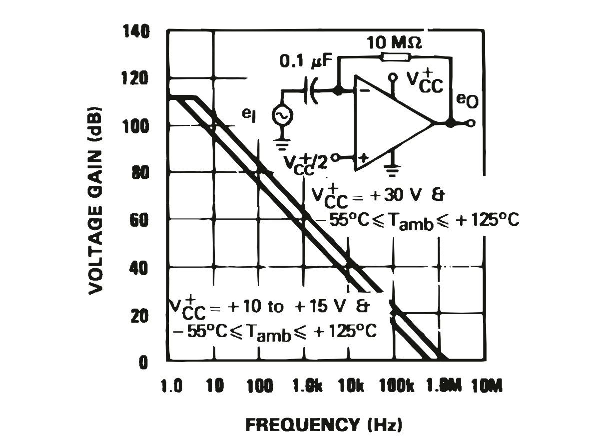


Figure 10. Large signal frequency response

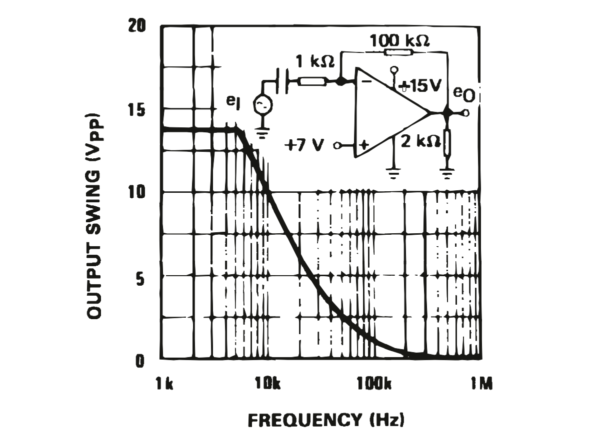


Figure 11. Voltage follower pulse response

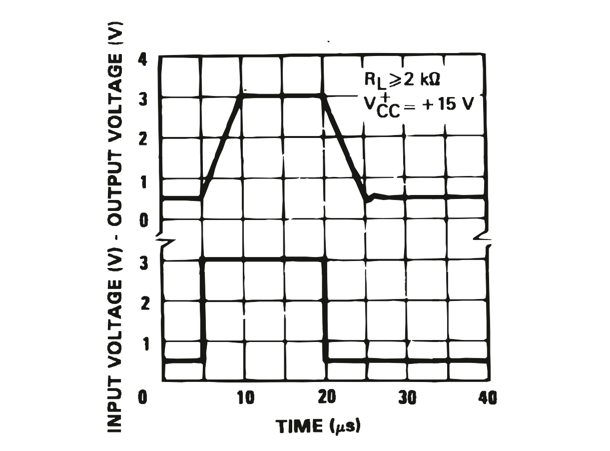


Figure 12. Output characteristics (current sinking)

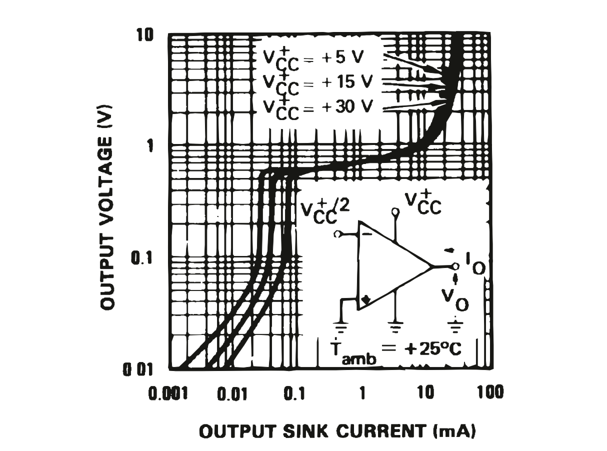


Figure 13. Voltage follower pulse response (small signal)

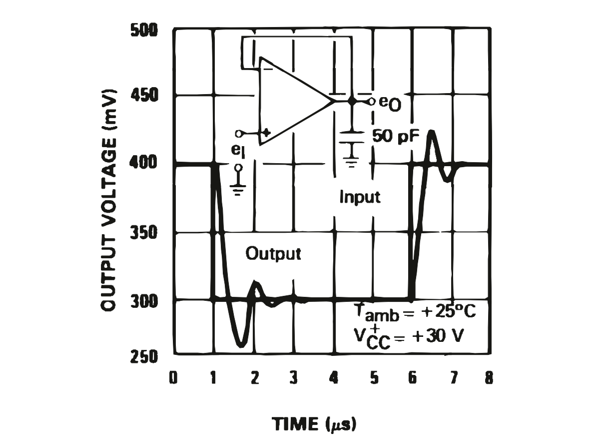


Figure 14. Output characteristics (current sourcing)

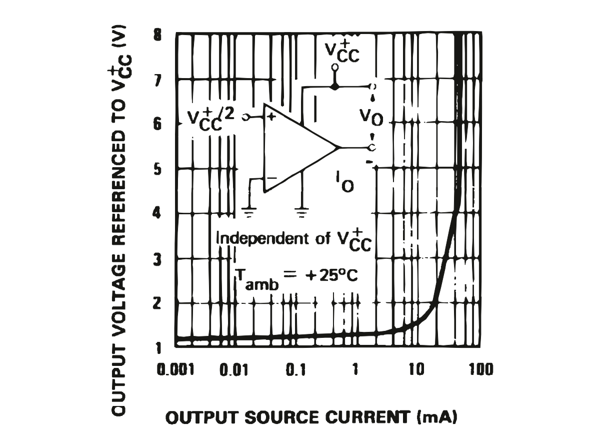


Figure 15. Input current vs. supply voltage

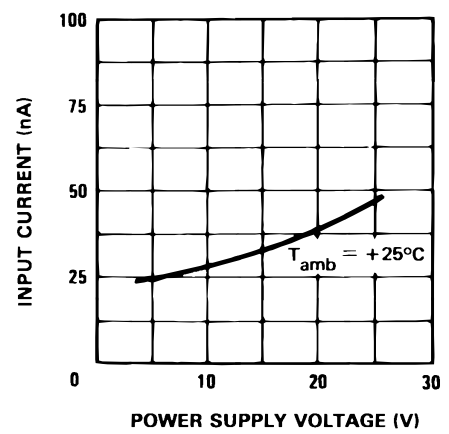


Figure 16. Large signal voltage gain vs. temperature

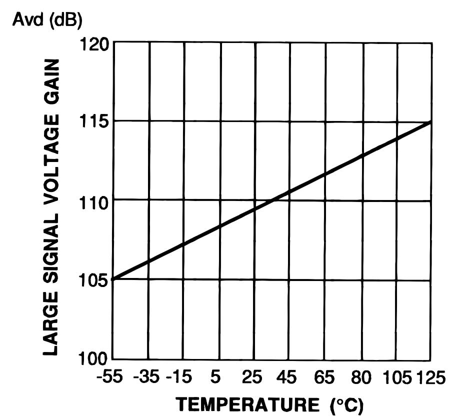


Figure 17. Power supply and common mode rejection ratio vs. temperature

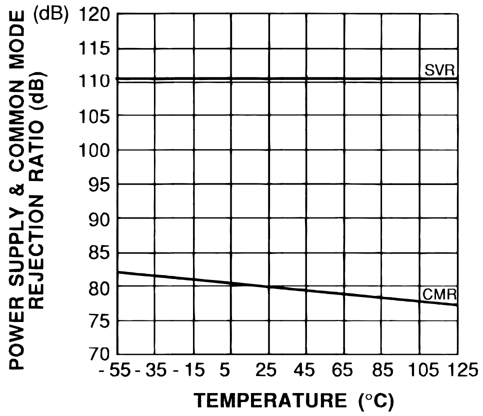
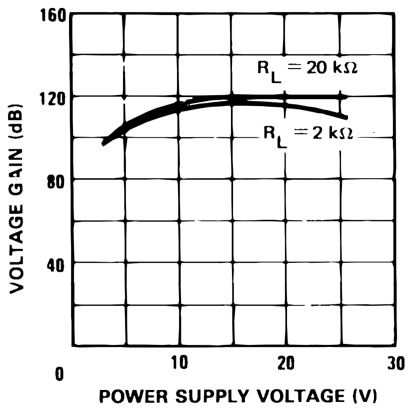


Figure 18. Voltage gain vs. supply voltage



4 Typical single-supply applications

Figure 19. AC coupled inverting amplifier

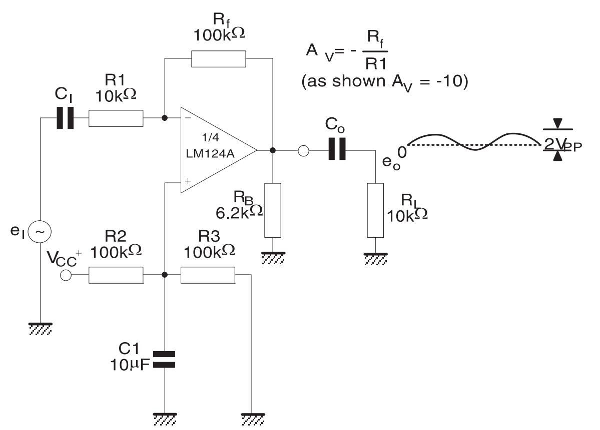
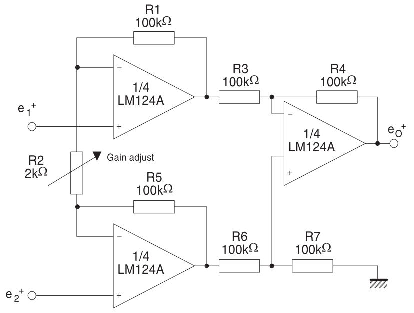


Figure 20. High input Z adjustable gain DC instrumentation amplifier



if R1 = R5 and R3 = R4 = R6 = R7

$$e_0 = \left[1 + \frac{2R_1}{R_2}\right](e_2 - e_1)$$

As shown $e_0 = 101\ (e_2 - e_1)$.

Figure 21. AC coupled non inverting amplifier

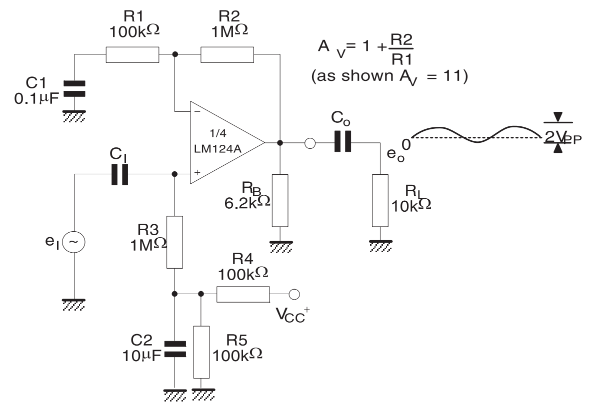
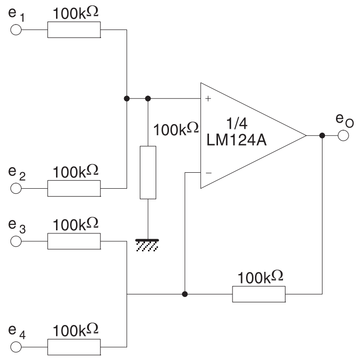


Figure 22. DC summing amplifier



$e_0 = e_1 + e_2 - e_3 - e_4$
Where $(e_1 + e_2) \geq (e_3 + e_4)$
to keep $e_0 \geq 0V$

Figure 23. Non-inverting DC gain

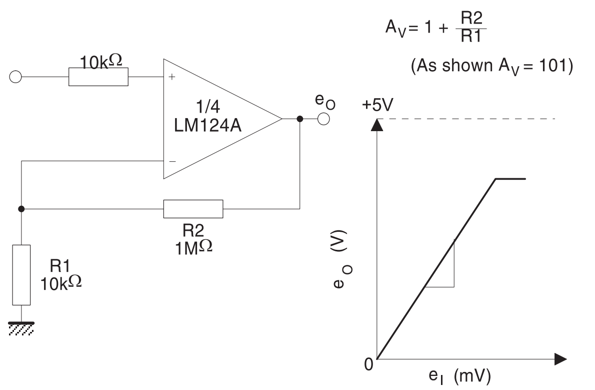
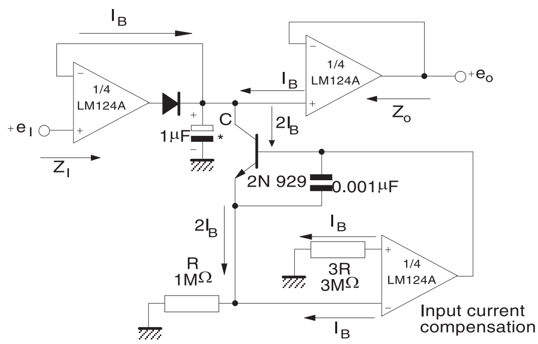
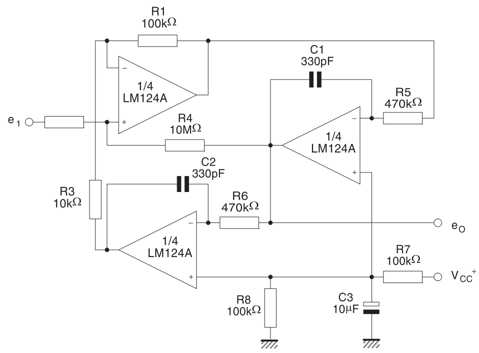


Figure 24. Low drift peak detector



* Polycarbonate or polyethylene

Figure 25. Active bandpass filter

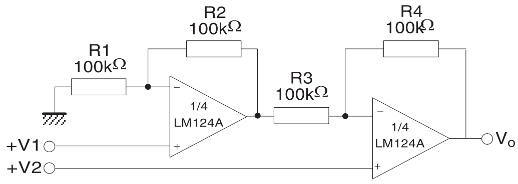


Fo = 1kHz
Q = 50
Av = 100 (40dB)

Figure 26. High input Z, DC differential amplifier

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$

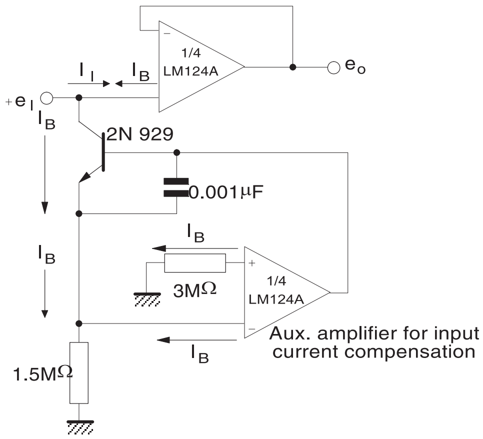
(CMRR depends on this resistor ratio match)



$e_0 \left(1 + \frac{R_4}{R_3}\right) (e_2 - e_1)$

As shown $e_0 = (e_2 - e_1)$

Figure 27. Using symmetrical amplifiers to reduce input current (general concept)



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 SO14 package information

Figure 28. SO14 package mechanical drawing

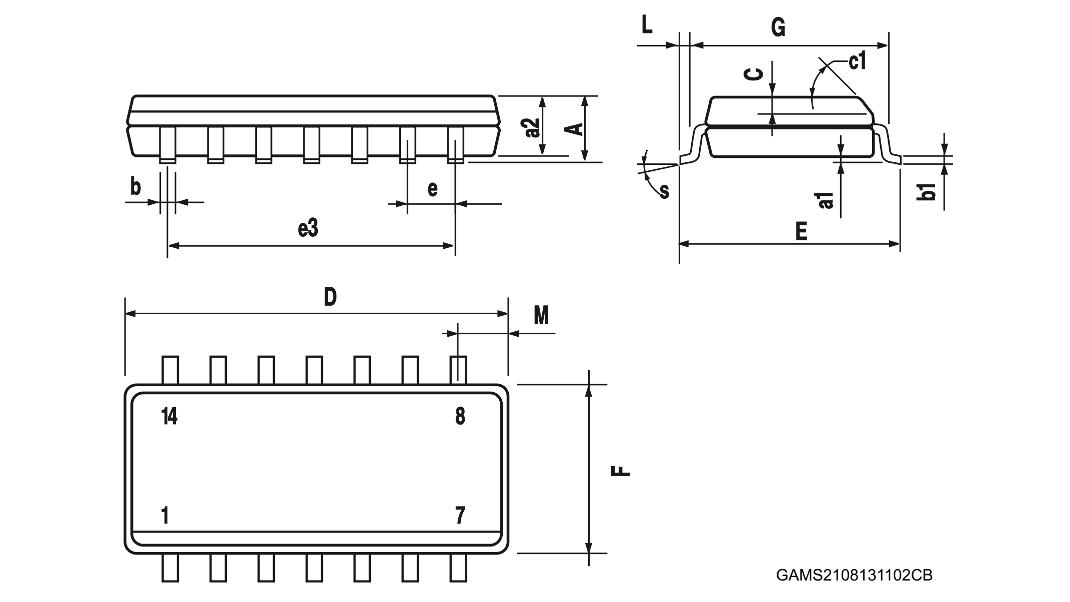


Figure 29. SO14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S			8 °			8 °

5.2 TSSOP14 package information

Figure 30. TSSOP14 package mechanical drawing

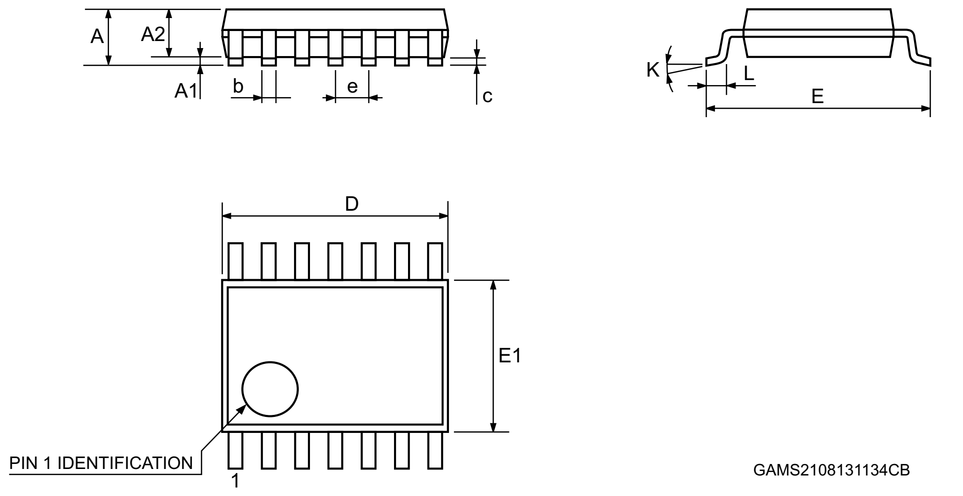


Figure 31. TSSOP14 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0 °		8 °	0 °		8 °
L	0.45	0.60	0.75	0.018	0.024	0.030

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
1-Mar-2001	1	First Release
1-Feb-2005	2	Added explanation of V_{id} and V_i limits in *Table 2 on page 4*. Updated macromodel.
1-Jun-2005	3	ESD protection inserted in *Table 2 on page 4*.
25-Sep-2006	4	Editorial update.
22-Aug-2013	5	Removed DIP package and all information pertaining to it *Table 1: Device summary*: Removed order codes LM224AN, LM224AD, LM324AN, and LM324AD; updated packaging. *Table 2: Absolute maximum ratings*: removed N suffix power dissipation data; updated footnotes *5* and *6*. Renamed *Figure 3*, *Figure 4*, *Figure 6*, *Figure 7*, *Figure 16*, *Figure 17*, *Figure 18*, and *Figure 19*. Updated axes titles of *Figure 4*, *Figure 5*, *Figure 7*, and *Figure 17*. Removed duplicate figures. Removed *Section 5: Macromodels*