2.95V to 6V Input, 3A Output, 2MHz, Synchronous Step-Down Converter

General Description

The RT8079 is a high efficiency step-down converter and capable of delivering 3A output current over a wide input voltage range from 2.95V to 6V.

The RT8079 provides accurate regulation for a variety of loads with ±3% accuracy. For reducing inductor size, it provides up to 2MHz switching frequency. The efficiency is maximized through the integrated 45mΩ MOSFETs and 550μA typical supply current.

Under voltage lockout voltage of the RT8079 is 2.7V, and it also provides external setting by a resistor network on the enable pin.

The RT8079 provides protections such as inductor current limit under voltage lockout and thermal shutdown. The over temperature threshold is 145°C.

The RT8079 is available in WQFN-16L 3x3 package.

Ordering Information

RT8079□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

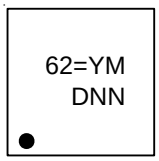
Features

- **Integrated 45mΩ MOSFETs**
- **Input Range : 2.95V to 6V**
- **Adjustable PWM Frequency : 300kHz to 2MHz**
- **Output Current : 3A**
- **95% Efficiency**
- **Adjustable Soft-Start**
- **Power Good Indicator**
- **Enable Control**
- **Under Voltage Lockout**
- **Current Limit**
- **Thermal Shutdown**
- **16-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- Low-Voltage, High-Density Power Systems
- Distributed Power Systems
- Point-of-Load Conversions

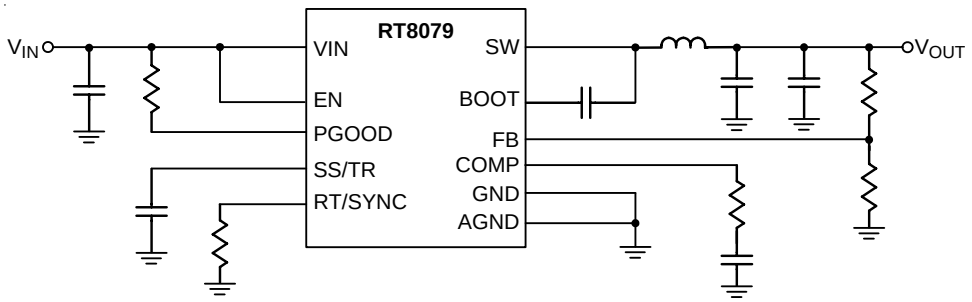
Marking Information



62= : Product Code

YMDNN : Date Code

Simplified Application Circuit



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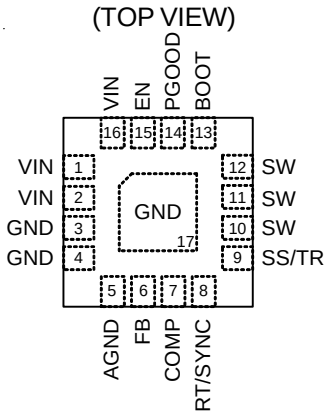
Pin Configurations

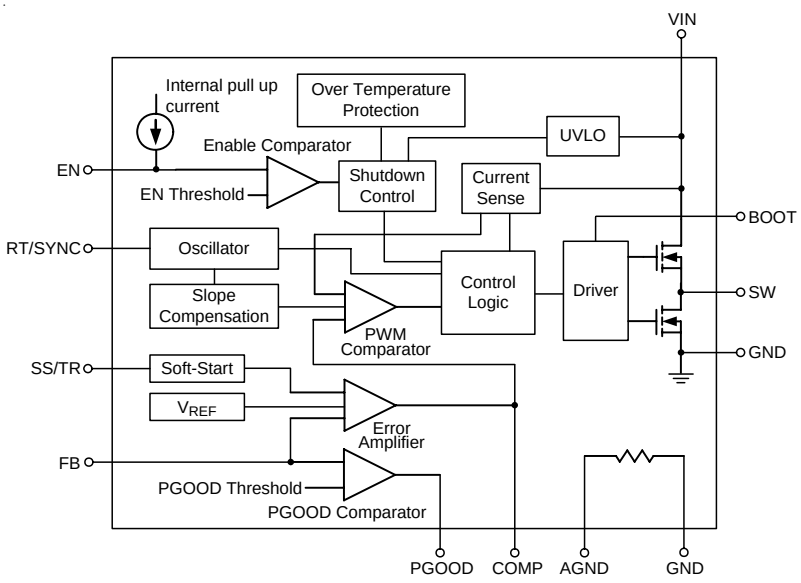


WQFN-16L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2, 16	VIN	Power Input.
3, 4, 17 (Exposed Pad)	GND	Power Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	AGND	Analog Ground.
6	FB	Feedback Input.
7	COMP	Compensation Node for Converter Stability.
8	RT/SYNC	Frequency Setting and External Synchronous. Clock input.
9	SS/TR	Soft-Start and Tracking.
10 to 12	SW	Switch Node. Connect this pin to external L-C filter.
13	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a capacitor between the BOOT and SW pin.
14	PGOOD	Output of Power Good Indicator.
15	EN	Chip Enable. Externally pulled high to enable and pulled low to disable this chip. It is internally pulled up to high when the pin is floating.

Function Block Diagram



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Operation

The RT8079 is a synchronous step-down DC/DC converter with two integrated power MOSFETs. It can deliver up to 3A output current from a 2.95V to 6V input supply. The RT8079's current mode architecture allows the transient response to be optimized over a wider input voltage and load range. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT8079 is synchronizable to an external clock with frequency ranging from 300kHz to 2MHz. The RT8079 is available in WQFN-16L 3x3 package.

High side MOSFET peak current is measured by internal sensing resistor. The Current Signal is where Slope Compensator works together with sensing voltage sensing resistor. The error amplifier adjusts COMP voltage by comparing the feedback signal (V_{FB}) from the output voltage with the internal 0.827V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference, the COMP voltage then rises to allow higher inductor current to match the load current.

EN Comparator

The RT8079 is enable when EN pin is higher than 1.25V. It is disable when EN pin lower than 1.18V. There is an internal pull-high current source to charge the EN pin to high when the EN pin is floating.

Oscillator (OSC)

The internal oscillator that provides switching frequency from 300kHz to 2MHz. It is adjusted using an external timing resistor. It also can be synchronized by an external clock in the range between 300kHz and 2MHz from RT/SYNC pin.

PGOOD Comparator

When the feedback voltage (V_{FB}) rises above 93% or falls below 107% of reference voltage the PGOOD open drain output will be high impedance. The PGOOD open drain output will be internally pulled low when the feedback voltage (V_{FB}) falls below 88% or rises above 113% of reference voltage.

Soft-Start (SS)

An internal current source (2.2μA) charges an external capacitor to build the soft-start ramp voltage (V_{SS}). The V_{FB} voltage will track the V_{SS} during soft-start interval. The Soft-Start setting capacitor (C_{SS}) for the Soft-Start time (T_{SS}) can be easily calculated by the following equation :

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times 2.2\ (\mu A)}{0.827\ (V)}$$

Over Temperature Protection (OTP)

The RT8079 implement an internal over temperature protection. When junction temperature is higher than 145°C, it will stop switching. Until the junction temperature decreases below 125°C, the RT8079 will re-soft-start from initial condition.

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Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 7V
- Switch Note Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- BOOT to SW ---------- –0.3V to 7V
- Other Pins ---------- –0.3V to (V_{IN} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 2.128W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 47°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.95V to 6V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C t o 85°C

Electrical Characteristics

(V_{IN} = 5V, C_{IN} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Power Supply							
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.7	2.8	V
Under Voltage Lockout Hysteresis		ΔV_{UVLO}		--	200	--	mV
Quiescent Current		I_Q	Active, V_{FB} = 1V, Not Switching	--	550	800	µA
Shutdown Current		I_{SHDN}		--	2	5	µA
Feedback Voltage							
Feedback Voltage		V_{FB}		0.802	0.827	0.852	V
Enable							
EN Input Voltage Threshold	Logic-High	V_{IH}	Rising	--	1.25	--	V
	Logic-Low	V_{IL}	Falling	--	1.18	--	
Input Current			V_{EN} = V_{IH} + 50mV	--	–4.6	--	µA
			V_{EN} = V_{IL} – 50mV	--	–1.2	--	
Power Good Threshold Voltage			PGOOD Falling (Fault)	--	88	--	%V_{REF}
			PGOOD Rising (Good)	--	93	--	
			PGOOD Rising (Fault)	--	113	--	
			PGOOD Falling (Good)	--	107	--	

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency Setting and External Synchronization (RT/SYNC pin)						
Switching Frequency Range in RT Mode	f_{OSC}		300	--	2000	kHz
Oscillator Frequency		R_{RT} = 180kΩ	--	1000	--	kHz
Switching Frequency Range in ExtSYNC Mode	f_{SYNC}		300	--	2000	kHz
MOSFET						
High Side MOSFET Resistance		$V_{BOOT} - V_{SW}$ = 5V	--	45	--	mΩ
Low Side MOSFET Resistance			--	42	--	mΩ
Current Limit						
Current Limit Threshold	I_{LIM}		4.2	6.6	--	A
Over Temperature Protection						
Thermal Shutdown Temperature	T_{SD}		--	145	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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Typical Application Circuit

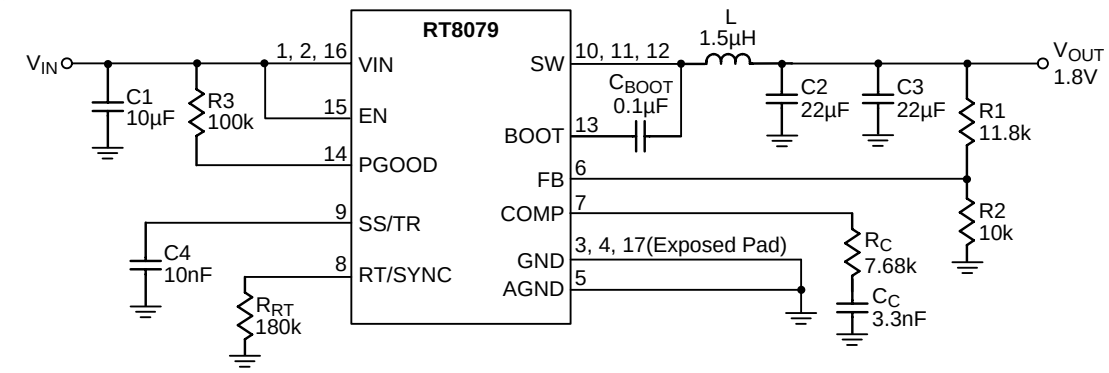

Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)
1.2	4.3	10	11.8	1	1 to 1.5
1.8	11.8	10	7.68	3.3	1 to 1.5
2.5	20.4	10	10.7	2.2	1 to 2.2
3.3	30	10	14	1.8	1 to 2.2

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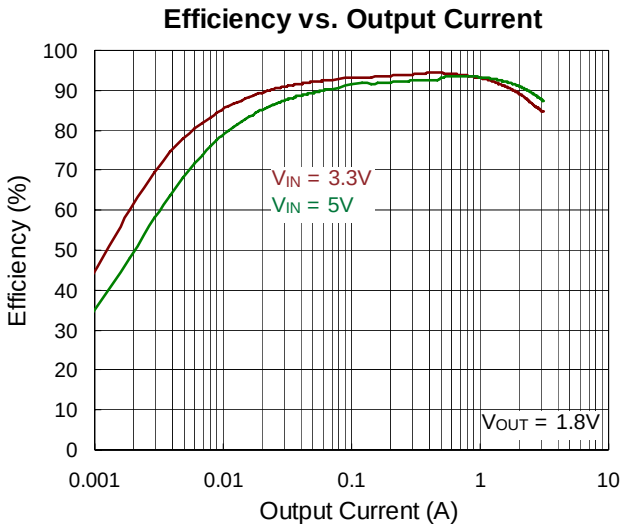
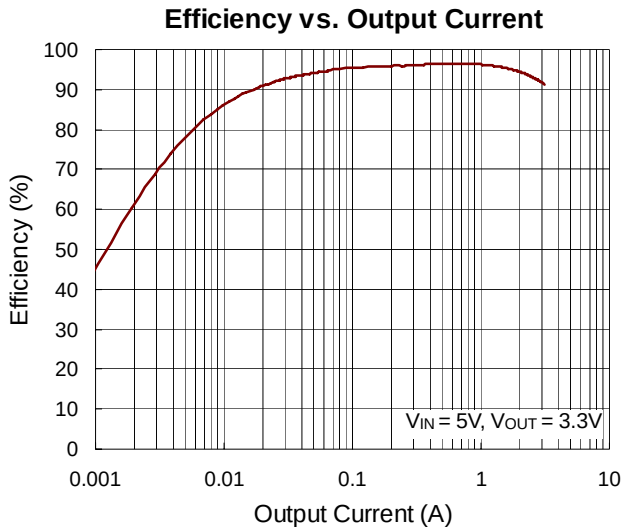
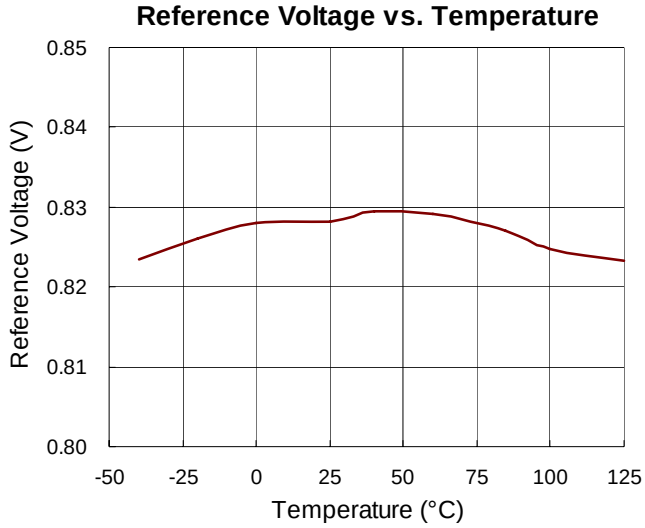
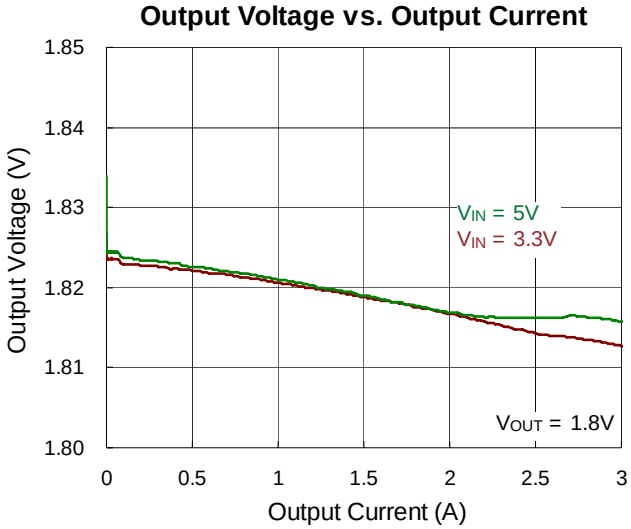
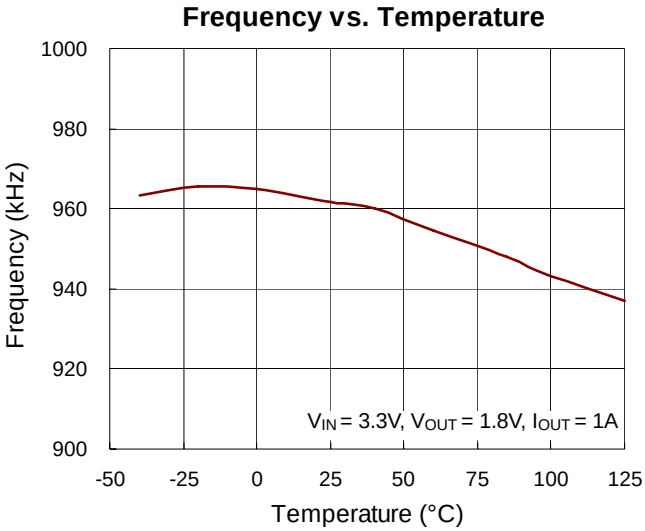
Typical Operating Characteristics

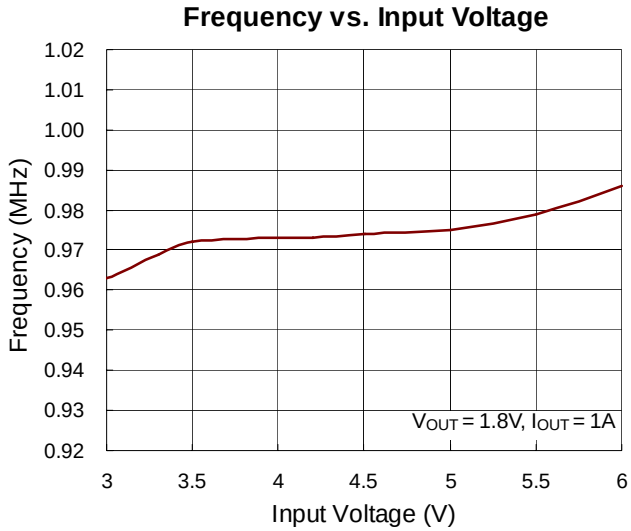












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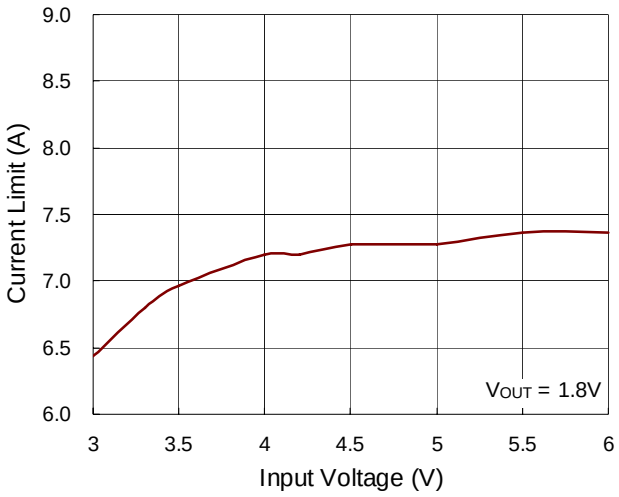
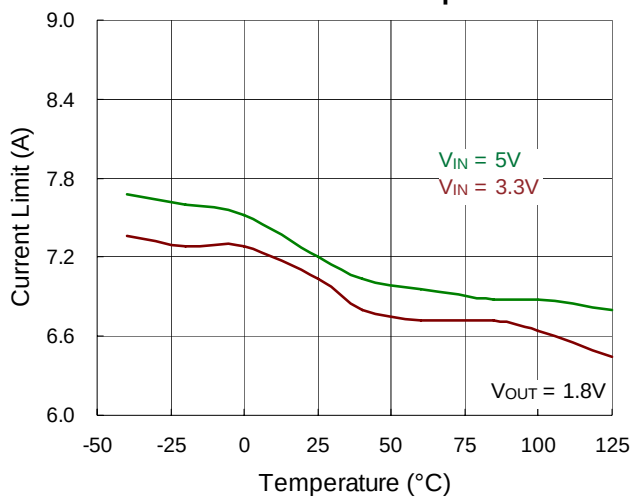
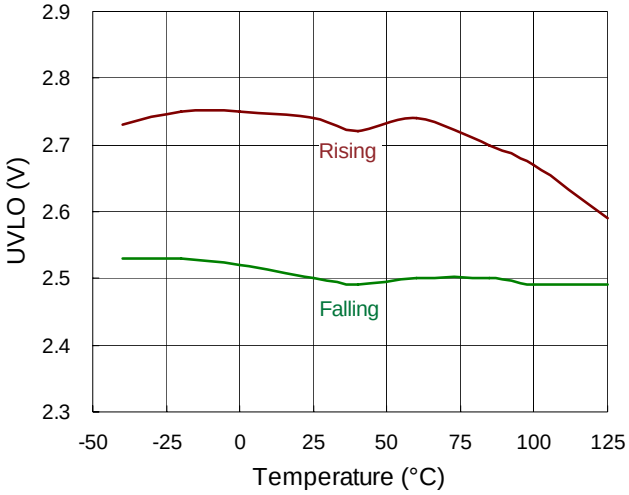
Current Limit vs. Input Voltage



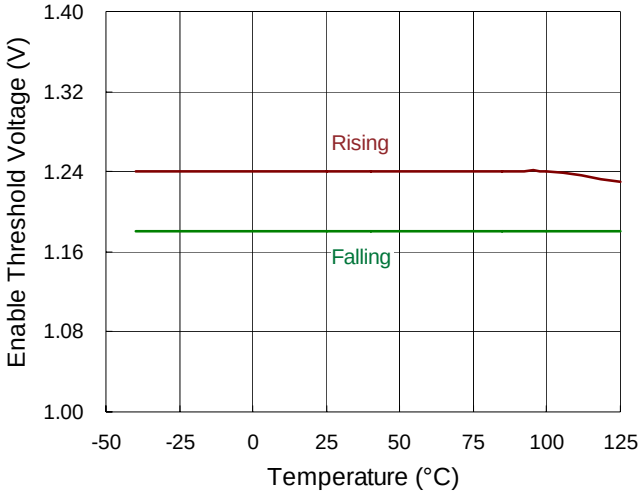
Current Limit vs. Temperature



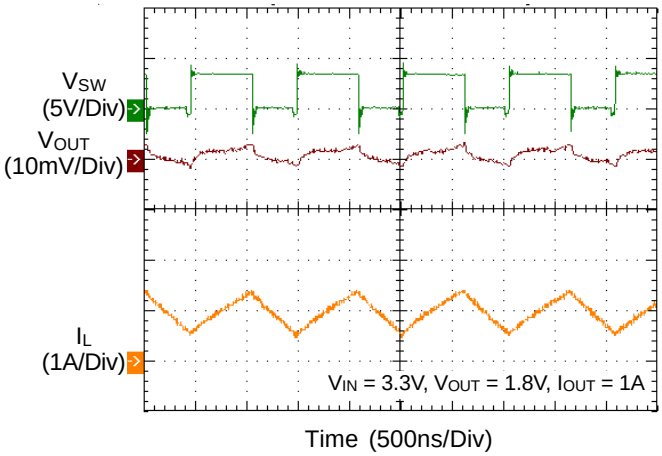
UVLO vs. Temperature



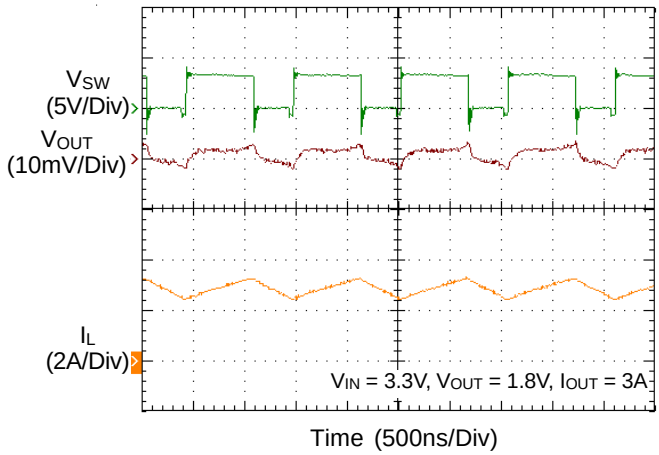
Enable Threshold Voltage vs. Temperature



Output Ripple



Output Ripple



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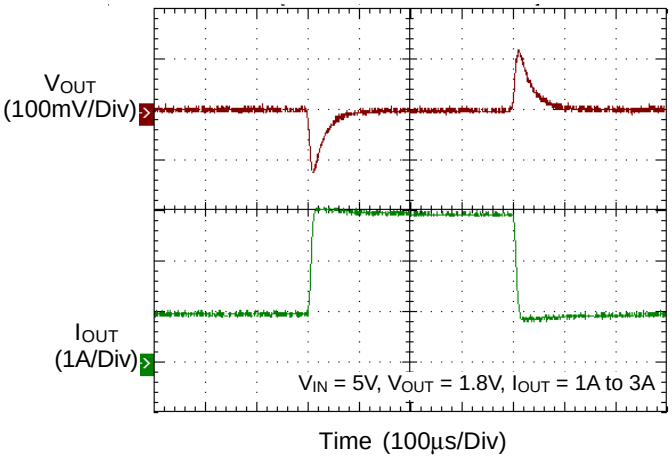
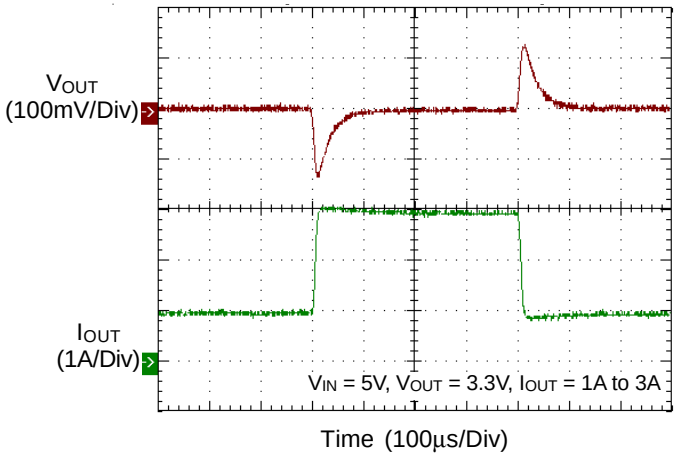
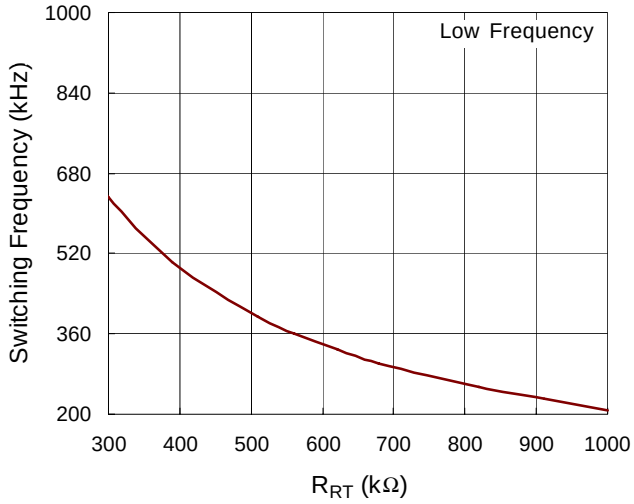
Load Transient Response



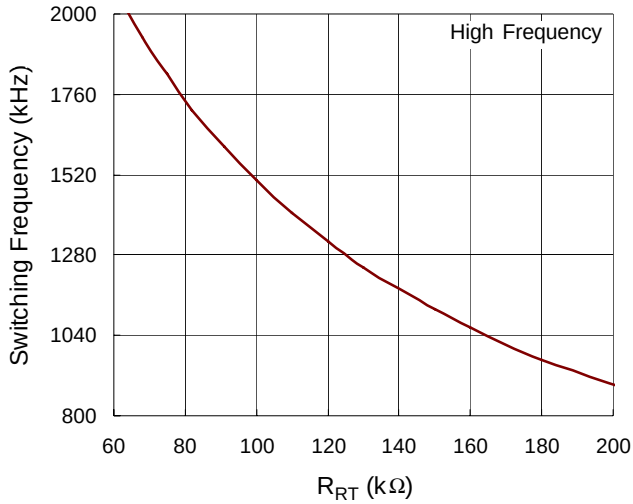
Load Transient Response



Switching Frequency vs. R_{RT}



Switching Frequency vs. R_{RT}



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Application Information

The basic RT8079 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}. The switching frequency range from 300kHz to 2MHz. It is adjusted by using a resistor to ground on the RT/SYNC pin.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

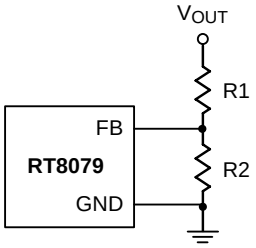

Figure 1. Setting the Output Voltage

The output voltage setting range is 0.827V to 3.6V and the set by an external resistive divider is according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage 0.827V (typ.).

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance :

$$\Delta I_L = \left[\frac{V_{OUT}}{f_{OSC}\times L}\right]\times\left[1-\frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is ΔI_L = 0.4 (IMAX). The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f_{OSC}\times\Delta I_{L(MAX)}}\right]\times\left[1-\frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)}\frac{V_{OUT}}{V_{IN}}\sqrt{\frac{V_{IN}}{V_{OUT}}-1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life, which makes it advisable to either further derate the capacitor or choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design. The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple, load step transients, and the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be examined by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \le \Delta I_L\left[ESR+\frac{1}{8f_{OSC}C_{OUT}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple with the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

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Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 47°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (47°C/W) = 2.128W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

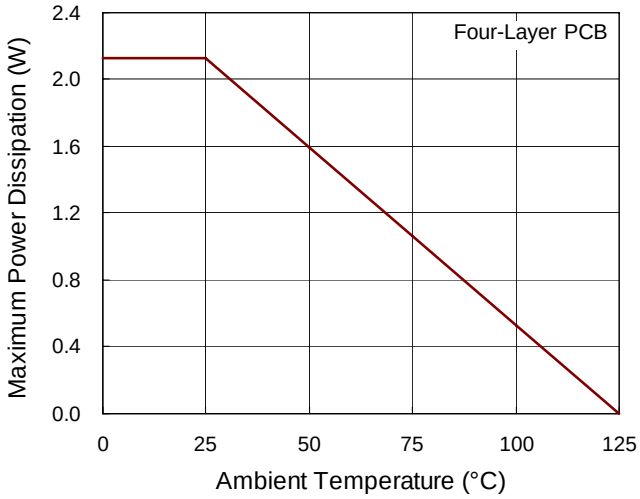

Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

For the best performance of the RT8079, the following guidelines must be strictly followed.

- The input capacitor should be placed as close as possible to the device pins (VIN and GND).
- The RT/SYNC pin is sensitive. The RT resistor should be located as close as possible to the IC and minimal lengths of trace.
- The SW node is with high frequency voltage swing. It should be kept at a small area.
- Place the feedback components as close as possible to the IC and keep away from the noisy devices.
- The GND and AGND should be connected to a strong ground plane for heat sinking and noise protection.

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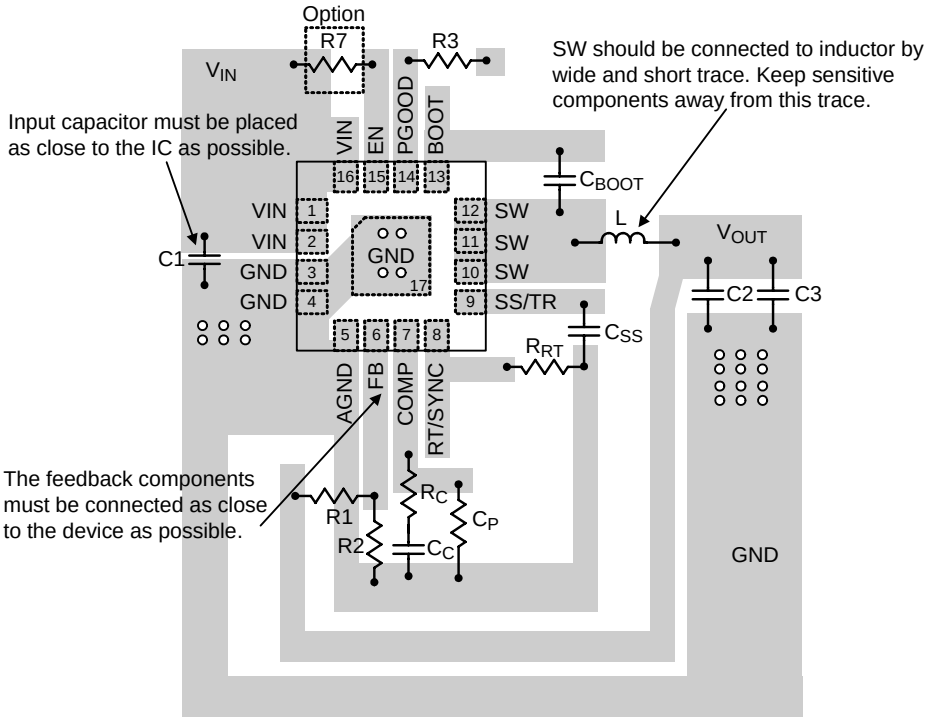

Figure 3. PCB Layout Guide

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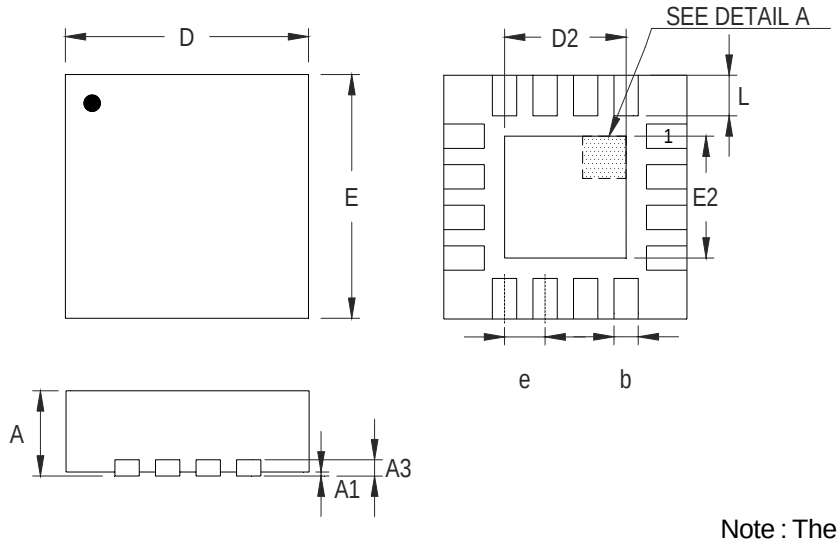
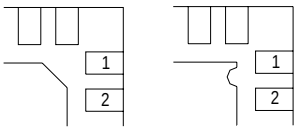
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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