90V Boost DC/DC Converter with APD Current Monitor

General Description

The RT8541/A is a constant frequency current mode PWM step-up DC/DC converter designed to bias avalanche photodiodes (APD) at high voltage in optical receivers. It includes a voltage doubler charge pump to significantly reduce the noise level at output up to 90V. The RT8541A switching frequency can be adjusted by a resistor while RT8541 is internally set at 650kHz. The RT8541/A has a built-in APD current mirror that delivers 1/5 of the APD current with high accuracy for monitoring the APD current from 0.2μA to 2.5mA. This current can be used as a reference to provide a digital programmed output voltage via the CTRL pin. To protect the optical receiver system, the RT8541/A provides a built-in adjustable APD current limit function by sensing a 200mV voltage threshold between VOUT2 and MONIN pins. Only one resistor is needed to program the desired current limit. A charge pump voltage doubler is designed to achieve significantly lower noise level at the APD comparing to a simple boost converter type bias circuit.

The RT8541/A also features a built-in 9ms soft-start function to eliminate the inrush current during start-up interval. The RT8541/A provides a low cost optical receiver solution and can fit in very small PCB area.

The RT8541/A is available in the WQFN-16L 3x3 package.

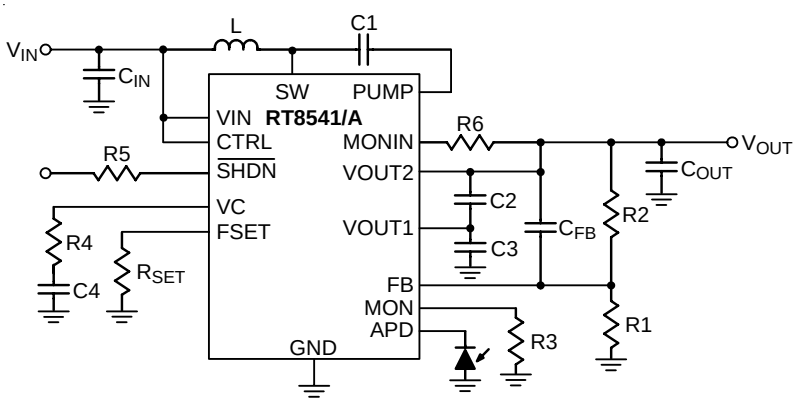
Features

- **Integrated Schottky Diodes for Boost Converter and Charge Pump Voltage Doubler**
- **50V, 400mA Internal Switch**
- **High Side Low Noise and Accurate APD Current Monitor**
- **650kHz Fixed Switching Frequency for RT8541 and Adjustable Switching Frequency for RT8541A**
- **Wide VIN Range : 2.7V to 16V**
- **Adjustable APD Current Limit with External Resistor**
- **Low Shutdown Current <1μA**
- **Built-In Soft-Start**
- **CTRL Pin Allows Output Adjustment with no Polarity Inversion**
- **Thin 16-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- APD Bias
- PIN Diode Bias
- Optical Receivers and Modules
- Fiber Optic Network Equipment

Simplified Application Circuit



Ordering Information

RT8541/A□□

- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- Adjustable Switching Frequency
- Fixed Switching Frequency

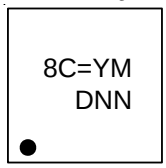
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

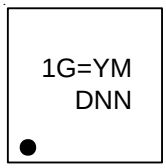
RT8541GQW



8C= : Product Code

YMDNN : Date Code

RT8541AGQW



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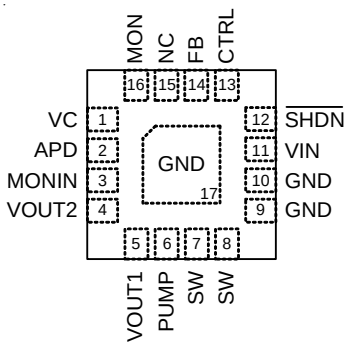
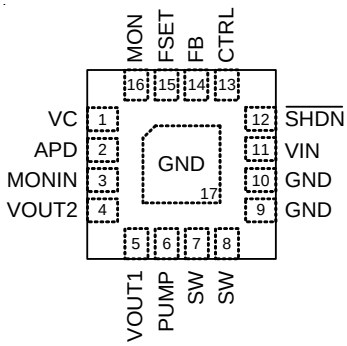
Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

RT8541



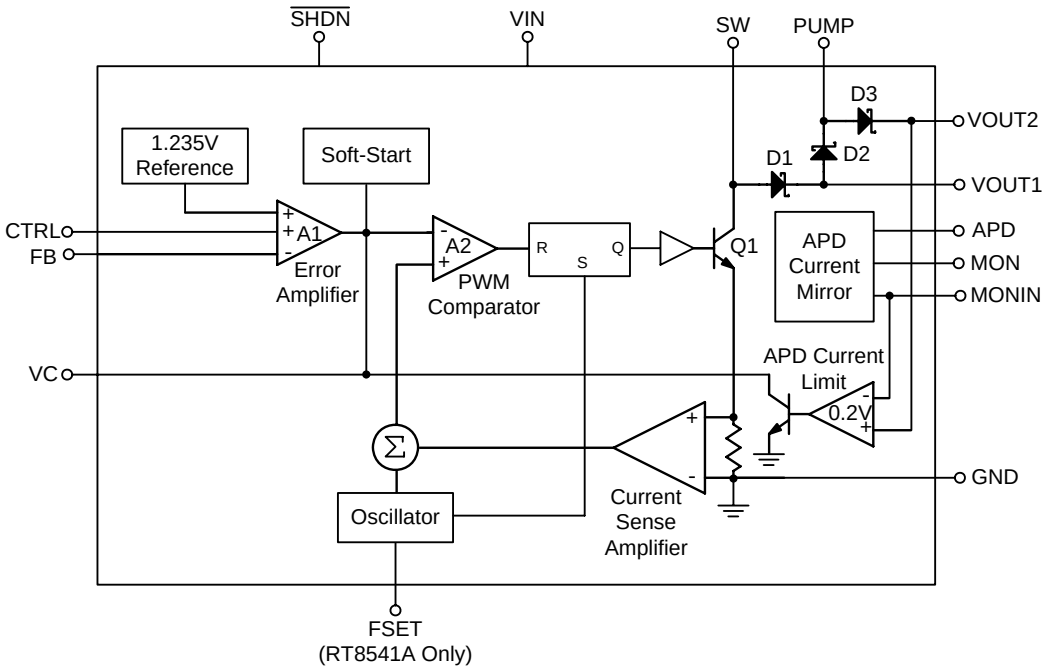
WQFN-16L 3x3

RT8541A

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VC	Compensation Node for Control Loop.
2	APD	Output for APD. Connect this Pin to the APD Cathode.
3	MONIN	Current Monitor Input Power Pin. An optional resistor between the VOUT2 and MONIN pins can be used for current limit setting.
4	VOUT2	Voltage Doubler Output Pin. A 50V rated capacitor is needed between this pin and VOUT1 pin. A resistor divider for output voltage feedback is connected between this pin and GND pin.
5	VOUT1	Output Pin of Boost Converter. A capacitor is needed between this pin and GND pin. The trace length from this pin to the capacitor should be minimized.
6	PUMP	Charge Pump Pin for Voltage Doubler. Put a 50V capacitor between the SW and PUMP pins to form a complete voltage doubler with the internal Schottky diodes.
7, 8	SW	Switch Node of Boost Converter. Minimize the trace area on this pin to reduce EMI.
9, 10, 17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
11	VIN	Supply Voltage Input. Connect a 1μF capacitor from this pin to GND.
12	$\overline{\text{SHDN}}$	Shutdown Control Input. Tie to 2V or higher with a resistor 200kΩ to enable device.
13	CTRL	External Reference Control Input. This allows the FB voltage to follow the external reference between 0V and 1.2V. Tie this pin higher than 1.5V to use the internal reference of 1.235V.
14	FB	Feedback Input. Connect the pin to the output resistor divider for output voltage setting.
15	NC (RT8541)	No Internal Connection. The switching frequency is set at 650kHz internally.
	FSET (RT8541A)	Oscillator Frequency Setting. Connect a resistor between this pin and GND for frequency setting.
16	MON	Output for Current Monitor. It sources a current equal to 20% of the APD current and converts to a reference voltage through an external resistor.

Function Block Diagram



Operation

The RT8541/A Boost converter uses a constant frequency current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Functional Diagram. At the start of each oscillator cycle, the SR latch is set, which turns on the power switch, Q1. A voltage proportional to the switch current is added to a stabilizing slope compensation and the resulting sum is fed into the positive terminal of the PWM comparator, A2. When this voltage exceeds the level at the negative input of A2, the SR latch is reset and the power switch is turned off . The level at the negative input of A2 is set by the error amplifier A1, and is simply an amplified version of the difference between the feedback voltage and the reference voltage of 1.235V, or externally provided CTRL voltage. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered.

The RT8541/A has an integrated high side APD current monitor with a 5:1 ratio. The MONIN pin can accept a supply voltage up to 90V, which is suitable for APD photodiode applications. The MON pin has an open-circuit protection feature and is internally clamped to 15V.

If an APD is tied to the APD pin, the current will be mirrored to the MON pin and converted to a voltage signal by the resistor between MON and GND pins. This voltage signal can be used to drive an external control block to adjust the APD voltage by adjusting the feedback threshold of Error Amplifier A1 through the CTRL input.

The RT8541/A features a built-in 9ms soft-start function and provides current limit function with a 0.2V threshold between VOUT2 and MONIN pins to protect the APD system. The APD current limit can be adjusted by an external resistor between the VOUT2 and MONIN pins.

Absolute Maximum Ratings (Note 1)

- VIN, $\overline{SHDN}$, FSET, CTRL, MON ---------- 16V
- VOUT1, SW ---------- 50V
- VOUT2, PUMP, MONIN, APD ---------- 90V
- FB, VC, FSET ---------- 5V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, VIN ---------- 3V to 12V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage			2.7	--	16	V
Feedback Voltage	V_{FB}	CTRL = 1.5V	1.215	1.235	1.255	V
Feedback Line Regulation		V_{IN} = 3V to 10V	--	0.025	0.07	%/V
FB Pin Bias Current			--	30	100	nA
Supply Current	I_{VIN}	FB = 1.3V, $V_{\overline{SHDN}}$ = 2V	--	3.3	4	mA
Shutdown Current		$V_{\overline{SHDN}}$ = 0V, Not Switching	--	0.1	0.5	μA
Switching Frequency	f_{SW}	RSET = NC (RT8541)	--	650	--	kHz
		RSET = 30k (RT8541A)	--	650	--	
Maximum Duty Cycle	D_{MAX}	f_{SW} = 650kHz	95	--	--	%
Switch Current Limit	I_{LIM}		320	400	480	mA
Switch VCESAT		I_{SW} = 150mA	--	130	220	mV
Switch Leakage Current		SW = 5V	--	--	2	μA
Schottky Forward Voltage		$I_{SCHOTTKY}$ = 150mA	--	720	--	mV
Schottky Reverse Leakage		VOUT1 – SW = 50V	--	--	5	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{SHDN}$ Voltage High	V_{IH}		2	--	--	V
$\overline{SHDN}$ Voltage Low	V_{IL}		--	--	0.4	V
$\overline{SHDN}$ Pin Bias Current			--	1	2	μA
Internal Soft-Start Time			--	9	--	ms
VC Threshold Voltage			--	0.7	--	V
APD Current Monitor Gain	G_{APD}	I_{APD} = 250nA, 10V ≤ MONIN ≤ 90V	0.18	0.2	0.215	V/V
		I_{APD} = 2.5mA, 20V ≤ MONIN ≤ 90V	0.18	0.2	0.215	
Monitor Output Voltage Clamp			--	15	16	V
APD Monitor Voltage Drop		MONIN – APD at I_{APD} = 1mA, MONIN = 90V	--	--	5	V
MONIN Pin Current Limit Threshold Voltage		APD = 0V, MONIN = 40V	--	200	--	mV
CTRL to FB Offset		CTRL = 0.5V	–5	2	12	mV
OTP Threshold Temperature			--	150	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

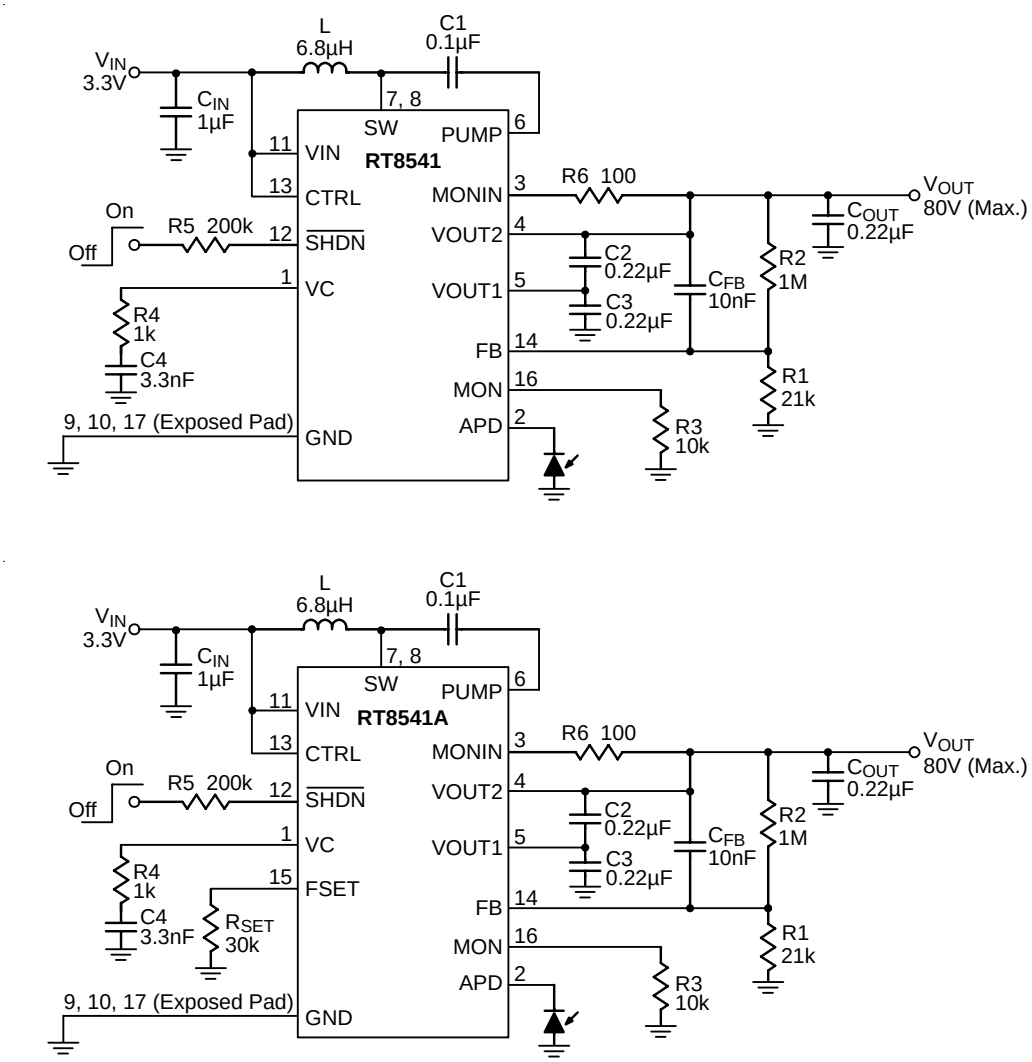
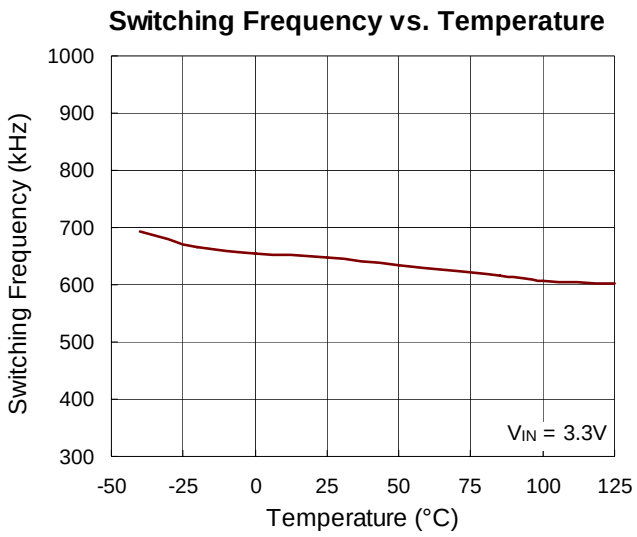
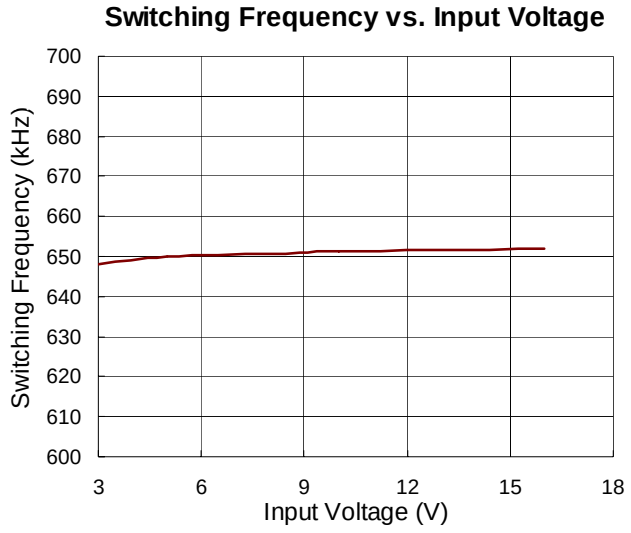
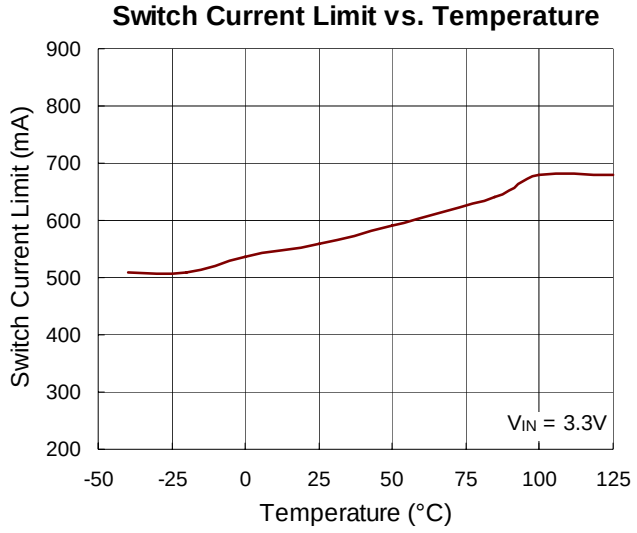


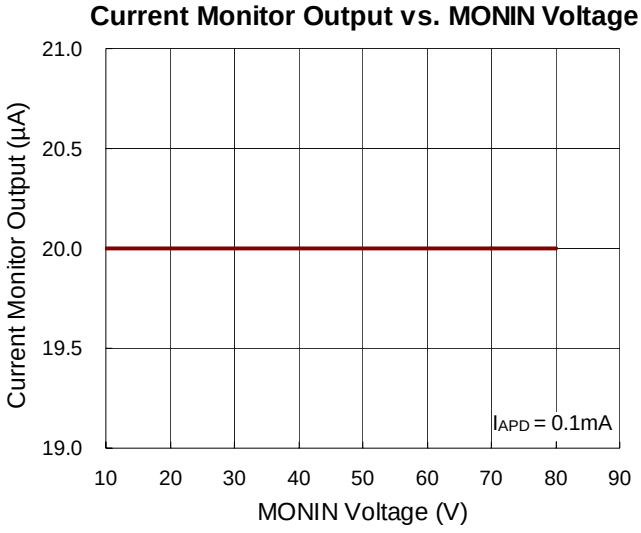
Figure 1. 3.3V to 63V/2mA APD Bias Power Supply Application Circuit

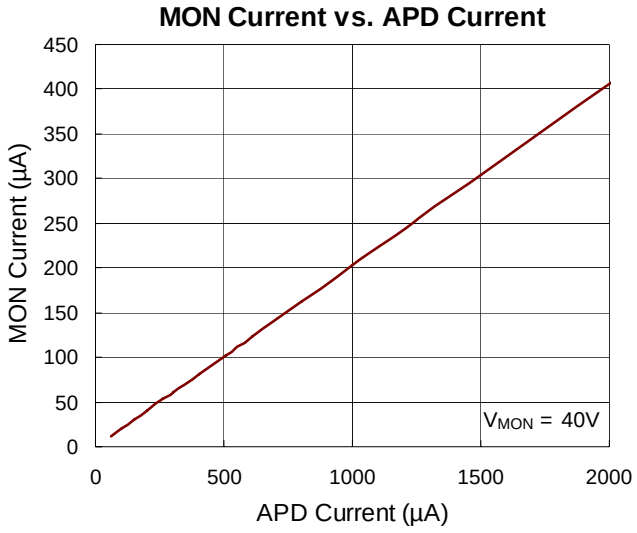
Typical Operating Characteristics

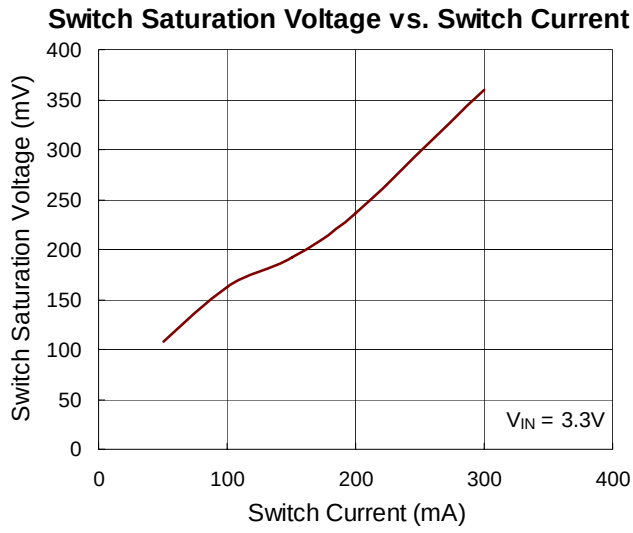




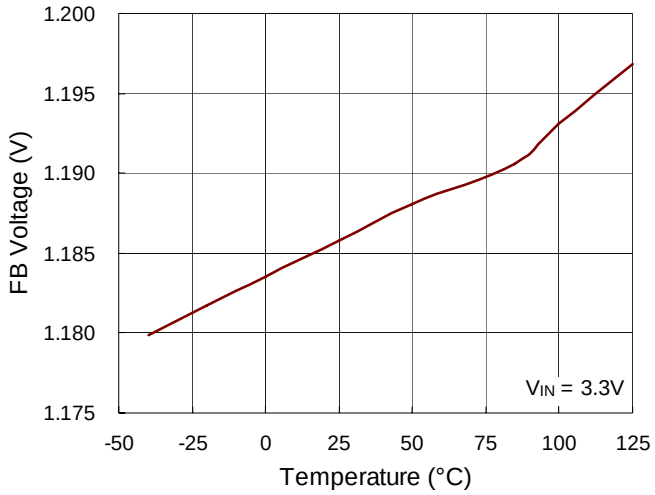




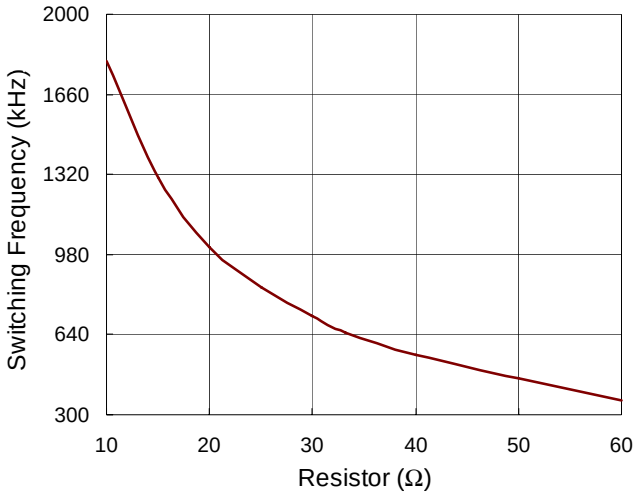




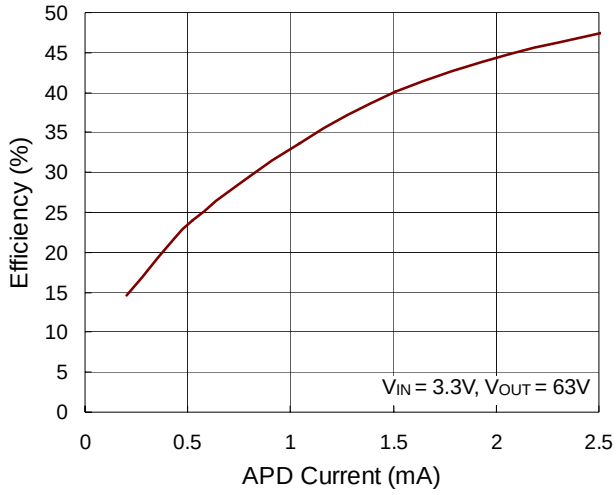
FB Voltage vs. Temperature



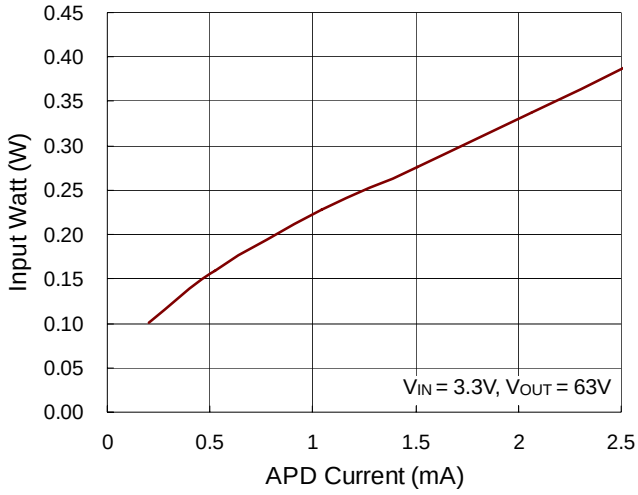
Switching Frequency vs. Resistor



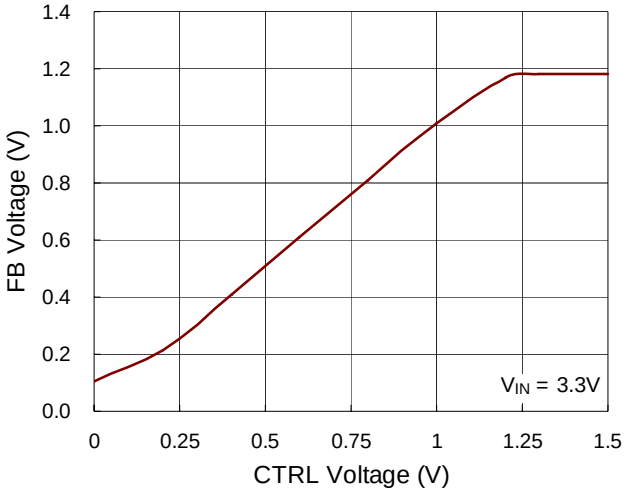
Efficiency vs. APD Current



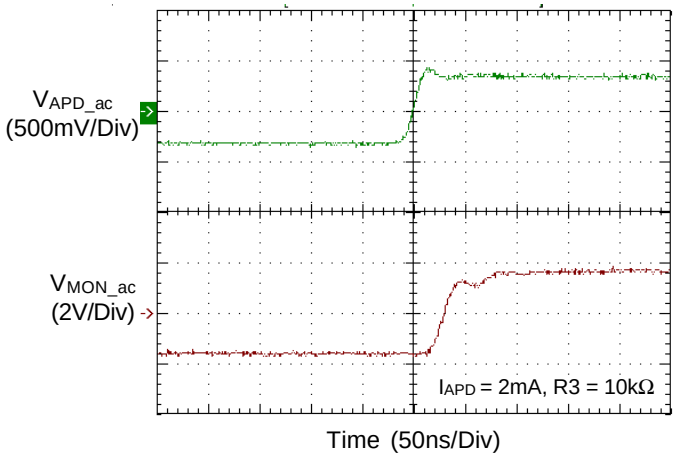
Input Watt vs. APD Current



FB Voltage vs. CTRL Voltage



Monitor Step Response



Application Information

Boost Regulator

The RT8541/A is a current mode Boost converter integrated with a 50V/400mA power switch over a wide VIN range from 2.8V to 16V. It performs fast transient responses to support the avalanche photodiodes (APDs) in optical receivers. The high operation frequency allows the use of small components to minimize the thickness of the optical transceiver.

The output voltage can be adjusted by an external resistive voltage divider connected to the FB pin. The error amplifier varies the VC voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal summed with the current sense signal will be compared with the VC voltage to determine the current trip point and duty cycle.

Output Voltage Setting

The RT8541/A regulated output voltage is showed as the following equation :

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right), \text{ where } V_{FB} = 1.235V \quad \text{(typ.)}$$

The recommended value for R2 should be at least 10kΩ. Place the resistive voltage divider as close as possible to the chip to reduce noise sensitivity.

Loop Compensation

The voltage feedback loop can be compensated with an external compensation network consisting of R4. Choose R4 to set high frequency integrator gain for fast transient response and C4 to set the integrator zero to maintain loop stability. For example, V_{IN} = 3.3V, V_{OUT2} = 63V, C_{OUT} = 0.22μF, L = 6.8μH, the recommended value for the compensation network is R4 = 1kΩ and C4 = 3.3nF.

Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor current can be calculated according to the following equation :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{APD}}{\eta \times V_{IN}}$$

where η is the efficiency of the converter, $I_{IN(MAX)}$ is the maximum input current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current.

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than I_{PEAK}. The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT2} - V_{IN})}{0.4 \times (V_{OUT2})^2 \times I_{APD} \times f_{SET}}$$

where f_{SET} is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Switching Frequency

The RT8541A FSET frequency adjust pin allows the user to program the switching frequency from 100kHz to 1.3MHz for optimized efficiency, performance, and external component size. For an appropriate R_{SET} resistor value see Table 1. An external resistor from the FSET pin to GND is required. Do not leave this pin open. For RT8541 the switching frequency is fixed and set at 650kHz typically.

Table 1. Switching Frequency vs. RSET Value (1% Resistors)

RSET (kΩ)	Frequency (kHz)
15	1300
20	1000
25	840
30	720
32	650
40	556
50	456
60	360

Output Capacitor Selection

The output ripple voltage is an important index for estimating chip performance. This portion consists of two parts. One is the product of the inductor current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. As shown in Figure 1, ΔV_{OUT2} can be evaluated based on the ideal energy equalization. According to the definition of Q, the Q value can be calculated as the following equation :

$$Q = \frac{1}{2} \times \left[\left(I_{IN} + \frac{1}{2} \Delta I_L - I_{APD} \right) + \left(I_{IN} - \frac{1}{2} \Delta I_L - I_{APD} \right) \right] \times \frac{V_{IN}}{V_{OUT2}} \times \frac{1}{f_{SET}} = C_{OUT} \times \Delta V_{OUT2}$$

where f_{SET} is the switching frequency, and ΔI_L is the inductor ripple current. Bring C_{OUT} to the left side to estimate the value of ΔV_{OUT2} according to the following equation :

$$\Delta V_{OUT2} = \frac{D \times I_{APD}}{\eta \times C_{OUT} \times f_{SET}}$$

where D is the duty cycle and η is the Boost converter efficiency. Finally, taking ESR into account, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = I_{IN} \times ESR \times \frac{D \times I_{OUT}}{\eta \times C_{OUT} \times f_{OSC}}$$

For applications with out voltage less than 45V, intermediate output pin VOUT1 can directly serve as the output pin. Typically use a 2μF capacitor for output voltage less than 25V and 1μF capacitor for output voltage between 25V and 45V. When output voltage goes beyond 45V, a charge pump must be formed with cascaded 0.47μF capacitors C1 and C2 at the output nodes. A typical 0.1μF capacitor is used as the flying capacitor CFLY to form the charge pump. Always use a capacitor with sufficient voltage rating. Either ceramic or solid tantalum capacitors may be used for the input decoupling capacitor, which should be placed as close as possible to the RT8541. A 1μF capacitor is sufficient for most applications.

Input Capacitor Selection

Low ESR ceramic capacitors are recommended for input capacitor applications. Low ESR will effectively reduce the input voltage ripple caused by switching operation. A 10μF capacitor is sufficient for most applications. Nevertheless, this value can be decreased for lower output current requirement. Another consideration is the voltage rating of the input capacitor which must be greater than the maximum input voltage.

APD Current Monitor

The power supply switching noise associated with a switching power supply can interfere with the photodiode DC measurement. To suppress this noise, a 0.1μF capacitor is recommended at APD pin. An additional output low-pass filter, a 10k resistor and a 10nF capacitor in parallel at MON pin might limit the measurement accuracy of low level signals. For applications requiring fast current monitor response time, a RC low-pass filter at MONIN pin is used to replace the 0.1μF capacitor at APD pin to reduce the power supply noise and other wide band noise.

APD Short Current Protection

In some applications, a long cable or wire is used to connect the RT8541/A to APD. When APD is shorted to GND, APD pin voltage might ring below ground and damage the internal circuitry. To prevent damage from short-circuit event, a 100Ω resistor must be added between MONIN and VOUT2 pins. The APD short current is 200mV/R6. For a typical 2mA short current protection of APD, the R6 should be set at 100Ω.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For

WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

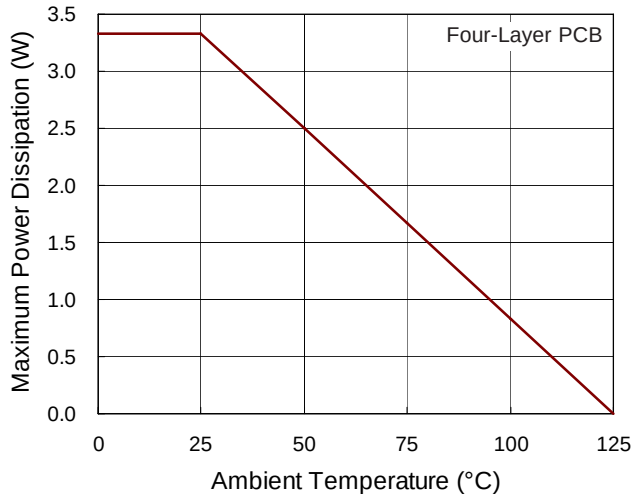


Figure 2. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout is very important for designing switching power converter circuits. The following layout guides should be strictly followed for best performance of the RT8541/A.

- Place L and C1 as close as possible to the SW and PUMP pin. The trace should be as short and wide as possible.
- The compensation circuit should be kept away from the power loops and should be shielded with a ground trace to prevent any noise coupling. Place the compensation components as close as possible to VC pin.
- The exposed pad of the chip should be connected to ground plane for thermal consideration.

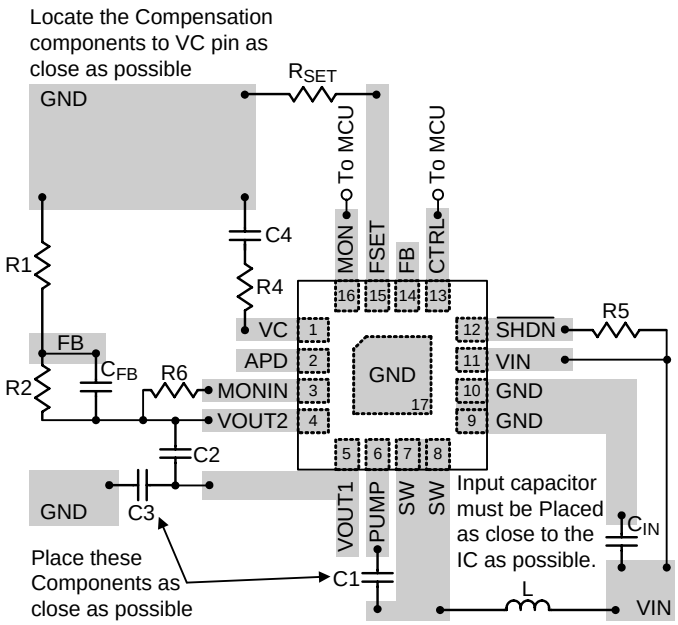
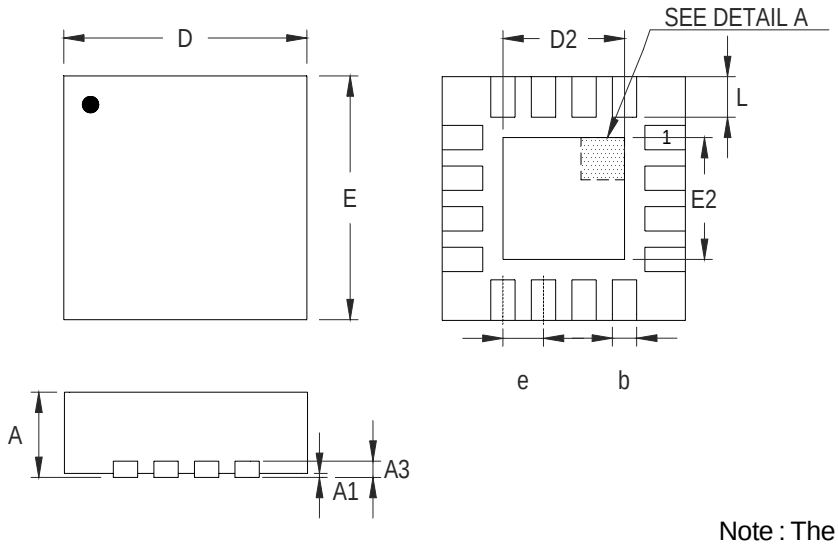
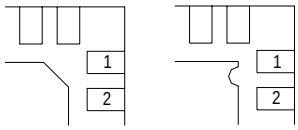


Figure 3. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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