Address: Midas Displays, Electra House, 32 Southtown Road, Great Yarmouth, Norfolk, NR31 0DU
Telephone: +44 (0)1493 602602
Fax: +44 (0)1493 665111
Email: sales@midasdisplays.com
Website: www.midasdisplays.com

Specification

MCOT128064NZ-YM

Midas Displays OLED Part Number System

MCO	B	21605	A	*	V	-	E	W	I	*
1	2	3	4	5	6		7	8	9	10

1	=	**MCO:**	Midas Displays OLED
2	=	**Blank:**	**B**: COB (Chip on Board) **T**: TAB (Taped Automated Bonding)
3	=	**No of dots:**	**(**e.g. 240064 = 240 x 64 dots) (e.g. 21605 = 2 x 16 5mm C.H.)
4	=	**Series**	A to Z
5	=	**Series Variant:**	A to Z and 1 to 9 **– see addendum**
6	=	**Operating Temp Range:**	**A:** -30+85° C **V:** -40+80° C **Y:** -40 +70° C **Z:** -30+70° C **X**: -40 +85° C
7	=	**Character Set:**	**Blank**: Not Applicable **E:** Multi European Font Set (English/Japanese – Western European (K) – Cyrillic (R))
8	=	**Colour:**	**Y:** Yellow **W:** White **B:** Blue **R:** Red **G:** Green **RGB**: Full Colour
9	=	**Interface:**	**P:** Parallel **I:** I²C **S:** SPI **M:** Multi
10	=	**Voltage Variant:**	e.g. **3** = 3v

1. Revision History

DATE	VERSION	REVISED PAGE NO.	Note
2013/06/18	1		First issue

2. General Specification

The Features is described as follow:

- Module dimension: 26.7×19.26×1.45 (max.) mm^3
- Active area: 21.738 × 10.858 mm^2
- Number of dots: 128 x 64
- Pixel Pitch: 0.17 × 0.17mm2
- Pixel Size: 0.148 × 0.148 mm2
- Display Mode: Passive Matrix
- Duty: 1/64
- Display Color: (Yellow)

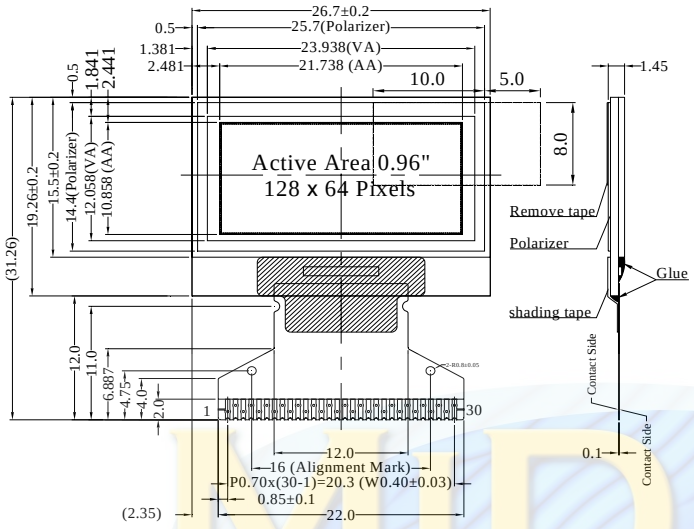
4. Interface Pin Function

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>N.C. (GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
<tr><td>2</td><td>C2P</td><td rowspan="4">Positive Terminal of the Flying Inverting Capacitor
Negative Terminal of the Flying Boost Capacitor
The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>3</td><td>C2N</td></tr>
<tr><td>4</td><td>C1P</td></tr>
<tr><td>5</td><td>C1N</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>7</td><td>NC</td><td>NC</td></tr>
<tr><td>8</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>9</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>10</td><td>BS0</td><td rowspan="3">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><th></th><th>BS0</th><th>BS1</th><th>BS2</th></tr>
<tr><td>I2C</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3-wire SPI</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>4-wire SPI</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>8-bit 68XX Parallel</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>11</td><td>BS1</td></tr>
<tr><td>12</td><td>BS2</td></tr>
<tr><td>13</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>14</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
</table>

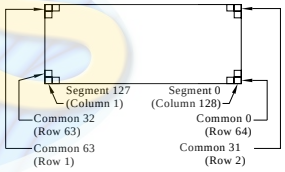
15	D/C#	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.
16	R/W#	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
17	E/RD#	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
18~25	D0~D7	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.

26	IREF	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5μA.
27	VCOMH	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
28	VCC	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
29	VLSS	*Ground of Analog Circuit* This is an analog ground pin. It should be connected to VSS externally.
30	NC(GND)	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

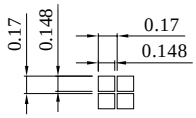
5. Outline Dimension



PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	NC(GND)	14	RES#
2	C2P	15	D/C#
3	C2N	16	R/W#
4	C1P	17	E/RD#
5	C1N	18	D0
6	VBAT	19	D1
7	NC	20	D2
8	VSS	21	D3
9	VDD	22	D4
10	BS0	23	D5
11	BS1	24	D6
12	BS2	25	D7
13	CS#	26	IREF
		27	VCOMH
		28	VCC
		29	VLSS
		30	NC(GND)



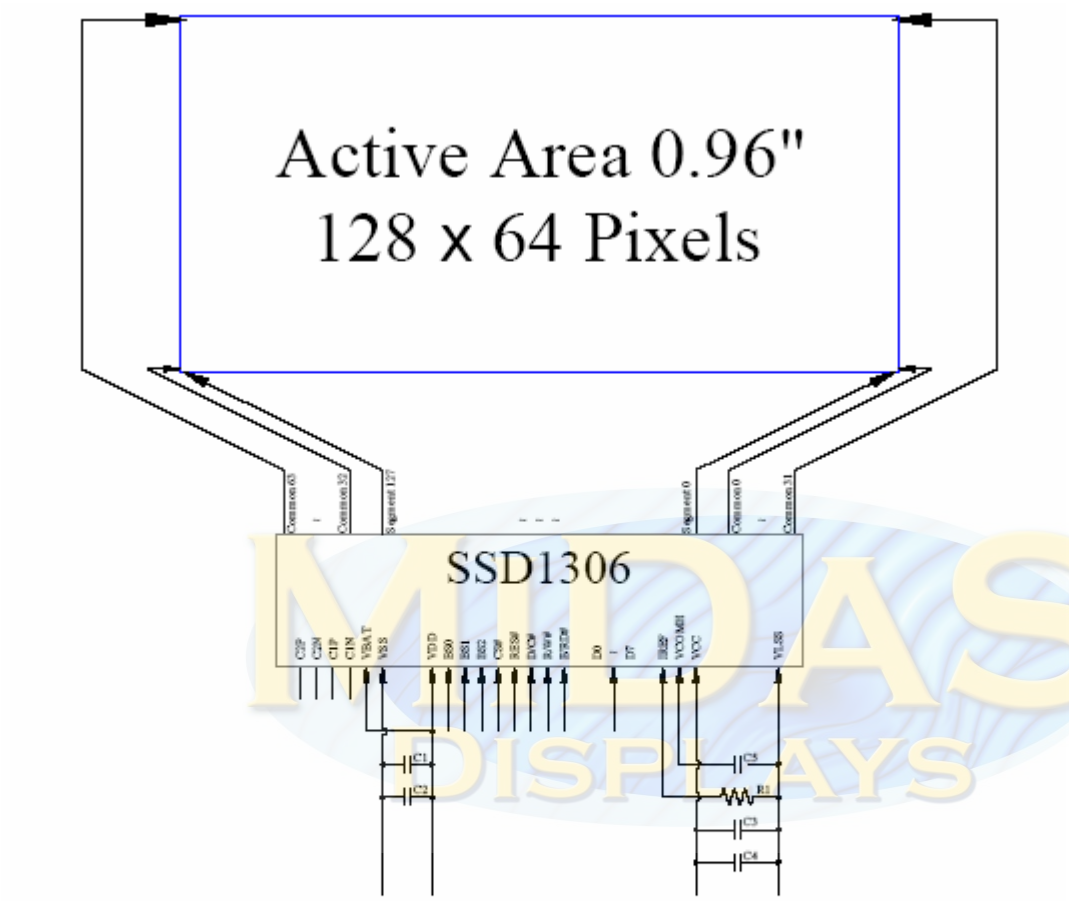
The non-specified tolerance of dimension is ±0.3mm.



SCALE: 20/1

6.Block Diagram

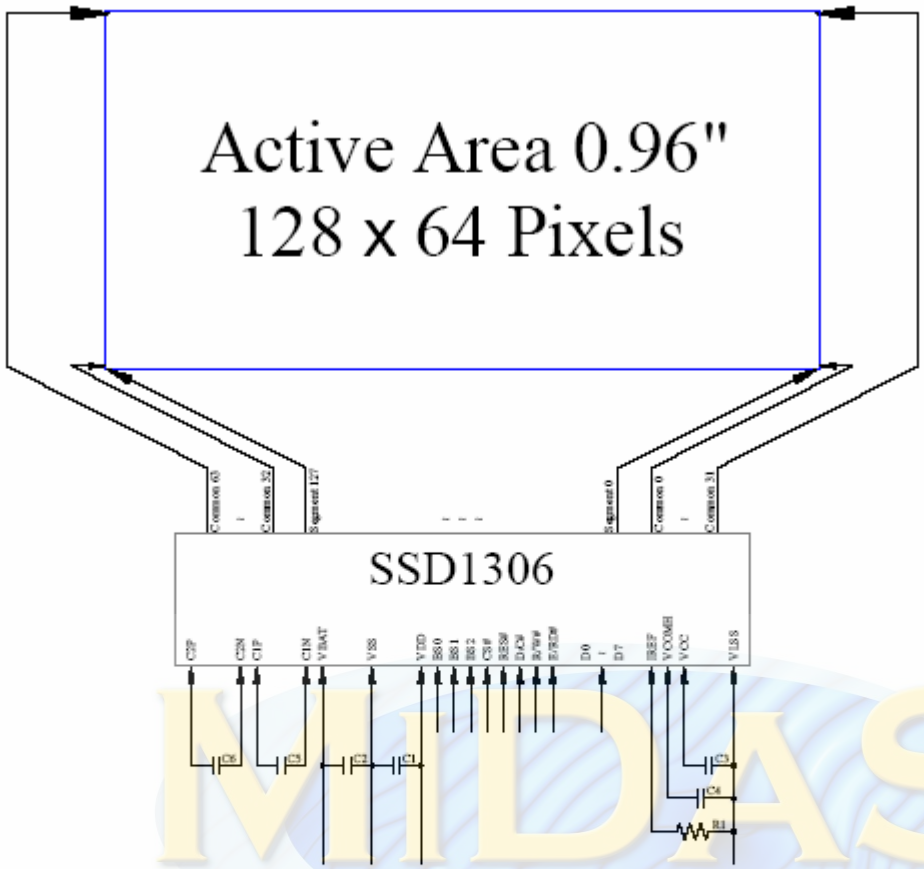
VCC Supplied Externally



MCU Interface Selection: BS0, BS1 and BS2
Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C3: 0.1µF
C2, C4, C5: 4.7µF
R1: 560kΩ, R1 = (Voltage at IREF – VSS) / IREF

V_{CC} Generated by Internal DC/DC Circuit



MCU Interface Selection:	BS0, BS1 and BS2
Pins connected to MCU interface:	CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

C1, C2, C5, C6:	1µF
C3, C4:	4.7µF
R1:	390kΩ, R1 = (Voltage at IREF – VSS) / IREF

7. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	VDD	-0.3	4	V	1,2
Supply Voltage for Display	VCC	0	11	V	1,2
Operating Temperature	TOP	-30	70	°C	—
Storage Temperature	TSTG	-40	80	°C	—

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.“Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

8. Optics & Electrical Characteristics

8.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC}Supplied Externally)	L_{br}	With Polarizer (Note 3)	80	100	-	cd/m2
Brightness (V_{CC}Generated by Internal DC/DC)	*L_{br}*	*With Polarizer (Note 4)*	*50*	*60*	-	*cd/m2*
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.43 0.46	0.47 0.50	0.51 0.54	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 9V & *7.35V*.

Software configuration follows Section 4.4 Initialization.

8.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}	-	1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 3	8.5	9	9.5	V
Supply Voltage for DC/DC	V_{BAT}	Internal DC/DC Enable	3.5	-	4.2	V
Supply Voltage for Display (Generated by Internal DC/DC)	V_{CC}	Note 4	7	7.35	7.5	V
High Level Input	V_{IH}	-	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	-	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT}= 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT}= 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}	-	-	180	300	μA
Operating Current for V_{CC} (V_{CC}Supplied Externally)	I_{CC}	Note 5 Note 6	--	6.0 10.8	7.5 13.5	mA mA
Operating Current for V_{BAT} (V_{CC}Generated by Internal DC/DC)	I_{BAT}	Note 7 Note 8	--	11.6 20.9	14.5 26.1	mA mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$	-	-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$	-	-	1	5	μA

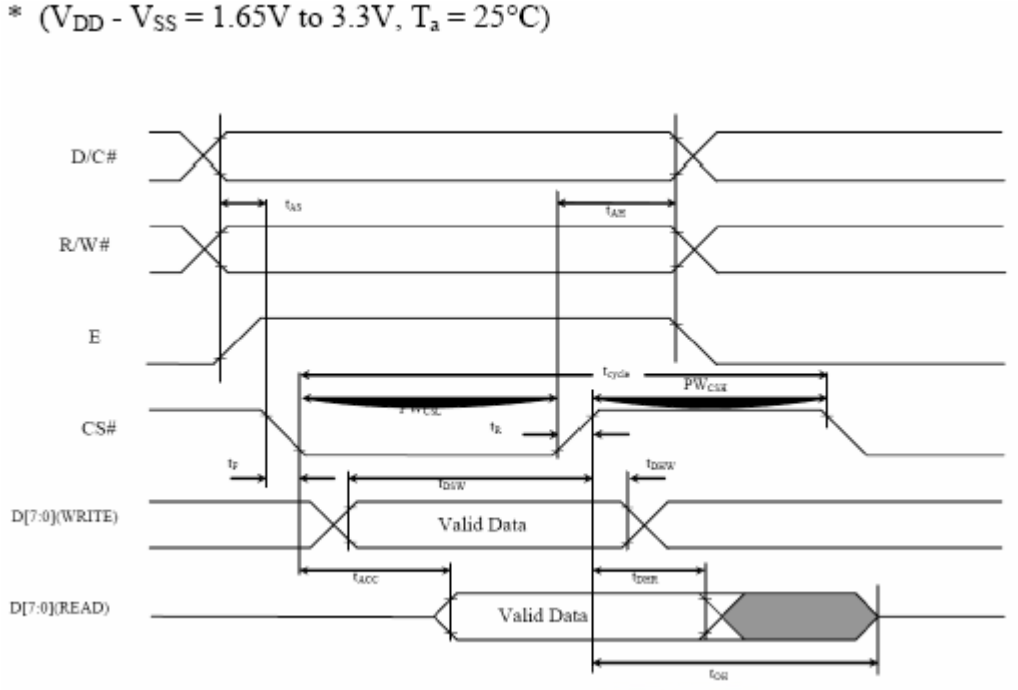
Note 3 & 4: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 5: V_{DD} = 2.8V, V_{CC} = 9V, 50% Display Area Turn on.
Note 6: V_{DD} = 2.8V, V_{CC} = 9V, 100% Display Area Turn on.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.35V, 50% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 7.35V, 100% Display Area Turn on.

8.3 AC Characteristics

8.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

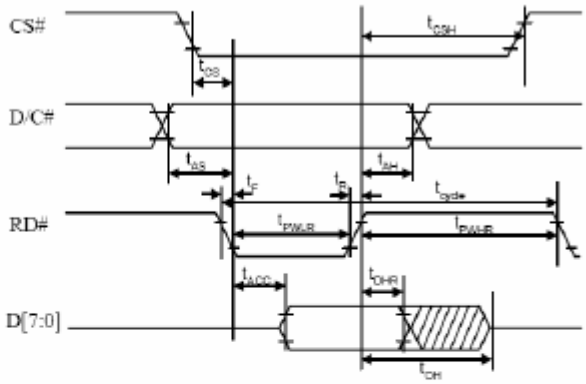
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



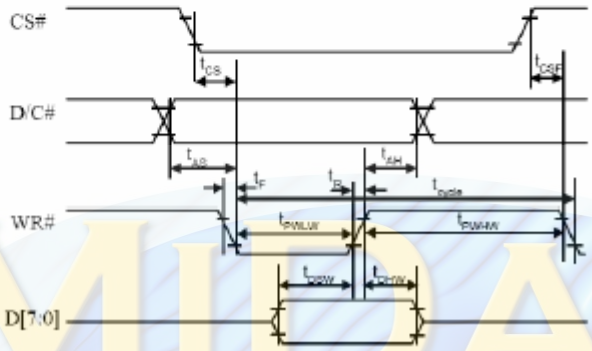
8.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



(Read Timing)

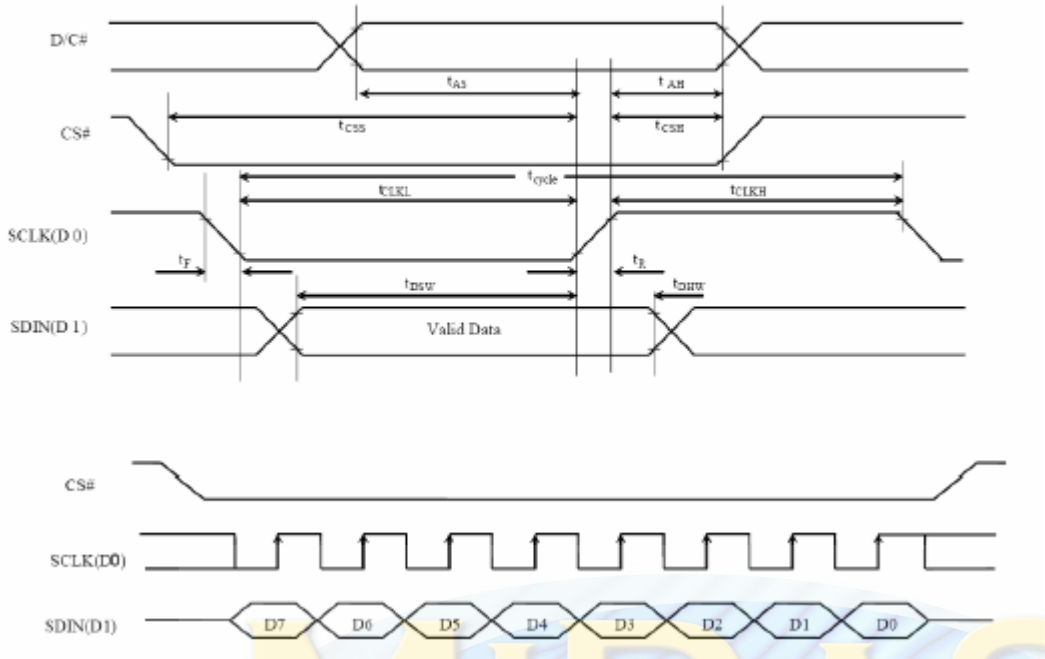


(Write Timing)

8.3.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

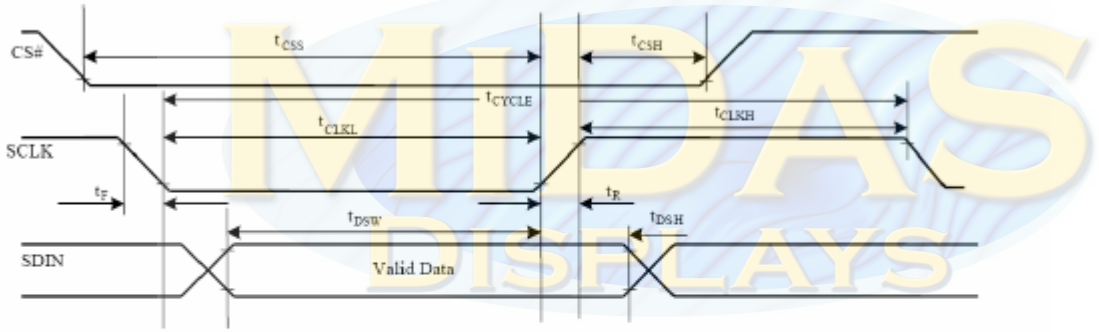
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

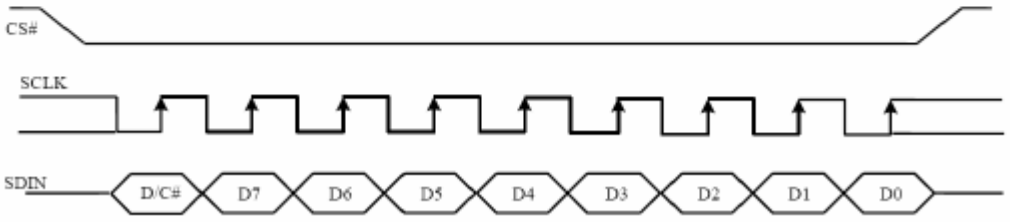


8.3.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)

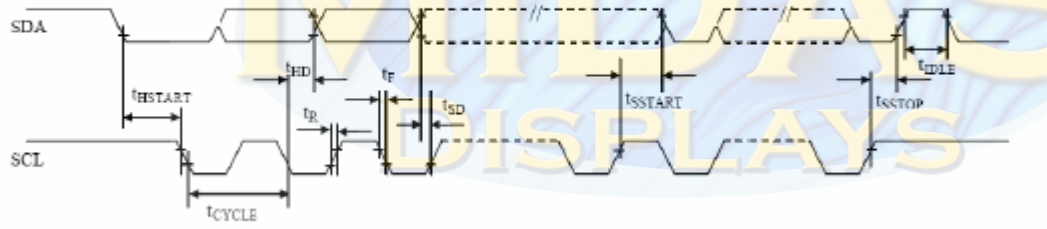




8.3.5 I2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	us
t_{HSTART}	Start Condition Hold Time	0.6	-	us
t_{HD}	Data Hold Time (for "SDA$_{OUT}$" Pin) Data Hold Time (for "SDA$_{IN}$" Pin)	0 300	-	ns
t_{SD}	Data Setup Time	100	-	ns
	Start Condition Setup Time			
t_{SSTART}	(Only relevant for a repeated Start condition)	0.6	-	us
t_{SSTOP}	Stop Condition Setup Time	0.6	-	us
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	us

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



9. Reliability

9.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation Low Temperature Operation	70℃,240hrs -30℃,240hrs	The operational functions work.
High Temperature Storage Low Temperature Storage	80℃,240hrs -40℃,240hrs	
High Temperature/Humidity Operation/ Thermal Shock	60℃,90%RH,120hrs， -40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

9.2 Lifetime

End of lifetime is specified as 50% of initial brightness reached.

Parameter	Min	Typ.	Max	Unit	Condition	Notes
Operating Life Time	-		-	hr	100 cd/m2, 50% Checkerboard	6

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

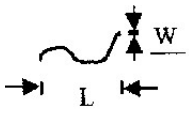
9.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

9.4Mechanical Test

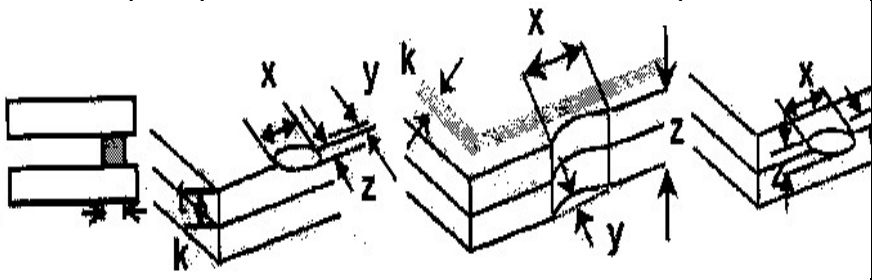
Mechanical Test			
Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——

10. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 Viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">Black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
<table>
<tr><th>Size Φ</th><th>Acceptable Q TY</th></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20＜Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50＜Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00＜Φ</td><td>0</td></tr>
<tr><td>Total Q TY</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
</table>

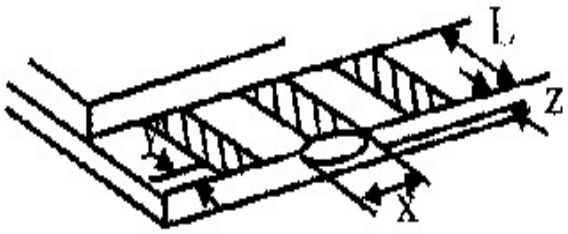
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 Black spots, white spots, contamination</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>
Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length:

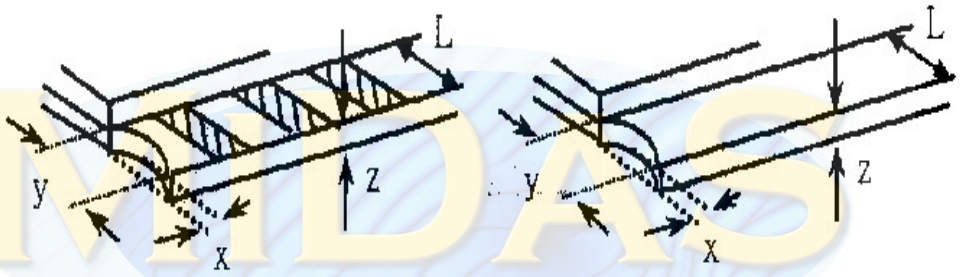
6.1 General glass chip :
6.1.1 Chip on panel surface and crack between panels:


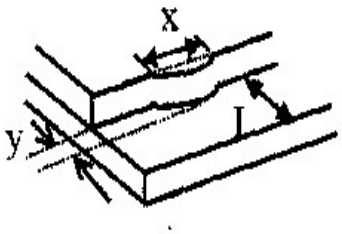
<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.

6.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
</td><td></td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: Side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


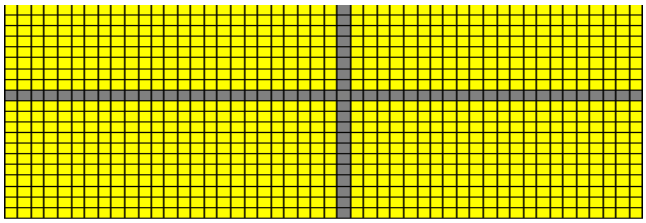
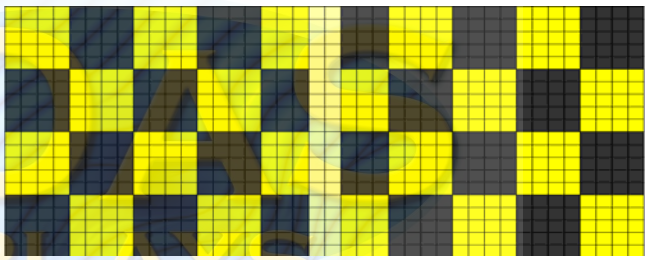
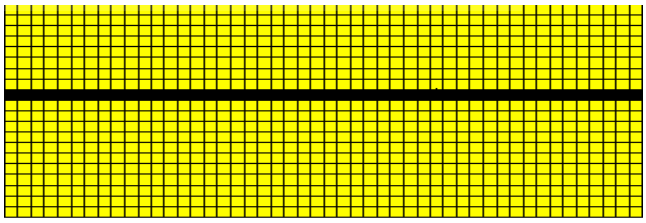
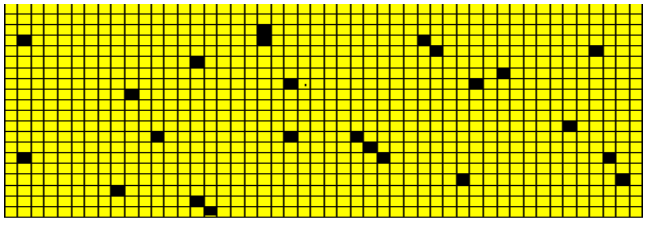
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


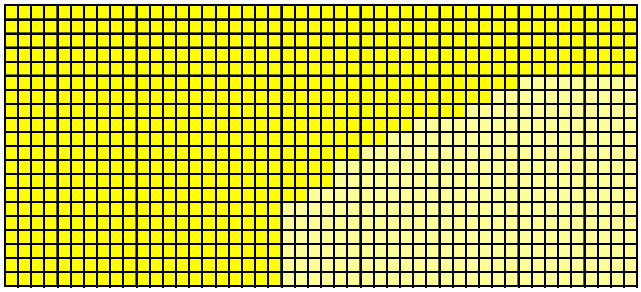
<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	With extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using Spot, lines and contamination standards. 8.3 Backlight doesn't light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down.	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 Pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

Standard：

Defect item	Sorting	Defect judgment
No Display	Major	
Dark crisscross line	Major	
Short	Major	
Miss line	Major	
Wrong Display	Major	

Display Uneven	Major	
Dark dot and light line	Major