

12.5 Gb/s Driver Amplifier

PSPL5865 Datasheet



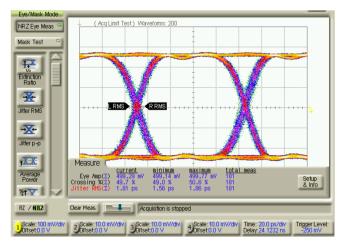
The Model PSPL5865 Driver Amplifier is intended for use driving Lithium Niobate modulators or as a linear amplifier.

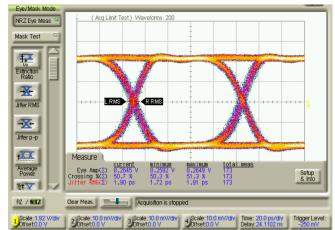
The PSPL5865 includes internal temperature compensation for excellent output stability over temperature, and exhibits both high output and low power dissipation. It also incorporates internal sequencing circuitry, making it insensitive to power supply application sequence.

Key performance specifications

- 8 V output amplitude 12.5 Gb/s Modulator Driver
- Linear amplifier with 26 dB gain
- 30 kHz to 12 GHz bandwidth
- Temperature compensated design for output stability
- Includes bias network, crossing point control & adjustable output voltage

Typical 10.66 Gb/s Eye Measurements





Input Test Signal

Output Response

PSPL5865 12.5 Gb/s Driver Amplifier

Specifications

Parameter	Symbol	Units	Min	Typical	Max	Comments
Impedance	Z	Ohms		50		
Upper 3 dB freq.	f _{c,h}	GHz		12		Relative to gain at 2 GHz
Lower 3 dB freq.	f _{c,l}	kHz		30		Relative to gain at 2 GHz
Small signal gain	S ₂₁	dB		26.5		Measured at 2 GHz
Max Power Out (-1 dB gain comp)	P _{1dB}	dBm		23.5		Measured at 2 GHz
Output Eye Voltage with V _{GC} = 0 V	V _{OUT}	V _{amp}	7.5	8.0		V _{in} = 0.5 V _{amp} , 12.5 Gb/s PRBS
Output Eye Voltage with V _{GC} = -15 V	V _{OUT}	V _{amp}		1.0	2.0	V _{in} = 0.5 V _{amp} , 12.5 Gb/s PRBS
Return Loss, Input and Output	S ₁₁ , S ₂₂	dB		-14 -11	12 9	50 MHz < f < 5 GHz 5 GHz ≤ f < 12 GHz
Rise Time	t _r	ps		32	41	10-90%, V _{in} = 0.5 V _{amp} , 12.5 Gb/s PRBS
Fall Time	t _f	ps		36	44	
Additive Jitter RMS Peak-to-Peak		ps ps _{pp}		0.7	2.0	V _{in} = 0.5 V _{amp} , 12.5 Gb/s PRBS, meas. at crossing point
Overshoot		%		5		12.5 Gb/s PRBS
Undershoot		%		5		12.5 Gb/s PRBS
Eff. Input RMS Noise Voltage		μV rms		120		
Noise Figure	NF	dB		5.75	6.5	f = 1 GHz
Output Eye Voltage Variation	ΔV _{OUT}	%		+/-3	+/-5	$\begin{split} V_{gc} &= 0 \text{ V, } V_{in} = 0.5 \text{ V}_{amp}, \\ T_{CASE} &= -5 \text{ to } 75^{\circ}\text{C} \end{split}$
Crossing Point Adjust		%	+/- 15	+/- 20		+/- 5 V input at V_{cp} , $V_{in} = 0.5 V_{amp}$
Crossing Point Variation		%		+/- 1.0	+/- 2.0	V _{in} = 0.5 V _{amp} , 12.5 Gb/s PRBS, T _{CASE} = -5 to 75°C
Polarity	Non-Inverting					
Coupling	AC, input and output					
RF Connectors	SMA jacks (f)					
DC Connector	Solder pins					

Operating Specifications

Parameter	Symbol	Units	Min	Typical	Max	Comments
Voltage Supply (+)	+V _{DC}	V	8	8	8.25	
Voltage Supply (-)	-V _{DC}	V	-5.25	-5	-4.75	
Supply Current (+)	+I _{DC}	mA		275		V _{out} = 8 V _{amp} [1]
Supply Current (-)	-I _{DC}	mA		20		
Power Dissipation	P _{diss}	W		2.3	2.6	V _{out} = 8 V _{amp} [2]
Max Allowed Input		V _{amp}			1.5	Input damage threshold
Output Voltage Bias	V _{bias}	V _{DC}	-17	0	33	No connection required [3]
Gain Control Bias	V _{gc}	V _{DC}	-15	0	0	No connection required
Crossing Point Bias	V _{cp}	V _{DC}	-5	0	5	No connection required
Operating Temp	T _{CASE}	Deg C	-5		75	Case temperature
Storage Temp	T _{stor}	Deg C	-40		125	Case tempurature
Warranty	One Year					

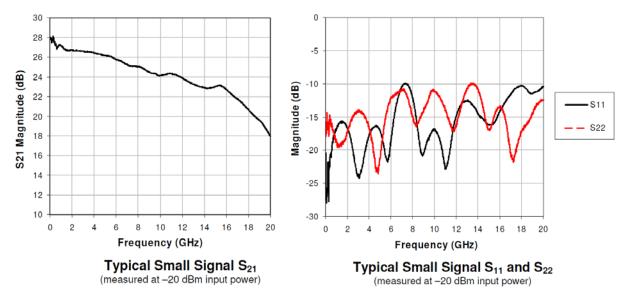
Notes:

[1] The PSPL5865 may be damaged by excessive heat that is produced when driving low duty cycle positive pulses. To ensure the amplifier will not be damaged by overheating, it is recommended the positive supply voltage has its current limit set to 320 mA.

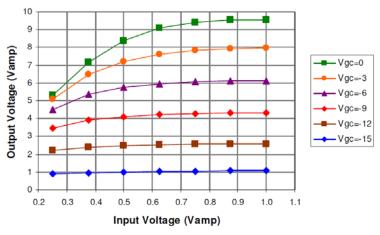
[2] V_{gc} may be utilized to lower the output level and power dissipated. $V_{cp} > 0$ V will lower the crossing point and increase the power dissipated.

[3] A 2.5 k Ω resistor is connected to the output from the V_{bias} pin for adding a low current (\leq 3.5mA) DC bias.

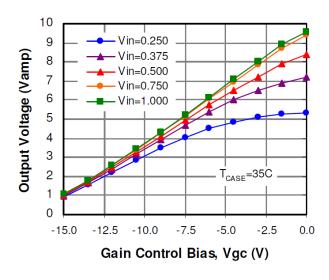
Microwave frequency response

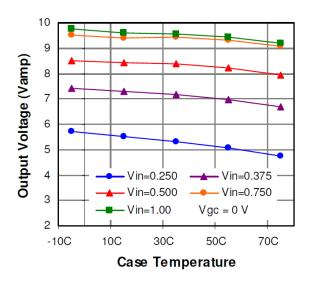


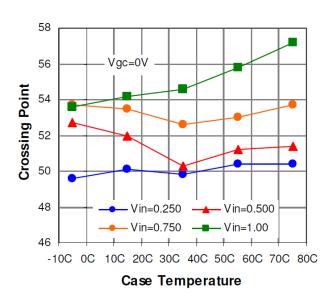
Typical performance plots

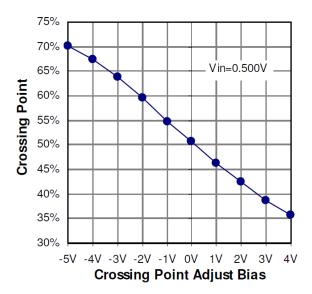


Typical Output Voltage versus Input Voltage (Gain Control Bias = Vgc, T_{CASE} = 35C)



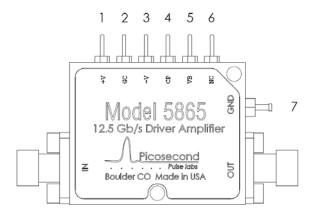






Instructions for use

The PSPL5865 12.5 Gb/s modulator driver may be operated using only three of the available 7 pins. The DC pins required for operation are 1, 3, and 7. The RF connectors and DC pins are diagramed and defined below.



Pin Descriptions

Pin #	Pin Label	Description
	IN	SMA, signal input, V _{amp} ≤ 1.5 V (damage threshold)
1	+V	Positive DC voltage supply, 8 V (see Note 1 and Note 2)
2	GC	V_{qc} , Variable output control, -15 V \leq $V_{qc} \leq$ 0 V (see Note 3)
3	-V	Negative DC voltage supply, -5.25 V ≤ V ≤ -4.75 V (see Note 2)
4	CP	Crossing point adjust, -5 V \leq V _{cp} \leq 5 V (see Note 4)
5	VB	DC Voltage bias, -17 ≤ VB ≤ +33 (see Note 5)
6	NC	No connection / Not used
7	GND	Ground connection
	OUT	SMA, signal output

Warning: The PSPL5865 requires a ground connection at pin#7 prior to voltage application to prevent damage.

NOTES:

Note 1: At 8V, approximately 2.3W is dissipated.

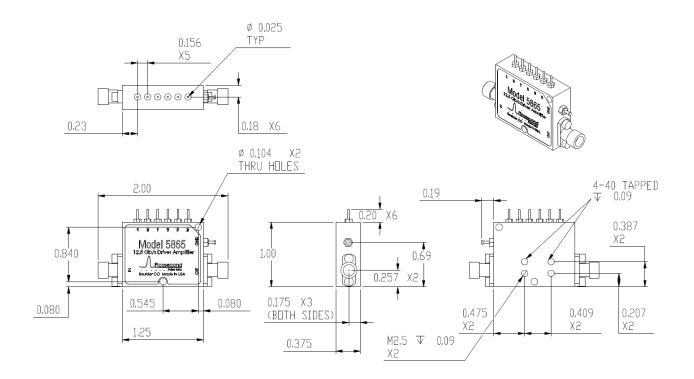
Note 2: No power sequencing is necessary. Voltages may be applied in any order after ground is applied.

Note 3: Output Control: With V_{GC} at 0V, or left floating (disconnected), the driver will provide maximum gain and maximum output voltage. The user may decrease V_{GC} to decrease the RF signal gain when the driver is operating in the linear regime, or to reduce the output voltage level when the driver is operated in saturation (this will also reduce the power dissipated).

Note 4: The crossing point may vary until unit achieves thermal equilibrium. $V_{CP} > 0$ V will lower the output crossing point and increase power dissipation. Care must be taken to ensure that the positive supply current does not exceed 320 mA.

Note 5: Voltage Bias: The VB pin allows the user to apply a low current (less than 3.5 mA) DC offset to the Signal Output for biasing electro-optic modulators through a 2.5 k Ω resistor.

PSPL5865 Mechanical dimensions



Ordering information

Model **Description**

12.5 GB/S DRIVER AMPLIFIER, SMA J-J **PSPL5865**

Datasheet

ASEAN / Australasia (65) 6356 3900

Belgium 00800 2255 4835* Central East Europe and the Baltics +41 52 675 3777 Finland +41 52 675 3777 Hong Kong 400 820 5835 Japan 81 (3) 6714 3010 Middle East, Asia, and North Africa +41 52 675 3777 People's Republic of China 400 820 5835 Republic of Korea 001 800 8255 2835 Spain 00800 2255 4835* Taiwan 886 (2) 2722 9622 * European toll-free number. If not accessible, call: +41 52 675 3777 Austria 00800 2255 4835*

Brazil +55 (11) 3759 7627 Central Europe & Greece +41 52 675 3777 France 00800 2255 4835* India 000 800 650 1835 Luxembourg +41 52 675 3777 The Netherlands 00800 2255 4835* Poland +41 52 675 3777 Russia & CIS +7 (495) 6647564 Sweden 00800 2255 4835* United Kingdom & Ireland 00800 2255 4835* Balkans, Israel, South Africa and other ISE Countries +41 52 675 3777

Canada 1 800 833 9200 Denmark +45 80 88 1401 Germany 00800 2255 4835* Italy 00800 2255 4835*

Mexico, Central/South America & Caribbean 52 (55) 56 04 50 90

Norway 800 16098 Portugal 80 08 12370 South Africa +41 52 675 3777 Switzerland 00800 2255 4835* USA 1 800 833 9200

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