SAMG53G, SAMG53N

ARM-based Flash MCU

SUMMARY DATASHEET

Description

The Atmel® SAM G53 series is a member of the SAM G family of Flash microcontrollers based on the high-performance 32-bit ARM® Cortex®-M4 RISC processor. It operates at a maximum speed of 48 MHz and features up to 512 Kbytes of Flash and 96 Kbytes of SRAM. The peripheral set includes one USART, two UARTs, three I^2C-bus interfaces (TWI), up to two SPIs, two three-channel general-purpose 16-bit timers, two I2S controllers with two-way, one-channel pulse density modulation, one real-time timer (RTT) and one 8-channel 12-bit ADC.

A general-purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set, the SAM G53 series sustains a wide range of applications including consumer, industrial control, and PC peripherals.

The device operates from 1.70V to 3.6V and is available in a 49-ball WLCSP package and a 100-pin LQFP package.

Features

- Core
  - ARM Cortex-M4 up to 48 MHz
  - Memory Protection Unit (MPU)
  - DSP Instructions
  - Floating Point Unit (FPU)
  - Thumb®-2 instruction set
- Memories
  - 512 Kbytes embedded Flash
  - 96 Kbytes embedded SRAM
- System
  - Embedded voltage regulator for single-supply operation
  - Power-on reset (POR) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or device clock
  - High-precision 8/16/24 MHz factory-trimmed internal RC oscillator. In-application trimming access for frequency adjustment

This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

  - Slow clock internal RC oscillator as permanent low-power mode device clock
  - PLL range from 24 MHz to 48 MHz for device clock
  - 28 peripheral DMA (PDC) channels
  - 8 x 32-bit General-Purpose Backup Registers (GPBR)
  - 16 external interrupt lines
- Power consumption in active mode
  - 102 µA/MHz running Fibonacci in SRAM
- Low power modes (typical value)
  - Wait mode down to 8 µA
  - Wake-up time less than 5 µs
  - Asynchronous partial wake-up (SleepWalking™)
- Peripherals
  - One USART with SPI mode
  - Two Inter-IC Sound Controllers (I2S)
  - Two-way one-channel Pulse Density Modulation (PDM) (interfaces up to two microphones in PDM mode)
  - Two two-wire UARTs
  - Three Two-wire Interface (TWI) modules featuring twoTWI masters and one high-speed TWI slave
  - One fast SPI at up to 24Mbit/s
  - Two three-channel 16-bit Timer/Counters (TC) with capture, waveform, compare and PWM modes
  - One 32-bit Real-Time Timer (RTT)
- I/O
  - Up to 38 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die series resistor termination. Individually programmable open-drain, pull-up and pull-down resistor and synchronous output
  - Two up to 25-bit PIO Controllers
- Analog
  - One 8-channel ADC, resolution up to 12 bits, sampling rate up to 800 kSps
- Package
  - 49-ball WLCSP
  - 100-pin LQFP, 14 x 14 mm, pitch 0.5 mm
- Temperature operating range
  - Industrial (-40 °C to +85 °C)

1. Configuration Summary

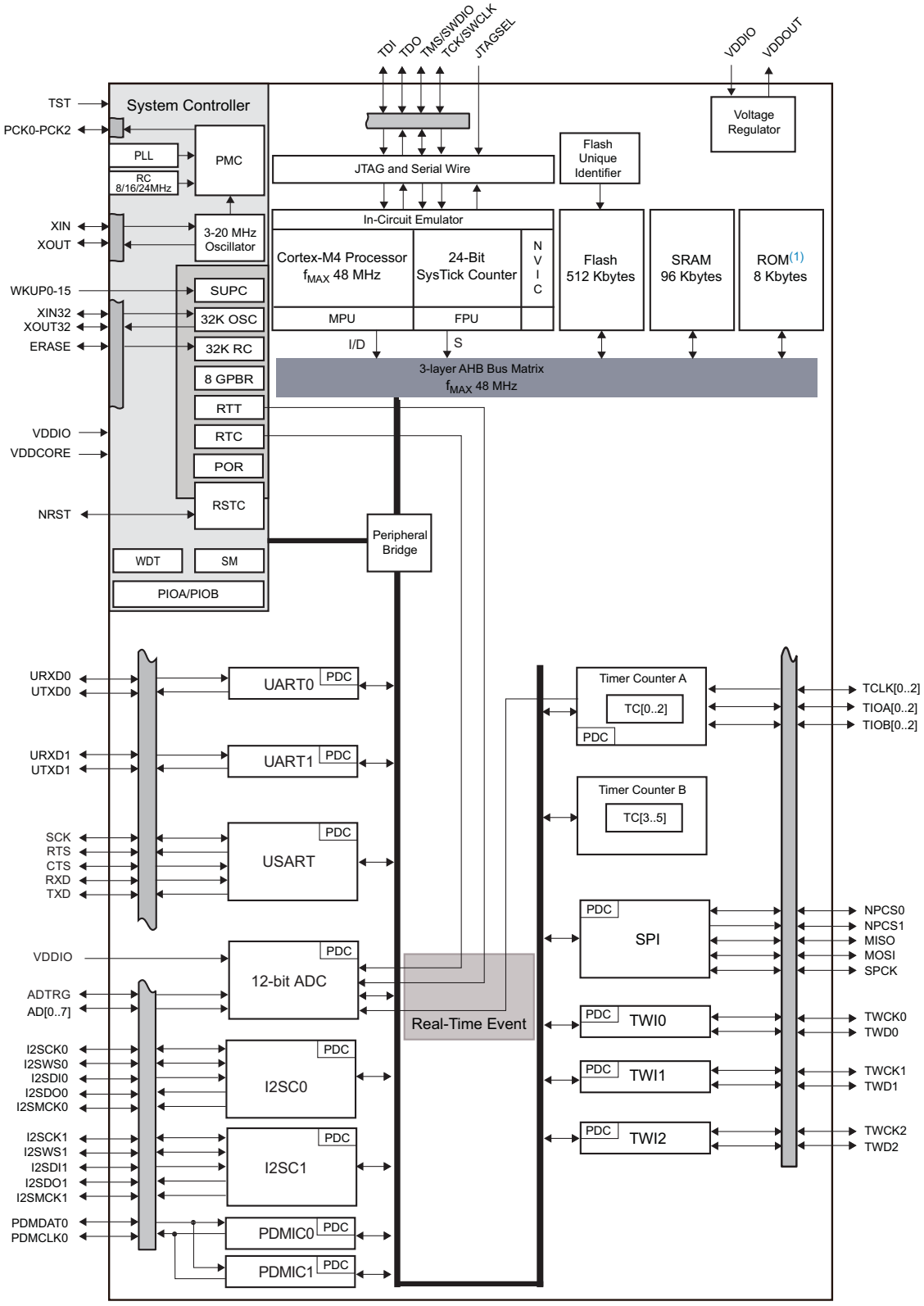
Table 1-1 summarizes the SAM G53 device configurations.

Table 1-1. Configuration Summary

Feature	SAM G53G19	SAM G53N19
Flash	512 Kbytes	512 Kbytes
SRAM	96 Kbytes	96 Kbytes
Package	WLCSP49	LQFP100
Number of PIOs	38	38
Event System	Yes	Yes
12-bit ADC	8 channels Performance: 800 KSps at 10-bit resolution 200 KSps at 11-bit resolution 50 KSps at 12-bit resolution	8 channels Performance 800 KSps at 10-bit resolution 200 KSps at 11-bit resolution 50 KSps at 12-bit resolution
16-bit Timer	6 channels (3 external channels)	6 channels (3 external channels)
I2SC/PDM	2 / 1-channel 2-way	2 / 1-channel 2-way
PDC Channels	28	28
USART/UART	1/2	1/2
SPI	1	1
TWI	2 masters at 400Kbits/s and 1 slave at 3.4Mbit/s	2 masters 400Kbits/s and 1 slave 3.4Mbit/s

2. Block Diagram

Figure 2-1. SAM G53 Block Diagram



Note: 1. The ROM is reserved for future use.

3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripheral I/O Lines, Voltage Regulator, ADC Power Supply	Power	–	–	1.70V to 3.6V
VDDOUT	Voltage Regulator Output	Power	–	–	–
VDDCORE	Core Chip Power Supply	Power	–	–	Connected externally to VDDOUT
GND	Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	Reset state: - PIO input - Internal pull-up disabled - Schmitt Trigger enabled
XOUT	Main Oscillator Output	Output	–	–	
XIN32	Slow Clock Oscillator Input	Input	–	VDDIO	
XOUT32	Slow Clock Oscillator Output	Output	–	–	
PCK0 - PCK2	Programmable Clock Output	Output	–	–	Reset state: - PIO input - Internal pull-up enabled - Schmitt Trigger enabled
ICE and JTAG					
TCK	Test Clock	Input	–	VDDIO	No pull-up resistor
TDI	Test Data In	Input	–	VDDIO	No pull-up resistor
TDO	Test Data Out	Output	–	VDDIO	–
TRACESWO	Trace Asynchronous Data Out	Output	–	VDDIO	–
SWDIO	Serial Wire Input/Output	I/O	–	VDDIO	–
SWCLK	Serial Wire Clock	Input	–	VDDIO	–
TMS	Test Mode Select	Input	–	VDDIO	No pull-up resistor
JTAGSEL	JTAG Selection	Input	High	VDDIO	Pull-down resistor
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Pull-down (15 kΩ) resistor

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Reset/Test					
NRST	Microcontroller Reset	I/O	Low	VDDIO	Pull-up resistor
TST	Test Mode Select	Input	–	VDDIO	Pull-down resistor
Universal Ansynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input	–	–	–
UTXDx	UART Transmit Data	Output	–	–	–
PIO Controller - PIOA - PIOB					
PA0 - PA24	Parallel I/O Controller A	I/O	–	VDDIO	Pulled-up input at reset. No pull-down for PA3/PA4/PA14.
PB0 - PB12	Parallel I/O Controller B	I/O	–	VDDIO	Pulled-up input at reset
Wake-up Pins					
WKUP 0-15	Wake-up Pin / External Interrupt	I/O	–	VDDIO	Wake-up pins are used also as External Interrupt
Universal Synchronous Asynchronous Receiver Transmitter USART					
SCK	USART Serial Clock	I/O	–	–	–
TXD	USART Transmit Data	I/O	–	–	–
RXD	USART Receive Data	Input	–	–	–
RTS	USART Request To Send	Output	–	–	–
CTS	USART Clear To Send	Input	–	–	–
Timer/Counter - TCx					
TCLKx	TC Channel x External Clock Input	Input	–	–	–
TIOAx	TC Channel x I/O Line A	I/O	–	–	–
TIOBx	TC Channel x I/O Line B	I/O	–	–	–
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O	–	–	–
MOSI	Master Out Slave In	I/O	–	–	–
SPCK	SPI Serial Clock	I/O	–	–	High-speed pad
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
NPCS1	SPI Peripheral Chip Select 1	Output	Low	–	–

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Two-Wire Interface- TWIx					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	High-speed pad for TWD0
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	High-speed pad for TWDCK0
10-bit Analog-to-Digital Converter - ADCC					
AD0 - AD7	Analog Inputs	Analog	–	–	–
ADTRG	ADC Trigger	Input	–	–	–
Inter-IC Sound Controller - I2SCx					
I2SMCKx	Master Clock	Output	–	–	–
I2SCKx	Serial Clock	I/O	–	–	–
I2SWSx	I2S Word Select	I/O	–	–	–
I2SDIx	Serial Data Input	Input	–	–	–
I2SDOx	Serial Data Output	Output	–	–	–
PDMCLK0	Pulse Density Modulation Clock	Output	–	–	–
PDMDAT0	Pulse Density Modulation Data	Input	–	–	–

4. Package and Pinout

Table 4-1. SAM G53 Packages

Device	Package
SAM G53G19	WLCSP49
SAM G53N19	LQFP100

4.1 49-ball WLCSP Pinout

Table 4-2. SAM G53G19 49-ball WLCSP Pinout

A1	PA9	C1	VDDCORE	E1	PB2/AD6	G1	VDDIO
A2	GND	C2	PA11	E2	PB0/AD4	G2	VDDOUT
A3	PA24	C3	PA12	E3	PA18/AD1	G3	GND
A4	PB8/XOUT	C4	PB6	E4	PA14	G4	VDDIO
A5	PB9/XIN	C5	PA4	E5	PA10	G5	PA22
A6	PB4	C6	PA3	E6	TST	G6	PA15
A7	VDDIO	C7	PA0	E7	PA7/XIN32	G7	PA6
B1	PB11	D1	PA13	F1	PA20/AD3		
B2	PB5	D2	PB3/AD7	F2	PA19/AD2		
B3	PB7	D3	PB1/AD5	F3	PA17/AD0		
B4	PA2	D4	PB10	F4	PA21		
B5	JTAGSEL	D5	PA1	F5	PA23		
B6	NRST	D6	PA5	F6	PA16		
B7	PB12	D7	VDDCORE	F7	PA8/XOUT32		

4.2 100-lead LQFP Pinout

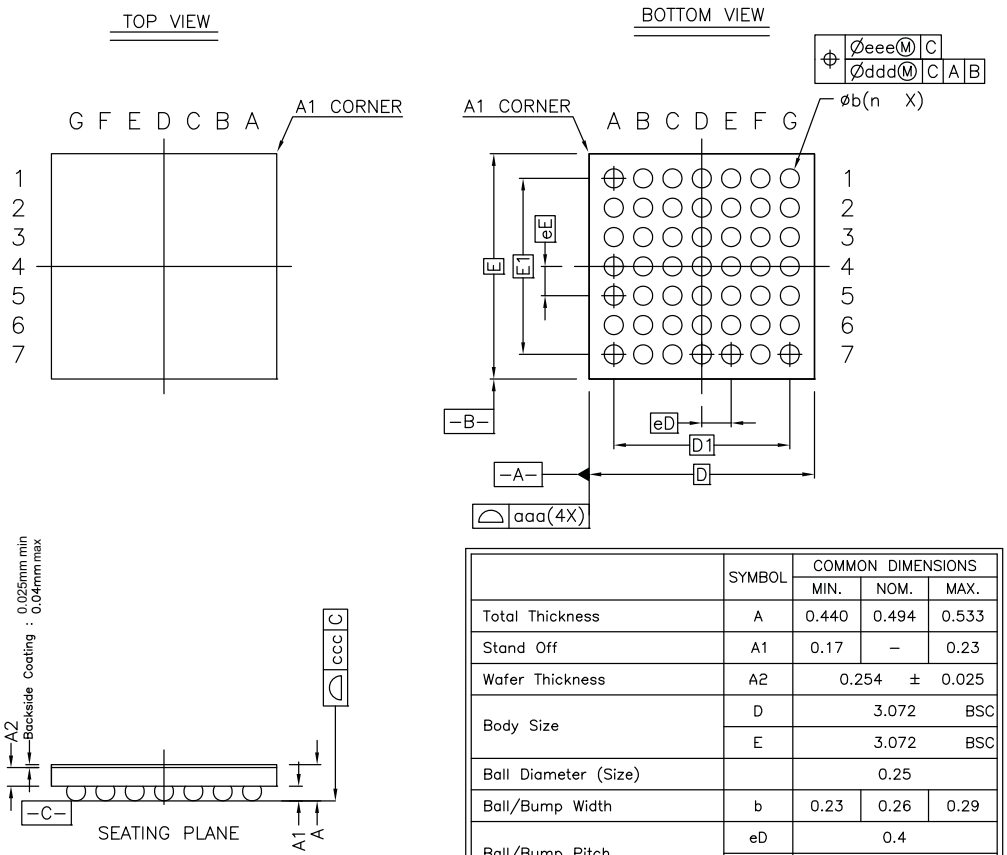
Table 4-3. SAM G53N19 100-pin LQFP Pinout

1	NC	26	NC	51	NC	76	NC
2	NC	27	NC	52	NC	77	NC
3	NC	28	PA6	53	PA17	78	NC
4	NC	29	VDDIO	54	PA18	79	PA9
5	VDDIO	30	PA16	55	PA19	80	PB5
6	VDDIO	31	PA15	56	PA20	81	GND
7	NRST	32	PA23	57	PB0	82	GND
8	PB12	33	NC	58	PB1	83	GND
9	PA4	34	NC	59	PB2	84	PB6
10	PA3	35	PA22	60	PB3	85	PB7
11	PA0	36	PA21	61	VDDIO	86	PA24
12	PA1	37	VDDIO	62	PA14	87	PB8
13	PA5	38	VDDIO	63	PA13	88	PB9
14	VDDIO	39	GND	64	PA12	89	VDDIO
15	VDDCORE	40	GND	65	PA11	90	PA2
16	VDDCORE	41	GND	66	VDDCORE	91	PB4
17	TEST	42	GND	67	VDDCORE	92	NC
18	PA7	43	GND	68	PB10	93	JTAGSEL
19	PA8	44	VDDOUT	69	PB11	94	VDDIO
20	GND	45	VDDOUT	70	GND	95	VDDIO
21	NC	46	VDDIO	71	GND	96	NC
22	NC	47	VDDIO	72	PA10	97	NC
23	NC	48	VDDIO	73	NC	98	NC
24	NC	49	NC	74	NC	99	NC
25	NC	50	NC	75	NC	100	NC

5. Mechanical Characteristics

5.1 49-lead WLCSP Package

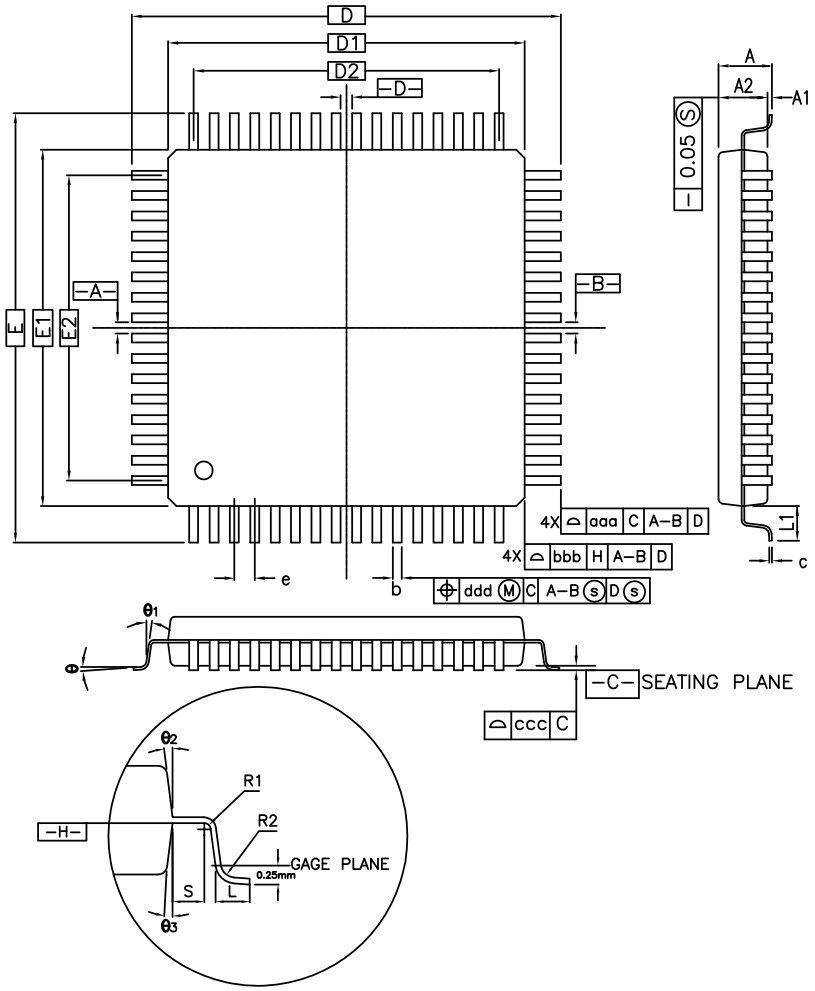
Figure 5-1. 49-lead WLCSP Package Mechanical Drawing



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.440	0.494	0.533
Stand Off	A1	0.17	–	0.23
Wafer Thickness	A2		0.254 ± 0.025	
Body Size	D		3.072 BSC	
	E		3.072 BSC	
Ball Diameter (Size)			0.25	
Ball/Bump Width	b	0.23	0.26	0.29
Ball/Bump Pitch	eD		0.4	
	eE		0.4	
Ball/Bump Count	n		49	
Edge Ball Center to Center	D1		2.4 BSC	
	E1		2.4 BSC	
Package Edge Tolerance	aaa		0.03	
Coplanarity (whole wafer)	ccc		0.075	
Ball/Bump Offset (Package)	ddd		0.05	
Ball/Bump Offset (Ball)	eee		0.015	

5.2 100-lead LQFP Package

Figure 5-2. 100-lead LQFP Package Mechanical Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	100L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

6. Ordering Information

Table 6-1. Ordering Codes for SAM G53 Devices

Ordering Code	MRL	Flash (Kbytes)	Package	Carrier Type	Package Type	Temperature Operating Range
ATSAMG53G19A-UUT	A	512	WLCSP49	Tape and Reel	Green	Industrial -40°C to 85°C
ATSAMG53N19A-AU	A	512	LQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAMG53N19A-AUT	A	512	LQFP100	Tape and Reel	Green	Industrial -40°C to 85°C

7. Revision History

In the tables that follow, the most recent version of the document appears first.

Table 7-1. SAM G53 Datasheet Rev. 11240CS Revision History

Doc. Rev. 11240CS	Changes
04-Jun-14	Updated document title on first page Minor formatting changes throughout
	Section 6. “Ordering Information” Table 6-1, “Ordering Codes for SAM G53 Devices”: added prefix ‘AT’ to ordering codes; deleted “(Kbytes)” from “Package” column header; added “Carrier Type” column

Table 7-2. SAM G53 Datasheet Rev. 11240BS Revision History

Doc. Rev. 11240Bs	Changes
06-May-14	Operating voltage range changed to 1.70V to 3.6V throughout. Figure 2-1 “SAM G53 Block Diagram”: added VDDIO on ADC. Table 4-3, “SAM G53N19 100-pin LQFP Pinout”: corrected pin 92 to NC. Figure 5-1 “49-lead WLCSP Package Mechanical Drawing”: changed values for backside coating and for min of Total Thickness.

Table 7-3. SAM G53 Datasheet Rev. 11240As Revision History

Doc. Rev. 11240AS	Changes
14-Jan-14	First issue

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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