ACPL-798J

Optically Isolated Sigma-Delta Modulator with LVDS Interface

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The ACPL-798J is a 1-bit, second-order sigma-delta (Σ–Δ) modulator that oversamples an analog input signal into a highspeed data stream with galvanic isolation based on optical coupling technology. The ACPL-798J operates from a 5 V power supply with dynamic range of 82 dB with an appropriate digital filter. The differential inputs of ±200 mV (full scale ±320 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by means of sigma-delta over-sampling using external clock, coupled across the isolation barrier, which allows synchronous operation with any digital controller. The signal information is contained in the modulator data, as a density of ones with data rate up to 25 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The ACPL-798J comes with an LVDS interface on both clock inputs and data outputs for better signal integrity.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5 mm minimum distance through insulation (DTI), the ACPL-798J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive or magnetic-coupling with DTI in micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

Features

- Up to 25 MHz external clock input range
- LVDS clock and data interface.
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (12 bits ENOB)
- 75dB Typical SNDR
- 3.5µV/°C maximum offset drift
- ±1% maximum gain error
- ±200 mV linear range with single 5 V supply
- –40°C to +105°C operating temperature range
- SO-16 package
- 25 kV/µs common-mode transient immunity
- Safety and regulatory approval (pending):
  IEC/EN/DIN EN 60747-5-5: 1414 Vpeak working insulation voltage
  UL 1577: 5000 Vrms/1min double protection rating
  CSA: Component Acceptance Notice #5

Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing
- Industrial process control
- Data acquisition systems
- General purpose current and voltage sensing
- Traditional current transducer replacement

Functional Block Diagram

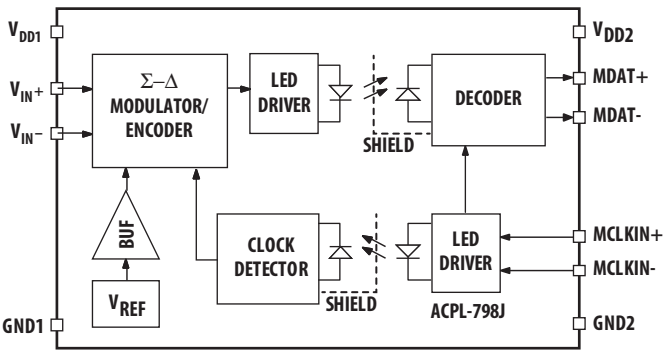


Figure 1.

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pin Configuration and Descriptions

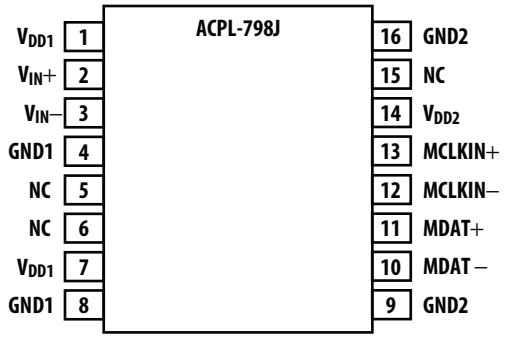


Figure 2. Pin configuration.

Table 1. Pin descriptions.

Pin No.	Symbol	Description
1,7	V_{DD1}	Supply voltage for input side relative to GND1.
2	V_{IN}+	Positive analog input, recommended input range ±200 mV.
3	V_{IN}–	Negative analog input, recommended input range ±200 mV (normally connected to GND1).
4,8	GND1	Supply ground for signal input side.
5,6,15	NC	No connection. Leave floating.
9, 16	GND2	Supply ground for data output side (digital side).
11	MDAT+	Positive LVDS modulator data output.
10	MDAT-	Negative LVDS modulator data output.
13	MCLKIN+	Positive LVDS modulator clock input
12	MCLKIN-	Negative LVDS modulator clock input
8	V_{DD2}	Supply voltage for output side, referenced to GND2.

Table 2. Ordering Information

Part number	Option (RoHS Compliant)	Package	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-798J	-000E	SO-16		X	45 per tube
	-500E		X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

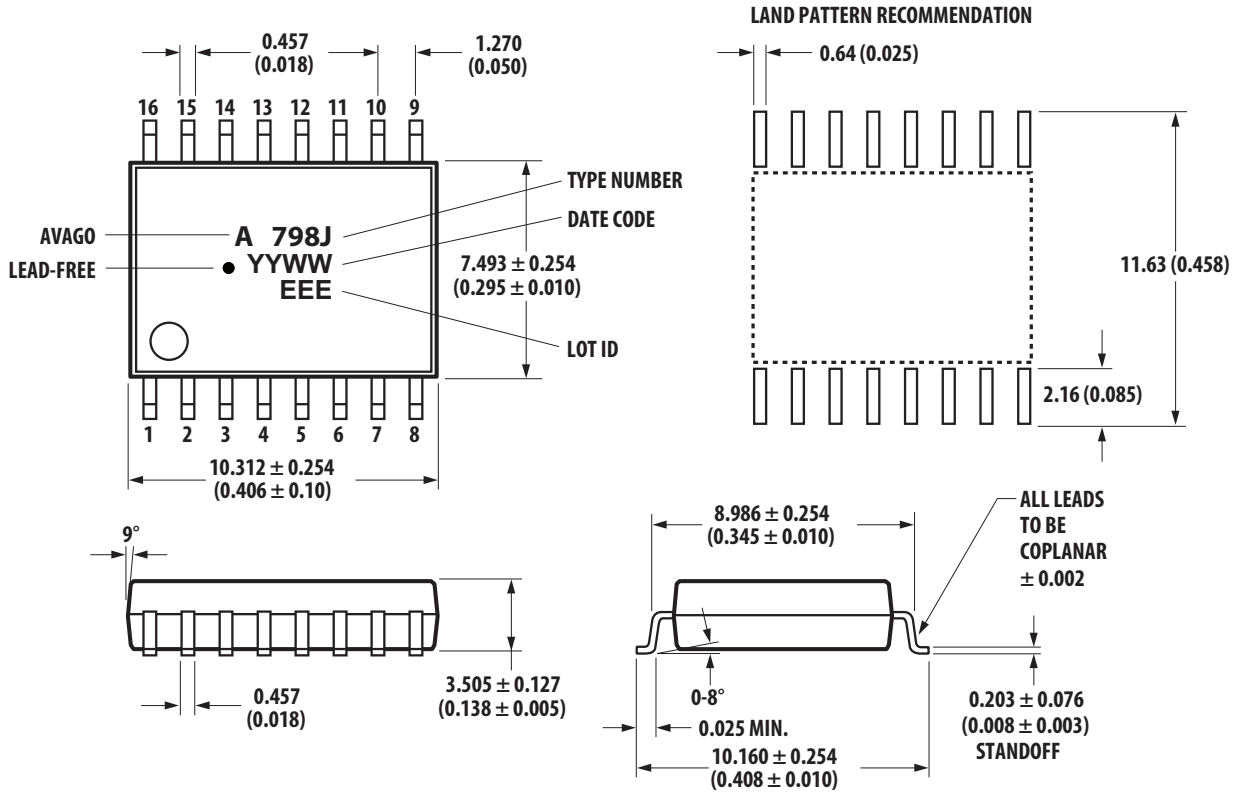
Example:

ACPL-798J-500E to order product in Tape and Reel packaging.

Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

16-Lead Surface Mount (SO-16)



Dimensions in millimeters and (inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device.

Figure 3. 16-Lead Surface Mount.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Regulatory Information

The ACPL-798J is pending for approvals by the following organizations:

IEC/EN/DIN EN 60747-5-5 Approved with Maximum Working Insulation Voltage V_{IORM} = 1414 Vpeak.

UL Approval under UL 1577, component recognition program up to V_{ISO} = 5000 Vrms/1min. File E55361.

CSA Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 3. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[1]

Description	Symbol	Value	Units
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 Vrms		I-IV	
for rated mains voltage ≤ 300 Vrms		I-IV	
for rated mains voltage ≤ 450 V rms		I-IV	
for rated mains voltage ≤ 600 Vrms		I-IV	
for rated mains voltage ≤ 1000 Vrms		I-III	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	Vpeak
Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec, Partial Discharge < 5 pC	V_{PR}	2652	Vpeak
Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10$ sec, Partial Discharge < 5 pC	V_{PR}	2262	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage, $t_{ini} = 60$ sec)	V_{IOTM}	8000	Vpeak
Safety-limiting values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current[2]	$I_{S,INPUT}$	400	mA
Output Power[2]	$P_{S,OUTPUT}$	600	mW
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$\geq 10^9$	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.
2. Safety-limiting parameters are dependent on ambient temperature. Refer to the following figure for dependence of P_S and I_S on ambient temperature.

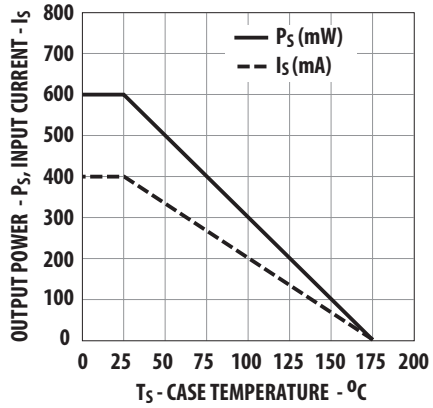


Figure 4. Case Temperature chart

Table 4. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (External Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	–55	+125	°C
Ambient Operating Temperature	T_A	–40	+105	°C
Supply voltage	V_{DD1}, V_{DD2}	–0.5	6.0	V
Steady-State Input Voltage[1,3]	V_{IN}+, V_{IN}–	–2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[2]	V_{IN}+, V_{IN}–	–6	V_{DD1} + 0.5	V
Digital Input/Output Voltages	MCLKIN, MDAT	–0.5	V_{DD2} + 0.5	V
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			

Notes:
1. DC voltage of up to –2 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
2. Transient voltage of 2 seconds up to –6 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
3. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	–40	+105	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3.3	5.5	V
Analog Input Voltage[1]	V_{IN}+, V_{IN}–	–200	+200	mV

Notes:
1. Full scale signal input range ±320 mV.

Table 7. Electrical Specifications

Unless otherwise noted, T_A = –40°C to +105°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3.3 V to 5.5 V, V_{IN}+ = –200 mV to +200 mV, and V_{IN}– = 0 V (single-ended connection); tested with Sinc^3 filter, 256 decimation ratio, f_{MCLKIN} = 20 MHz.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Test Conditions/Notes	Fig.
STATIC CHARACTERISTICS							
Resolution		16			Bits	Decimation filter output set to 16bits	
Integral Nonlinearity	INL	-15	3	15	LSB	T_A = –40°C to +85°C; see definitions section.	
		-25	3	25	LSB	T_A = 85°C to +105°C	
Differential Nonlinearity	DNL	-0.9		0.9	LSB	No missing codes, guaranteed by design; see Definitions section	
Input Offset Voltage	V_{OS}	-1.5	0.6	2.5	mV	T_A = –40°C to +105°C	9, 10
Input Offset Voltage vs. Temperature	TCV_{OS}		1	3.5	µV/°C	T_A = –40°C to +105°C **note: Direct short across inputs.	9
Input Offset Drift vs V_{DD1}			110		µV/V		
Gain Error	G_E	-2		2	%	T_A = –40°C to +105°C, V_{IN+} = –200 to +200 mV; see Definitions section	11
		-1		1	%	T_A = 25°C, V_{IN+} = –200 to +200mV	11
Gain Error Drift vs. Temperature	T_{CGE}		60		ppm/°C	T_A = –40°C to +105°C;	11
Gain Drift vs. V_{DD1}			0.15%		%/V	T_A = –40°C to +105°C;	12
ANALOG INPUTS							
Full-Scale Differential Voltage Input Range	FSR		±320		mV	Referenced to GND1	
Linear Input Range	V_{IN+}, V_{IN-}		±200		mV	Referenced to GND1	
Average Input Bias Current	I_{INA}		-0.5		µA	V_{DD1} = 5V, V_{DD2} = 5V, V_{IN+} = 0 V; Note 3	
Average Input Resistance	R_{IN}		12.5		kΩ	Across V_{IN+} or V_{IN-} to GND1; Note 3; F_{CLKIN}=20MHz.	
Input Capacitance	C_{INA}		16		pF	Across V_{IN+} or V_{IN-} to GND1	
AC CHARACTERISTICS							
Signal-to-Noise Ratio	SNR	68	82		dB	T_A = –40°C to +105°C; see Definitions section. Note 4.	
Signal-to- (Noise + Distortion) Ratio	SNDR	65	75		dB	T_A = –40°C to +105°C; see Definitions section. Note 4.	13,14,15
Effective Number of Bits	ENOB		12		Bits	See definitions section	
Isolation Transient Immunity	CMR (CMTI)		25		kV/µs	V_{CM} = 1 kV, T_A = 25°C	
DIGITAL INPUTS AND OUTPUTS							
Output differential Voltage (Mdat+, Mdat-)	V_{od}		350		mV	Rload = 100ohm; Mdat+ - Mdat-, V_{DD1}, V_{DD2} =5V. Note 5.	
Output Common Mode Voltage	V_{ocm}	1	1.25	1.5	V	Vdd1, Vdd2 = 5V.	
Output Short Circuit Current (Mdat+, Mdat-)	IOSD		3.5		mA	Output shorted to gnd.	
Input Threshold high (MCLKin+, MCLKin-)	V_{thH}			100	mV	Referenced to Vocm.	
Input Threshold Low (MCLKin+, MCLKin-)	V_{thL}	-100			mV	Referenced to Vocm.	
POWER SUPPLY							
Input Side Supply Current	I_{DD1}		15.5	20	mA	V_{DD1} = 5.5 V	16, 17,18
	I_{DD2}		14.5	18	mA	V_{DD2} = 3.3 V	
			17	20	mA	V_{DD2} = 5 V	19, 20, 21

Notes:
1. All Typical values are under Typical Operating Conditions at TA = 25°C, VDD1 = 5 V, VDD2 = 5 V.
2. Beyond the full-scale input range the data output is either all zeroes or all ones.
3. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.
4. Input signal frequency = 1Khz.
5. Output differential voltage Vod = Mdat+ - Mdat-.

Table 8. Timing Specifications

Unless otherwise noted, T_A = –40°C to +105°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3.3 V to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions/Notes	Fig.
Modulator Clock Input Frequency	f_{MCLKIN}	5	20	25	MHz	Clock Duty Cycle 40% to 60%. Note 1.	
Data Delay upon MCLKIN Input Startup	T_{CS}		150		uS	V_{IN} = 0V, V_{DD1} and V_{DD2} = 5V, T_A = 25°C.	Refer to figure 5.
Data Propagation Delay after MCLKIN edge [1]	T_D		15		nS	V_{IN} = 0V, V_{DD1} and V_{DD2} = 5V.	Refer to figure 6.
Data Delay Upon V_{DD1} power up	T_{PS1}		250		uS	V_{IN} = 0V, V_{DD1} > 3.8V V_{DD2} supplied, MCLKIN active, T_A = 25°C, Note 2.	Refer to figure 7.
Data Delay Upon V_{DD2} power up	T_{PS2}		165		uS	V_{IN} = 0V, V_{DD1} supplied, T_A = 25°C , MCLKIN active	Refer to figure 8.

Notes:
1. The ACPL-798J has an in-built clock conditioning scheme that makes it tolerant to variations on the input clock duty cycle.
2. When V_{DD1} is not supplied, MDAT+ is high and MDAT- is low ie modulator output level is "1".

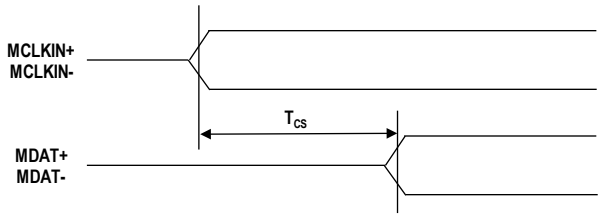


Figure 5. Data delay upon clock input startup

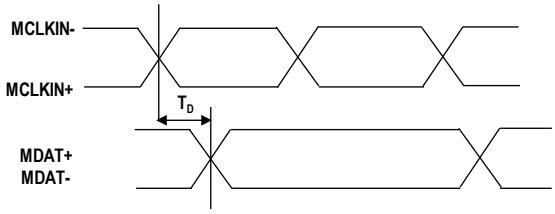


Figure 6. Data propagation delay

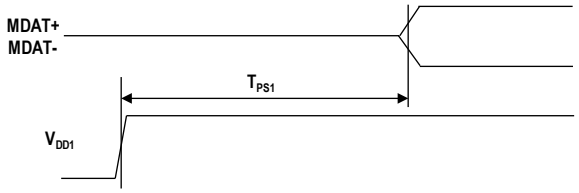


Figure 7. Data delay upon VDD1 startup

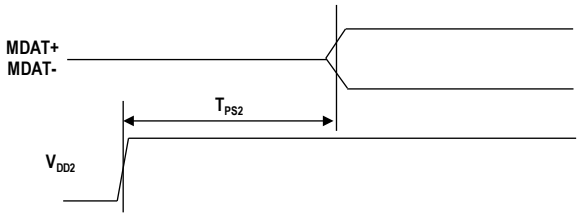


Figure 8. Data delay upon VDD2 startup

Table 9. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH ≤ 50%, t = 1 min; T_A = 25°C	1, 2
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	V_{I-O} = 500 Vdc	2
		10^{11}			Ω	T_A = 100°C	2
Input-Output Capacitance	C_{I-O}		1.4		pF	f = 1 MHz	2
Input IC Junction-to-Ambient Thermal Resistance	θ_{JAI}		83		°C/W	1 oz. trace, 2-layer PCB, still air, T_A = 25°C	3
Output IC Junction-to- Ambient Thermal Resistance	θ_{JAO}		85		°C/W	1 oz. trace, 2-layer PCB, still air, T_A = 25°C	3

Notes:
1. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
2. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
3. Maximum power dissipation in analog side and digital side IC's needs to be limited to ensure that their respective junction temperature is less than 125°C. The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature.

Typical Performance Plots

Unless otherwise noted, T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 5 V, V_{IN}+ = –200 mV to +200 mV, and V_{IN}– = 0 V, f_{MCLKIN} = 20 MHz, with Sinc^3 filter, 256 decimation ratio.

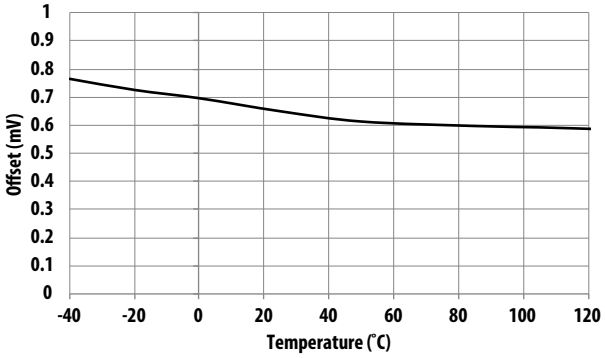


Figure 9. Offset vs. Temperature

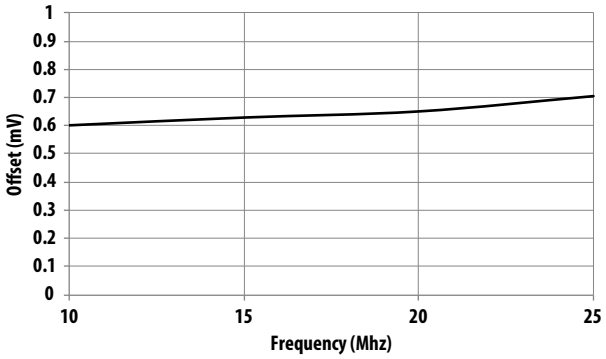


Figure 10. Offset vs. MCLKIN Clock

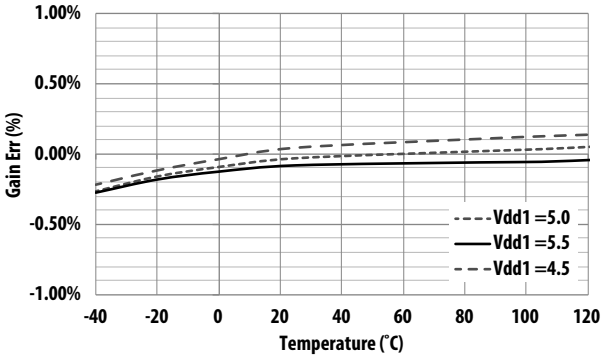


Figure 11. Gain vs. Temperature

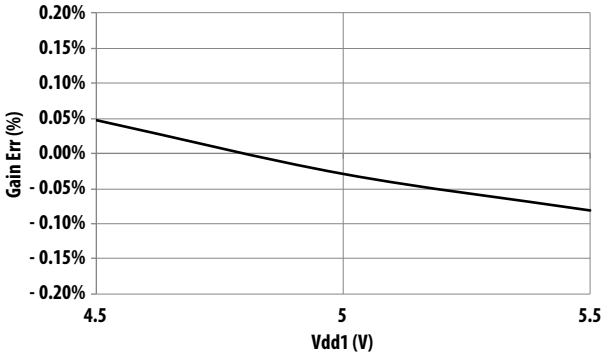


Figure 12. Gain vs. V_{DD1}

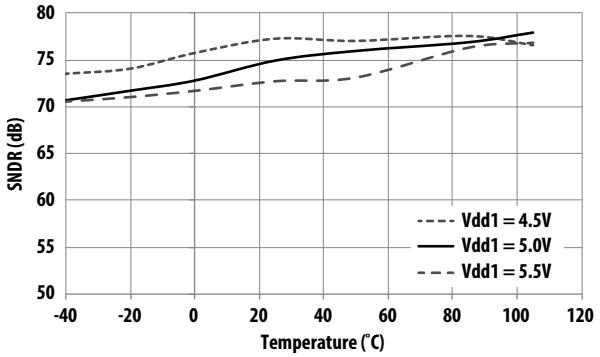


Figure 13. SNDR vs. Temperature

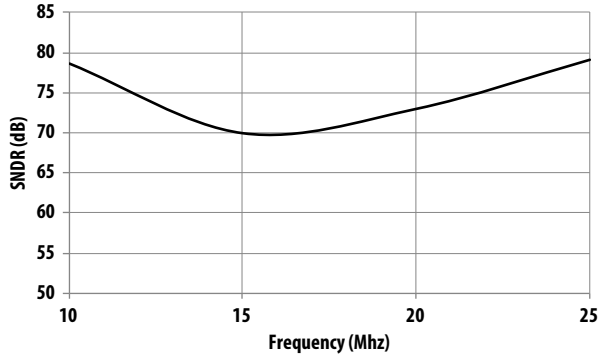


Figure 14. SNDR vs. MCLKIN Frequency

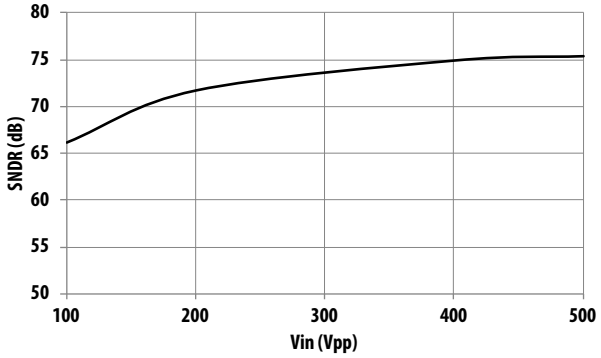


Figure 15. SNDR vs. Input Voltage V_{IN}

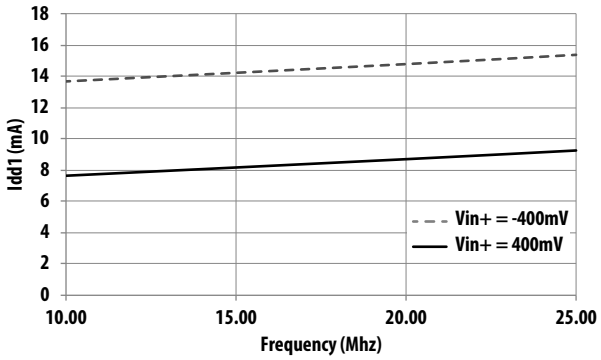


Figure 16. I_{DD1} vs. MCLKIN Frequency

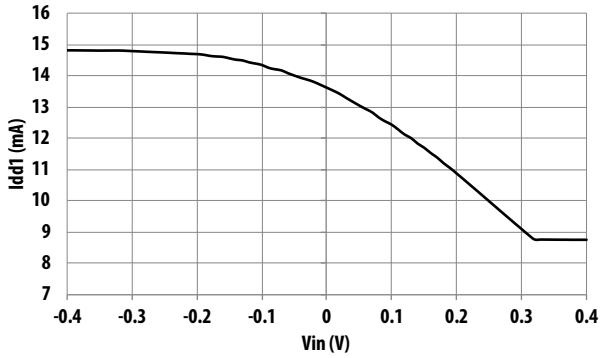


Figure 17. I_{DD1} vs. Input Voltage V_{IN}

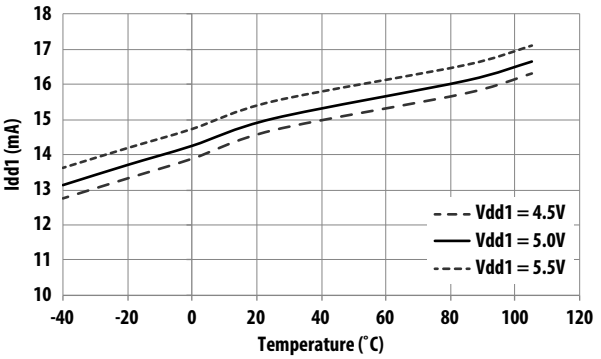


Figure 18. I_{DD1} vs. Temperature

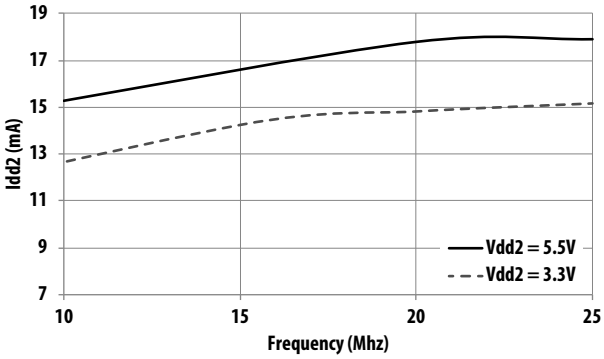


Figure 19. I_{DD2} vs. MCLKIN Frequency

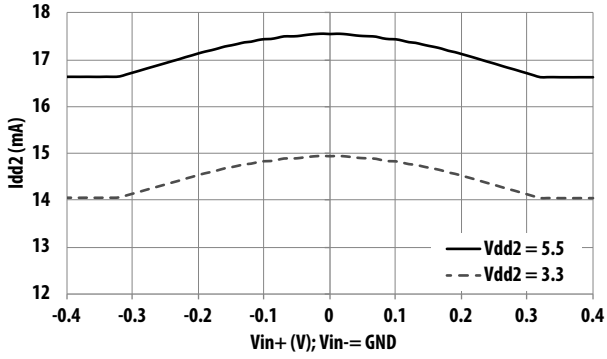


Figure 20. I_{DD2} vs Input Voltage V_{IN}

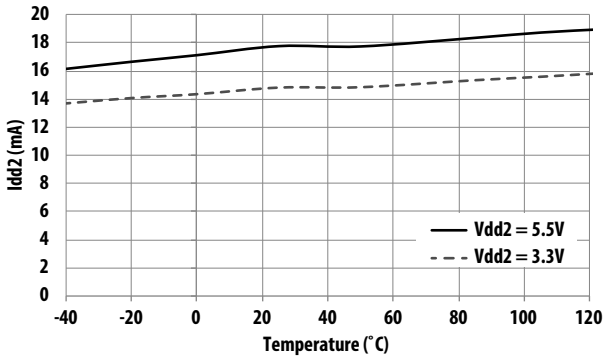


Figure 21. I_{DD2} vs. Temperature

Definitions

Integral Nonlinearity (INL)

INL is the maximum deviation of a transfer curve from a straight line passing through the endpoints of the ADC transfer function, with offset and gain errors adjusted out.

Differential Nonlinearity (DNL)

DNL is the deviation of an actual code width from the ideal value of 1 LSB between any two adjacent codes in the ADC transfer curve. DNL is a critical specification in closed-loop applications. A DNL error of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

Offset error is the deviation of the actual input voltage corresponding to the mid-scale code (32,768 for a 16-bit system with an unsigned decimation filter) from 0 V. Offset error can be corrected by software or hardware.

Gain Error

Gain error is the the difference between the ideal gain slope and the actual gain slope, with offset error adjusted out. Gain error includes reference error. Gain error can be corrected by software or hardware.

Signal-to-Noise Ratio (SNR)

The SNR is the measured ratio of AC signal power to noise power below half of the sampling frequency. The noise power excludes harmonic signals and DC.

Signal-to-(Noise + Distortion) Ratio (SNDR)

The SNDR is the measured ratio of AC signal power to noise plus distortion power at the output of the ADC. The signal power is the rms amplitude of the fundamental input signal. Noise plus distortion power is the rms sum of all non-fundamental signals up to half the sampling frequency (excluding DC).

Effective Number of Bits (ENOB)

The ENOB determines the effective resolution of an ADC, expressed in bits, defined by ENOB = (SNDR – 1.76)/6.02

Isolation Transient Immunity (CMR)

The isolation transient immunity (also known as Common-Mode Rejection or CMR) specifies the minimum rate-of-rise/fall of a common-mode signal applied across the isolation boundary beyond which the modulator clock or data is corrupted.

Product Overview

Description

The ACPL-798J isolated sigma-delta (∑–Δ) modulator converts an analog input signal into a high-speed (up to 25MHz) single-bit data stream by means of a sigma-delta over-sampling modulator. The time average of the modulator data is directly proportional to the input signal voltage. The modulator uses external clock ranges from 5 MHz to 25 MHz that is coupled across the isolation barrier. This arrangement allows synchronous operation of data acquisition to any digital controller, and adjustable clock for speed requirements of the application. The modulator data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information is represented by the density of ones in the data output.

The other main function of the modulator (optocoupler) is to provide galvanic isolation between the analog signal input and the digital data output. It provides high noise margins and excellent immunity against isolation-mode transients that allows direct measurement of low-level signals in highly noisy environments, for example measurement of motor phase currents in power inverters.

With 0.5 mm minimum DTI, the ACPL-798J provides reliable double protection and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in an SO-16 package, the isolated ADC delivers the reliability, compact size, superior isolation and over-temperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

Analog Input

The differential analog inputs of the ACPL-798J are implemented with a fully-differential, switched-capacitor circuit. The ACPL-798J accepts signal of ±200 mV (full scale ±320 mV), which is ideal for direct connection to shunt based current sensing or other low-level signal sources applications such as motor phase current measurement. An internal voltage reference determines the full-scale analog input range of the modulator (±320 mV); an input range of ±200 mV is recommended to achieve optimal performance. Users are able to use higher input range, for example ±250 mV, as long as within full-scale range, for purpose of over-current or overload detection. Figure 22 shows the simplified equivalent circuit of the analog input.

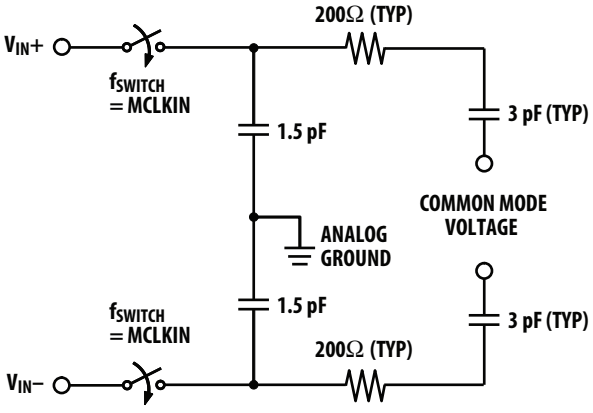


Figure 22. Analog input equivalent circuit.

In the typical application circuit (Figure 25.), the ACPL-798J is connected in a single-ended input mode. Given the fully differential input structure, a differential input connection method (balanced input mode as shown in Figure 23) is recommended to achieve better performance. The input currents created by the switching actions on both of the pins are balanced on the filter resistors and cancelled out each other. Any noise induced on one pin will be coupled to the other pin by the capacitor C and creates only common mode noise which is rejected by the device. The resistors and the capacitor also forms an anti-aliasing filter for the sigma-delta modulator. Typical value for RA and RB is 22 Ω and 10 nF for C.

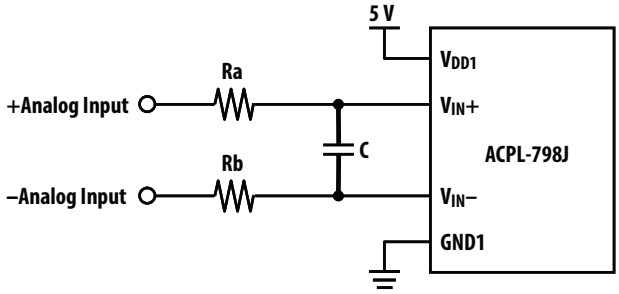


Figure 23. Simplified differential input connection diagram.

Latch-up Consideration

Latch-up risk of CMOS devices needs careful consideration, especially in applications with direct connection to signal source that is subject to frequent transient noise. The well designed analog input structure of the ACPL-798J is resilient to transients, which are often encountered in highly noisy application environments such as motor drive and other power inverter systems. Other situations could cause transient voltages to the inputs include short circuit and overload conditions. The ACPL-798J is tested to be able to reject DC voltage of –2 V and 2-second transient voltage of –6 V presented to the analog inputs without any latch-up or damage to the device.

Modulator Data Output

Input signal information is contained in the modulator output data stream, represented by the density of ones and zeros. The density of ones is proportional to the input signal voltage, as shown in Figure 24. A differential input signal of 0 V ideally produces a data stream of ones 50% of the time and zeros 50% of the time. A differential input of –200 mV corresponds to 18.75% density of ones, and a differential input of +200 mV is represented by 81.25% density of ones in the data stream. A differential input of +320 mV or higher results in ideally all ones in the data stream, while input of –320 mV or lower will result in all zeros ideally. Table 10 shows this relationship.

Digital Filter

The original analog signal that is converted to a digital bit stream by the over-sampling sigma-delta modulator, can be recovered by means of filtering in the digital domain. A common and simple way is through implementation of a cascaded integrated comb (CIC) filter or Sinc3 filter. The digital filter averages or decimates the over-sampled bit stream and effectively converts it into a multi-bit digital equivalent code of the original analog input signal. With a 20MHz external clock frequency, 256 decimation ratio and 16-bit word settings, the output data rate is 58 kHz (= 20MHz/256). This filter can be implemented in an ASIC, an FPGA or a DSP. Some of the equivalent digital codes with corresponding input voltages are shown in Table 10.

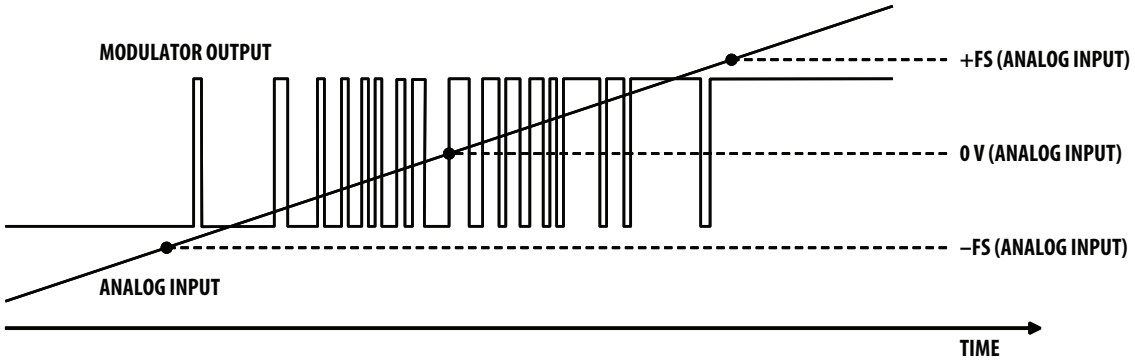
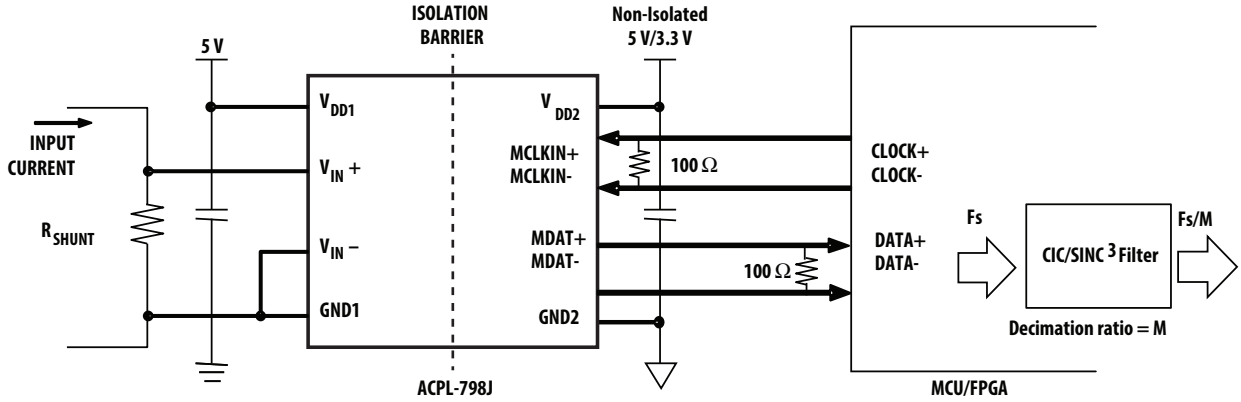


Figure 24. Moudlator output vs. analog input.

Table 10. Input voltage with ideal corresponding density of 1s at modulator data output, and ADC code.

Analog Input	Voltage Input	Density of 1s	ADC Code (16-bit unsigned decimation)
Full-Scale Range	640 mV		
+Full-Scale	+320 mV	100%	65,535
+Recommended Input Range	+200 mV	81.25%	53,248
Zero	0 mV	50%	32,768
–Recommended Input Range	–200 mV	18.75%	12,288
–Full-Scale	–320 mV	0%	0

Notes:
1. With bipolar offset binary coding scheme, the digital code begins with digital 0 at –FS input and increases proportionally to the analog input until the full-scale code is reached at the +FS input. The zero crossing occurs at the mid-scale input.
2. Ideal density of 1s at modulator data output can be calculated with V_{IN}/640 mV + 50%; similarly, the ADC code can be calculated with (V_{IN}/640 mV) × 65,536 + 32,768, assuming a 16-bit unsigned decimation filter.



Note: In applications, a 0.1 μF bypass capacitor must be connected between pins V_{DD1} and GND1, and between pins V_{DD2} and GND2 of the ACPL-798J.

Figure 25. Typical application circuit with a Sinc^3 filter.

Application Information

Digital Current Sensing Circuit

Figure 26 shows a typical application circuit for motor control phase current sensing. By choosing the appropriate shunt resistance, any range of current can be monitored, from less than 1 A to more than 100 A.

Power Supplies and Bypassing

As shown in Figure 26, a floating power supply (which in many applications could be the same supply that is used to drive the high-side power transistor) is regulated to 5 V using a low cost and common regulator like the LM78L05.

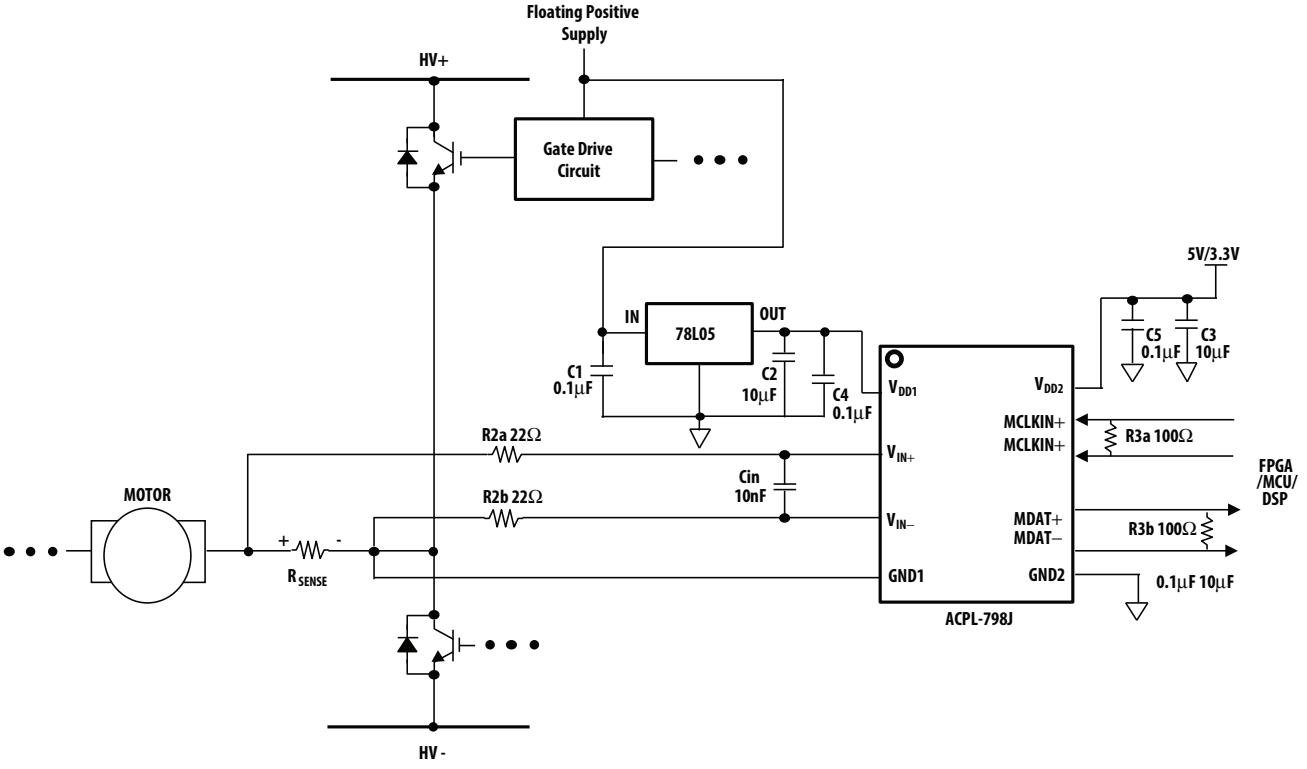


Figure 26. Typical application circuit for motor phase current sensing.

Alternatively a simple zener diode could also be used to in place of the regulator to provide the required power supply. The voltage from the current sensing resistor or shunt (RSENSE) is applied to the input of the ACPL- 798J through an RC anti-aliasing filter (R2 and Cin). Although the application circuit is relatively simple, a few recommendations should be followed to ensure optimal performance. The power supply for the isolated modulator is most often obtained from the same supply used to power the power transistor gate drive circuit. If a dedicated supply is required, in many cases it is possible to add an additional winding on an existing transformer. Otherwise, some sort of simple isolated supply can be used, such as a line powered transformer or a high-frequency DC-DC converter. To help attenuate high-frequency power supply noise or ripple, a resistor or inductor can be used in series with the input of the regulator to form a low-pass filter with the regulator's input bypass capacitor. A ferrite bead is also recommended to be placed close to Vdd1 pin to filter out any high-frequency noise in the supply. As shown in Figure 26, bypass capacitors (C2 to C5) should be located as close as possible to the input and output power-supply pins of the isolated modulator (U2). The bypass capacitors are required because of the high-speed digital nature of the signals inside the isolated modulator. Tantalum capacitors are also recommended over electrolytic capacitors due to their lower ESR which translates to faster response to support the switching currents required by the isolated modulator. A 10nF bypass capacitor (Cin) is also recommended at the input due to the switched-capacitor nature of the input circuit. The input bypass capacitor together with the resistors R2a and R2b also forms part of the anti-aliasing filter, which is recommended to prevent high frequency noise from aliasing down to lower frequencies and interfering with the input signal.

LVDS Interface

One of the features on the ACPL-798J is that it uses a Low Voltage Differential Signalling (LVDS) interface on both the clock input and the modulator output. In a typical motor drive application where the ACPL-798J is used, the surrounding environment is usually noisy. Very often, the current sensor or modulator can be partitioned on another separate board and interfaced through connecters or cables to the controller board. The benefits of using LVDS in this case helps to make the interface between the modulator and the controller more robust and less susceptible to electromagnetic interference from the surroundings. LVDS also helps to reduce the EMI emissions associated with high speed digital signaling. Being high speed in general, LVDS signals are treated as transmission lines and must be resistively terminated properly (as shown in figure 26) to reduce or eliminate transmission line reflection. The same resistors (R3a and R3b) also perform the function of terminating the LVDS lines which are current mode outputs, and should be place as close as possible to the end receiver. The value of the differential terminating resistor is typically 100Ω which should match the differential impedence of the transmission line. The LVDS interface is in accordance to the TIA/EIA-644-A standard.

PC Board Layout

The design of the printed circuit board (PCB) should follow good layout practices, such as keeping bypass capacitors close to the supply pins, keeping output signals away from input signals, the use of ground and power planes, etc. The input anti-aliasing filter network should be placed as close as possible to the input pin to minimize any stray inductance. The termination resistor for the LVDS interfaces should be placed as close as possible at the receiver pins, and the differential traces should be of the same length and be running along side each other. In addition, the layout of the PCB can also affect the isolation transient immunity (CMR) of the isolated modulator, due primarily to stray capacitive coupling between the input and the output circuits. To obtain optimal CMR performance, the layout of the PC board should minimize any stray coupling by maintaining the maximum possible distance between the input and output sides of the circuit and ensuring that any ground or power plane on the PC board does not pass directly below or extend much wider than the body of the isolated modulator.

Shunt Resistors

The current-sensing shunt resistor should have low resistance (to minimize power dissipation), low inductance (to minimize di/dt induced voltage spikes which could adversely affect operation), and reasonable tolerance (to maintain overall circuit accuracy). Choosing a particular value for the shunt is usually a compromise between minimizing power dissipation and maximizing accuracy. Smaller shunt resistances decrease power dissipation, while larger shunt resistances can improve circuit accuracy by utilizing the full input range of the isolated modulator. The first step in selecting a shunt is determining how much current the shunt will be sensing. The graph in Figure 27 shows the RMS current in each phase of a three-phase induction motor as a function of average

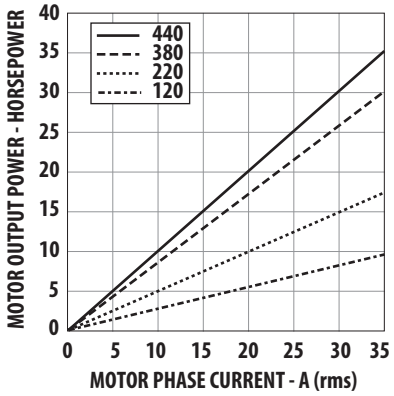


Figure 27. Motor Output Horsepower vs. Motor Phase Current and Supply.

motor output power (in horsepower, hp) and motor drive supply voltage. The maximum value of the shunt is determined by the current being measured and the maximum recommended input voltage of the isolated modulator. The maximum shunt resistance can be calculated by taking the maximum recommended input voltage and dividing by the peak current that the shunt should see during normal operation. For example, if a motor will have a maximum RMS current of 10 A and can experience up to 50% overloads during normal operation, then the peak current is 21.1 A (=10x1.414x1.5). Assuming a maximum input voltage of 200 mV, the maximum value of shunt resistance in this case would be about 10 mΩ. The maximum average power dissipation in the shunt can also be easily calculated by multiplying the shunt resistance times the square of the maximum RMS current, which is about 1 W in the previous example. If the power dissipation in the shunt is too high, the resistance of the shunt can be decreased below the maximum value to decrease power dissipation. The minimum value of the shunt is limited by precision and accuracy requirements of the design. As the shunt value is reduced, the output voltage across the shunt is also reduced, which means that the offset and noise, which are fixed, become a larger percentage of the signal amplitude. The selected value of the shunt will fall somewhere between the minimum and maximum values, depending on the particular requirements of a specific design. When sensing currents large enough to cause significant heating of the shunt, the temperature coefficient (tempco) of the shunt can introduce nonlinearity due to the signal dependent temperature rise of the shunt. The effect increases as the shunt-to-ambient thermal resistance increases. This effect can be minimized either by reducing the thermal resistance of the shunt or by using a shunt with a lower tempco. Lowering the thermal resistance can be accomplished by repositioning the shunt on the PC board, by using larger PC board traces to carry away more heat, or by using a heat sink. For a two-terminal shunt, as the value of shunt resistance decreases, the resistance of the leads becomes a significant percentage of the total shunt resistance. This has two primary effects on shunt accuracy. First, the effective resistance of the shunt can become dependent on factors such as how long the leads are, how they are bent, how far they are inserted into the board, and how far solder wicks up the lead during assembly (these issues will be discussed in more detail shortly). Second, the leads are typically made from a material such as copper, which has a much higher tempco than the material from which the resistive element itself is made, resulting in a higher tempco for the shunt overall. Both of these effects are eliminated when a four-terminal shunt is used. A four-terminal shunt has two additional terminals that are Kelvin-connected directly across the resistive element itself; these two terminals are used to monitor the voltage across the resistive element while the other two terminals are used to carry the load current. Because of the Kelvin connection, any voltage drops across the leads carrying the load current should have no impact on the measured voltage. Several four-terminal shunts from Isotek (Isabellenhütte) suitable for sensing currents in motor drives up to 71 Arms (71 hp or 53 kW) are shown in Table 11; the maximum current and motor power range for each of the PBVseries shunts are indicated. For shunt resistances from 50mΩ down to 10μm, the maximum current is limited by the input voltage range of the isolated modulator. For the 5 mΩ and 2 mΩ shunts, a heat sink may be required due to the increased power dissipation at higher currents. When laying out a PC board for the shunts, a couple of points should be kept in mind. The Kelvin connections to the shunt should be brought together under the body of the shunt and then run very close to each other to the input of the isolated modulator; this minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal. If the shunt is not located on the same PC board as the isolated modulator circuit, a tightly twisted pair of wires can accomplish the same thing. Also, multiple layers of the PC board can be used to increase current carrying capacity. Numerous plated-through vias should surround each non-Kelvin terminal of the shunt to help distribute the current between the layers of the PC board. The PC board should use 2 or 4 oz. copper for the layers, resulting in a current carrying capacity in excess of 20 A. Making the current carrying traces on the PC board fairly large can also improve the shunt's power dissipation capability by acting as a heat sink. Liberal use of vias where the load current enters and exits the PC board is also recommended.

Shunt Connections

The recommended method for connecting the isolated modulator to the shunt resistor is shown in Figure 26. V_{IN+} is connected to the positive terminal of the shunt resistor, while V_{IN-} is shorted to GND1, with the power-supply return path functioning as the sense line to the negative terminal of the current shunt. This allows a single pair of wires or PC board traces to connect the isolated modulator circuit to the shunt resistor. By referencing the input circuit to the negative side of the sense resistor, any load current induced noise transients on the shunt are seen as a common-mode signal and will not interfere with the current-sense signal. This is important because the large load currents flowing through the motor drive, along with the parasitic inductances inherent in the wiring of the circuit, can generate both noise spikes and offsets that are relatively large compared to the small voltages that are being measured across the current shunt. If the same power supply is used both for the gate drive circuit and for the current sensing circuit, it is very important that the connection from GND1 of the isolated modulator to the sense resistor be the only return path for supply current

to the gate drive power supply in order to eliminate potential ground loop problems. The only direct connection between the isolated modulator circuit and the gate drive circuit should be the positive power supply line.

In some applications, however, supply currents flowing through the power-supply return path may cause offset or noise problems. In this case, better performance may be obtained by connecting V_{IN+} and V_{IN-} directly across the shunt resistor with two conductors, and connecting GND1 to the shunt resistor with a third conductor for the power-supply return path, as shown in Figure 27. When connected this way, both input pins should be bypassed. To minimize electromagnetic interference of the sense signal, all of the conductors (whether two or three are used) connecting the isolated modulator to the sense resistor should be either twisted pair wire or closely spaced traces on a PC board. The 22Ω resistor in series with the input lead (R2) forms a lowpass anti-aliasing filter with the 20nF input bypass capacitor (Cin) with a 723KHz bandwidth. The resistor performs another important function as well; it dampens any ringing which might be present in the circuit formed by the shunt, the input bypass capacitor, and the inductance of wires or traces connecting the two. Undamped ringing of the input circuit near the input sampling frequency can alias into the baseband producing what might appear to be noise at the output of the device.

Table 11. Four-terminal shunts

Shunt Resistor Part Number	Shunt Resistance mΩ	Tol. %	Maximum RMS Current A	Motor Power Range 120 V_{AC} - 440 V_{AC} hp	kW
PBV-R050-0.5	50	0.5	3	0.8 - 3	0.6 - 2
PBV-R020-0.5	20	0.5	7	2 - 7	0.6 - 2
PBV-R010-0.5	10	0.5	14	4 - 14	3 - 10
PBV-R005-0.5	5	0.5	25 [28]	7 - 25 [8 - 28]	5 - 19 [6 - 21]
PBV-R002-0.5	2	0.5	39 [71]	11 - 39 [19 - 71]	8 - 29 [14 - 53]

Note: Values in brackets are with a heatsink for the shunt.

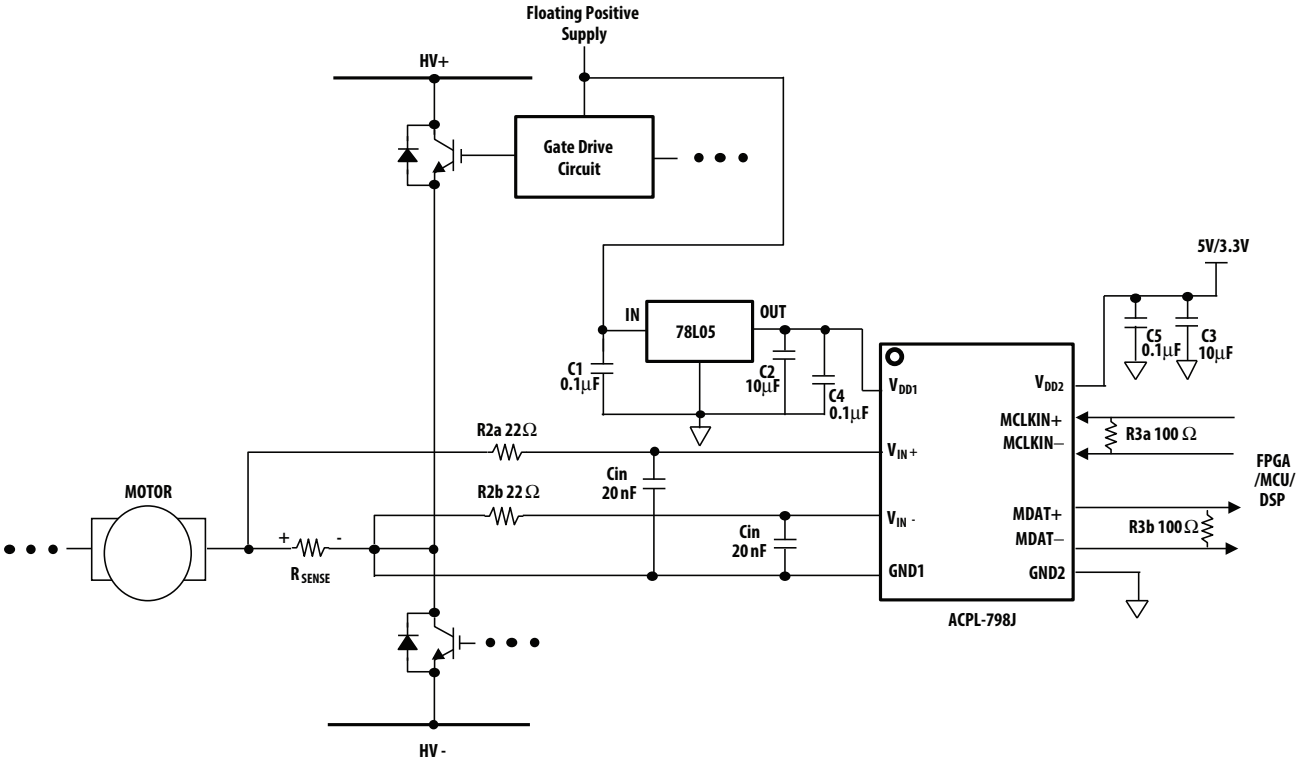


Figure 28. Schematic for three conductor shunt connection.

Voltage Sensing

The ACPL-798J can also be used to isolate signals with amplitudes larger than its recommended input range with the use of a resistive voltage divider at its input. The only restrictions are that the impedance of the divider be relatively small (less than 1 kΩ) so that the input resistance (12.8KΩ) and input bias current (0.5μA) do not affect the accuracy of the measurement. An input bypass capacitor is still required, although the 22Ω series damping resistor is not (the resistance of the voltage divider provides the same function). The low-pass filter formed by the divider resistance and the input bypass capacitor may limit the achievable bandwidth. To obtain higher bandwidth, the input bypass capacitor (C2) can be reduced, but it should not be reduced much below 1000 pF to maintain adequate input bypassing of the isolated modulator.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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