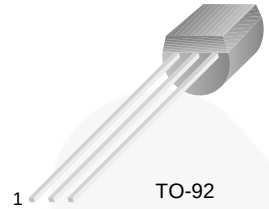
October 2014

BC327
PNP Epitaxial Silicon Transistor

Features

- Switching and Amplifier Applications
- Suitable for AF-Driver Stages and Low-Power Output Stages
- Complement to BC337 / BC338



TO-92

1. Collector 2. Base 3. Emitter

Ordering Information

Part Number	Top Mark	Package	Packing Method
BC327BU	BC327	TO-92 3L	Bulk
BC32716BU	BC32716	TO-92 3L	Bulk
BC32716TA	BC32716	TO-92 3L	Ammo
BC32725BU	BC32725	TO-92 3L	Bulk
BC32725TA	BC32725	TO-92 3L	Ammo
BC32740BU	BC32740	TO-92 3L	Bulk
BC32740TA	BC32740	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage	-50	V
V_{CEO}	Collector-Emitter Voltage	-45	V
V_{EBO}	Emitter-Base Voltage	-5	V
I_C	Collector Current (DC)	-800	mA
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 to 150	°C

Thermal Characteristics[1]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	625	mW
	Derate Above 25°C	5.0	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	°C/W

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = -10 mA, I_B = 0	-45			V
BV_{CES}	Collector-Emitter Breakdown Voltage	I_C = -0.1 mA, V_{BE} = 0	-50			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = -10 µA, I_C = 0	-5			V
I_{CES}	Collector Cut-Off Current	V_{CE} = -45 V, I_B = 0		-2	-100	nA
h_{FE1}	DC Current Gain	V_{CE} = -1 V, I_C = -100 mA	100		630	
h_{FE2}		V_{CE} = -1 V, I_C = -300 mA	60			
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = -500 mA, I_B = -50 mA			-0.7	V
V_{BE}(on)	Base-Emitter On Voltage	V_{CE} = -1 V, I_C = -300 mA			-1.2	V
f_T	Current Gain Bandwidth Product	V_{CE} = -5 V, I_C = -10 mA, f = 20 MHz		100		MHz
C_{ob}	Output Capacitance	V_{CB} = -10 V, I_E = 0, f = 1 MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60 ~	100 ~	170 ~

Typical Performance Characteristics

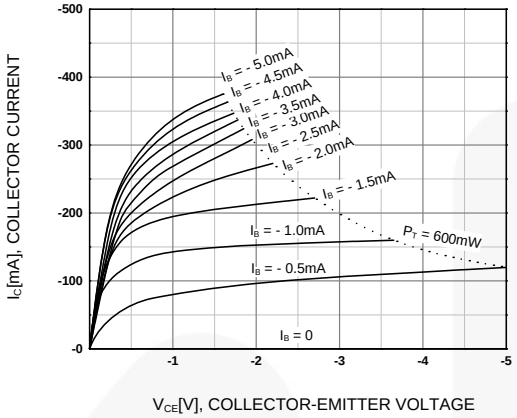


Figure 1. Static Characteristic

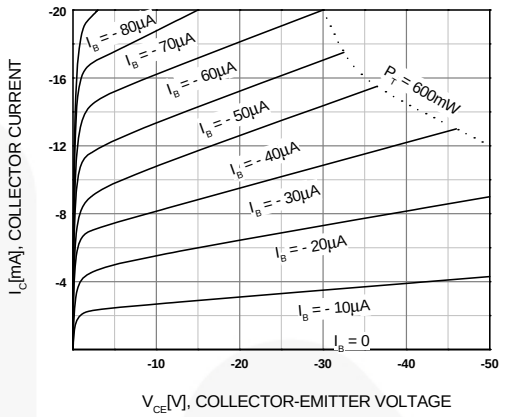


Figure 2. Static Characteristic

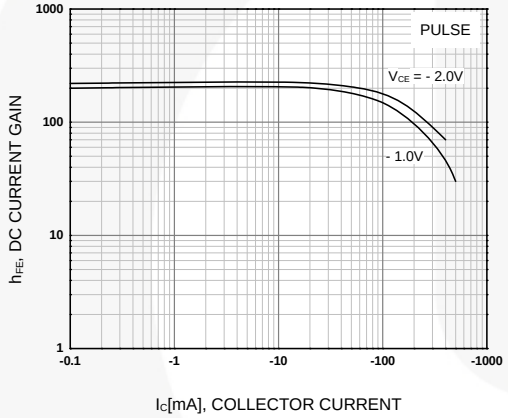


Figure 3. DC current Gain

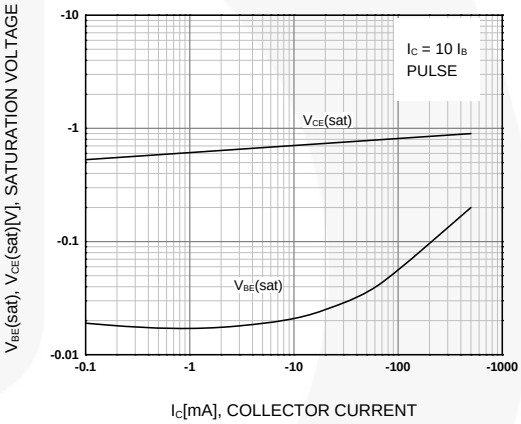


Figure 4. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

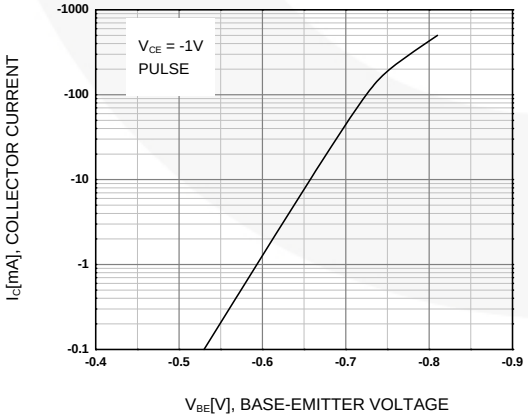


Figure 5. Base-Emitter On Voltage

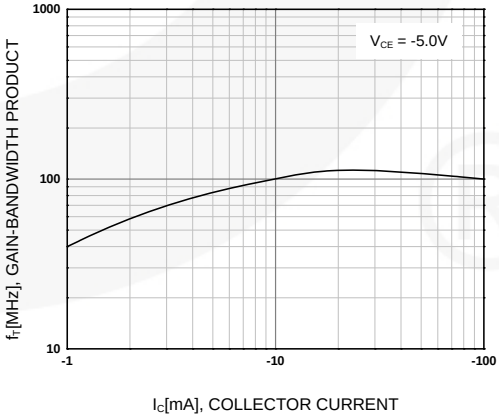
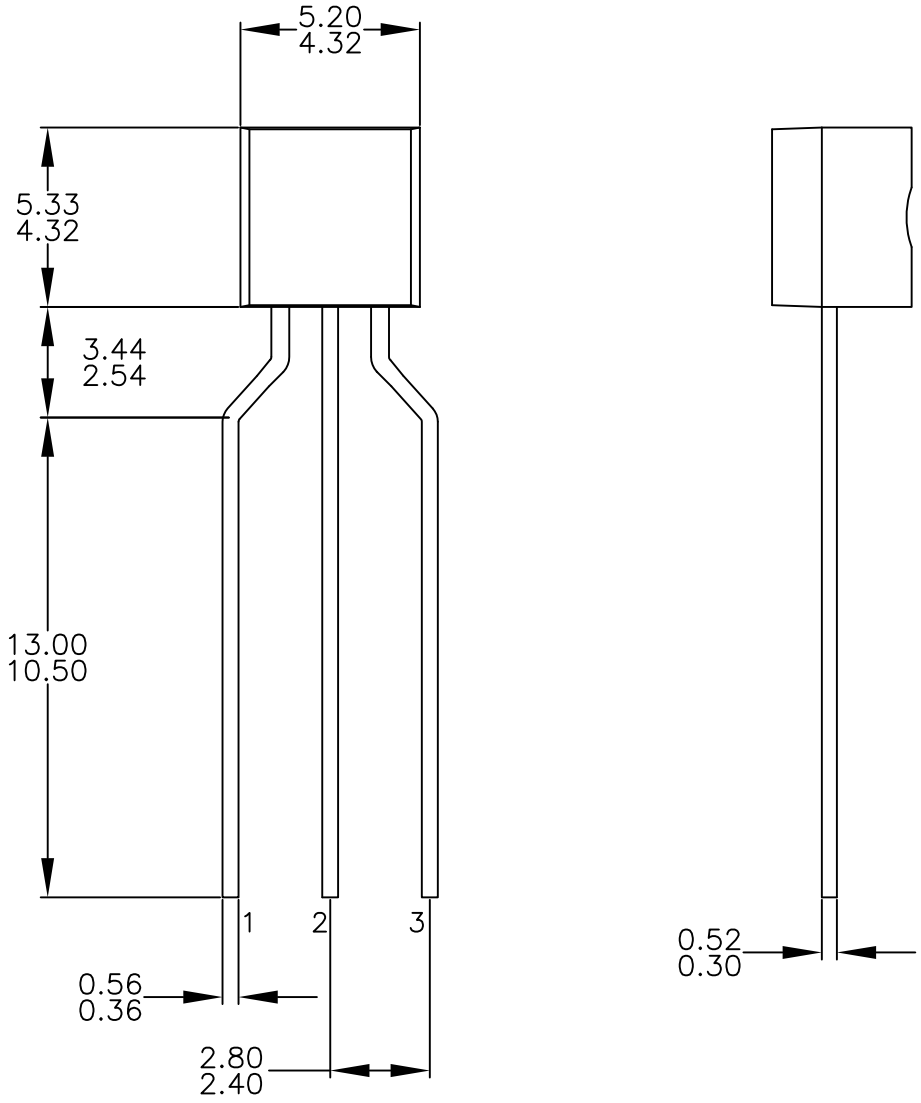
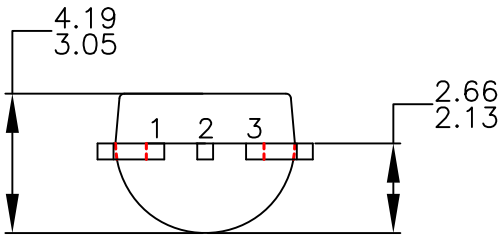


Figure 6. Gain Bandwidth Product





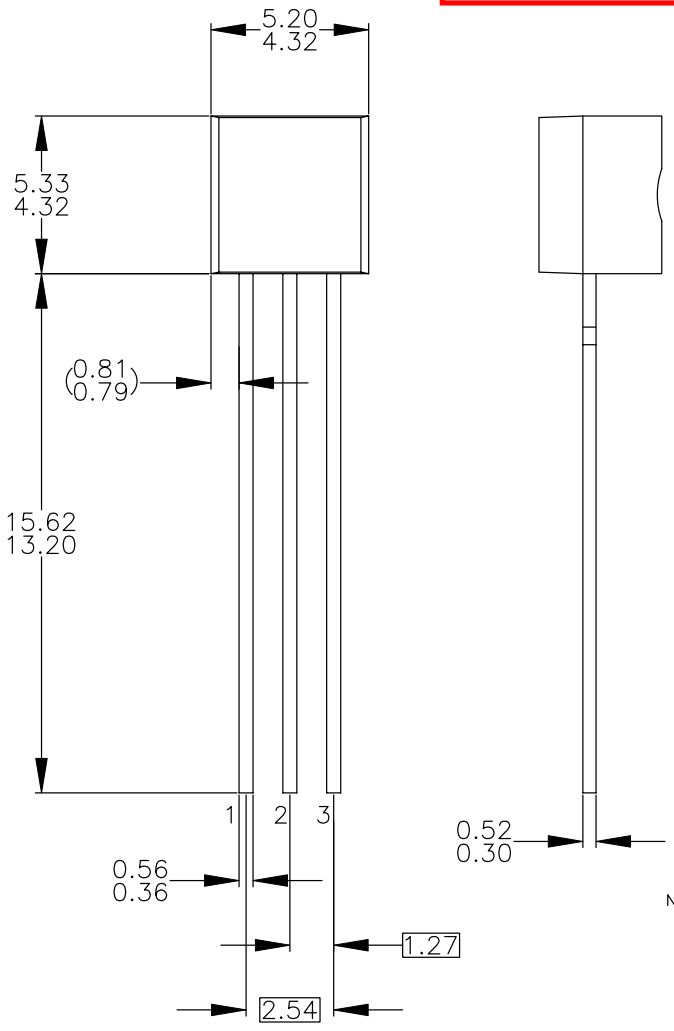
NOTES: UNLESS OTHERWISE SPECIFIED

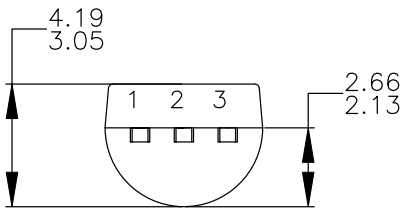
A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14–1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32– 4.70 TO 4.32–4.83; CHG PKG HEIGHT DIM FR 4.32–4.70 TO 4.32–4.78; CHG LD THICK DIM FR 0.30– 0.48 TO 0.30–0.52; DAMBAR–PKG DIM FR 1.27–1.65 TO 0.90–1.65; LD LGH DIM FR 14.47–15.64 TO 14.47–15.62; PKG DIM: 1.02–1.52 TO 0.92–1.52, 3.81–4.45 TO 3.40–4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C; MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	40CT1999	RCM/MRG
3	CHG LD LEN FR $^{15.61}_{14.07}$ TO $^{15.62}_{13.20}$; CHG MOLD BODY HT FR $^{4.78}_{4.32}$ TO $^{5.33}_{4.32}$; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO $^{(0.81)}_{(0.79)}$; CHG MOLD BODY WIDTH FR $^{4.83}_{4.32}$ TO $^{5.20}_{4.32}$; ADD PKG THICKNESS DIM 'E'; CHG 's' DIM FR $^{2.41}_{2.15}$ TO $^{2.66}_{2.13}$; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M–1994; REMOVE NOTE ON L34Z OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP

APPROVED
July-14-2008





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO–92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M–1994.
D) TO–92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT–ZA03DREV3.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	03APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO–92,MOLDED
STD STRAIGHT LD
(NO EOL CODE)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT–ZA03D	3

FORMERLY: N/A
SHEET : 1 OF 1

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I73