

# Kinetis K11D Sub-Family Data Sheet

## 50 MHz ARM® Cortex®-M4-based Microcontroller

The K11 product family members are optimized for cost-sensitive applications requiring low-power, processing efficiency and the need for extensive tamper protection, such as Electronic Point of Sales. This device shares the comprehensive enablement and scalability of the Kinetis family.

This product offers:

- Up to 512 KB of flash memory with up to 64 KB of SRAM
- DryIce Tamper Detection with active/passive pin, temperature, clock, supply voltage monitoring
- Run power consumption down to 189  $\mu$ A/MHz and Static power consumption down to 3.1  $\mu$ A with full state retention and 6  $\mu$ s wakeup. Lowest Static mode down to 359 nA

**MK11DX128AVMC5**  
**MK11DX256AVMC5**  
**MK11DN512AVMC5**



121 BGA  
8 x 8 x 1.4 mm Pitch 0.65 mm

### Performance

- Up to 50 MHz ARM® Cortex®-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

### Memories and memory interfaces

- Up to 512 KB of program flash
- Up to 64 KB RAM
- 64 KB FlexNVM and 4 KB FlexRAM on FlexMemory devices

### System peripherals

- Multiple low-power modes
- 16-channel DMA controller
- External watchdog monitor
- Software watchdog

### Clocks

- 32 kHz and 3-32 MHz crystal oscillator
- Multipurpose clock generator

### Security and integrity modules

- Hardware CRC module
- Tamper detect and secure storage
- Hardware random-number generator
- Hardware encryption supporting DES, 3DES, AES, MD5, SHA-1, and SHA-256 algorithms
- 128-bit unique identification (ID) number per chip

### Communication interfaces

- Two SPI modules
- Two I2C modules
- Four UART modules
- I2S module

### Timers

- 8-channel motor control/general purpose/PWM timers
- Two 2-channel general purpose timers
- 32-bit PITs and 16-bit low-power timer
- Carrier modulator transmitter
- Real-time clock
- Programmable delay block

### Analog modules

- 16-bit SAR ADC
- Two analog comparators (CMP)
- 12-bit DAC
- Voltage reference

### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C

### Ordering Information <sup>1</sup>

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MK11DX128AVMC5	128 KB	32	64
MK11DX256AVMC5	256 KB	32	64
MK11DN512AVMC5	512 KB	64	64

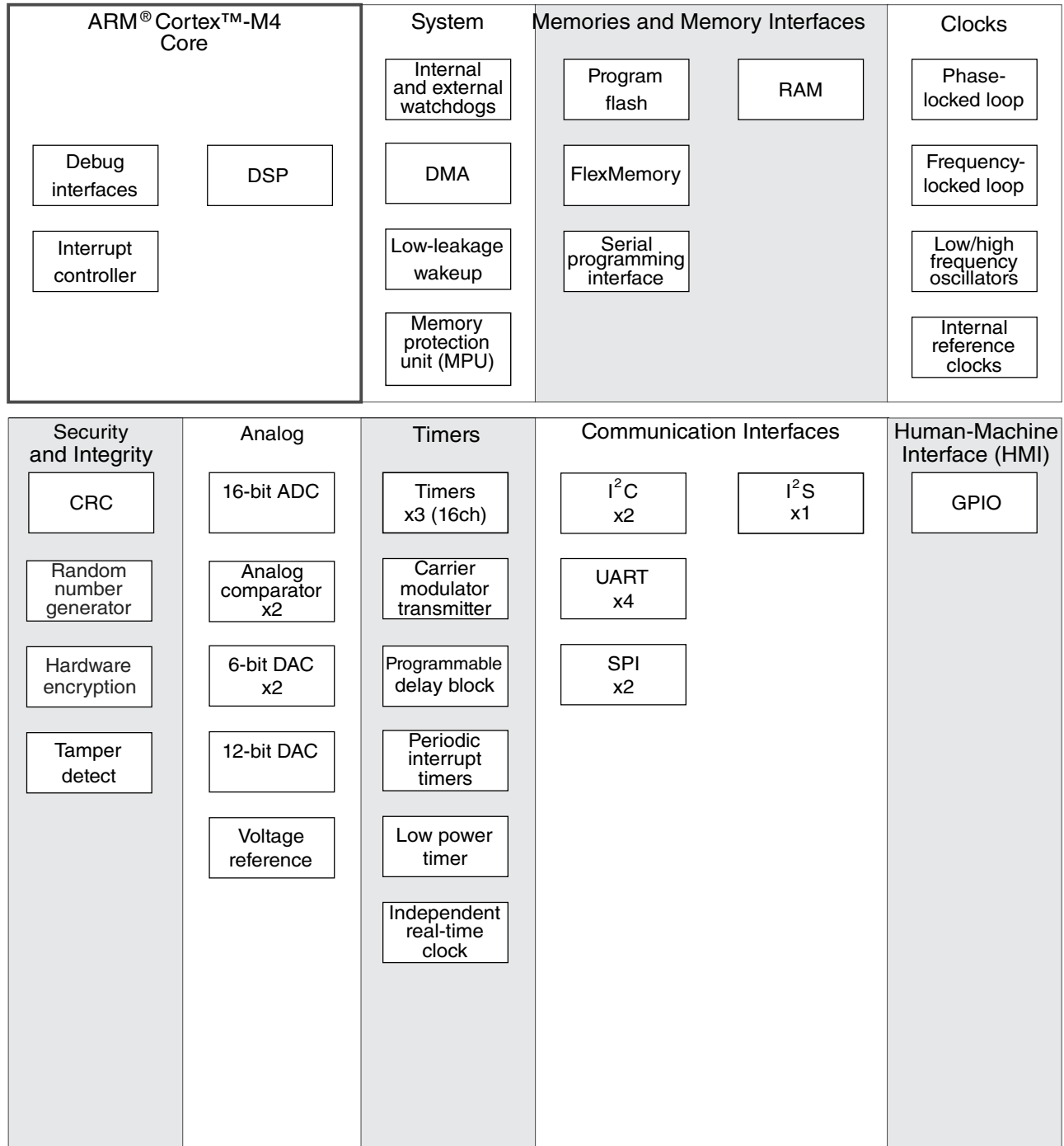
1. To confirm current availability of orderable part numbers, go to <http://www.freescale.com> and perform a part number search.

### Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Solution Advisor</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	K10PB <sup>1</sup>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	K11P121M50SF4V2RM <sup>1</sup>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	K11P121M50SF4V2 <sup>1</sup>
Package drawing	Package dimensions are provided in package drawings.	<ul style="list-style-type: none"> <li>• MAPBGA 121-pin: 98ASA00344D<sup>1</sup></li> </ul>

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

## Kinetic K11D Family



**Figure 1. K11D block diagram**

# Table of Contents

1	Ratings.....	5	3.6.2	CMP and 6-bit DAC electrical specifications.....	36
1.1	Thermal handling ratings.....	5	3.6.3	12-bit DAC electrical characteristics.....	38
1.2	Moisture handling ratings.....	5	3.6.4	Voltage reference electrical specifications.....	41
1.3	ESD handling ratings.....	5	3.7	Timers.....	42
1.4	Voltage and current operating ratings.....	5	3.8	Communication interfaces.....	42
2	General.....	6	3.8.1	DSPI switching specifications (limited voltage range).....	42
2.1	AC electrical characteristics.....	6	3.8.2	DSPI switching specifications (full voltage range).....	44
2.2	Nonswitching electrical specifications.....	6	3.8.3	I2C switching specifications.....	46
2.2.1	Voltage and current operating requirements.....	6	3.8.4	UART switching specifications.....	46
2.2.2	LVD and POR operating requirements.....	7	3.8.5	I2S switching specifications.....	46
2.2.3	Voltage and current operating behaviors.....	8	4	Dimensions.....	50
2.2.4	Power mode transition operating behaviors.....	9	4.1	Obtaining package dimensions.....	50
2.2.5	Power consumption operating behaviors.....	10	5	Pinout.....	50
2.2.6	EMC radiated emissions operating behaviors.....	14	5.1	K11 Signal Multiplexing and Pin Assignments.....	50
2.2.7	Designing with radiated emissions in mind.....	15	5.2	K11 Pinouts.....	55
2.2.8	Capacitance attributes.....	15	6	Ordering parts.....	56
2.3	Switching specifications.....	15	6.1	Determining valid orderable parts.....	56
2.3.1	Device clock specifications.....	15	7	Part identification.....	57
2.3.2	General switching specifications.....	16	7.1	Description.....	57
2.4	Thermal specifications.....	17	7.2	Format.....	57
2.4.1	Thermal operating requirements.....	17	7.3	Fields.....	57
2.4.2	Thermal attributes.....	17	7.4	Example.....	58
3	Peripheral operating requirements and behaviors.....	18	7.5	Small package marking.....	58
3.1	Core modules.....	18	8	Terminology and guidelines.....	59
3.1.1	JTAG electricals.....	19	8.1	Definition: Operating requirement.....	59
3.2	System modules.....	22	8.2	Definition: Operating behavior.....	59
3.3	Clock modules.....	22	8.3	Definition: Attribute.....	60
3.3.1	MCG specifications.....	22	8.4	Definition: Rating.....	60
3.3.2	Oscillator electrical specifications.....	24	8.5	Result of exceeding a rating.....	60
3.3.3	32 kHz oscillator electrical characteristics.....	26	8.6	Relationship between ratings and operating requirements.....	61
3.4	Memories and memory interfaces.....	27	8.7	Guidelines for ratings and operating requirements.....	61
3.4.1	Flash electrical specifications.....	27	8.8	Definition: Typical value.....	62
3.4.2	EzPort switching specifications.....	30	8.9	Typical value conditions.....	63
3.5	Security and integrity modules.....	31	9	Revision History.....	63
3.5.1	DryIce Tamper Electrical Specifications.....	31			
3.6	Analog.....	31			
3.6.1	ADC electrical specifications.....	31			

# 1 Ratings

## 1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

## General

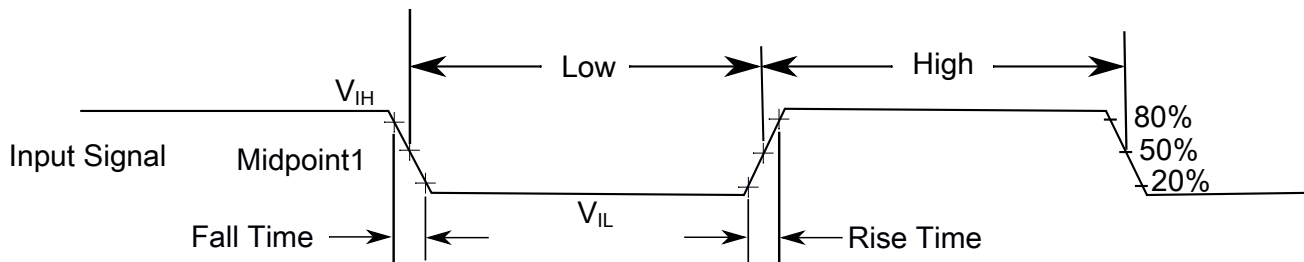
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	155	mA
$V_{DIO}$	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{BAT}$	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

**Figure 2. Input signal measurement reference**

### 2.2 Nonswitching electrical specifications

## 2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	3.6	V	
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> - V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	-0.1	0.1	V	
V <sub>SS</sub> - V <sub>SSA</sub>	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	-0.1	0.1	V	
V <sub>BAT</sub>	RTC battery supply voltage	1.71	3.6	V	
V <sub>IH</sub>	Input high voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub> 0.75 × V <sub>DD</sub>	— —	V V	
V <sub>IL</sub>	Input low voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	— —	0.35 × V <sub>DD</sub> 0.3 × V <sub>DD</sub>	V V	
V <sub>HYS</sub>	Input hysteresis	0.06 × V <sub>DD</sub>	—	V	
I <sub>ICIO</sub>	I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> <li>• V<sub>IN</sub> &gt; V<sub>DD</sub>+0.3V (Positive current injection)</li> </ul>	-3 —	— +3	mA	1
I <sub>ICcont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> <li>• Positive current injection</li> </ul>	-25 —	— +25	mA	
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	
V <sub>RFVBAT</sub>	V <sub>BAT</sub> voltage required to retain the VBAT register file	V <sub>POR_VBAT</sub>	—	V	

1. All analog pins are internally clamped to V<sub>SS</sub> and V<sub>DD</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>AIO\_MIN</sub> or greater than V<sub>AIO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICAO}|$ . The positive injection current limiting resistor is calculated as  $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICAO}|$ . Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.

## 2.2.2 LVD and POR operating requirements

Table 2. V<sub>DD</sub> supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

**Table 2.  $V_{DD}$  supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{LVW1H}$	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> <li>Level 2 falling (LVWV=01)</li> <li>Level 3 falling (LVWV=10)</li> <li>Level 4 falling (LVWV=11)</li> </ul>	2.62	2.70	2.78	V	1
$V_{LVW2H}$		2.72	2.80	2.88	V	
$V_{LVW3H}$		2.82	2.90	2.98	V	
$V_{LVW4H}$		2.92	3.00	3.08	V	
$V_{HYSH}$	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
$V_{LVDL}$	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
$V_{LVW1L}$	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>Level 1 falling (LVWV=00)</li> <li>Level 2 falling (LVWV=01)</li> <li>Level 3 falling (LVWV=10)</li> <li>Level 4 falling (LVWV=11)</li> </ul>	1.74	1.80	1.86	V	1,
$V_{LVW2L}$		1.84	1.90	1.96	V	
$V_{LVW3L}$		1.94	2.00	2.06	V	
$V_{LVW4L}$		2.04	2.10	2.16	V	
$V_{HYSL}$	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
$V_{BG}$	Bandgap voltage reference	0.97	1.00	1.03	V	
$t_{LPO}$	Internal low power oscillator period — factory trimmed	900	1000	1100	$\mu$ s	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

**Table 3. VBAT power operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR\_VBAT}$	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

## 2.2.3 Voltage and current operating behaviors

**Table 4. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — high drive strength <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -9\text{ mA}</math></li> <li><math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -3\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	
		$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength	$V_{DD} - 0.5$	—	V	

Table continues on the next page...



**Table 4. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -2\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -0.6\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OL}$	Output low voltage — high drive strength	—	0.5	V	
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 9\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 3\text{ mA}</math></li> </ul>	—	0.5	V	
	Output low voltage — low drive strength	—	0.5	V	
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 2\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 0.6\text{ mA}</math></li> </ul>	—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin)	—	1.0	$\mu\text{A}$	1
	<ul style="list-style-type: none"> <li>• @ full temperature range</li> <li>• @ <math>25\text{ }^\circ\text{C}</math></li> </ul>	—	0.1	$\mu\text{A}$	
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$I_{OZ}$	Total Hi-Z (off-state) leakage current (all input pins)	—	4	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	22	50	k $\Omega$	2
$R_{PD}$	Internal pulldown resistors	22	50	k $\Omega$	3

1. Tested by ganged leakage method
2. Measured at  $V_{input} = V_{SS}$
3. Measured at  $V_{input} = V_{DD}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$ , and  $VLLSx \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

**Table 5. Power mode transition operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	$\mu\text{s}$	1

Table continues on the next page...

**Table 5. Power mode transition operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>1.71 \text{ V}/(V_{\text{DD}} \text{ slew rate}) \leq 300 \mu\text{s}</math></li> <li>• <math>1.71 \text{ V}/(V_{\text{DD}} \text{ slew rate}) &gt; 300 \mu\text{s}</math></li> </ul>	—	$1.7 \text{ V} / (V_{\text{DD}} \text{ slew rate})$		
	• VLLS0 → RUN	—	150	$\mu\text{s}$	
	• VLLS1 → RUN	—	150	$\mu\text{s}$	
	• VLLS2 → RUN	—	79	$\mu\text{s}$	
	• VLLS3 → RUN	—	79	$\mu\text{s}$	
	• LLS → RUN	—	6	$\mu\text{s}$	
	• VLPS → RUN	—	5.2	$\mu\text{s}$	
	• STOP → RUN	—	5.2	$\mu\text{s}$	

1. Normal boot (FTFL\_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

**Table 6. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{\text{DDA}}$	Analog supply current	—	—	See note	mA	1
$I_{\text{DD\_RUN}}$	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8 V	—	12.98	14	mA	
	• @ 3.0 V	—	12.93	13.8	mA	
$I_{\text{DD\_RUN}}$	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8 V	—	17.04	19.3	mA	
	• @ 3.0 V					
	• @ 25°C	—	17.01	18.9	mA	
	• @ 125°C	—	19.8	21.3	mA	
$I_{\text{DD\_WAIT}}$	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.95	9.5	mA	2
$I_{\text{DD\_WAIT}}$	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.88	7.4	mA	5
$I_{\text{DD\_STOP}}$	Stop mode current at 3.0 V	—	320	436	$\mu\text{A}$	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>		360 410 610	489 620 1100		
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	754	—	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.1	—	mA	7
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V	—	437	—	μA	8
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	7.33 14 28 110	24.2 32 48 280	μA	
I <sub>DD_LLS</sub>	Low leakage stop mode current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	3.14 6.48 13.85 55.53	4.8 28.3 44.6 71.3	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	2.19 4.35 8.92 35.33	3.4 4.35 24.6 45.3	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	1.77 2.81 5.20 19.88	3.1 13.8 22.3 34.2	μA	
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	1.03 1.92 4.03 17.43	1.8 7.5 15.9 28.7	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.543 1.36 3.39 16.52	1.1 7.58 14.3 24.1	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> </ul>	—	0.359 1.03 2.87	0.95 6.8 15.4	μA	

Table continues on the next page...

**Table 6. Power consumption operating behaviors (continued)**

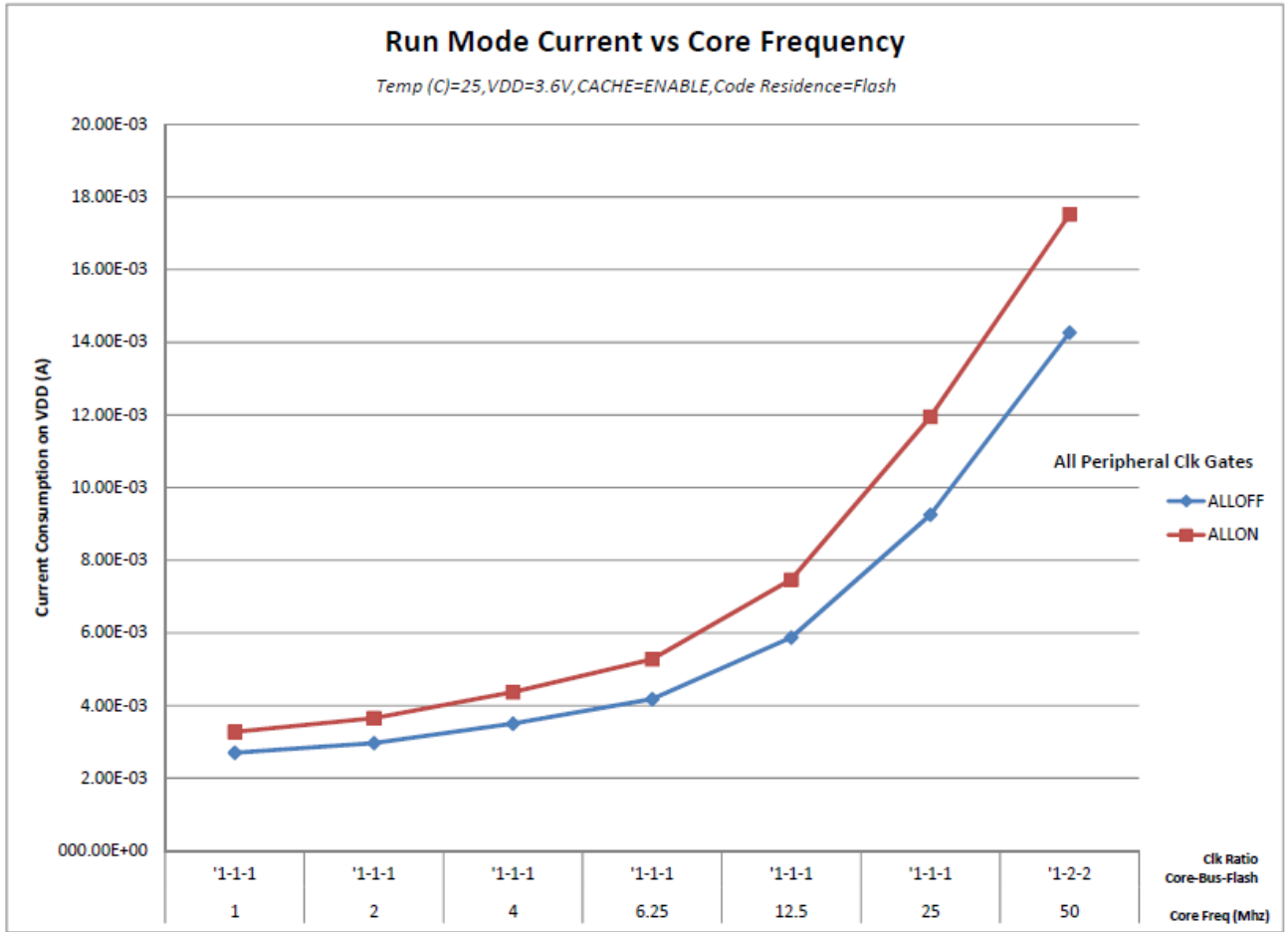
Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>		15.20	25.3		
I <sub>DD_VBAT</sub>	Average current when CPU is not accessing RTC registers at 3.0 V <ul style="list-style-type: none"> <li>• @ -40 to 25°C</li> <li>• @ 50°C</li> <li>• @ 70°C</li> <li>• @ 105°C</li> </ul>	—	0.91	1.1	μA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25 MHz core and system clock, 25 MHz bus clock, and 12.5 MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32 kHz oscillator current and RTC operation.

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL



**Figure 3. Run mode supply current vs. core frequency**

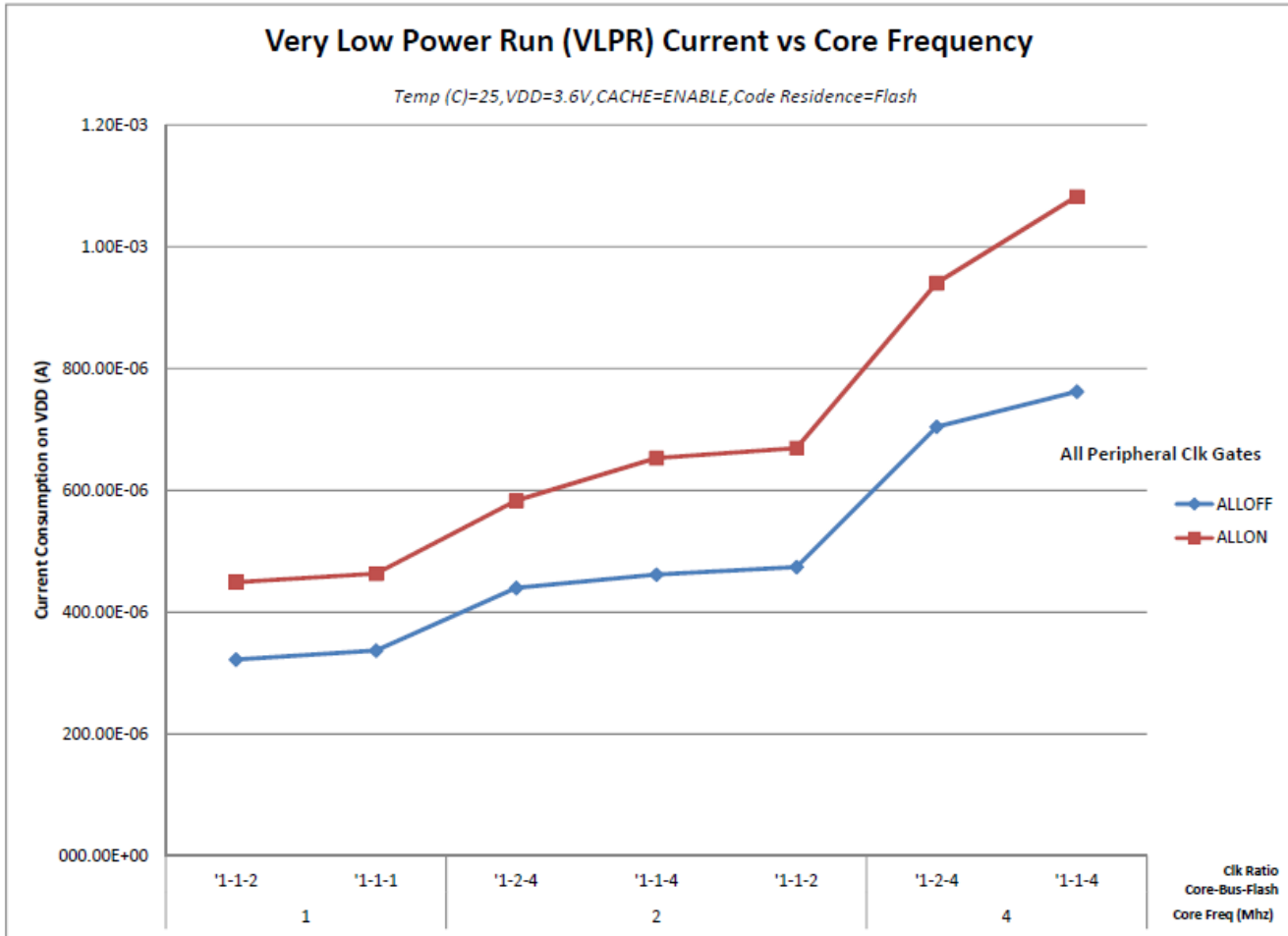


Figure 4. VLPR mode supply current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors 1

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	19	dBμV	2, 3
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	21	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	19	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	11	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	L	—	3, 4

1. This data was collected on a MK20DN128VLH5 64pin LQFP device.
2. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions— TEM Cell and*

*Wideband TEM Cell Method.* Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ ,  $f_{OSC} = 12\text{ MHz}$  (crystal),  $f_{SYS} = 48\text{ MHz}$ ,  $f_{BUS} = 48\text{ MHz}$
- Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- Go to [www.freescale.com](http://www.freescale.com).
- Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN\_A}$	Input capacitance: analog pins	—	7	pF
$C_{IN\_D}$	Input capacitance: digital pins	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
$f_{SYS}$	System and core clock	—	50	MHz	
$f_{BUS}$	Bus clock	—	50	MHz	
$f_{FLASH}$	Flash clock	—	25	MHz	
$f_{LPTMR}$	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
$f_{SYS}$	System and core clock	—	4	MHz	
$f_{BUS}$	Bus clock	—	4	MHz	
$f_{FLASH}$	Flash clock	—	1	MHz	
$f_{ERCLK}$	External reference clock	—	16	MHz	

Table continues on the next page...

**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
$f_{LPTMR\_pin}$	LPTMR clock	—	25	MHz	
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz	
$f_{I2S\_MCLK}$	I2S master clock	—	12.5	MHz	
$f_{I2S\_BCLK}$	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 2.3.2 General switching specifications

These general purpose specifications apply to all pins configured for:

- GPIO signaling
- Other peripheral module signaling not explicitly stated elsewhere

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Port rise and fall time (high drive strength) <ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— —	13 7	ns ns	4
	Port rise and fall time (low drive strength) <ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— —	12 6	ns ns	5
	<ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	— —	36 24	ns ns	



1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T <sub>J</sub>	Die junction temperature	-40	125	°C
T <sub>A</sub>	Ambient temperature	-40	105	°C

### 2.4.2 Thermal attributes

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
Single-layer (1s)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	79	°C/W	1, 2
Four-layer (2s2p)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	46	°C/W	1, 3
Single-layer (1s)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	67	°C/W	1, 3
Four-layer (2s2p)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	°C/W	1, 3

Table continues on the next page...

## Peripheral operating requirements and behaviors

Board type	Symbol	Description	121 MAPBGA	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	29	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	°C/W	5
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	4	°C/W	6

### NOTES:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

### 3.1.1 JTAG electricals

**Table 12. JTAG limited voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

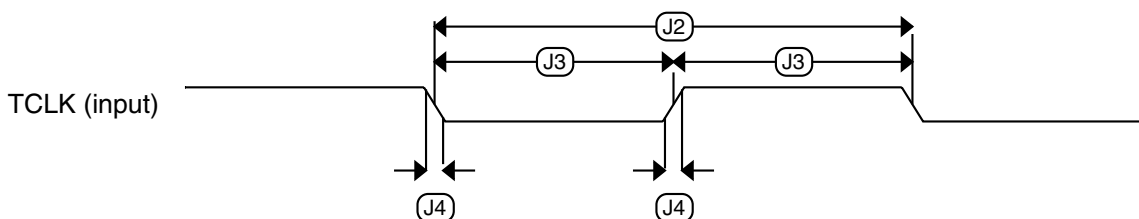
**Table 13. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> <li>• Serial Wire Debug</li> </ul>	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> </ul>	50	—	ns

*Table continues on the next page...*

**Table 13. JTAG full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
	<ul style="list-style-type: none"> <li>JTAG and CJTAG</li> </ul>	25	—	ns
	<ul style="list-style-type: none"> <li>Serial Wire Debug</li> </ul>	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns



**Figure 5. Test clock input timing**

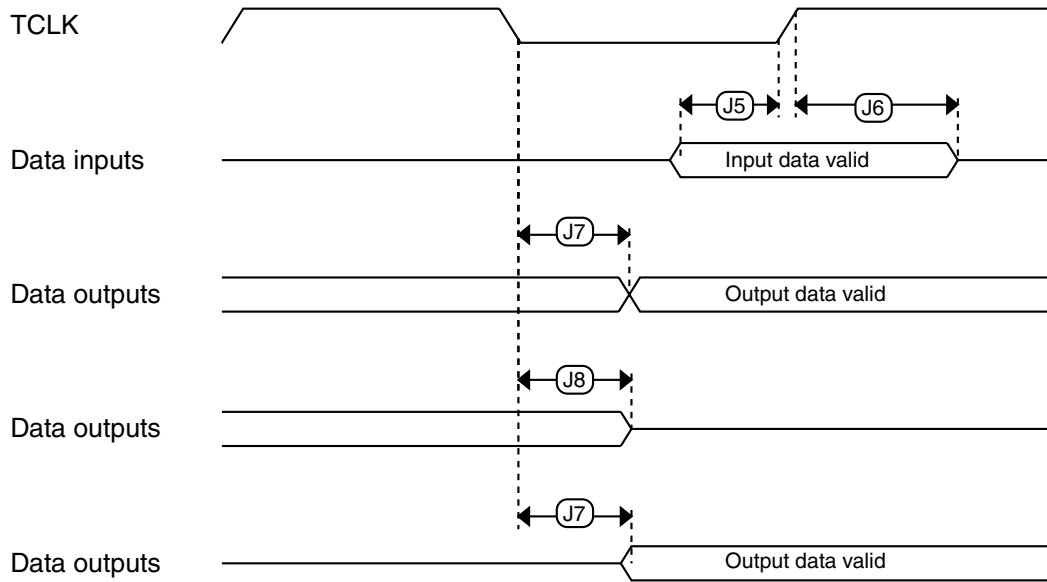


Figure 6. Boundary scan (JTAG) timing

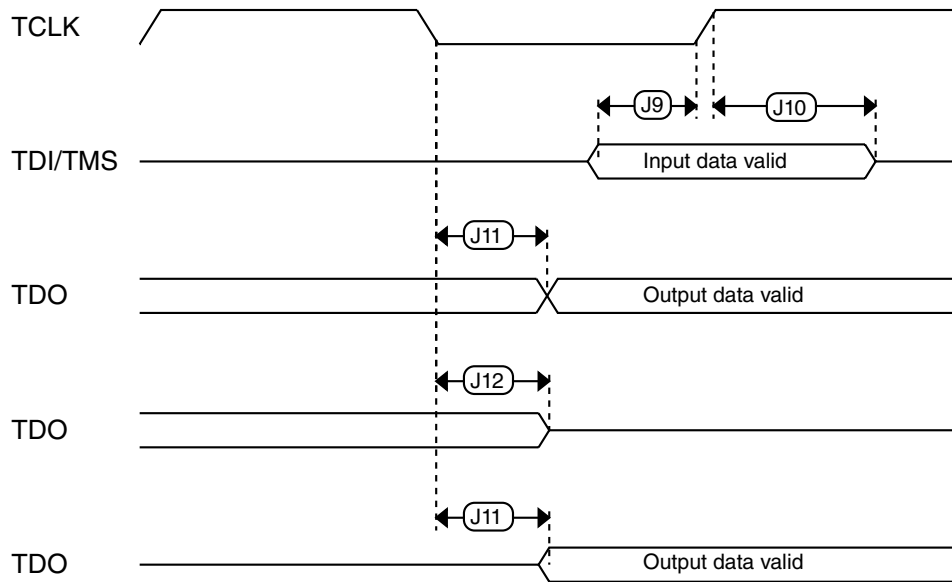
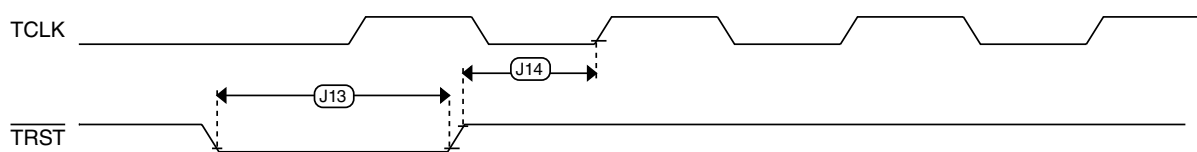


Figure 7. Test Access Port timing

## Peripheral operating requirements and behaviors



**Figure 8. TRST timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

**Table 14. MCG specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints\_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints\_t}}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	$\pm 0.3$	$\pm 0.6$	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco\_res\_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	$\pm 0.2$	$\pm 0.5$	$\%f_{\text{dco}}$	1
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	$\pm 2$	$\%f_{\text{dco}}$	1, 2
$\Delta f_{\text{dco\_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	$\pm 0.3$	$\pm 1$	$\%f_{\text{dco}}$	1, 2
$f_{\text{intf\_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf\_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc\_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints\_t}}$	—	—	kHz	

Table continues on the next page...

Table 14. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) $1280 \times f_{fill\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fill\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fill\_ref}$	80	83.89	100	MHz	
$f_{dco\_t\_DMX3\_2}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fill\_ref}$	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) $1464 \times f_{fill\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fill\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fill\_ref}$	—	95.98	—	MHz	
$J_{cyc\_fll}$	FLL period jitter • $f_{DCO} = 48$ MHz • $f_{DCO} = 98$ MHz	— —	180 150	— —	ps		
$t_{fill\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	7	
PLL							
$f_{vco}$	VCO operating frequency	48.0	—	100	MHz		
$I_{pll}$	PLL operating current • PLL @ 96 MHz ( $f_{osc\_hi\_1} = 8$ MHz, $f_{pll\_ref} = 2$ MHz, VDIV multiplier = 48)	—	1200	—	$\mu$ A	8	
$I_{pll}$	PLL operating current • PLL @ 48 MHz ( $f_{osc\_hi\_1} = 8$ MHz, $f_{pll\_ref} = 2$ MHz, VDIV multiplier = 24)	—	700	—	$\mu$ A	8	
$f_{pll\_ref}$	PLL reference frequency range	2.0	—	4.0	MHz		
$J_{cyc\_pll}$	PLL period jitter (RMS) • $f_{vco} = 48$ MHz • $f_{vco} = 100$ MHz	—	120	—	ps	9	
		—	75	—	ps		
$J_{acc\_pll}$	PLL accumulated jitter over 1 $\mu$ s (RMS)	—	1350	—	ps	9	
		—	600	—	ps		

Table continues on the next page...

**Table 14. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li><math>f_{VCO} = 48</math> MHz</li> <li><math>f_{VCO} = 100</math> MHz</li> </ul>					
$D_{lock}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%	
$D_{unl}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%	
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- 2.
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 3.3.2 Oscillator electrical specifications

#### 3.3.2.1 Oscillator DC electrical specifications

**Table 15. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>32 kHz</li> <li>4 MHz</li> <li>8 MHz (RANGE=01)</li> <li>16 MHz</li> <li>24 MHz</li> <li>32 MHz</li> </ul>	—	500	—	nA	1
$I_{DDOSC}$	Supply current — high-gain mode (HGO=1)					1

Table continues on the next page...



**Table 15. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	5	—	μA	
		—	500	—	μA	
		—	600	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C <sub>x</sub>	EXTAL load capacitance	—	—	—		2, 3
C <sub>y</sub>	XTAL load capacitance	—	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub> and C<sub>y</sub> can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 3.3.2.2 Oscillator frequency specifications

Table 16. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

#### NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

### 3.3.3 32 kHz oscillator electrical characteristics

#### 3.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{BAT}$	Supply voltage	1.71	—	3.6	V

Table continues on the next page...

**Table 17. 32kHz oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
$R_F$	Internal feedback resistor	—	100	—	M $\Omega$
$C_{para}$	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
$V_{pp}^1$	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.3.2 32 kHz oscillator frequency specifications

**Table 18. 32 kHz oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal	—	32.768	—	kHz	
$t_{start}$	Crystal start-up time	—	1000	—	ms	1
$V_{ec\_extal32}$	Externally provided input clock amplitude	700	—	$V_{BAT}$	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and  $V_{IH}$  and  $V_{IL}$  specifications do not apply. The voltage of the applied clock must be within the range of  $V_{SS}$  to  $V_{BAT}$ .

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvp4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

## Peripheral operating requirements and behaviors

1. Maximum time based on expectations at cycling end-of-life.

### 3.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk64k}$	Read 1s Block execution time • 64 KB data flash	—	—	0.9	ms	—
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	—
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu$ s	1
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	—
$t_{ersblk64k}$	Erase Flash Block execution time • 64 KB data flash	—	58	580	ms	2
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	2
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time • 512 bytes flash	—	2.4	—	ms	—
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	—
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	—
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rdonce}$	Read Once execution time	—	—	25	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	$\mu$ s	—
$t_{ersall}$	Erase All Blocks execution time	—	250	2000	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1
$t_{swapx01}$	Swap Control execution time • control code 0x01	—	200	—	$\mu$ s	—
$t_{swapx02}$	• control code 0x02	—	70	150	$\mu$ s	—
$t_{swapx04}$	• control code 0x04	—	70	150	$\mu$ s	—
$t_{swapx08}$	• control code 0x08	—	—	30	$\mu$ s	—
$t_{pgmpart64k}$	Program Partition for EEPROM execution time • 64 KB FlexNVM	—	138	—	ms	—
$t_{setramff}$	Set FlexRAM Function execution time: • Control Code 0xFF	—	70	—	$\mu$ s	—
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	—
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	—
Byte-write to FlexRAM for EEPROM operation						

Table continues on the next page...

**Table 20. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{\text{eewr8bers}}$	Byte-write to erased FlexRAM location execution time	—	175	260	$\mu\text{s}$	3
$t_{\text{eewr8b32k}}$ $t_{\text{eewr8b64k}}$	Byte-write to FlexRAM execution time: <ul style="list-style-type: none"> <li>32 KB EEPROM backup</li> <li>64 KB EEPROM backup</li> </ul>	—	385 475	1800 2000	$\mu\text{s}$ $\mu\text{s}$	—
Word-write to FlexRAM for EEPROM operation						
$t_{\text{eewr16bers}}$	Word-write to erased FlexRAM location execution time	—	175	260	$\mu\text{s}$	—
$t_{\text{eewr16b32k}}$ $t_{\text{eewr16b64k}}$	Word-write to FlexRAM execution time: <ul style="list-style-type: none"> <li>32 KB EEPROM backup</li> <li>64 KB EEPROM backup</li> </ul>	— —	385 475	1800 2000	$\mu\text{s}$ $\mu\text{s}$	—
Longword-write to FlexRAM for EEPROM operation						
$t_{\text{eewr32bers}}$	Longword-write to erased FlexRAM location execution time	—	360	540	$\mu\text{s}$	—
$t_{\text{eewr32b32k}}$ $t_{\text{eewr32b64k}}$	Longword-write to FlexRAM execution time: <ul style="list-style-type: none"> <li>32 KB EEPROM backup</li> <li>64 KB EEPROM backup</li> </ul>	— —	630 810	2050 2250	$\mu\text{s}$ $\mu\text{s}$	—

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

### 3.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{\text{DD\_PGM}}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{\text{DD\_ERS}}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 3.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{\text{nv mretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{\text{nv mretp1k}}$	Data retention after up to 1 K cycles	20	100	—	years	—

Table continues on the next page...

**Table 22. NVM reliability specifications (continued)**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcyd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	—
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	—
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq \text{°C}$ .
3. Write endurance represents the number of writes to each FlexRAM location at  $-40\text{ °C} \leq T_j \leq \text{°C}$  influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

### 3.4.2 EzPort switching specifications

**Table 23. EzPort switching specifications**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	$2 \times t_{\text{EZP\_CK}}$	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	—	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

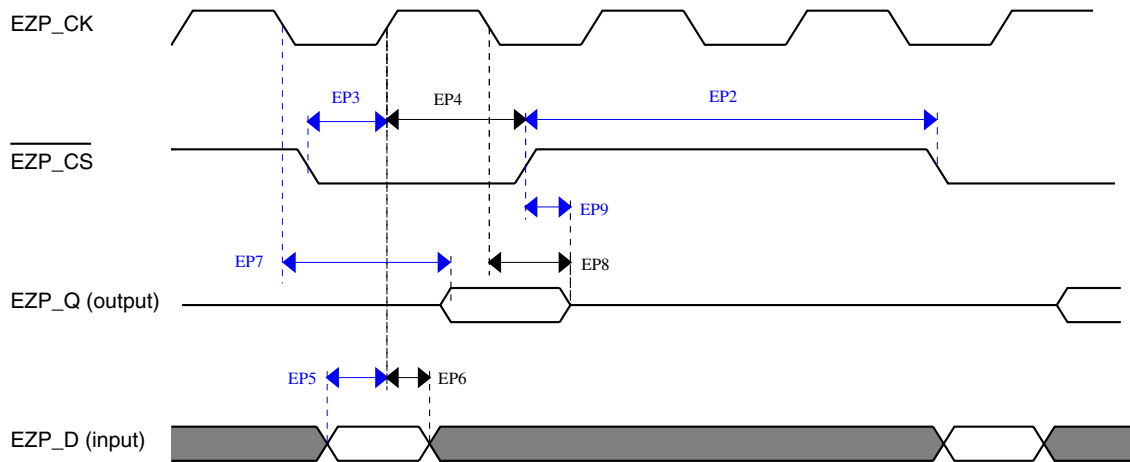


Figure 9. EzPort Timing Diagram

## 3.5 Security and integrity modules

### 3.5.1 DryIce Tamper Electrical Specifications

Information about security-related modules is not included in this document and is available only after a nondisclosure agreement (NDA) has been signed. To request an NDA, please contact your local Freescale sales representative.

## 3.6 Analog

### 3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 24](#) and [Table 25](#) are achievable on the differential pins ADC<sub>x</sub>\_DP0, ADC<sub>x</sub>\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

**3.6.1.1 16-bit ADC operating conditions****Table 24. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	V <sub>REFL</sub> V <sub>REFL</sub>	— —	31/32 * V <sub>REFH</sub> V <sub>REFH</sub>	V	—
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	— —	8 4	10 5	pF	—
R <sub>ADIN</sub>	Input series resistance		—	2	5	kΩ	—
R <sub>AS</sub>	Analog source resistance (external)	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C <sub>rate</sub>	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C <sub>rate</sub>	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.

2. DC potential difference.

3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R<sub>AS</sub>/C<sub>AS</sub> time constant should be kept to < 1 ns.

4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.

5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).



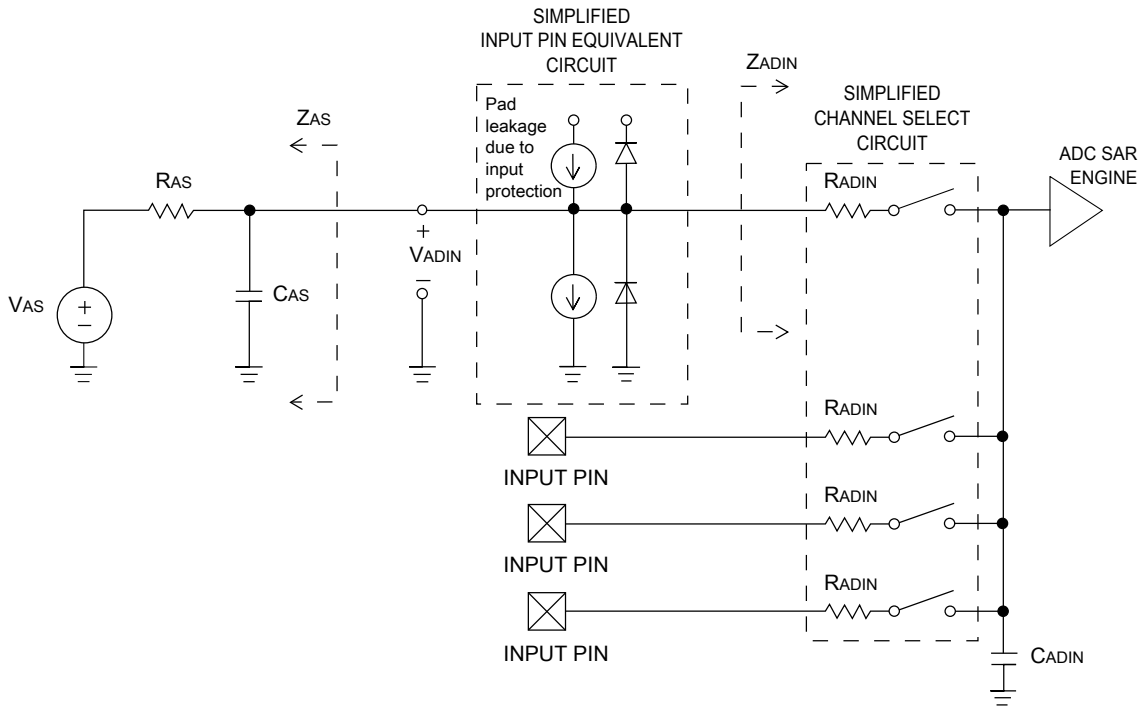


Figure 10. ADC input impedance equivalency diagram

### 3.6.1.2 16-bit ADC electrical characteristics

Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

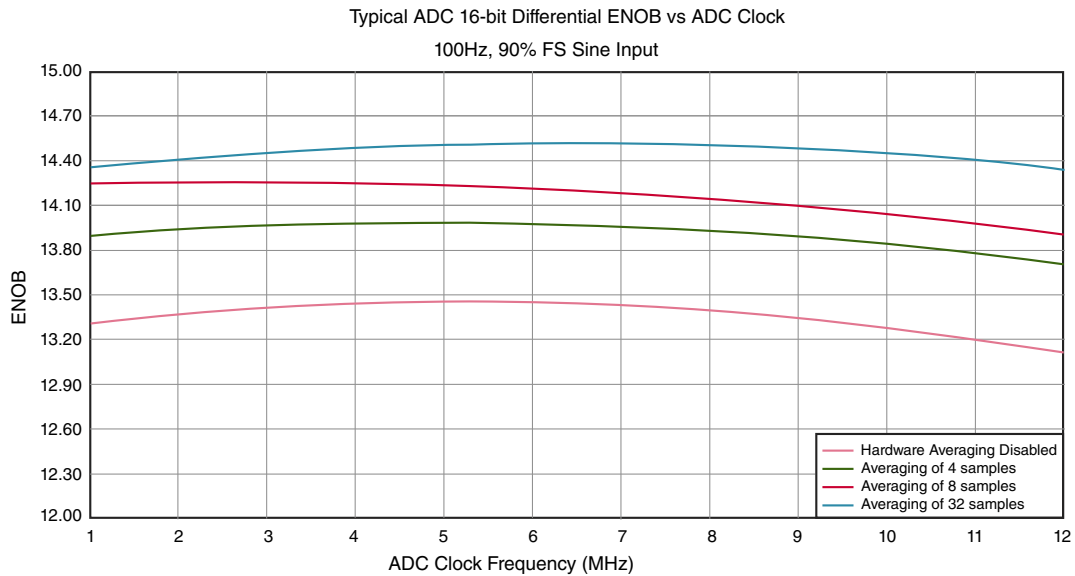
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	—	±4 ±1.4	±6.8 ±2.1	LSB <sup>4</sup>	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	—	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB <sup>4</sup>	5

Table continues on the next page...

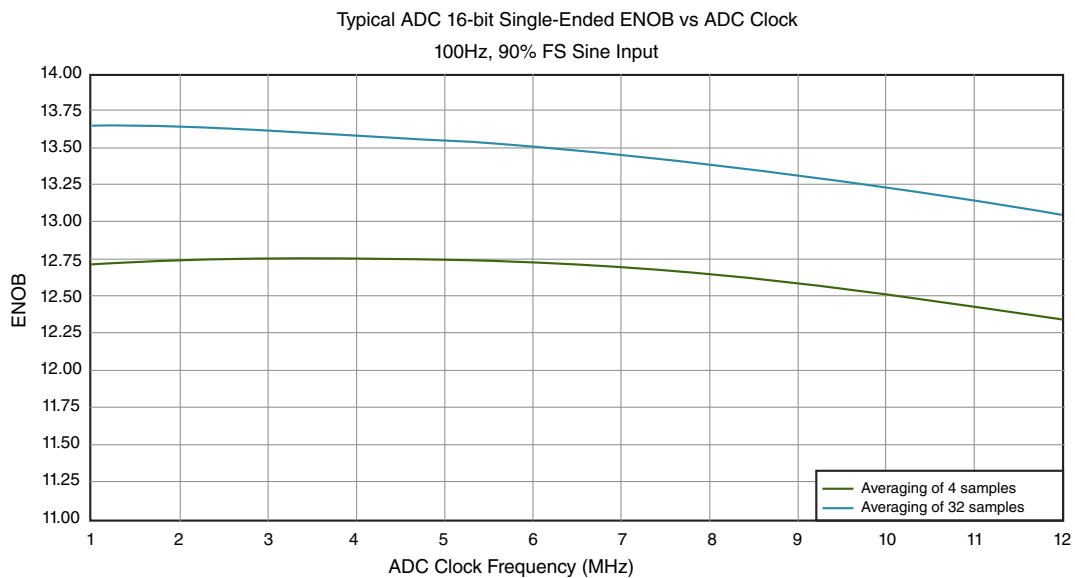
**Table 25. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±1.0	-2.7 to +1.9	LSB <sup>4</sup>	5
E <sub>FS</sub>	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	-4	-5.4	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ <sup>5</sup>
E <sub>Q</sub>	Quantization error	<ul style="list-style-type: none"> <li>16-bit modes</li> <li>≤13-bit modes</li> </ul>	—	-1 to 0	—	LSB <sup>4</sup>	
ENOB	Effective number of bits	16-bit differential mode	12.8	14.5	—	bits	6
		<ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul>	11.9	13.8	—	bits	
		16-bit single-ended mode	12.2	13.9	—	bits	
		<ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul>	11.4	13.1	—	bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode	—	-94	—	dB	7
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	—	-85	—	dB	
SFDR	Spurious free dynamic range	16-bit differential mode	82	95	—	dB	7
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	78	90	—	dB	
E <sub>IL</sub>	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V <sub>TEMP25</sub>	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^{\circ}\text{C}$ ,  $f_{ADCK} = 2.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz



**Figure 11. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**



**Figure 12. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

### 3.6.2 CMP and 6-bit DAC electrical specifications

**Table 26. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu$ A
$I_{DLS}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu$ A
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup>				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
$V_{CMPOh}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOl}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu$ s
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu$ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

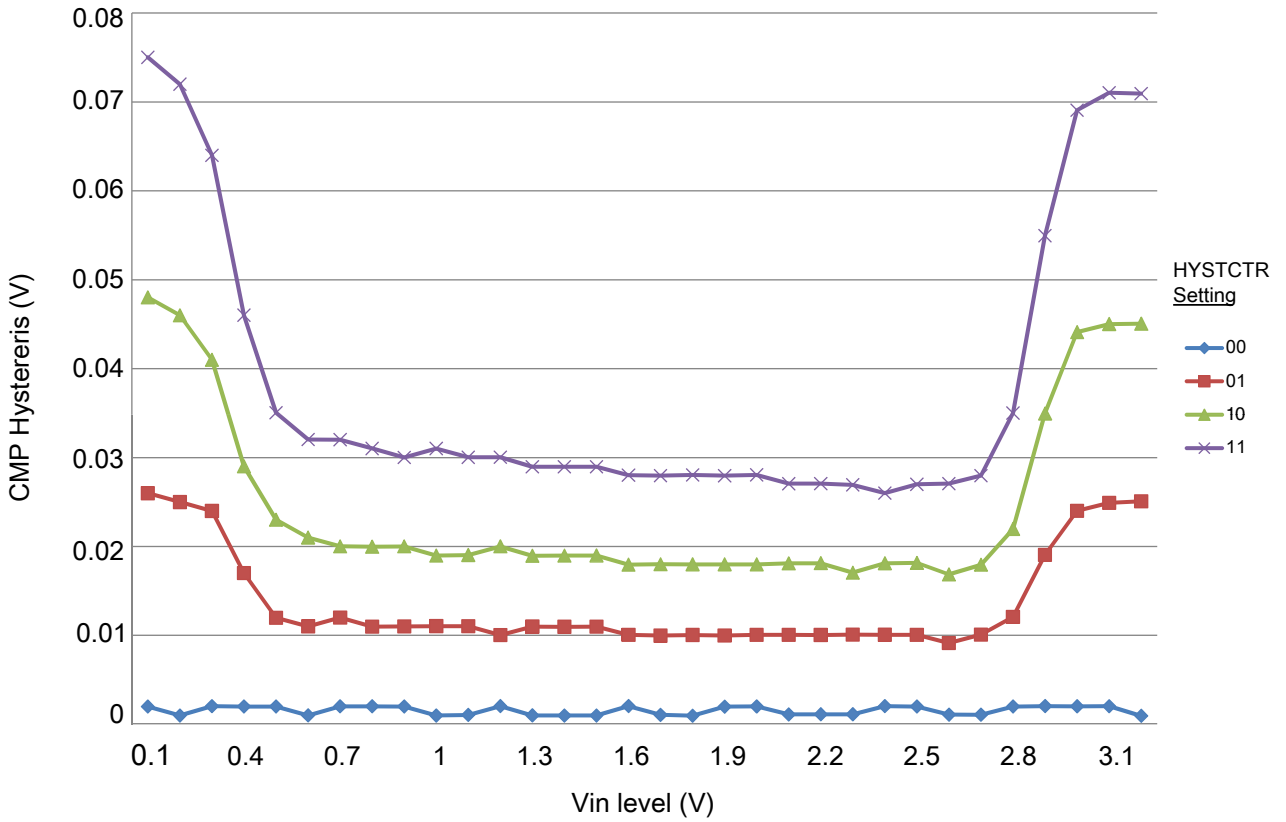


Figure 13. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

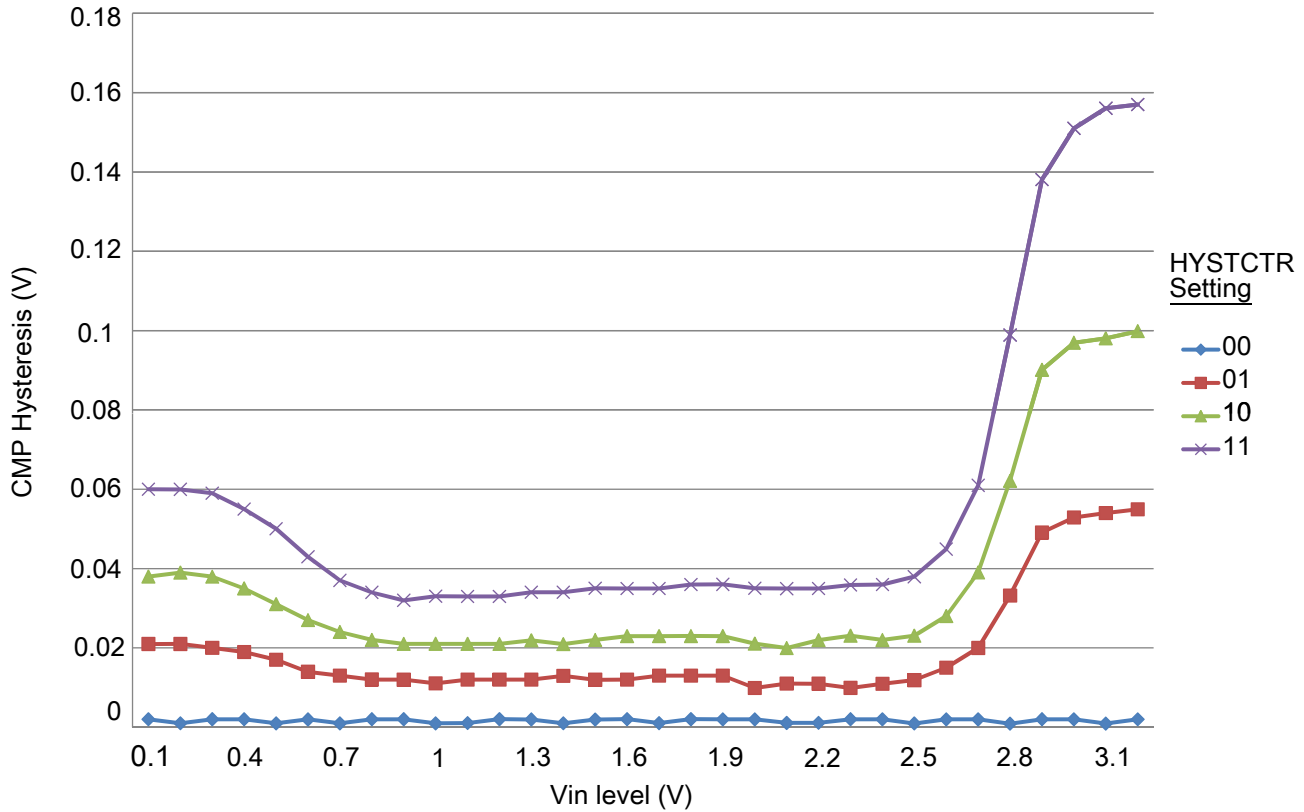


Figure 14. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 3.6.3 12-bit DAC electrical characteristics

#### 3.6.3.1 12-bit DAC operating requirements

Table 27. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REFH}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

### 3.6.3.2 12-bit DAC operating behaviors

Table 28. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	330	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	1200	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	$\text{V}/\mu\text{s}$	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100\text{ mV}$  with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100\text{ mV}$  to  $V_{DACR} - 100\text{ mV}$
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

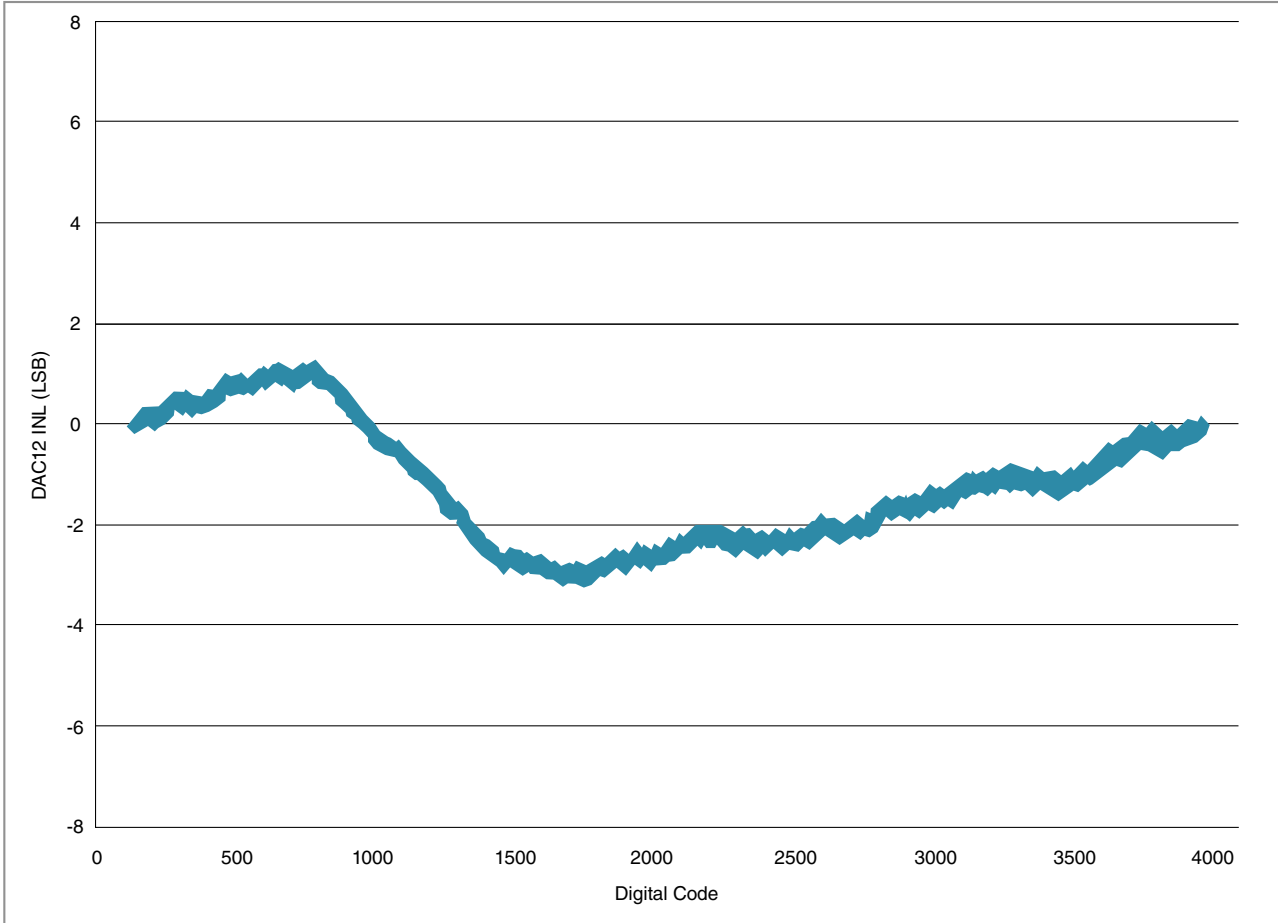


Figure 15. Typical INL error vs. digital code



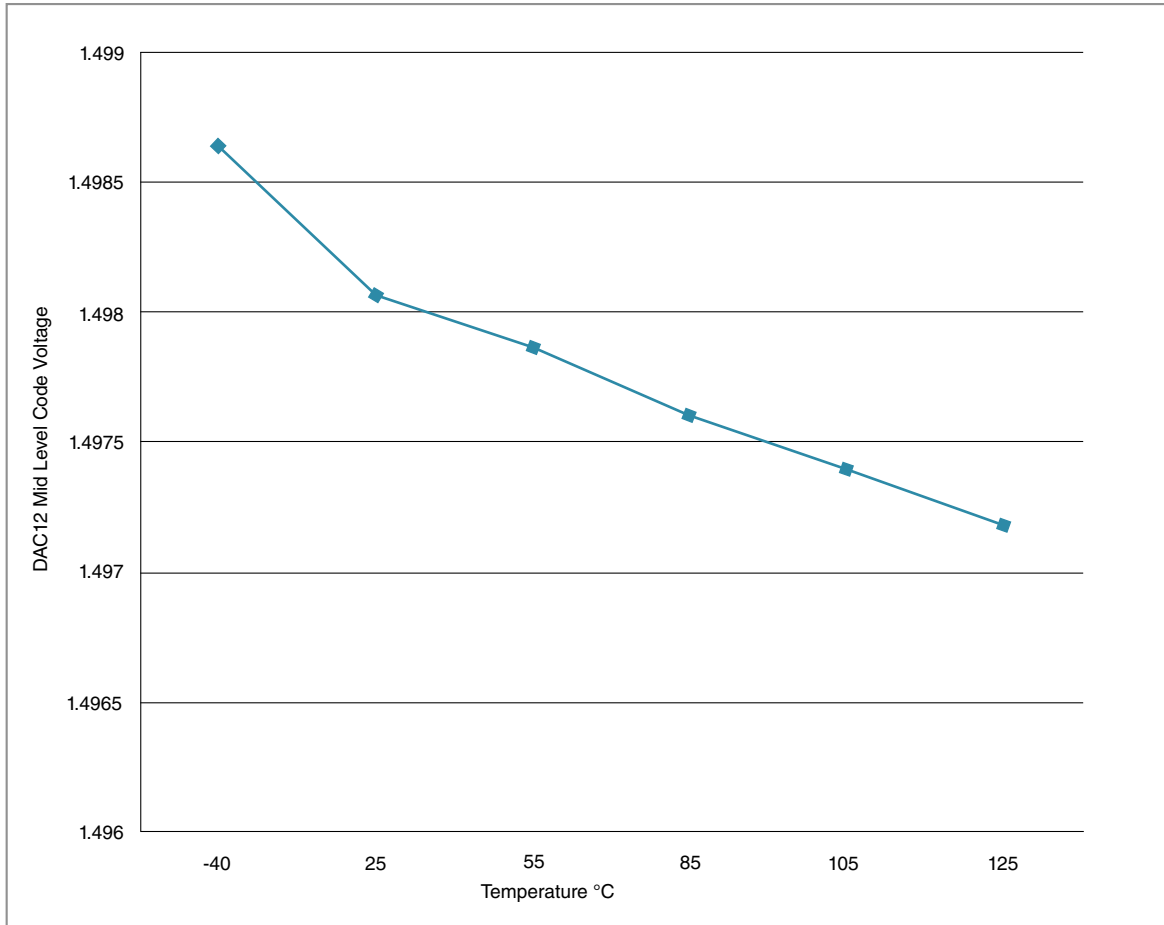


Figure 16. Offset at half scale vs. temperature

### 3.6.4 Voltage reference electrical specifications

Table 29. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	—
$T_A$	Temperature	Operating temperature range of the device		°C	—
$C_L$	Output load capacitance	100		nF	1, 2

- $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
- The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

**Table 30. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25C	1.1915	1.195	1.1977	V	1
$V_{out}$	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
$V_{out}$	Voltage reference output — user trim	1.193	—	1.197	V	1
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	1
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	1
$I_{bg}$	Bandgap only current	—	—	80	$\mu A$	1
$\Delta V_{LOAD}$	Load regulation • current = $\pm 1.0$ mA	—	200	—	$\mu V$	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu s$	—
$V_{vdrift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 31. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	50	$^{\circ}C$	—

**Table 32. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim	1.173	1.225	V	—

## 3.7 Timers

See [General switching specifications](#).

## 3.8 Communication interfaces

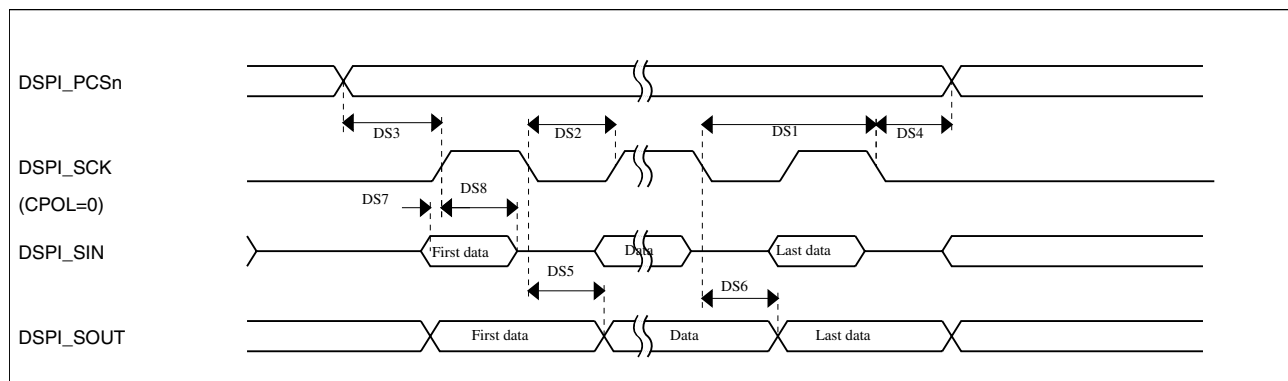
### 3.8.1 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 33. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].



**Figure 17. DSPI classic SPI timing — master mode**

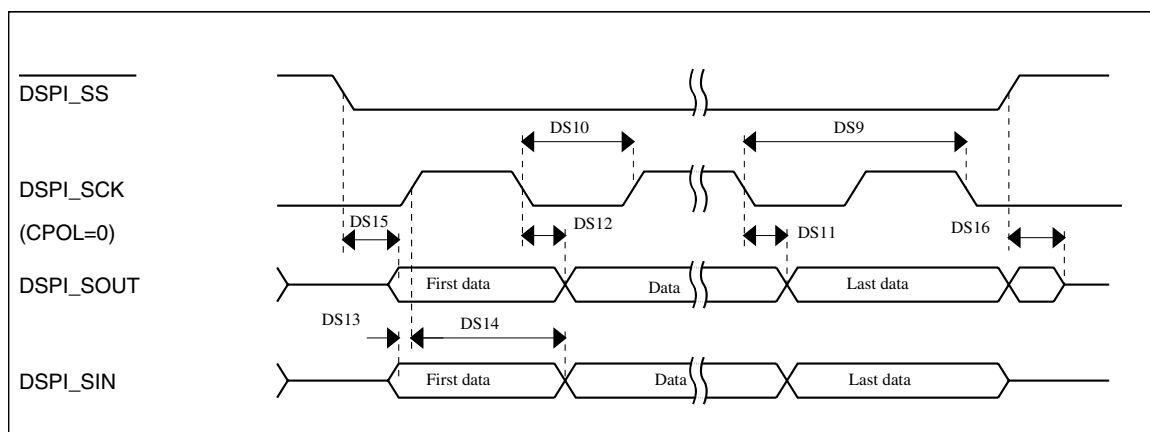
**Table 34. Slave mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz

Table continues on the next page...

**Table 34. Slave mode DSPI timing (limited voltage range) (continued)**

Num	Description	Min.	Max.	Unit
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns

**Figure 18. DSPI classic SPI timing — slave mode**

### 3.8.2 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 35. Master mode DSPI timing (full voltage range)**

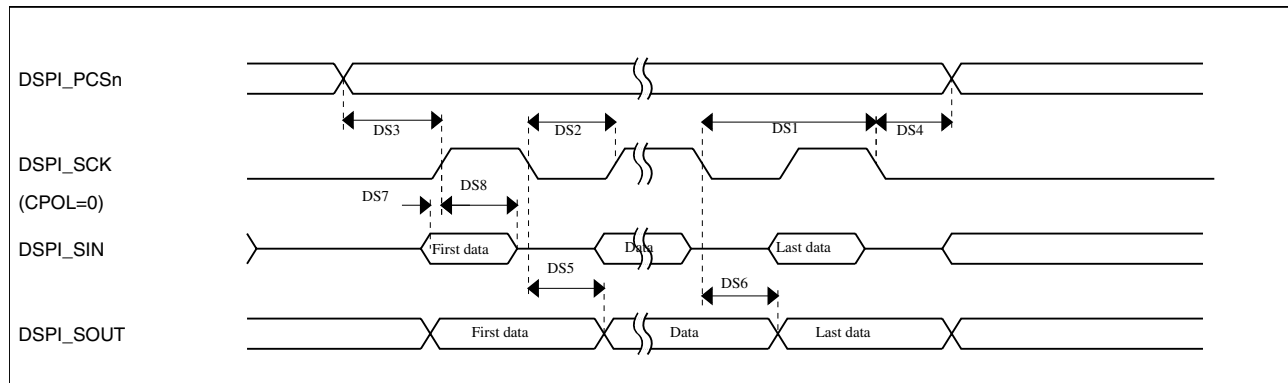
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	

Table continues on the next page...

**Table 35. Master mode DSPI timing (full voltage range) (continued)**

Num	Description	Min.	Max.	Unit	Notes
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].

**Figure 19. DSPI classic SPI timing — master mode****Table 36. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	19	ns

## I2S switching specifications

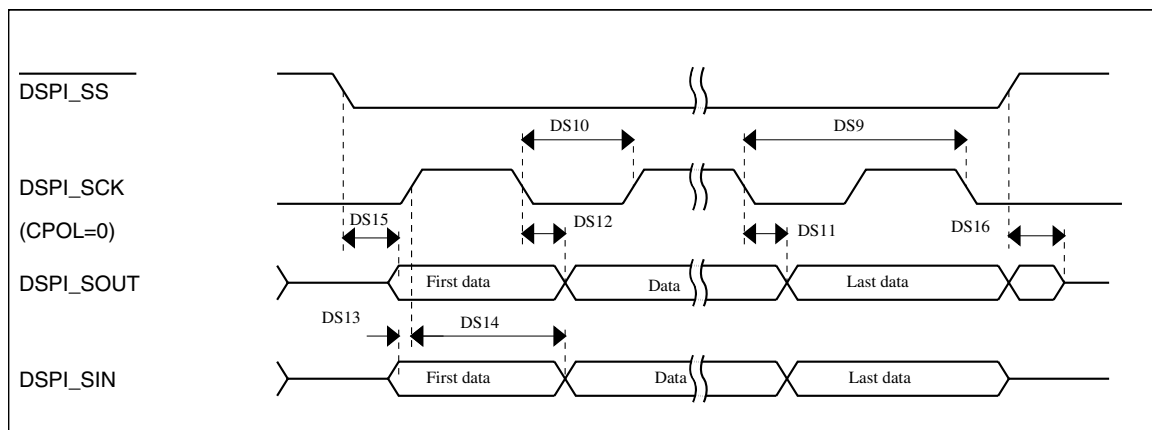


Figure 20. DSPI classic SPI timing — slave mode

### 3.8.3 I<sup>2</sup>C switching specifications

See [General switching specifications](#).

### 3.8.4 UART switching specifications

See [General switching specifications](#).

### 3.8.5 I2S switching specifications

#### 3.8.5.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

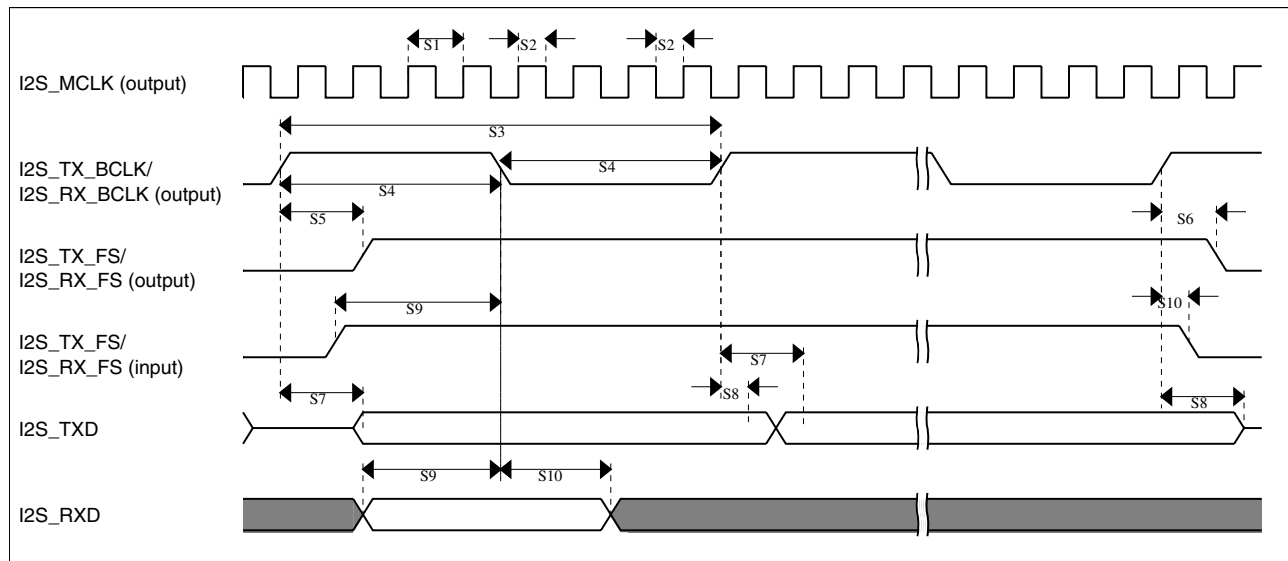
Table 37. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns

Table continues on the next page...

**Table 37. I2S/SAI master mode timing (continued)**

Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



**Figure 21. I2S/SAI timing — master modes**

**Table 38. I2S/SAI slave mode timing**

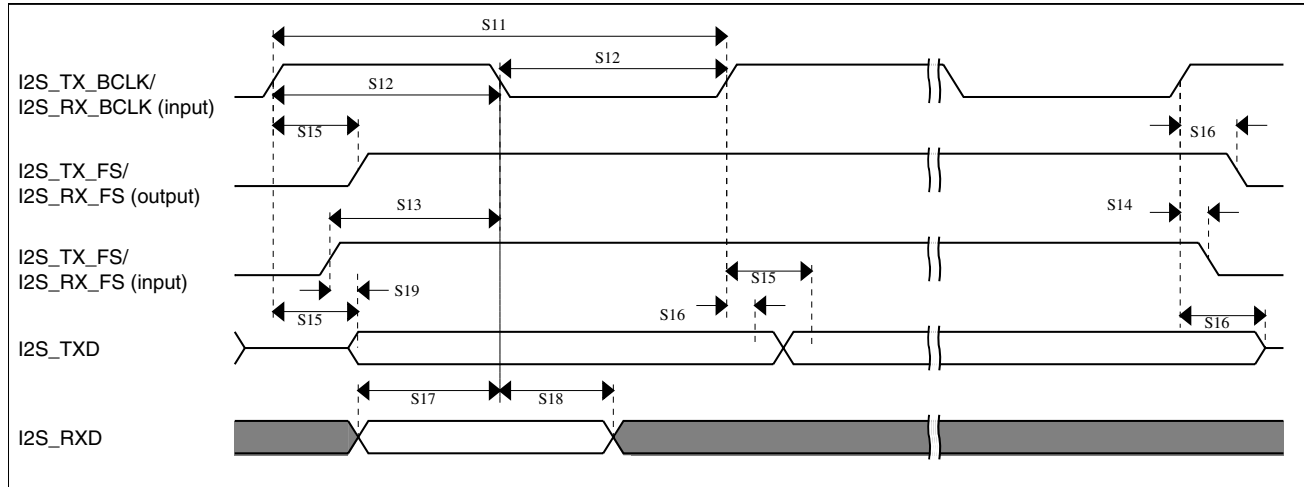
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns

Table continues on the next page...

**Table 38. I2S/SAI slave mode timing (continued)**

Num.	Characteristic	Min.	Max.	Unit
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



**Figure 22. I2S/SAI timing — slave modes**

### 3.8.5.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

**Table 39. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

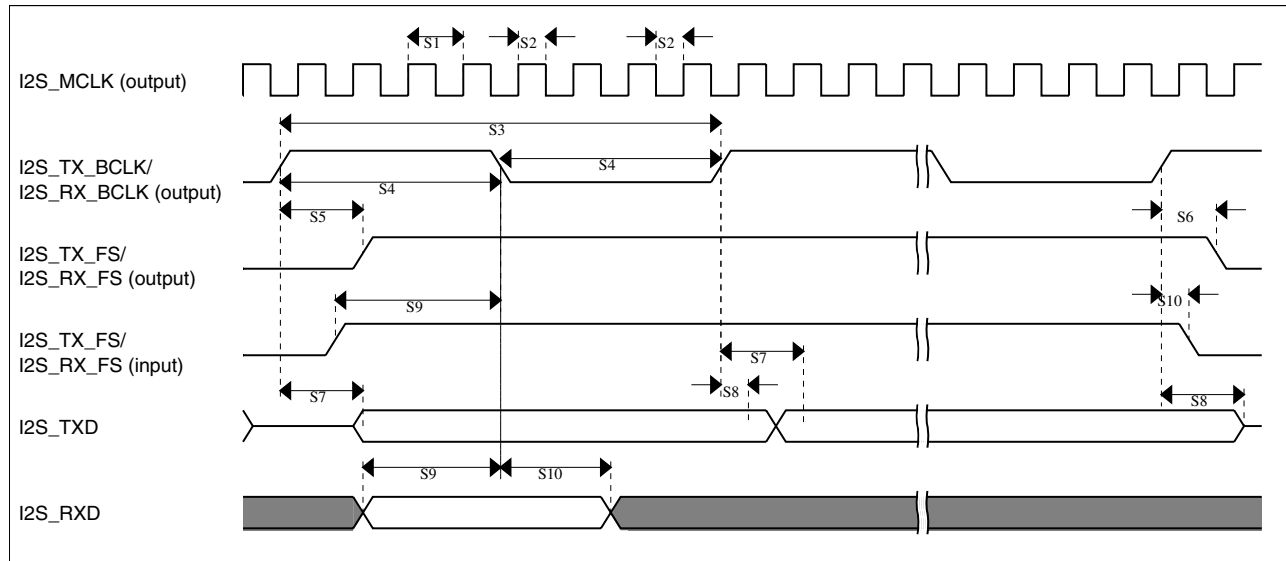
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns

Table continues on the next page...



**Table 39. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

Num.	Characteristic	Min.	Max.	Unit
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



**Figure 23. I2S/SAI timing — master modes**

**Table 40. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

## Dimensions

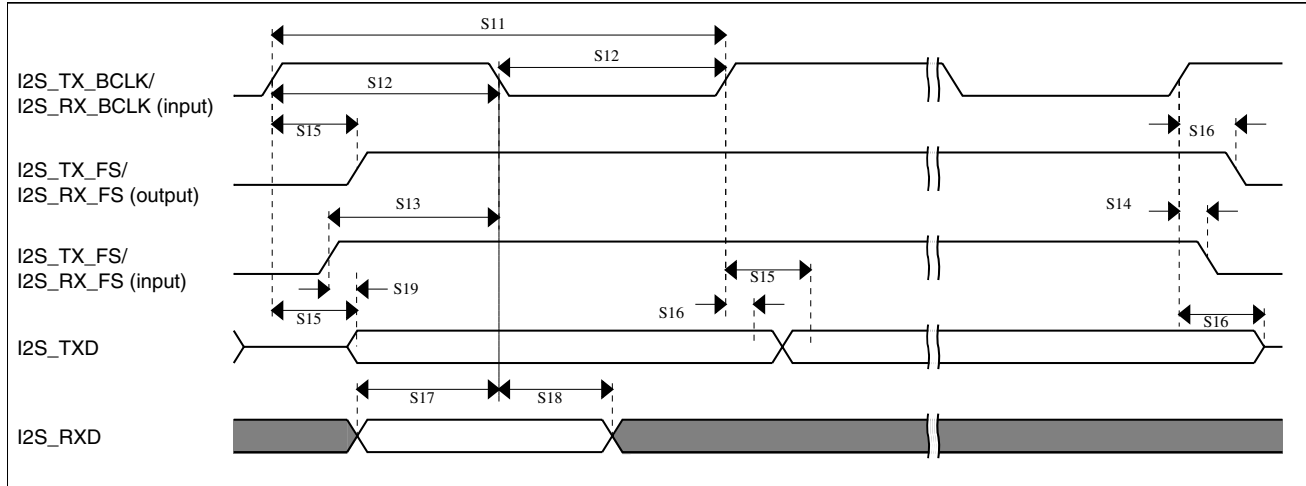


Figure 24. I2S/SAI timing — slave modes

## 4 Dimensions

### 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
81-pin MAPBGA	98ASA00344D
121-pin MAPBGA	98ASA00344D

## 5 Pinout

### 5.1 K11 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

- The analog input signals ADC0\_SE10, ADC0\_SE11, ADC0\_DP1, and ADC0\_DM1 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- The TRACE signals on PTE0, PTE1, PTE2, PTE3, and PTE4 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.
- If the VBAT pin is not used, the VBAT pin should be left floating. Do not connect VBAT pin to VSS.
- The FTM\_CLKIN signals on PTB16 and PTB17 are available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices. For K22D devices this signal is on ALT4, and for K22F devices, this signal is on ALT7.
- The FTM0\_CH2 signal on PTC5/LLWU\_P9 is available only for K11, K12, K21, and K22 devices and is not present on K10 and K20 devices.
- The I2C0\_SCL signal on PTD2/LLWU\_P13 and I2C0\_SDA signal on PTD3 are available only for K11, K12, K21, and K22 devices and are not present on K10 and K20 devices.

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	ADC0_SE10	ADC0_SE10	PTE0	SPI1_PCS1	UART1_TX		TRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT	
E3	ADC0_SE11	ADC0_SE11	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX		TRACE_D3	I2C1_SCL	SPI1_SIN	
E2	ADC0_DP1	ADC0_DP1	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b		TRACE_D2			
F4	ADC0_DM1	ADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b		TRACE_D1		SPI1_SOUT	
H7	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX		TRACE_D0			
G4	DISABLED		PTE5	SPI1_PCS2	UART3_RX					
E6	VDD	VDD								
G7	VSS	VSS								
K3	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
H4	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
A11	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
A10	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
L6	VSS	VSS								

## Pinout

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K1	ADC0_DP0	ADC0_DP0								
K2	ADC0_DM0	ADC0_DM0								
L1	ADC0_DP3	ADC0_DP3								
L2	ADC0_DM3	ADC0_DM3								
F5	VDDA	VDDA								
G5	VREFH	VREFH								
G6	VREFL	VREFL								
F6	VSSA	VSSA								
L3	VREF_OUT/ CMP1_IN5/ CMP0_IN5	VREF_OUT/ CMP1_IN5/ CMP0_IN5								
K5	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
L7	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B								
H5	TAMPER1	TAMPER1								
J5	TAMPER2	TAMPER2								
L4	XTAL32	XTAL32								
L5	EXTAL32	EXTAL32								
K6	VBAT	VBAT								
J6	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
J7	JTAG_TDO/ TRACE_SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	DISABLED		PTA5		FTM0_CH2			I2S0_TX_BCLK	JTAG_TRST_b	
K8	DISABLED		PTA12		FTM1_CH0			I2S0_TXD0	FTM1_QD_ PHA	
L8	DISABLED		PTA13/ LLWU_P4		FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
K9	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_RX_ BCLK	I2S0_TXD1	
L9	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD0		
J10	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b			I2S0_RX_FS	I2S0_RXD1	
H10	DISABLED		PTA17	SPI0_SIN	UART0_RTS_b			I2S0_MCLK		

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L10	VDD	VDD								
K10	VSS	VSS								
L11	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
J11	RESET_b	RESET_b								
G11	ADC0_SE8	ADC0_SE8	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
G10	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
G9	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b			FTM0_FLT3		
G8	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
D10	DISABLED		PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1		
C10	DISABLED		PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2		
B11	DISABLED		PTB12	UART3_RTS_b	FTM1_CH0	FTM0_CH4		FTM1_QD_ PHA		
C11	DISABLED		PTB13	UART3_CTS_b	FTM1_CH1	FTM0_CH5		FTM1_QD_ PHB		
B10	DISABLED		PTB16	SPI1_SOUT	UART0_RX			EWM_IN	FTM_CLKIN0	
E9	DISABLED		PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	FTM_CLKIN1	
D9	DISABLED		PTB18		FTM2_CH0	I2S0_TX_BCLK				
C9	DISABLED		PTB19		FTM2_CH1	I2S0_TX_FS				
B9	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1		
D8	ADC0_SE15	ADC0_SE15	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
C8	ADC0_SE4b/ CMP1_IN0	ADC0_SE4b/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
B8	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_BCLK		
G3	VSS	VSS								
E5	VDD	VDD								
A8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
D7	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	FTM0_CH2	
C7	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_ BCLK		I2S0_MCLK		
B7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS				
A7	CMP0_IN2	CMP0_IN2	PTC8			I2S0_MCLK				
D6	CMP0_IN3	CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0		
C6	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS				

## Pinout

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C5	DISABLED		PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD1				
B6	DISABLED		PTC12							
A6	DISABLED		PTC13							
D5	DISABLED		PTC16		UART3_RX					
C4	DISABLED		PTC17		UART3_TX					
D4	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_b					
D3	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b					
C3	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX	I2C0_SCL				
B3	DISABLED		PTD3	SPI0_SIN	UART2_TX	I2C0_SDA				
A3	ADC0_SE21	ADC0_SE21	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
A2	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5		EWM_OUT_b		
B2	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
A1	ADC0_SE22	ADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		
F3	NC	NC								
H1	NC	NC								
H2	NC	NC								
J1	NC	NC								
J2	NC	NC								
J3	NC	NC								
H3	NC	NC								
K4	NC	NC								
H6	NC	NC								
J9	NC	NC								
J4	NC	NC								
H11	NC	NC								
F11	NC	NC								
E11	NC	NC								
D11	NC	NC								
E10	NC	NC								
F10	NC	NC								
F9	NC	NC								
F8	NC	NC								
E8	NC	NC								
E7	NC	NC								
F7	NC	NC								

121 MAP BGA	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A5	NC	NC								
B5	NC	NC								
B4	NC	NC								
A4	NC	NC								
A9	NC	NC								
B1	NC	NC								
C2	NC	NC								
C1	NC	NC								
D2	NC	NC								
D1	NC	NC								
E1	NC	NC								

## 5.2 K11 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

## Ordering parts

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4/ LLWU_P14	NC	NC	PTC13	PTC8	PTC4/ LLWU_P8	NC	PTE19	PTE18	A
B	NC	PTD6/ LLWU_P15	PTD3	NC	NC	PTC12	PTC7	PTC3/ LLWU_P7	PTC0	PTB16	PTB12	B
C	NC	NC	PTD2/ LLWU_P13	PTC17	PTC11/ LLWU_P11	PTC10	PTC6/ LLWU_P10	PTC2	PTB19	PTB11	PTB13	C
D	NC	NC	PTD1	PTD0/ LLWU_P12	PTC16	PTC9	PTC5/ LLWU_P9	PTC1/ LLWU_P6	PTB18	PTB10	NC	D
E	NC	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	VDD	VDD	NC	NC	PTB17	NC	NC	E
F	NC	NC	NC	PTE3	VDDA	VSSA	NC	NC	NC	NC	NC	F
G	NC	NC	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0/ LLWU_P5	G
H	NC	NC	NC	PTE17	TAMPER1	NC	PTE4/ LLWU_P2	PTA1	PTA3	PTA17	NC	H
J	NC	NC	NC	NC	TAMPER2	PTA0	PTA2	PTA4/ LLWU_P3	NC	PTA16	RESET_b	J
K	ADC0_DP0	ADC0_DM0	PTE16	NC	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	ADC0_DP3	ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5	XTAL32	EXTAL32	VSS	TAMPER0/ RTC_ WAKEUP_B	PTA13/ LLWU_P4	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

**Figure 25. K11 121 MAPBGA Pinout Diagram**

## 6 Ordering parts

### 6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: PK11 and MK11



## 7 Part identification

### 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 7.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

### 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
K##	Kinetis family	<ul style="list-style-type: none"> <li>K11</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
M	Flash memory type	<ul style="list-style-type: none"> <li>N = Program flash only</li> <li>X = Program flash and FlexMemory</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>32 = 32 KB</li> <li>64 = 64 KB</li> <li>128 = 128 KB</li> <li>256 = 256 KB</li> <li>512 = 512 KB</li> <li>1M0 = 1 MB</li> <li>2M0 = 2 MB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>Z = Initial</li> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> <li>C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>FM = 32 QFN (5 mm x 5 mm)</li> <li>FT = 48 QFN (7 mm x 7 mm)</li> </ul>

*Table continues on the next page...*

## Part identification

Field	Description	Values
		<ul style="list-style-type: none"><li>• LF = 48 LQFP (7 mm x 7 mm)</li><li>• LH = 64 LQFP (10 mm x 10 mm)</li><li>• MP = 64 MAPBGA (5 mm x 5 mm)</li><li>• LK = 80 LQFP (12 mm x 12 mm)</li><li>• LL = 100 LQFP (14 mm x 14 mm)</li><li>• MC = 121 MAPBGA (8 mm x 8 mm)</li><li>• LQ = 144 LQFP (20 mm x 20 mm)</li><li>• MD = 144 MAPBGA (13 mm x 13 mm)</li></ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"><li>• 5 = 50 MHz</li><li>• 7 = 72 MHz</li><li>• 10 = 100 MHz</li><li>• 12 = 120 MHz</li><li>• 15 = 150 MHz</li><li>• 16 = 168 MHz</li><li>• 18 = 180 MHz</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li><li>• (Blank) = Trays</li></ul>

## 7.4 Example

This is an example part number:

MK11DN512VMC5

## 7.5 Small package marking

In an effort to save space, small package devices use special marking on the chip. These markings have the following format:

Q ## C F T PP

This table lists the possible values for each field in the part number for small packages (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"><li>• M = Fully qualified, general market flow</li><li>• P = Prequalification</li></ul>
C	Speed	<ul style="list-style-type: none"><li>• G = 50 MHz</li></ul>
F	Flash memory configuration	<ul style="list-style-type: none"><li>• G = 128 KB + Flex</li><li>• H = 256 KB + Flex</li><li>• 9 = 512 KB</li></ul>
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• V = -40 to 105</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• MC = 121 MAPBGA</li></ul>

This table lists some examples of small package marking along with the original part numbers:

Original part number	Alternate part number
MK11DX128VLK5	M11GGVLK
MK11DX256VMC5	M11GHVMC

## 8 Terminology and guidelines

### 8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

### 8.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

#### 8.2.1 Example

This is an example of an operating behavior:

## Terminology and guidelines

Symbol	Description	Min.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	130	$\mu A$

### 8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

#### 8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

### 8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

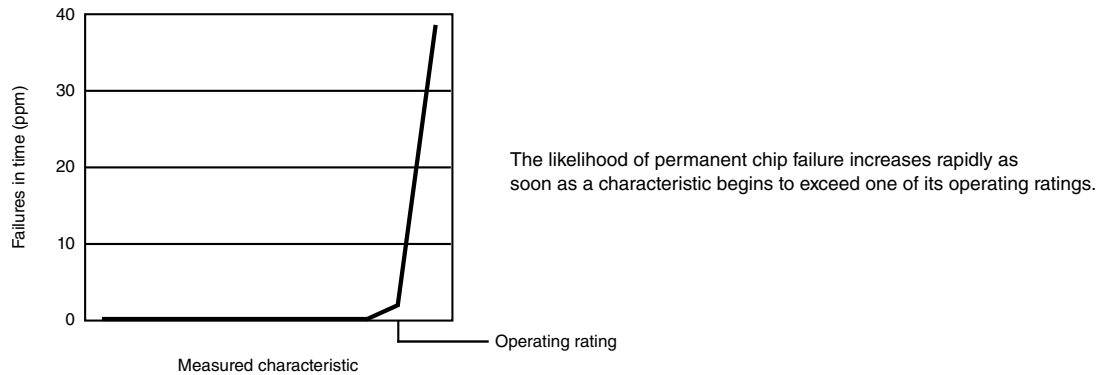
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

#### 8.4.1 Example

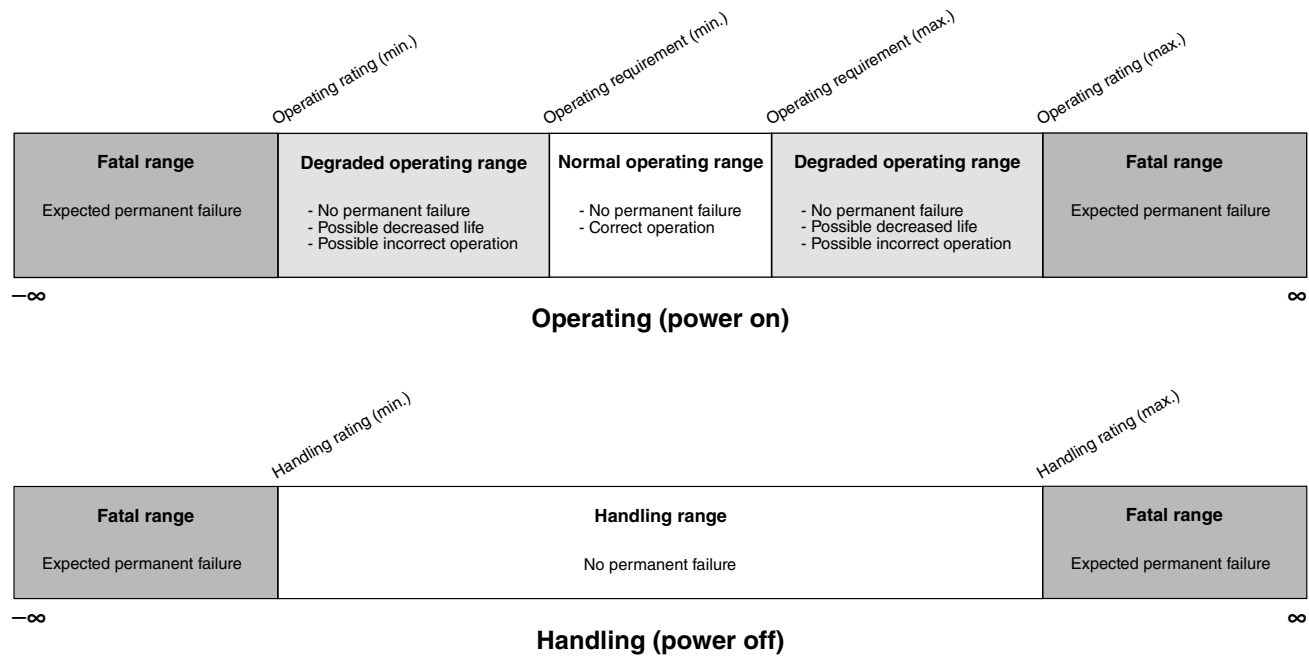
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	1.0 V core supply voltage	-0.3	1.2	V

## 8.5 Result of exceeding a rating



## 8.6 Relationship between ratings and operating requirements



## 8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

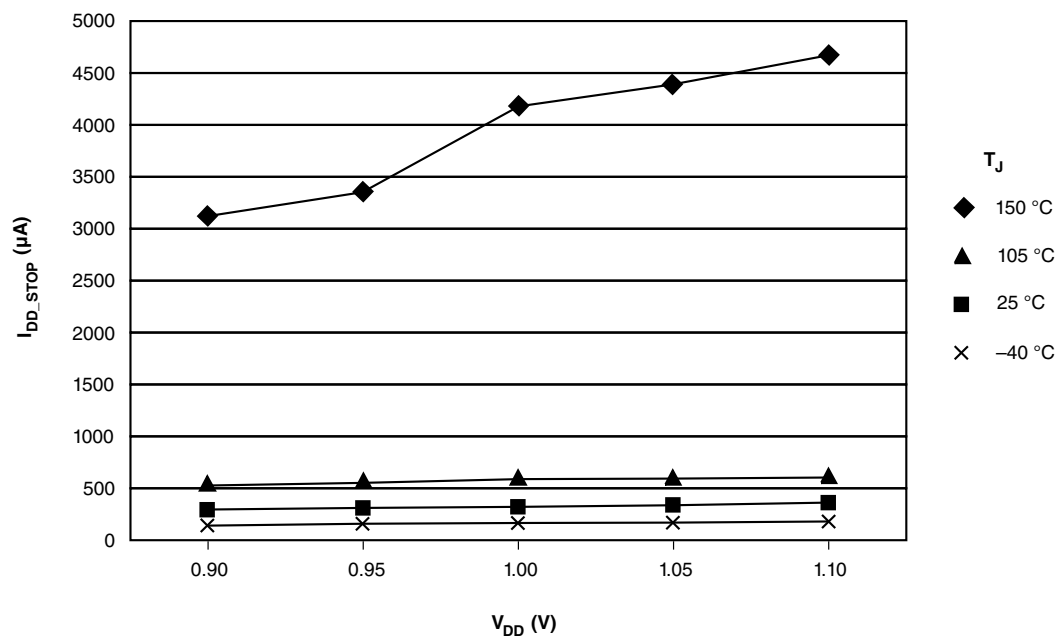
### 8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

### 8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 9 Revision History

The following table provides a revision history for this document.

**Table 41. Revision History**

Rev. No.	Date	Substantial Changes
1	6/2012	Alpha customer release.
2	7/2012	<ul style="list-style-type: none"> <li>Updated section "Power consumption operating behaviors".</li> <li>Updated section "Flash timing specifications — program and erase".</li> <li>Updated section "Flash timing specifications — commands".</li> <li>Removed the 32K ratio from "Write endurance" in section "Reliability specifications".</li> </ul>

*Table continues on the next page...*

## Revision History

**Table 41. Revision History (continued)**

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"><li>• Updated IDDstby maximum value in section "VREG electrical specifications".</li><li>• Added the charts in section "Diagram: Typical IDD_RUN operating behavior".</li></ul>
3	8/2012	<ul style="list-style-type: none"><li>• Updated section "Power consumption operating behaviors".</li><li>• Updated section "EMC radiated emissions operating behaviors".</li><li>• Updated section "MCG specifications".</li><li>• Added applicable notes in section "Signal Multiplexing and Pin Assignments".</li></ul>
4	12/2012	<ul style="list-style-type: none"><li>• Updated section "Power consumption operating behaviors"</li><li>• Updated section "MCG specifications"</li><li>• Updated section "16-bit ADC operating conditions"</li><li>• Added section "Small package marking"</li></ul>
5	01/2014	<ul style="list-style-type: none"><li>• Updated supported part numbers.</li><li>• Updated section "Power mode transition operating behaviors"</li><li>• Updated section "MCG specifications"</li><li>• Updated section "Oscillator DC electrical specifications"</li><li>• Updated section "Oscillator frequency specifications"</li></ul>
6	03/2014	<ul style="list-style-type: none"><li>• Initial public release</li></ul>





**How to Reach Us:**

**Home Page:**

[freescale.com](http://freescale.com)

**Web Support:**

[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. Freescale reserves the right to make changes without further notice to any products herein.

Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale, Freescale logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere.

©2012-2014 Freescale Semiconductor, Inc.

Document number:  
K11P121M50SF4V2  
Revision 6, 04/2014

