STM32F038x6

ARM®-based 32-bit MCU with 32 Kbyte Flash, timers, ADC and communication interfaces, 1.8 V

Datasheet - production data

Features

- Core: ARM® 32-bit Cortex®-M0 CPU, frequency up to 48 MHz
- Memories
  - 32 Kbytes of Flash memory
  - 4 Kbytes of SRAM with HW parity
- CRC calculation unit
- Power management
  - Digital and I/Os supply: V_{DD} = 1.8 V ±8%
  - Analog supply: V_{DDA} = from V_{DD} to 3.6 V
  - Low power modes: Sleep, Stop
  - V_{BAT} supply for RTC and backup registers
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Up to 39 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 25 I/Os with 5 V tolerant capability
- 5-channel DMA controller
- 1 × 12-bit, 1.0 µs ADC (up to 10 channels)
  - Conversion range: 0 to 3.6V
  - Separate analog supply from 2.4 up to 3.6 V
- Up to 9 timers
  - 1 x 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - 1 x 32-bit and 1 x 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - 1 x 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - 1 x 16-bit timer, with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - 1 x 16-bit timer with 1 IC/OC
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
- Calendar RTC with alarm and periodic wakeup from Stop
- Communication interfaces
  - 1 x I^2C interface; supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, and wakeup from Stop mode
  - 1 x USART supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA capability auto baud rate detection and wakeup feature
  - 1 x SPI (18 Mbit/s) with 4 to 16 programmable bit frames, with I^2S interface multiplexed
- Serial wire debug (SWD)
- 96-bit unique ID
- Extended temperature range: -40 to +105°C
- All packages ECOPACK®2

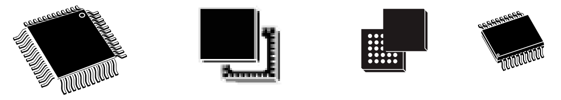
LQFP48 7x7 mm
UFQFPN32 5x5 mm
UFQFPN28 4x4 mm
WLCSP25
(2.1x2.1 mm)
TSSOP20

Table 1. Device summary

Reference	Part number
STM32F038x6	STM32F038C6, STM32F038E6, STM32F038F6, STM32F038G6, STM32F038K6

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F038x6 microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F038x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at a 48 MHz maximum frequency, high-speed embedded memories (32 Kbytes of Flash memory and 4 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I2C, one SPI/ I2S and one USART), one 12-bit ADC, five 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F038x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges at a 1.8 V ± 8% power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F038x6 microcontrollers include devices in five different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F038x6 peripherals proposed.

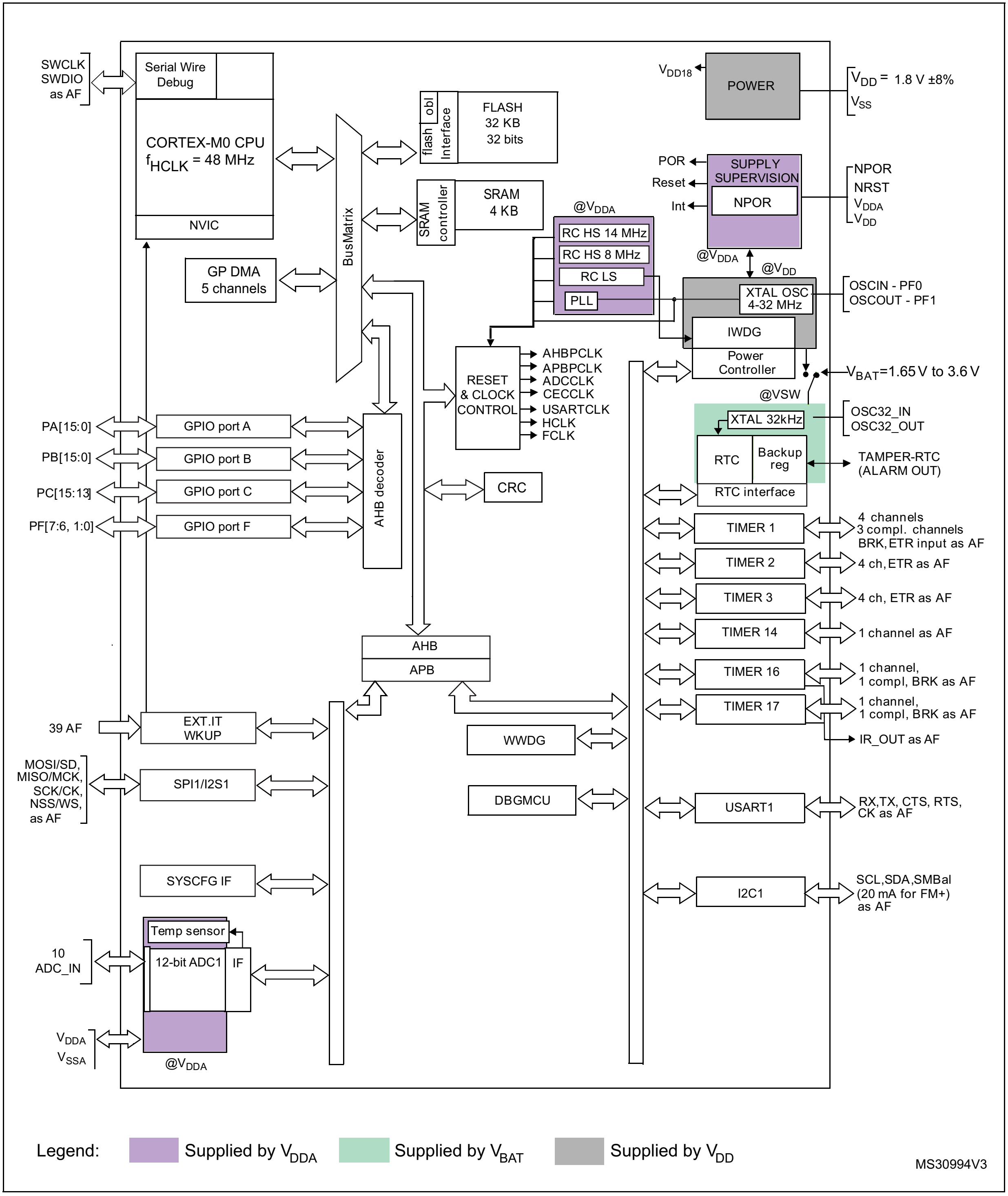
These features make the STM32F038x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F038x6 family device features and peripheral counts

Peripheral		STM32F038Fx	STM32F038Ex	STM32F038Gx	STM32F038Kx	STM32F038Cx
Flash (Kbyte)		32				
SRAM (Kbyte)		4				
Timers	Advanced control	1 (16-bit)				
	General purpose	4 (16-bit) 1 (32-bit)				
Comm. interfaces	SPI [I2S][1]	1 [1]				
	I^2C	1				
	USART	1				
12-bit ADC (number of channels)		1 (8 ext. + 3 int.)	1 (9 ext. + 3 int.)		1 (10 ext. + 3 int.)	
GPIOs		14	19	22	26	38
Max. CPU frequency		48 MHz				
Operating voltage		V_{DD} = 1.8 V ± 8%, V_{DDA} = from V_{DD} to 3.6 V				
Operating temperature		Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C				
Packages		TSSOP20	WLCSP25	UFQFPN28	UFQFPN32	LQFP48

1. The SPI interface can be used either in SPI mode or in I2S audio mode.

Figure 1. Block diagram



3 Functional overview

3.1 ARM®-Cortex®-M0 core with embedded Flash and SRAM

The ARM® Cortex®-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 4 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1}$ = 1.8 V ± 8%: external power supply for I/Os (V_{DDIO1}) and digital logic. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 11: Power supply scheme*.

3.5.2 Power-on reset

To guarantee a proper power-on reset, the NPOR pin must be held low until V_{DD} is stable. When V_{DD} is stable, the reset state can be exited either by:

- putting the NPOR pin in high impedance (NPOR pin has an internal pull-up), or by
- forcing the pin to high level by connecting it to V_{DDA}.

3.5.3 Low-power modes

The STM32F038x6 microcontrollers support two low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, RTC, I2C1 or USART1.

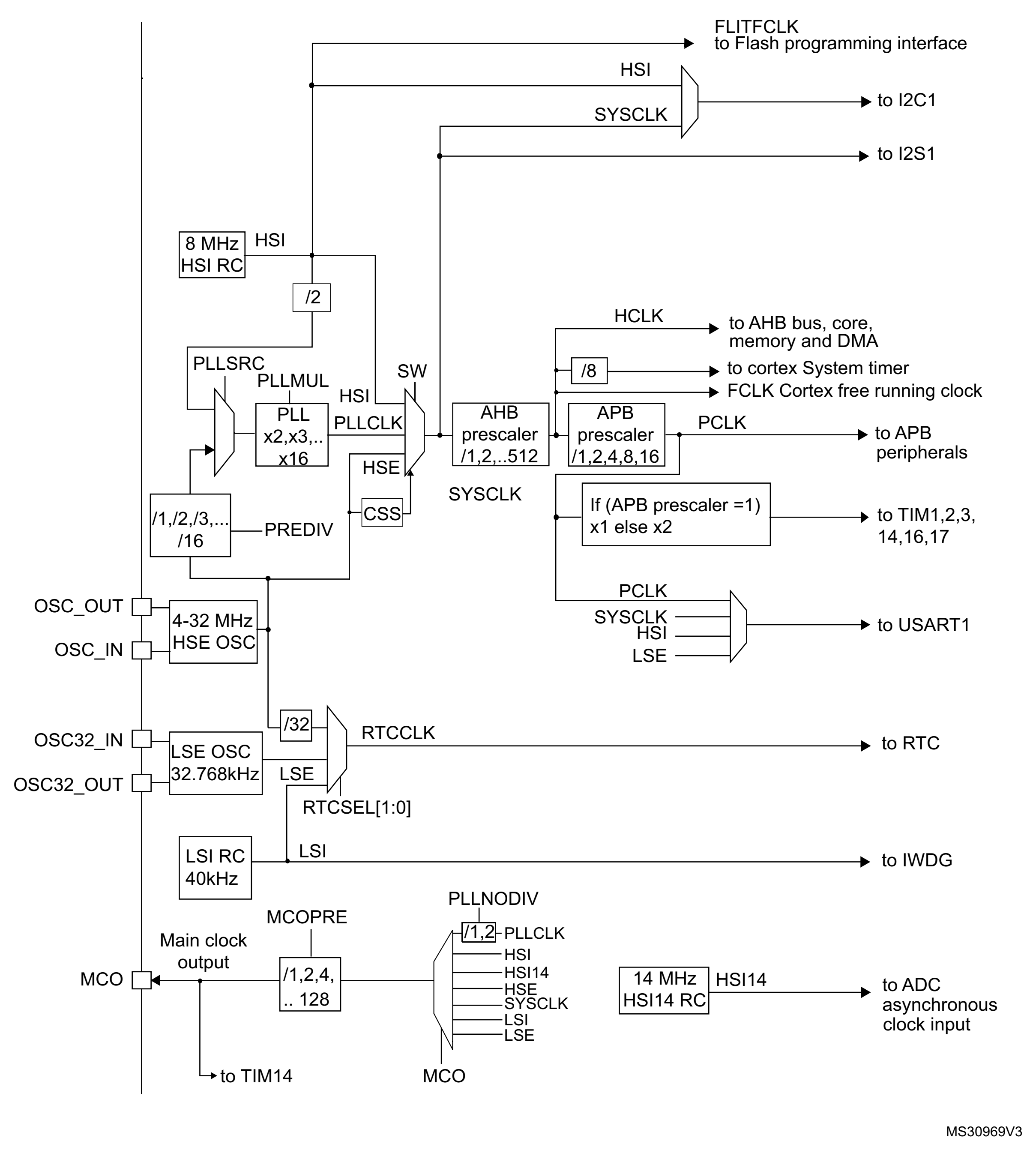
Note: *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop mode.*

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Figure 2. Clock tree



3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 39 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 10 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), V_{DDA}= 3.3 V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Timers and watchdogs

The STM32F038x6 devices include up to five general-purpose timers and an advanced control timer.

Table 5 compares the features of the different timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1

3.11.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.11.2 General-purpose timers (TIM2..3, TIM14, 16, 17)

There are six synchronizable general-purpose timers embedded in the STM32F038x6 devices (see *Table 5* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F038x6 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM16 and TIM17

Both timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

They each have a single channel for input capture/output compare, PWM or one-pulse mode output.

TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.11.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop mode. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.11.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.11.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.12 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop mode on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop mode on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.13 Inter-integrated circuit interfaces (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with extra output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interface can be served by the DMA controller.

Table 7. STM32F038x6 I^2C implementation

I2C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.14 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds one universal synchronous/asynchronous receiver transmitter (USART1), which communicate at speeds of up to 6 Mbit/s.

It provides hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interface can be served by the DMA controller.

3.15 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

The SPI is able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 8. STM32F038x6 SPI/I2S implementation

SPI features(1)	SPI
Hardware CRC calculation	X
Rx/Tx FIFO	X
NSS pulse mode	X
I2S mode	X
TI mode	X

1. X = supported.

3.16 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin description

Figure 3. LQFP48 48-pin package pinout

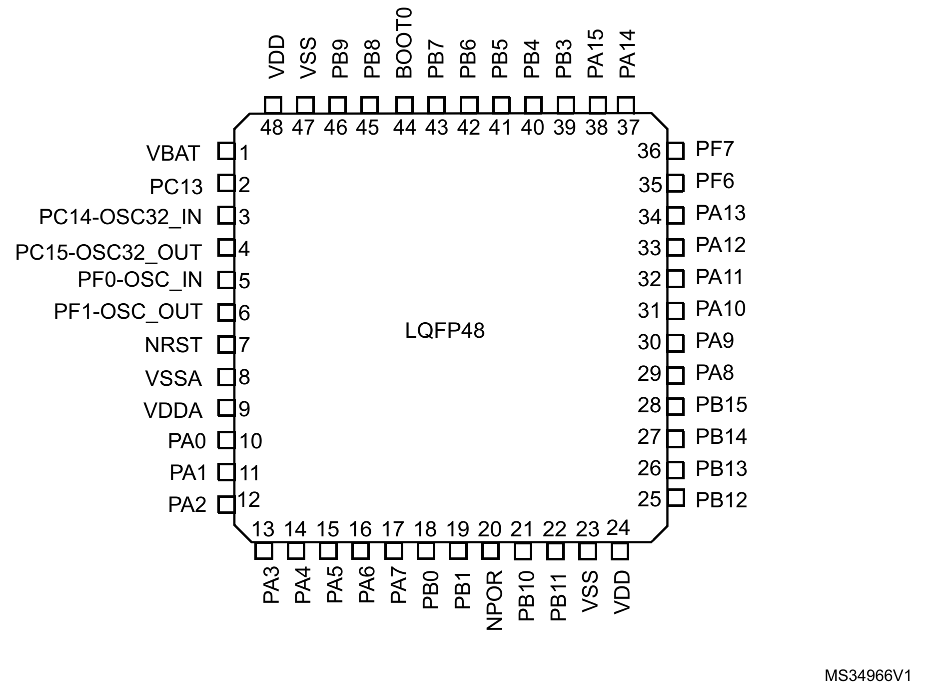


Figure 4. UFQFPN32 32-pin package pinout

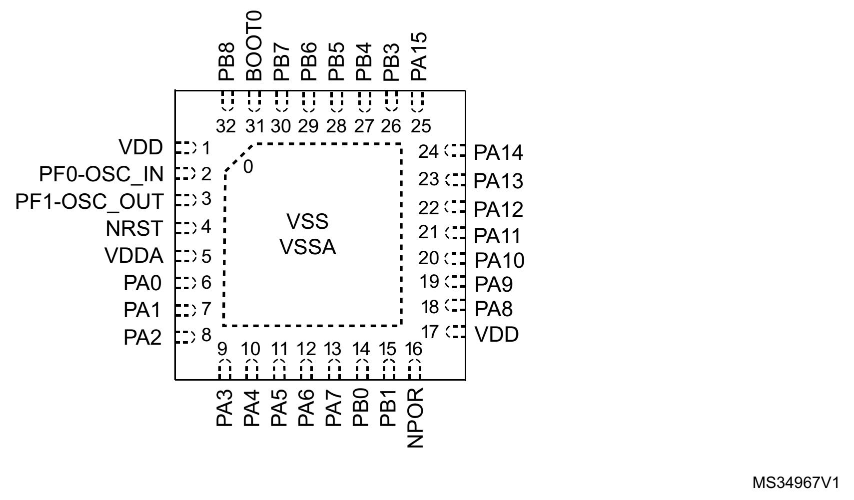


Figure 5. UFQFPN28 28-pin package pinout

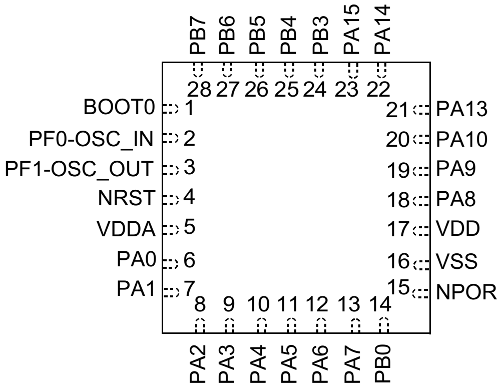
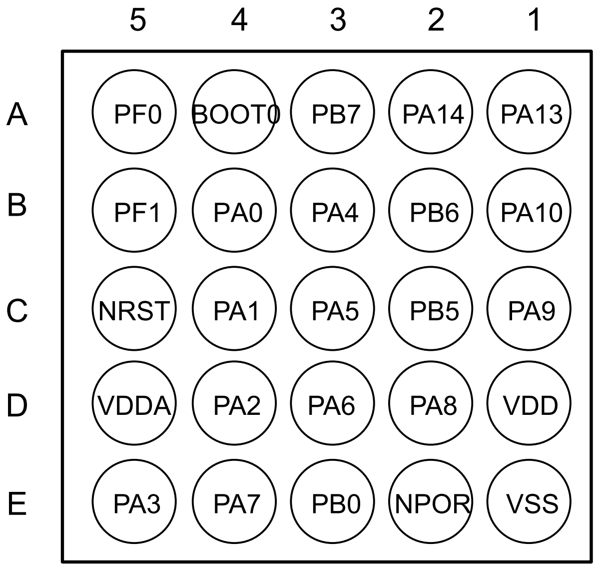


Figure 6. WLCSP25 25-ball package ballout (bump side)



	5	4	3	2	1
A	PF0	BOOT0	PB7	PA14	PA13
B	PF1	PA0	PA4	PB6	PA10
C	NRST	PA1	PA5	PB5	PA9
D	VDDA	PA2	PA6	PA8	VDD
E	PA3	PA7	PB0	NPOR	VSS

Figure 7. TSSOP20 20-pin package pinout

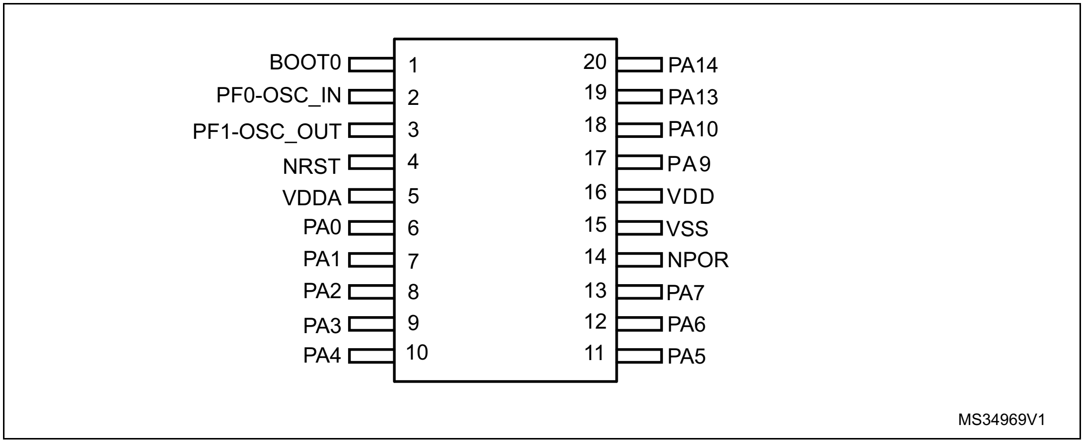


Table 9. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		POR	External power on reset pin with embedded weak pull-up resistor, powered from V_{DDA}
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 10. Pin definitions

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
1	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	-	-	-	-	PC13	I/O	TC	(1)(2)	-	RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)	-	OSC32_IN
4	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)	-	OSC32_OUT

Table 10. Pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	**UFQFPN32**	**UFQFPN28**	**WLCSP25**	**TSSOP20**					**Alternate functions**	**Additional functions**
5	2	2	A5	2	PF0-OSC_IN (PF0)	I/O	FT	-	-	OSC_IN
6	3	3	B5	3	PF1-OSC_OUT (PF1)	I/O	FT	-	-	OSC_OUT
7	4	4	C5	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	0	-	E1	-	VSSA	S		-	Analog ground	
9	5	5	D5	5	VDDA	S		-	Analog power supply	
10	6	6	B4	6	PA0	I/O	TTa	-	TIM2_CH1_ETR, USART1_CTS	ADC_IN0, RTC_TAMP2, WKUP1
11	7	7	C4	7	PA1	I/O	TTa	-	TIM2_CH2, EVENTOUT, USART1_RTS	ADC_IN1
12	8	8	D4	8	PA2	I/O	TTa	-	TIM2_CH3, USART1_TX	ADC_IN2
13	9	9	E5	9	PA3	I/O	TTa	-	TIM2_CH4, USART1_RX	ADC_IN3
14	10	10	B3	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, USART1_CK	ADC_IN4
15	11	11	C3	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, TIM2_CH1_ETR	ADC_IN5
16	12	12	D3	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, EVENTOUT	ADC_IN6

Table 10. Pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
17	13	13	E4	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, EVENTOUT	ADC_IN7
18	14	14	E3	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, EVENTOUT	ADC_IN8
19	15	-	-	-	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N	ADC_IN9
20	16	15	E2	14	NPOR	I	POR	(3)	Device power-on reset input	
21	-	-	-	-	PB10	I/O	FTf	-	TIM2_CH3, I2C1_SCL	-
22	-	-	-	-	PB11	I/O	FTf	-	TIM2_CH4, EVENTOUT, I2C1_SDA	-
23	0	16	E1	15	VSS	S	-	-	Ground	
24	17	17	D1	16	VDD	S	-	-	Digital power supply	
25	-	-	-	-	PB12	I/O	FT	-	TIM1_BKIN, EVENTOUT, SPI1_NSS	-
26	-	-	-	-	PB13	I/O	FT	-	TIM1_CH1N, SPI1_SCK	-
27	-	-	-	-	PB14	I/O	FT	-	TIM1_CH2N, SPI1_MISO	-
28	-	-	-	-	PB15	I/O	FT	-	TIM1_CH3N, SPI1_MOSI	RTC_REFIN
29	18	18	D2	-	PA8	I/O	FT	-	USART1_CK, TIM1_CH1, EVENTOUT, MCO	-

Table 10. Pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
30	19	19	C1	17	PA9	I/O	FTf	-	USART1_TX, TIM1_CH2, I2C1_SCL	-
31	20	20	B1	18	PA10	I/O	FTf	-	USART1_RX, TIM1_CH3, TIM17_BKIN, I2C1_SDA	-
32	21	-	-	-	PA11	I/O	FT	-	USART1_CTS, TIM1_CH4, EVENTOUT	-
33	22	-	-	-	PA12	I/O	FT	-	USART1_RTS, TIM1_ETR, EVENTOUT	-
34	23	21	A1	19	PA13 (SWDIO)	I/O	FT	(4)	IR_OUT, SWDIO	-
35	-	-	-	-	PF6	I/O	FTf	-	I2C1_SCL	-
36	-	-	-	-	PF7	I/O	FTf	-	I2C1_SDA	-
37	24	22	A2	20	PA14 (SWCLK)	I/O	FT	(4)	USART1_TX, SWCLK	-
38	25	23	-	-	PA15	I/O	FT	-	SPI1_NSS, I2S1_WS, TIM2_CH_ETR, EVENTOUT, USART1_RX	-
39	26	24	-	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, EVENTOUT	-
40	27	25	-	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, EVENTOUT	-

Table 10. Pin definitions (continued)

Pin number					Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN32	UFQFPN28	WLCSP25	TSSOP20					Alternate functions	Additional functions
41	28	26	C2	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	-
42	29	27	B2	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N	-
43	30	28	A3	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N	-
44	31	1	A4	1	BOOT0	I	B	-	Boot memory selection	
45	32	-	-	-	PB8	I/O	FTf	-	I2C1_SCL, TIM16_CH1	-
46	-	-	-	-	PB9	I/O	FTf	-	I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	-
47	0	-	E1	-	VSS	S	-	-	Ground	
48	1	-	-	-	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. These pins are powered by V_{DDA}.
4. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 11. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART1_CTS	TIM2_CH1_ ETR	-	-	-	-	-
PA1	EVENTOUT	USART1_RTS	TIM2_CH2	-	-	-	-	-
PA2	-	USART1_TX	TIM2_CH3	-	-	-	-	-
PA3	-	USART1_RX	TIM2_CH4	-	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART1_CK	-	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	-	TIM2_CH1_ ETR	-	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	-	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	-	USART1_TX	TIM1_CH2	-	I2C1_SCL	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	-	-	-
PA13	SWDIO	IR_OUT	-	-	-	-	-	-
PA14	SWCLK	USART1_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART1_RX	TIM2_CH1_ ETR	EVENTOUT	-	-	-	-

Table 12. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-
PB2	-	-	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	-
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	-
PB8	-	I2C1_SCL	TIM16_CH1	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	-	I2C1_SCL	TIM2_CH3	-
PB11	EVENTOUT	I2C1_SDA	TIM2_CH4	-
PB12	SPI1_NSS	EVENTOUT	TIM1_BKIN	-
PB13	SPI1_SCK	-	TIM1_CH1N	-
PB14	SPI1_MISO	-	TIM1_CH2N	-
PB15	SPI1_MOSI	-	TIM1_CH3N	-

5 Memory mapping

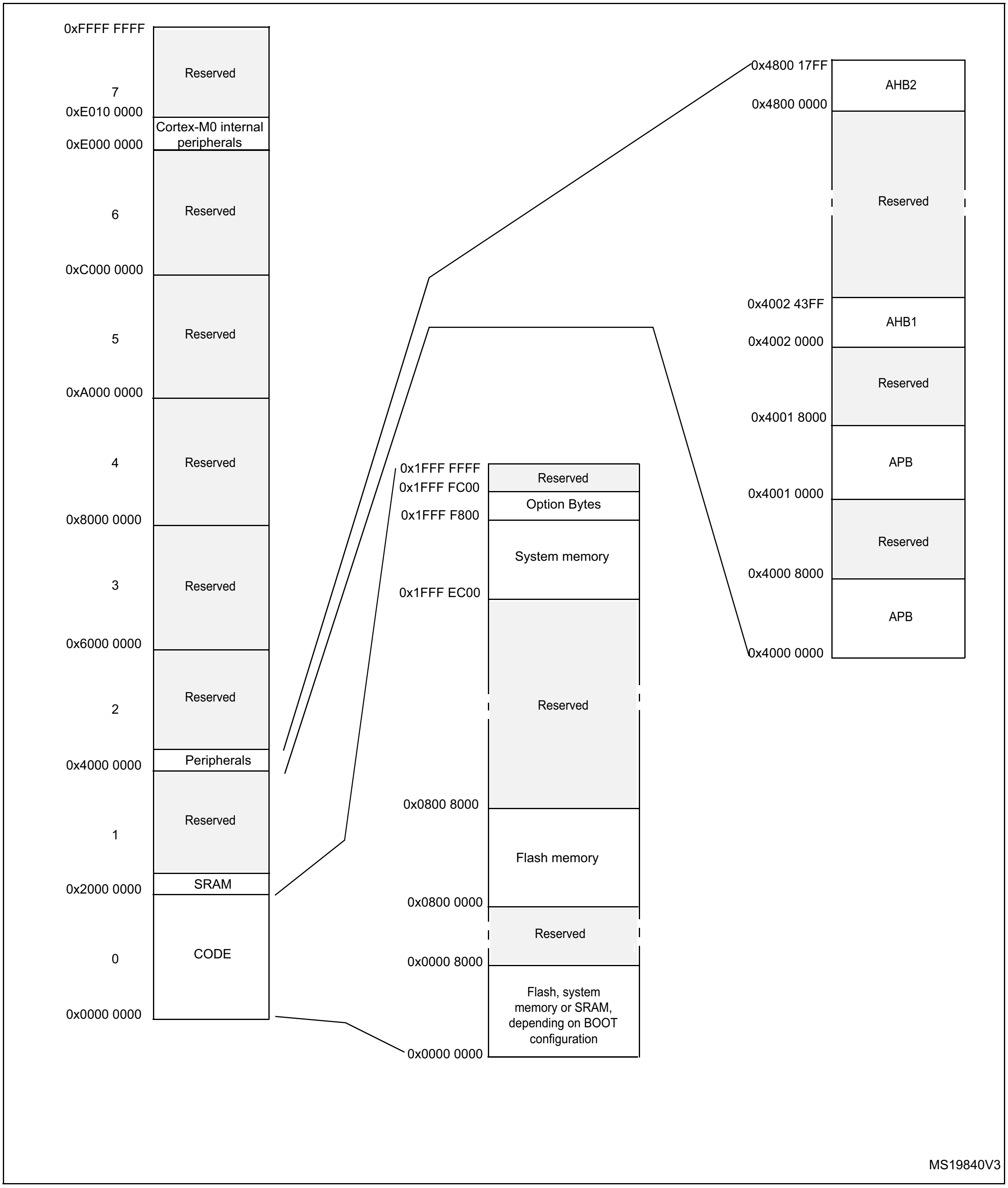


Figure 8. STM32F038x6 memory map

Table 13. STM32F038x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 13. STM32F038x6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7400 - 0x4000 7FFF	3KB	Reserved
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5800 - 0x4000 6FFF	6KB	Reserved
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 3400 - 0x4000 53FF	8KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and $T_A = T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 1.8 V and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

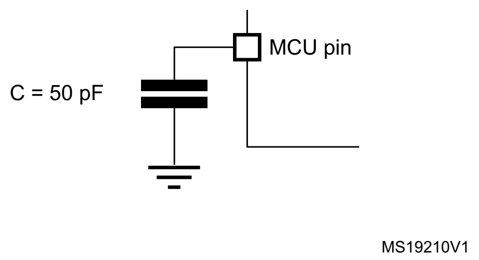
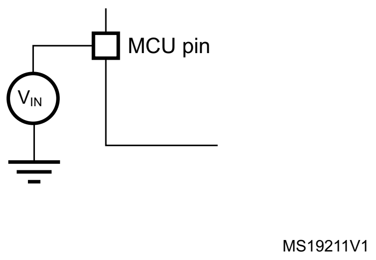
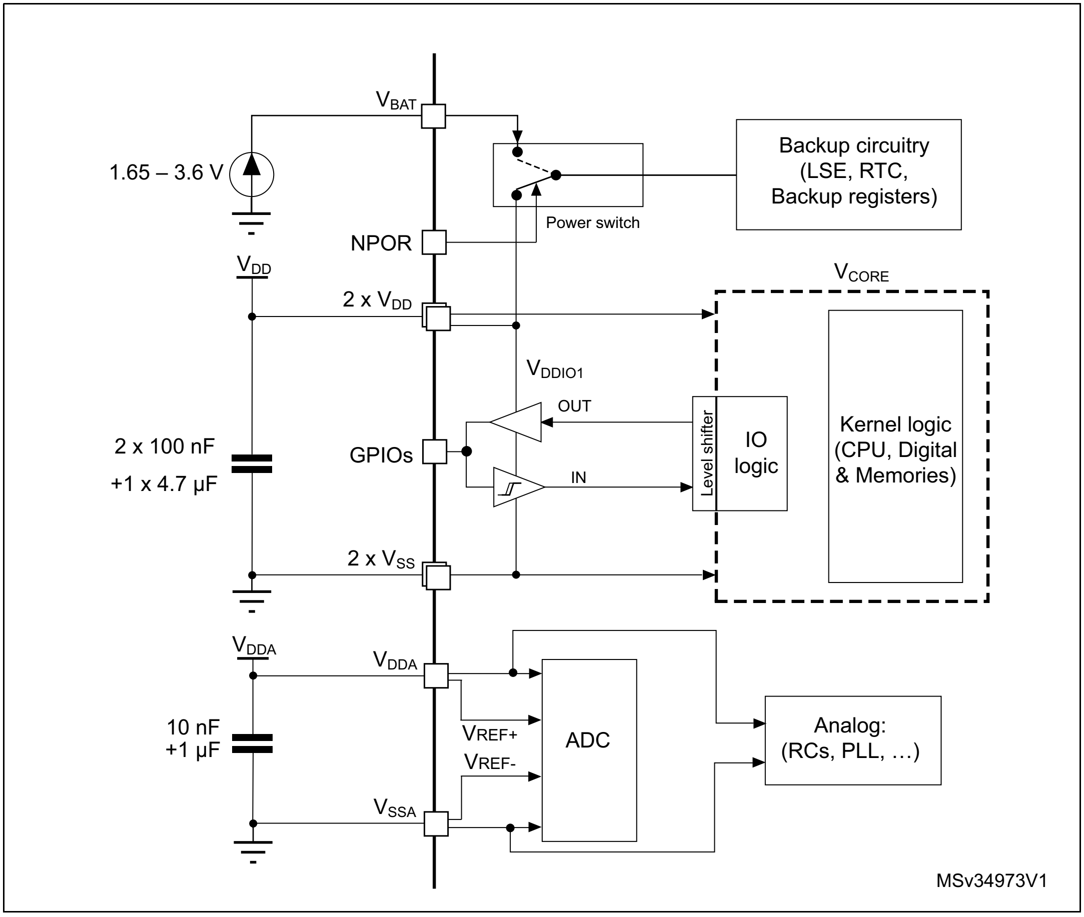


Figure 10. Pin input voltage



6.1.6 Power supply scheme

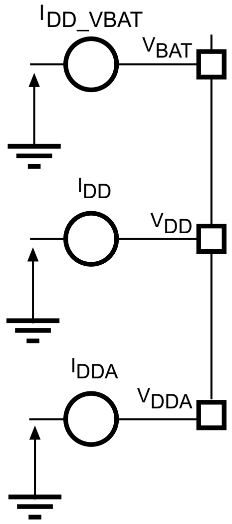
Figure 11. Power supply scheme



Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 14: Voltage characteristics*, *Table 15: Current characteristics* and *Table 16: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics[1]

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	-0.3	1.95	V
V_{DDA}–V_{SS}	External analog supply voltage	-0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{BAT}–V_{SS}	External backup supply voltage	-0.3	4.0	V
V_{IN}[2]	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DDIOx} + 4.0 [3]	V
	Input voltage on POR pins	V_{SS} – 0.3	4.0	V
	Input voltage on TTa pins	V_{SS} – 0.3	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	V_{SS} – 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.11: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 15: Current characteristics*for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
$I_{INJ(PIN)}$(3)	Injected current on POR, B, FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 14: Voltage characteristics* for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note (2) below *Table 50: ADC accuracy*.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	1.65	1.95	V
V_{DDA}	Analog operating voltage (ADC not used)	Must have a potential equal to or higher than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	–0.3	V_{DDIOx}+0.3	V
		TTa and POR I/O	–0.3	V_{DDA}+0.3(1)	
		FT and FTf I/O	–0.3	5.2(1)	
		BOOT0	0	5.2	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP48	-	364	mW
		UFQFPN32	-	526	
		UFQFPN28	-	169	
		WLCSP25	-	267	
		TSSOP20	-	182	
TA	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
TJ	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version	–40	125	

1. For operation with a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up resistor must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}. See *Section 7.6: Thermal characteristics*.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.6: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 18* are derived from tests performed under the ambient temperature condition summarized in *Table 17*.

Table 18. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reference voltage

The parameters given in *Table 19* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 19. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(1)	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(2)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(2)	mV
T_{Coeff}	Temperature coefficient	-	- 100(2)	-	100(2)	ppm/°C
$T_{VREFINT\_RDY}$(3)	Internal reference voltage temporization	-	1.5	2.5	4.5	ms

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. Guaranteed by design, not tested in production. This parameter is the latency between the time when pin NPOR is set to 1 by the application and the time when the VREFINTRDYF status bit is set to 1 by the hardware.

6.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 12: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 20* to *Table 24* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 20. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 1.8 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash	External clock (HSE bypass)	48 MHz	18.2	19.7	20.1	20.3	11.2	11.7	12.1	12.4	mA
			32 MHz	12.4	13.1	13.4	13.6	7.6	8.2	8.3	8.6	
			24 MHz	9.8	10.4	10.6	10.7	6.1	6.6	6.7	6.8	
			8 MHz	3.3	3.7	3.8	3.8	2.2	2.4	2.5	2.6	
			1 MHz	0.7	0.8	0.9	1.0	0.5	0.6	0.7	0.7	
		Internal clock (HSI)	48 MHz	18.5	20.0	20.4	20.6	11.6	12.1	12.4	12.8	
			32 MHz	12.7	13.4	13.6	14.0	7.9	8.5	8.7	9.0	
			24 MHz	10.0	10.6	10.8	10.9	6.2	6.7	6.8	6.9	
			8 MHz	3.4	3.8	3.9	4.0	2.3	2.5	2.6	2.6	
	Supply current in Run mode, code executing from RAM	External clock (HSE bypass)	48 MHz	17.2	18.7	19.1	19.3	10.2	10.6	11.1	11.4	
			32 MHz	11.4	12.2	12.4	12.7	6.7	7.2	7.4	7.6	
			24 MHz	8.9	9.4	9.6	9.7	5.1	5.5	5.7	5.7	
			8 MHz	2.8	3.2	3.3	3.3	1.7	2.0	2.0	2.1	
			1 MHz	0.3	0.5	0.5	0.5	0.2	0.3	0.3	0.3	
		Internal clock (HSI)	48 MHz	17.5	19.0	19.4	19.6	10.4	10.8	11.2	11.6	
			32 MHz	11.7	12.4	12.7	12.9	6.9	7.4	7.6	7.8	
			24 MHz	9.1	9.6	9.8	9.9	5.2	5.6	5.7	5.8	
			8 MHz	3.0	3.3	3.4	3.5	1.7	2.0	2.1	2.1	
	Supply current in Sleep mode, code executing from Flash or RAM	External clock (HSE bypass)	48 MHz	10.4	11.7	12.0	12.3	2.4	2.6	2.7	2.8	
			32 MHz	6.9	7.6	7.8	8.1	1.5	1.7	1.8	1.9	
			24 MHz	5.4	5.9	6.1	6.2	1.2	1.3	1.4	1.5	
			8 MHz	1.7	2.2	2.3	2.4	0.4	0.4	0.5	0.5	
			1 MHz	0.3	0.3	0.4	0.4	0.1	0.1	0.2	0.2	
		Internal clock (HSI)	48 MHz	10.6	11.8	12.1	12.4	2.4	2.7	2.7	2.8	
			32 MHz	7.2	7.9	8.1	8.3	1.6	1.8	1.9	2.0	
			24 MHz	5.5	6.1	6.3	6.4	1.3	1.4	1.5	1.5	
			8 MHz	1.9	2.4	2.5	2.6	0.5	0.5	0.5	0.6	

1. Data based on characterization results, not tested in production unless otherwise specified.

Table 21. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Parameter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash or RAM	HSE bypass, PLL on	48 MHz	147	170	180	184	160	183	195	199	µA
			32 MHz	101	121	127	129	109	129	137	140	
			24 MHz	79	97	101	103	86	104	110	112	
		HSE bypass, PLL off	8 MHz	1	3	3	3	2	3	3	4	
			1 MHz	1	2	2	2	2	2	3	3	
		HSI clock, PLL on	48 MHz	219	243	256	260	240	267	279	284	
			32 MHz	172	195	203	206	190	210	222	226	
			24 MHz	150	170	177	180	165	186	193	196	
		HSI clock, PLL off	8 MHz	71	83	87	88	81	95	97	98	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.

Table 22. Typical and maximum consumption in Stop mode

Symbol	Parameter	Conditions	Typ. @ V_{DD} = 1.8 V							Max			Unit
			V_{DDA} = 1.8 V	V_{DDA} = 2.0 V	V_{DDA} = 2.4 V	V_{DDA} = 2.7 V	V_{DDA} = 3.0 V	V_{DDA} = 3.3 V	V_{DDA} = 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	All oscillators OFF	0.4							2.3	14.9	35.6	µA
I_{DDA}			0.8	0.8	0.8	0.9	0.9	1.0	1.1	1.5	2.6	3.4	

Table 23. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V_{BAT}						Max(1)			Unit
			= 1.65 V	= 1.8 V	= 2.4 V	= 2.7 V	= 3.3 V	= 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	RTC domain supply current	LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00'	0.47	0.49	0.59	0.65	0.80	0.91	1.0	1.3	1.7	µA
		LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11'	0.76	0.79	0.88	0.98	1.13	1.21	1.3	1.6	2.1	

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 1.8$ V
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 24. Typical current consumption, code executing from Flash, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from V_{DD} supply	48 MHz	18.5	11.6	10.8	2.6	mA
		36 MHz	14.1	8.9	8.2	2.0	
		32 MHz	12.7	8.1	7.3	1.8	
		24 MHz	9.7	6.2	5.6	1.4	
		16 MHz	6.7	4.3	3.9	1.1	
		8 MHz	3.4	2.3	1.9	0.6	
		4 MHz	2.1	1.4	1.3	0.5	
		2 MHz	1.3	0.9	0.9	0.5	
		1 MHz	0.9	0.7	0.7	0.4	
		500 kHz	0.7	0.6	0.6	0.4	
I_{DDA}	Current consumption from V_{DDA} supply	48 MHz	136				µA
		36 MHz	105				
		32 MHz	96				
		24 MHz	76				
		16 MHz	56				
		8 MHz	1				
		4 MHz	1				
		2 MHz	1				
		1 MHz	1				
		500 kHz	1				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 43: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 26: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
V_{DDIOx} is the I/O supply voltage
f_{SW} is the I/O switching frequency
C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 25. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 1.8 V C_{EXT} = 0 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.09	mA
			4 MHz	0.17	
			8 MHz	0.34	
			18 MHz	0.79	
			36 MHz	1.50	
			48 MHz	2.06	
		V_{DDIOx} = 1.8 V C_{EXT} = 10 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.13	
			4 MHz	0.26	
			8 MHz	0.50	
			18 MHz	1.18	
			36 MHz	2.27	
			48 MHz	3.03	
		V_{DDIOx} = 1.8 V C_{EXT} = 22 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.18	
			4 MHz	0.36	
			8 MHz	0.69	
			18 MHz	1.60	
			36 MHz	3.27	
		V_{DDIOx} = 1.8 V C_{EXT} = 33 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.23	
			4 MHz	0.45	
			8 MHz	0.87	
			18 MHz	2.0	
			36 MHz	3.7	
		V_{DDIOx} = 1.8 V C_{EXT} = 47 pF $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.29	
			4 MHz	0.55	
			8 MHz	1.09	
			18 MHz	2.43	

1. C_S = 5 pF (estimated value).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 26*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 14: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in*Table 26*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 26. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix[(1)]	3.8	µA/MHz
	DMA1	6.3	
	SRAM	0.7	
	Flash interface	15.2	
	CRC	1.61	
	GPIOA	9.4	
	GPIOB	11.6	
	GPIOC	1.9	
	GPIOF	0.8	
	All AHB peripherals	**47.5**	

Table 26. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge (2)	2.6	µA/MHz
	SYSCFG	1.7	
	ADC (3)	4.2	
	TIM1	17.1	
	SPI1	9.6	
	USART1	17.4	
	TIM16	8.2	
	TIM17	8.0	
	DBG (MCU Debug Support)	0.5	
	TIM2	17.4	
	TIM3	12.8	
	TIM14	6.0	
	WWDG	1.5	
	I2C1	5.1	
	PWR	1.2	
	All APB peripherals	**110.9**	

1. The BusMatrix automatically is active when at least one master is ON (CPU or DMA1).
2. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.5 Wakeup time from low-power mode

The wakeup times given in *Table 27* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode.

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*..

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Typ @ V_{DDA}		Max	Unit
		= 1.8 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	3.5	2.8	5.3	µs
$t_{WUSLEEP}$	Wakeup from Sleep mode	4 SYSCLK cycles		-	µs

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

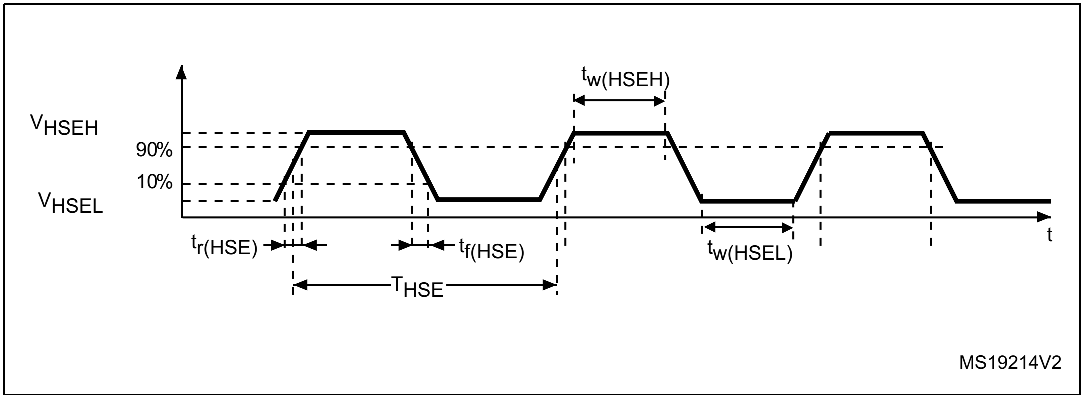
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 13: High-speed external clock source AC timing diagram*.

Table 28. High-speed external user clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

1. Guaranteed by design, not tested in production.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

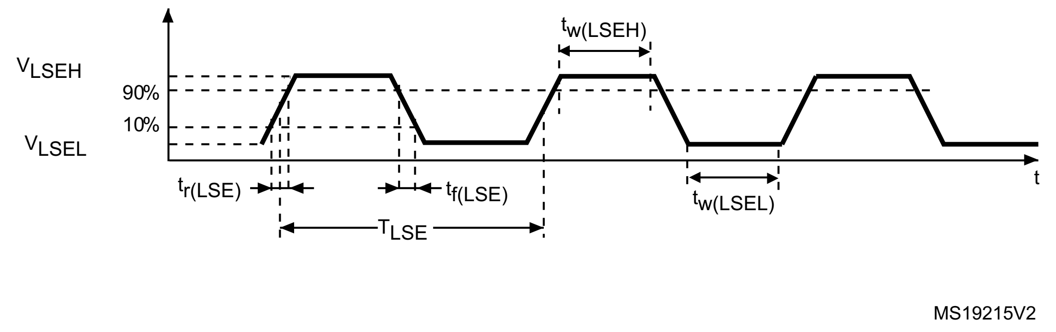
The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 29. Low-speed external user clock characteristics

Symbol	Parameter[1]	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 14. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 30*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 30. HSE oscillator characteristics

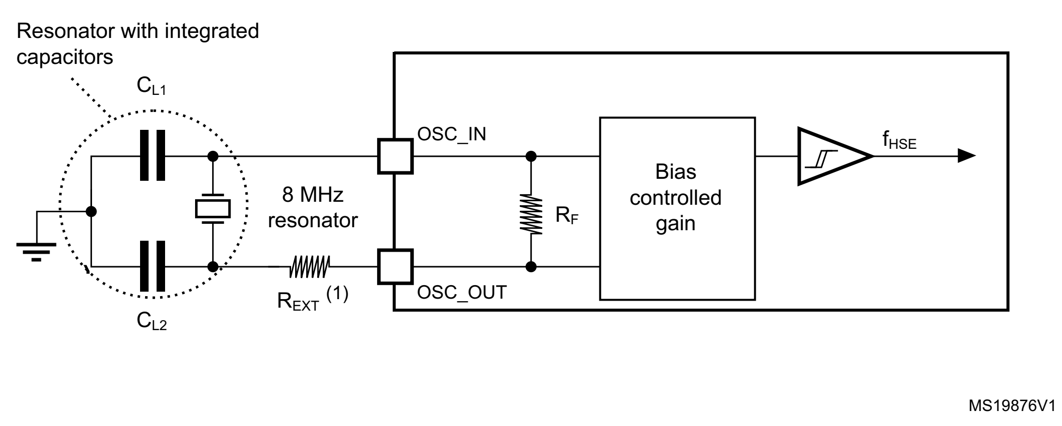
Symbol	Parameter	Conditions[1]	Min[2]	Typ	Max[2]	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	32	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
I_{DD}	HSE current consumption	During startup[3]	-		8.5	mA
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.4	-	
		V_{DD} = 1.8 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.5	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 5 pF@32 MHz	-	0.8	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 10 pF@32 MHz	-	1	-	
		V_{DD} = 1.8 V, Rm = 30 Ω, CL = 20 pF@32 MHz	-	1.5	-	
g_m	Oscillator transconductance	Startup	10	-	-	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 15*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 15. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 31*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

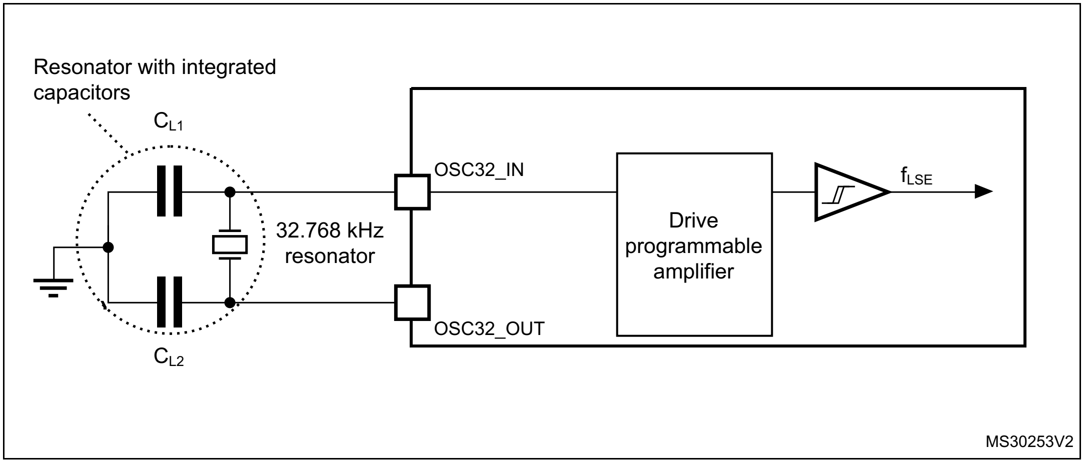
Table 31. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	LSEDRV[1:0]=00 lower driving capability	-	0.5	0.9	µA
		LSEDRV[1:0]= 01 medium low driving capability	-	-	1	
		LSEDRV[1:0] = 10 medium high driving capability	-	-	1.3	
		LSEDRV[1:0]=11 higher driving capability	-	-	1.6	
g_m	Oscillator transconductance	LSEDRV[1:0]=00 lower driving capability	5	-	-	µA/V
		LSEDRV[1:0]= 01 medium low driving capability	8	-	-	
		LSEDRV[1:0] = 10 medium high driving capability	15	-	-	
		LSEDRV[1:0]=11 higher driving capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 16. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.7 Internal clock source characteristics

The parameters given in *Table 32* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*. The provided curves are characterization results, not tested in production.

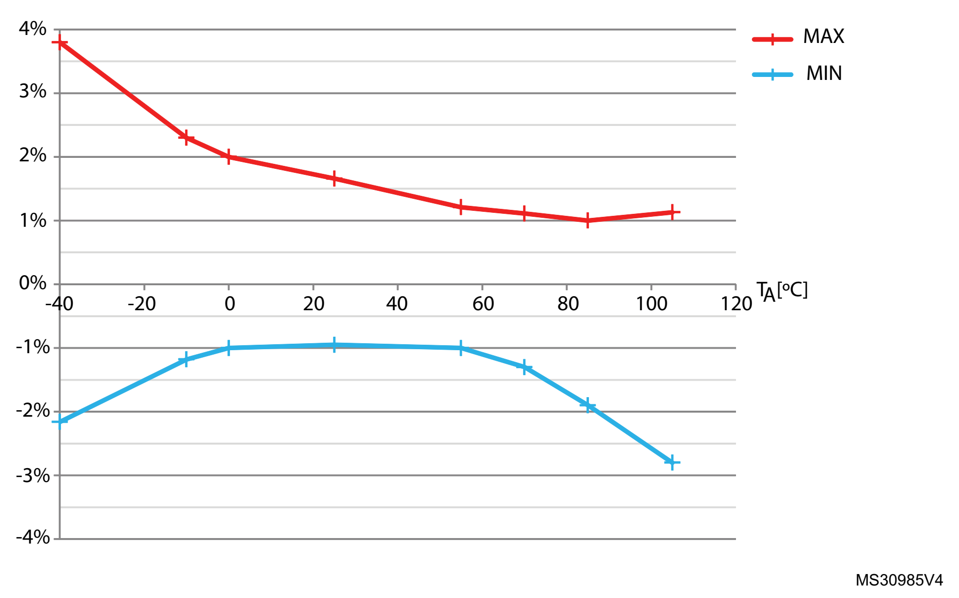
High-speed internal (HSI) RC oscillator

Table 32. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 17. HSI oscillator accuracy characterization results for soldered parts



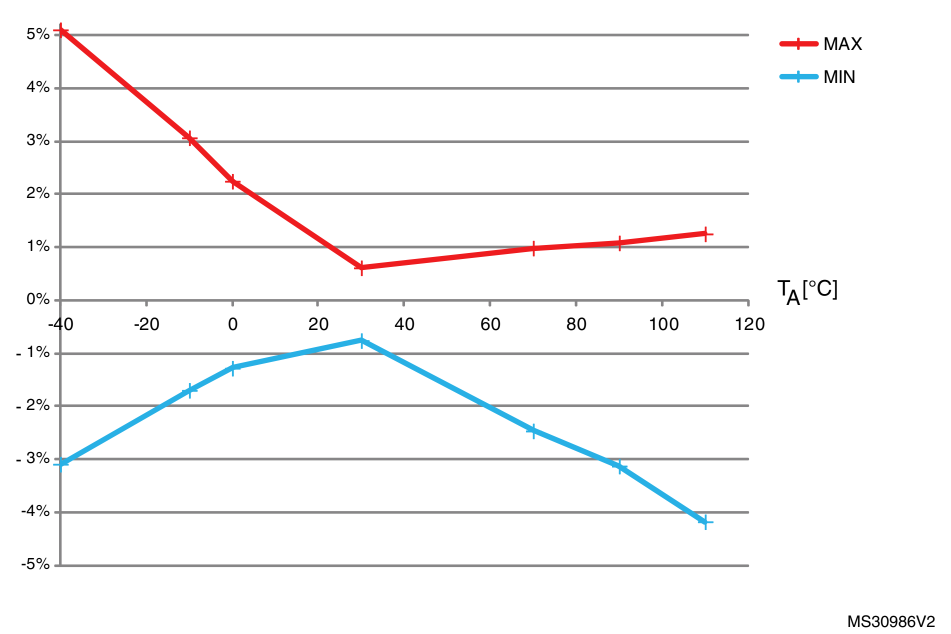
High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 33. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI14}	Frequency	-	-	14	-	MHz
TRIM	HSI14 user-trimming step	-	-	-	1(2)	%
$DuCy_{(HSI14)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	–4.2(3)	-	5.1(3)	%
		T_A = –10 to 85 °C	–3.2(3)	-	3.1(3)	%
		T_A = 0 to 70 °C	–2.5(3)	-	2.3(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI14)}$	HSI14 oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI14)}$	HSI14 oscillator power consumption	-	-	100	150(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 18. HSI14 oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 34. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time	-	-	85	µs
$I_{DDA(LSI)}$(2)	LSI oscillator power consumption	-	0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

6.3.8 PLL characteristics

The parameters given in *Table 35* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 35. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)	8.0	24(2)	MHz
	PLL input clock duty cycle	40(2)	-	60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200(2)	µs
$Jitter_{PLL}$	Cycle-to-cycle jitter	-	-	300(2)	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

6.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 36. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	53.5	60	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Table 37. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycle
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Year
		1 kcycle[2] at T_A = 105 °C	10	
		10 kcycle[2] at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 38*. They are based on the EMS levels and classes defined in application note AN1709.

Table 38. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 1.8 V, LQFP48, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 1.8 V, LQFP48, T_A = +25°C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 39. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	V_{DD} = 1.8 V, T_A = 25 °C, LQFP48 package compliant with IEC 61967-2	0.1 to 30 MHz	-1	dBμV
			30 to 130 MHz	21	
			130 MHz to 1 GHz	27	
			EMI Level	4	-

6.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 40. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	All	C3	250	V

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 41. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

6.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 42*.

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 42. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0	–0	NA	mA
	Injected current on all FT, FTf and POR pins	–5	NA	
	Injected current on all TTa, TC and RESET pins	–5	+5	

6.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under the conditions summarized in *Table 17: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 43. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	0.3 V_{DDIOx}+0.07[1]	V
		FT and FTf I/O	-	-	0.475 V_{DDIOx}–0.2[1]	
		BOOT0	-	-	0.3 V_{DDIOx}–0.3[1]	
		All I/Os except BOOT0 pin	-	-	0.3 V_{DDIOx}	
V_{IH}	High level input voltage	TC and TTa I/O	0.445 V_{DDIOx}+0.398[1]	-	-	V
		FT and FTf I/O	0.5 V_{DDIOx}+0.2[1]	-	-	
		BOOT0	0.2 V_{DDIOx}+0.95[1]	-	-	
		All I/Os except BOOT0 pin	0.7 V_{DDIOx}	-	-	

Table 43. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200[1]	-	mV
		FT and FTf I/O	-	100[1]	-	
		BOOT0	-	300[1]	-	
I_{lkg}	Input leakage current[2]	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O (3) $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (4)	$V_{IN} = V_{SS}$	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor[4]	$V_{IN} = V_{DDIOx}$	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 42: I/O current injection susceptibility*.
3. To sustain a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 19* for standard I/Os, and in *Figure 20* for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 19. TC and TTa I/O input characteristics

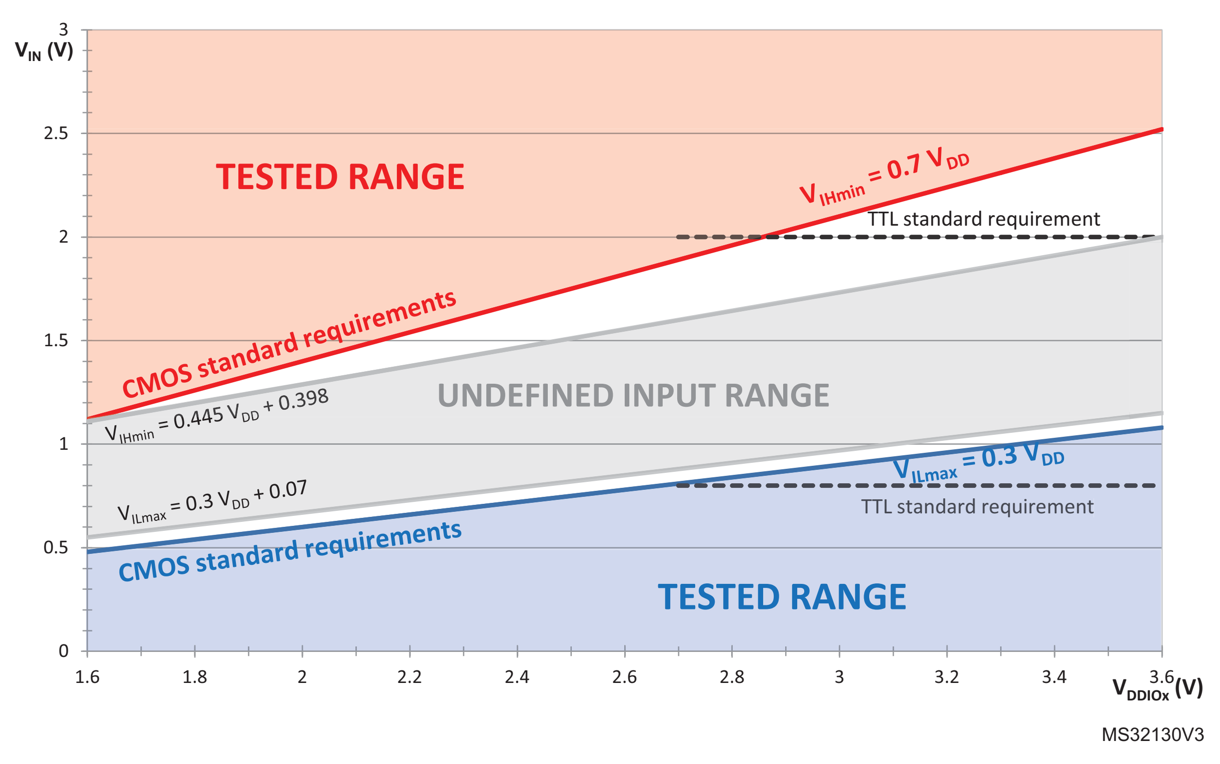
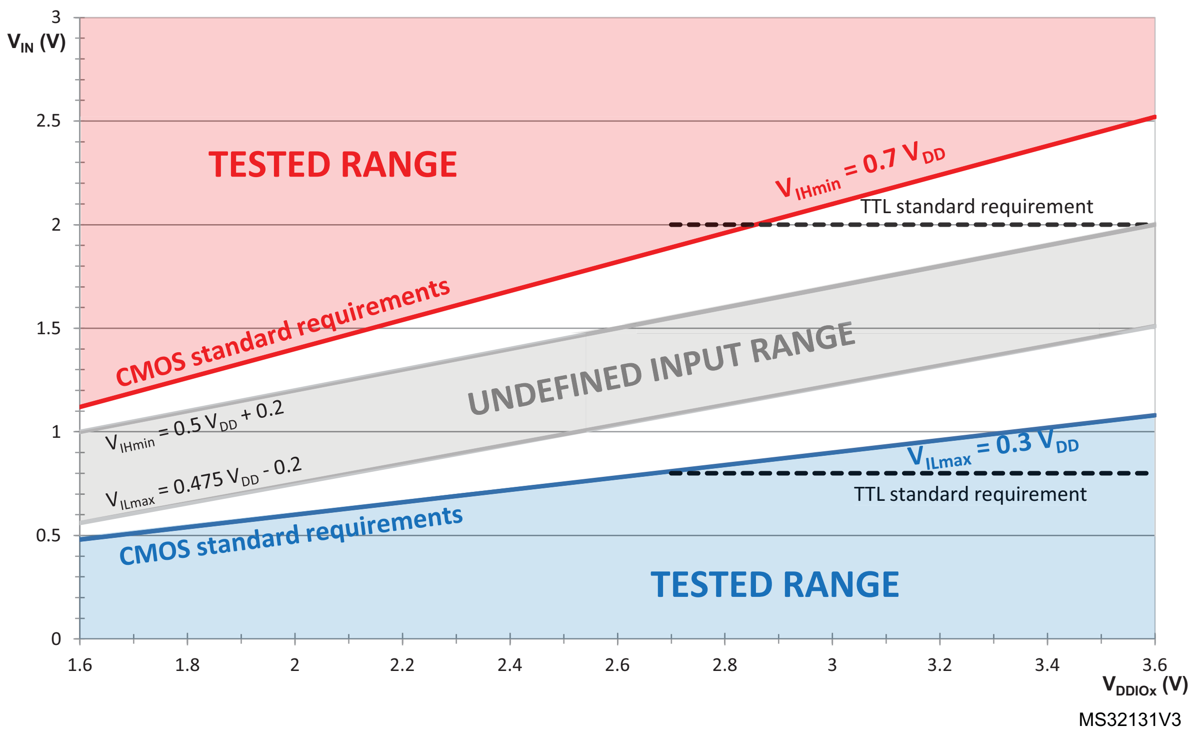


Figure 20. Five volt tolerant (FT and FTf) I/O input characteristics



MS32131V3

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*:

- The sum of the currents sourced by all the I/Os on $V_{DDIOx,}$ plus the maximum consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 14: Voltage characteristics*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 14: Voltage characteristics*).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 44. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(2)	Output low level voltage for an I/O pin	$\lvert I_{IO}\rvert$ = 4 mA	-	0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin		V_{DDIOx}–0.4	-	V
V_{OLFm+}(3)	Output low level voltage for an FTf I/O pin in Fm+ mode	$\lvert I_{IO}\rvert$ = 10 mA	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 14: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. Data based on characterization results. Not tested in production.
3. Data based on design simulation only. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 21* and *Table 45*, respectively.

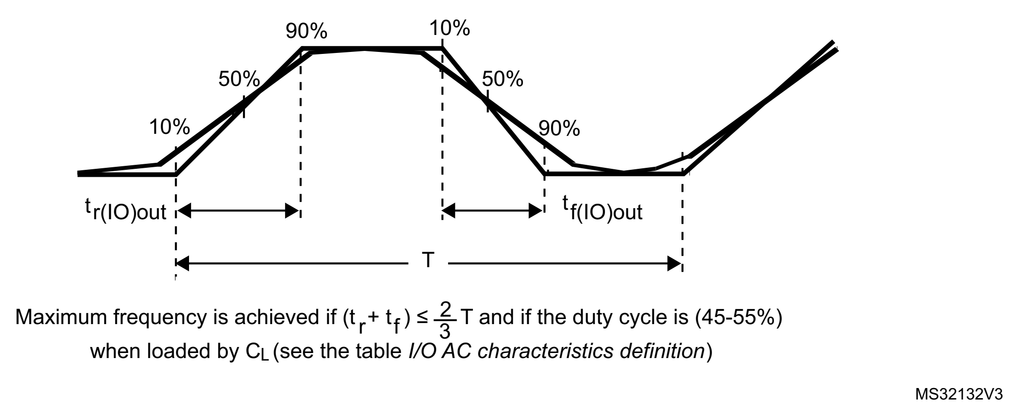
Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 45. I/O AC characteristics[1][2]

OSPEEDRy [1:0] value[1]	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency[3]	C_L = 50 pF	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	125	ns
	$t_{r(IO)out}$	Output rise time		-	125	
01	$f_{max(IO)out}$	Maximum frequency[3]	C_L = 50 pF	-	4	MHz
	$t_{f(IO)out}$	Output fall time		-	62.5	ns
	$t_{r(IO)out}$	Output rise time		-	62.5	
11	$f_{max(IO)out}$	Maximum frequency[3]	C_L = 50 pF	-	10	MHz
	$t_{f(IO)out}$	Output fall time		-	25	ns
	$t_{r(IO)out}$	Output rise time		-	25	
Fm+ configuration[4]	$f_{max(IO)out}$	Maximum frequency[3]	CL = 50 pF	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	16	ns
	$t_{r(IO)out}$	Output rise time		-	44	
	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 21*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 21. I/O AC characteristics definition



6.3.14 NRST and NPOR pin characteristics

NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

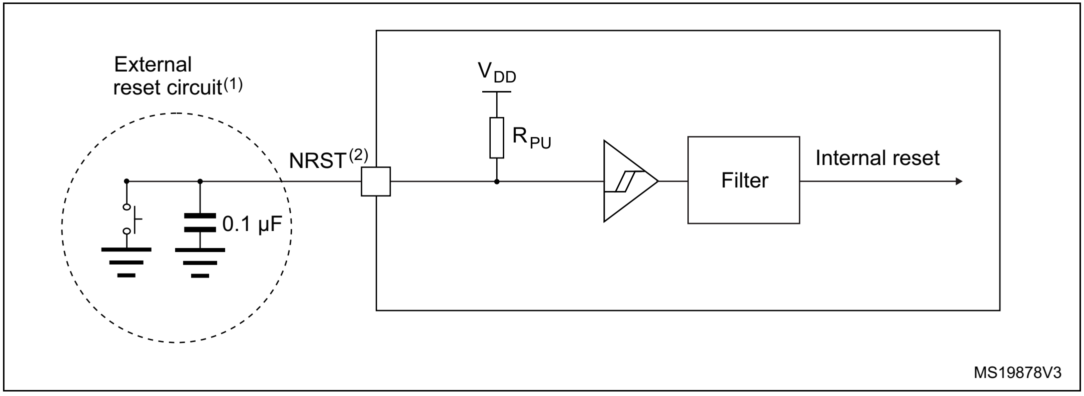
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 46. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	0.3 V_{DD}+0.07[1]	V
$V_{IH(NRST)}$	NRST input high level voltage	-	0.445 V_{DD}+0.398[1]	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor[2]	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100[1]	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	-	700[1]	-	-	ns

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

Figure 22. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 46: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

NPOR pin characteristics

The NPOR pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor to the V_{DDA}, R_{PU}.

Unless otherwise specified, the parameters given in *Table 47* below are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 17: General operating conditions*.

Table 47. NPOR pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NPOR)}$	NPOR Input low level voltage		-		0.475 V_{DDA} - 0.2(1)	V
$V_{IH(NPOR)}$	NPOR Input high level voltage		0.5 V_{DDA} + 0.2(1)		-	
$V_{hys(NPOR)}$	NPOR Schmitt trigger voltage hysteresis	-	-	100(1)	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 48* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 17: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 48. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	V_{DDA} = 3.3 V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12 bit resolution	0.043	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz, 12 bit resolution	-	-	823	kHz
		12 bit resolution	-	-	17	1/f_{ADC}
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 49* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			1/f_{ADC}
$W_{LATENCY}$(2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 14 MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			1/f_{PCLK}
		$f_{ADC} = f_{PCLK}/4$ = 12 MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			1/f_{PCLK}
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	1/f_{HSI14}
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	1/f_{ADC}
t_{STAB}(2)	Stabilization time	-	14			1/f_{ADC}
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12 bit resolution	1	-	18	µs
		12 bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			1/f_{ADC}

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 49. R_{AIN} max for f_{ADC} = 14 MHz

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)[1]
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 50. ADC accuracy(1)(2)(3)

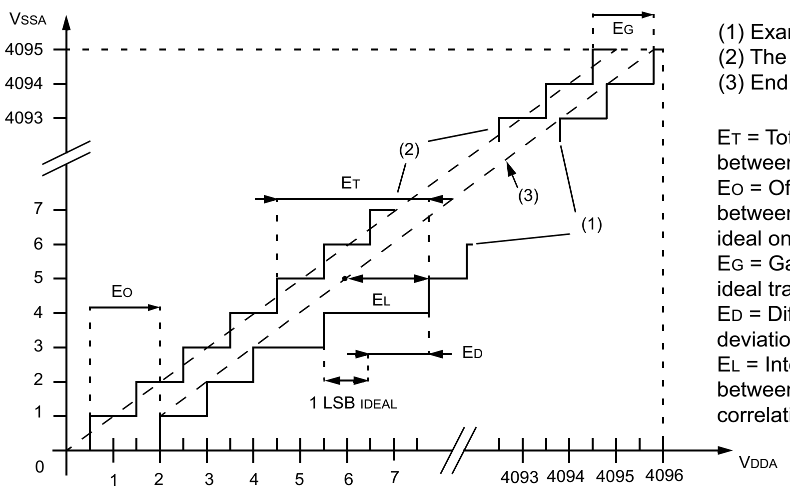
Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = –40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

Table 50. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 23. ADC accuracy characteristics

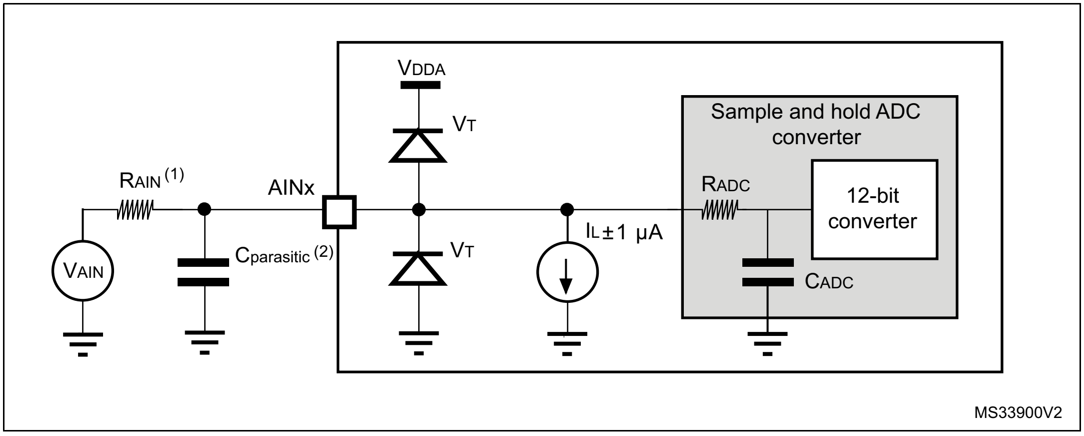


(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

ET = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
EO = Offset Error: maximum deviation between the first actual transition and the first ideal one.
EG = Gain Error: deviation between the last ideal transition and the last actual one.
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Figure 24. Typical connection diagram using the ADC



1. Refer to *Table 48: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 11: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.16 Temperature sensor characteristics

Table 51. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope[1]	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)[2]	1.34	1.43	1.52	V
t_{START}[1]	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 3: Temperature sensor calibration values*.

6.3.17 V_{BAT} monitoring characteristics

Table 52. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	

Table 52. V_{BAT} monitoring characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
Er(1)	Error on Q	–1	-	+1	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.18 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 53. TIMx characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)	-	16	bit
		TIM2	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	s

Table 54. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 55. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.19 Communication interfaces

I^2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 56. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(2)	260(3)	ns

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I^{2}S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I^{2}S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 17: General operating conditions*.

Refer to *Section 6.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^{2}S).

Table 57. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF	-	6	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4Tpclk	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2Tpclk + 10	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ $t_{su(SI)}$	Data input setup time	Master mode	4	-	
		Slave mode	5	-	
$t_{h(MI)}$	Data input hold time	Master mode	4	-	
$t_{h(SI)}$		Slave mode	5	-	
$t_{a(SO)}$[2]	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$[3]	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)	-	22.5	
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	6	
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)	11.5	-	
$t_{h(MO)}$		Master mode (after enable edge)	2	-	
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 25. SPI timing diagram - slave mode and CPHA = 0

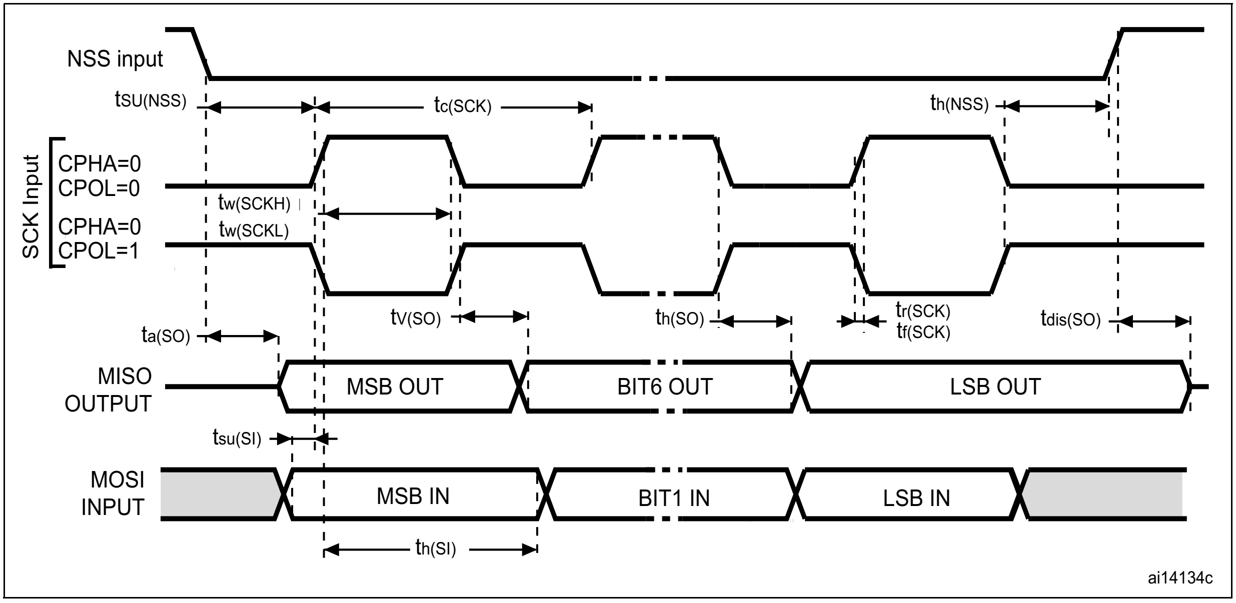
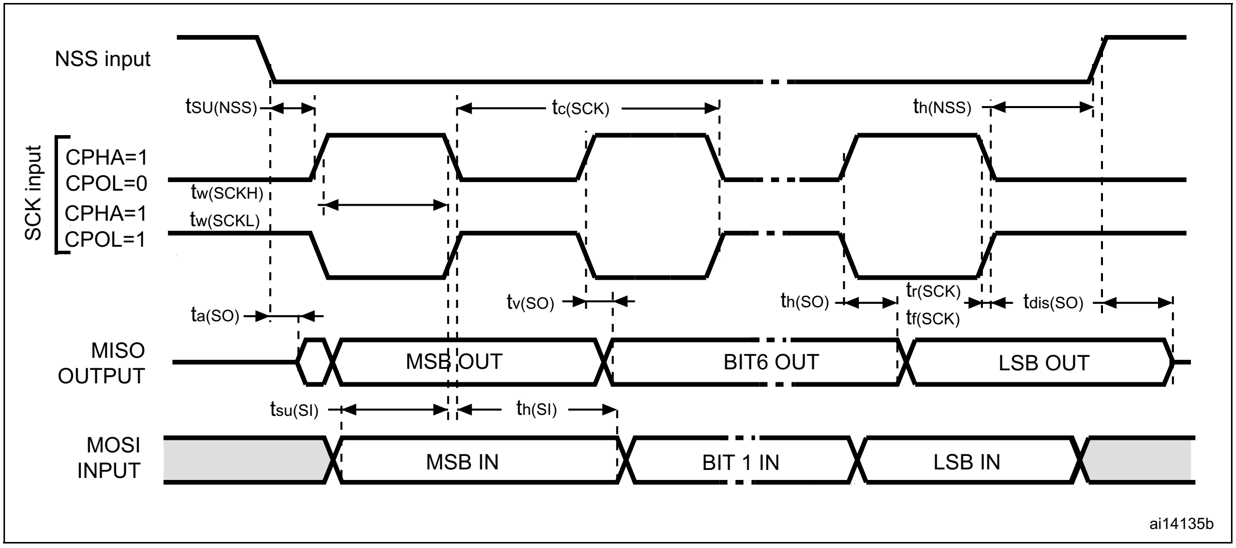
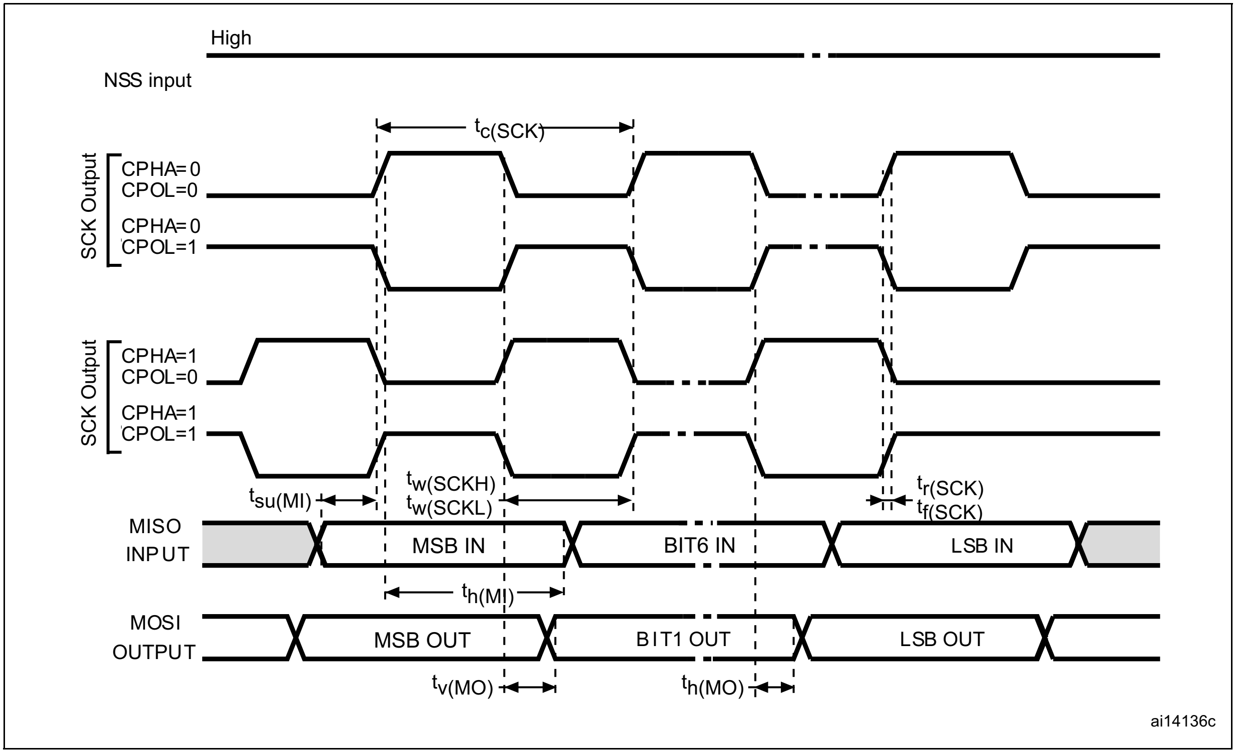


Figure 26. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 27. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 58. I^2S characteristics(1)

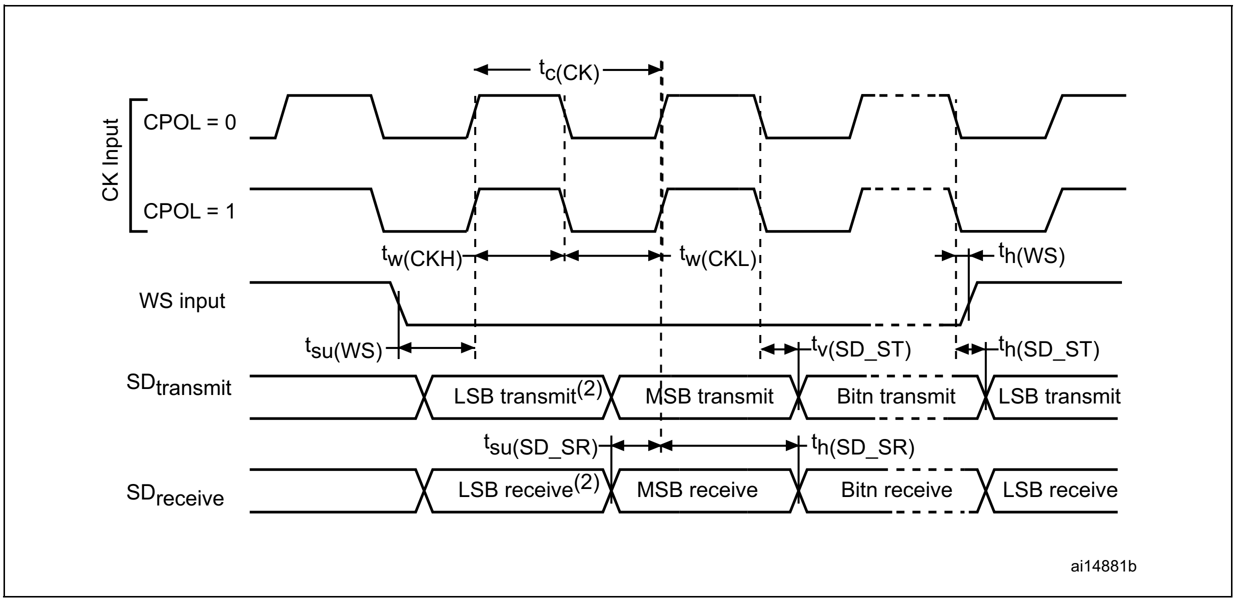
Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF	-	10	ns
$t_{f(CK)}$	I^2S clock fall time		-	12	
$t_{w(CKH)}$	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I2S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	%

Table 58. I^2S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(2)	Data output valid time	Slave transmitter (after enable edge)	-		
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	13	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter (after enable edge)	-	4	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

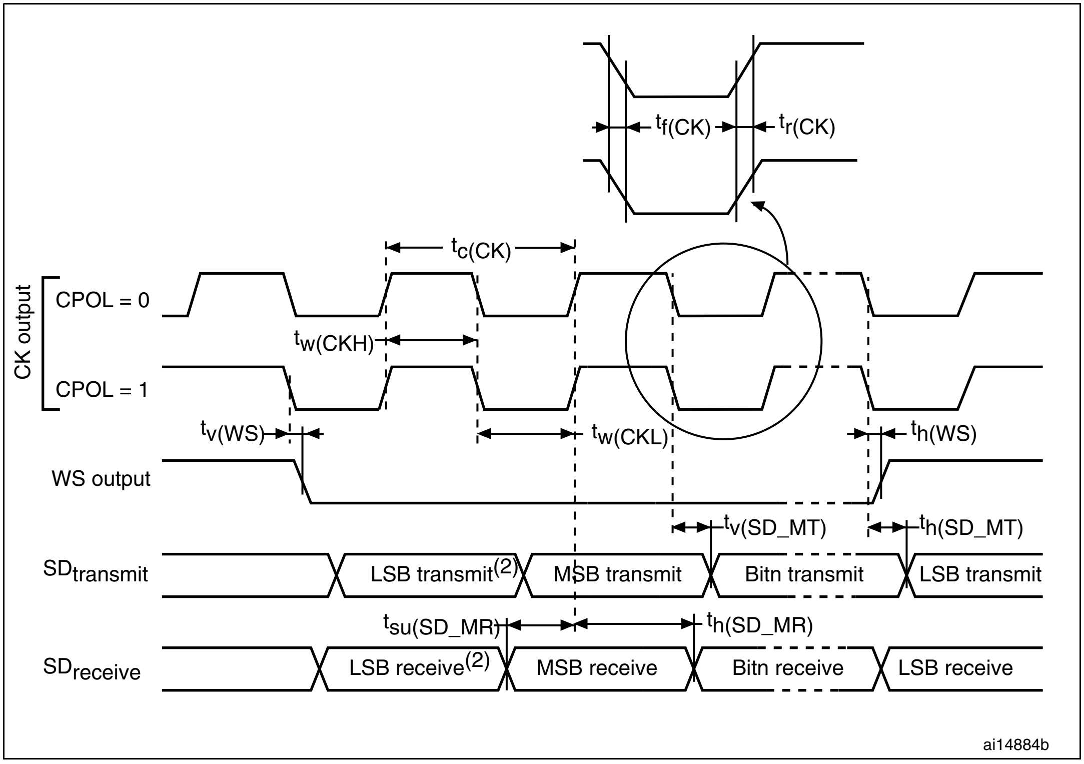
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ = 125 ns.

Figure 28. I2S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 29. I2S master timing diagram (Philips protocol)



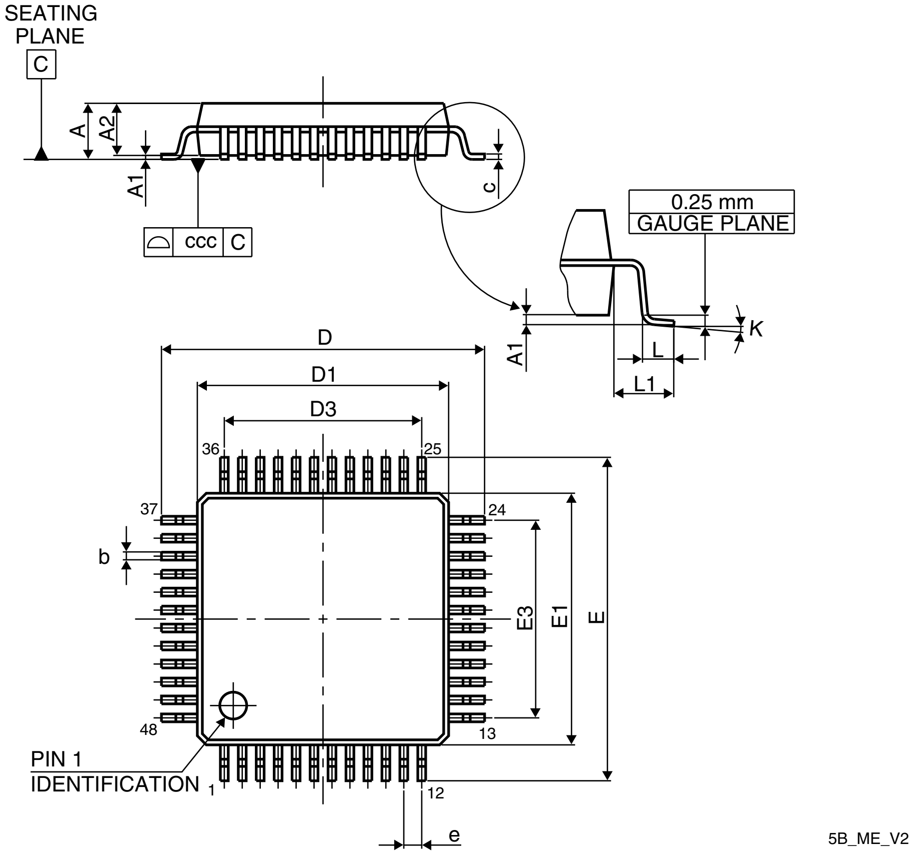
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP48 package information

Figure 30. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



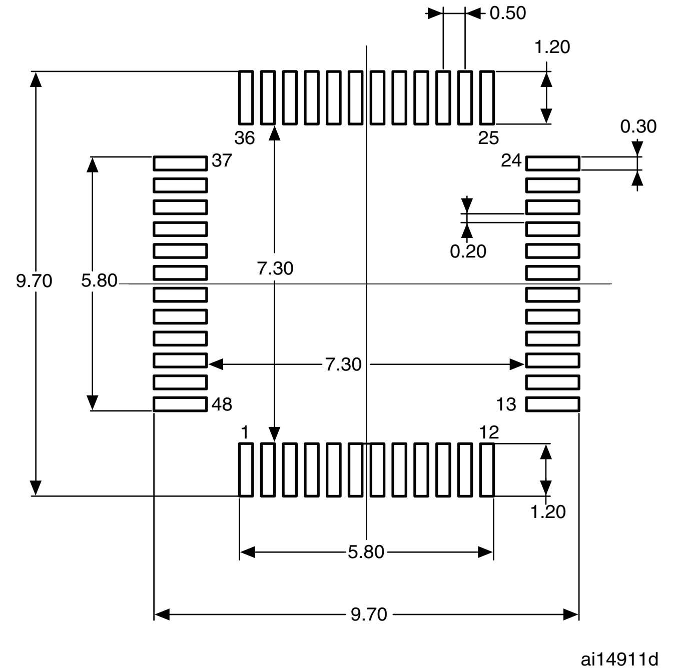
1. Drawing is not to scale.

Table 59. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 31. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint

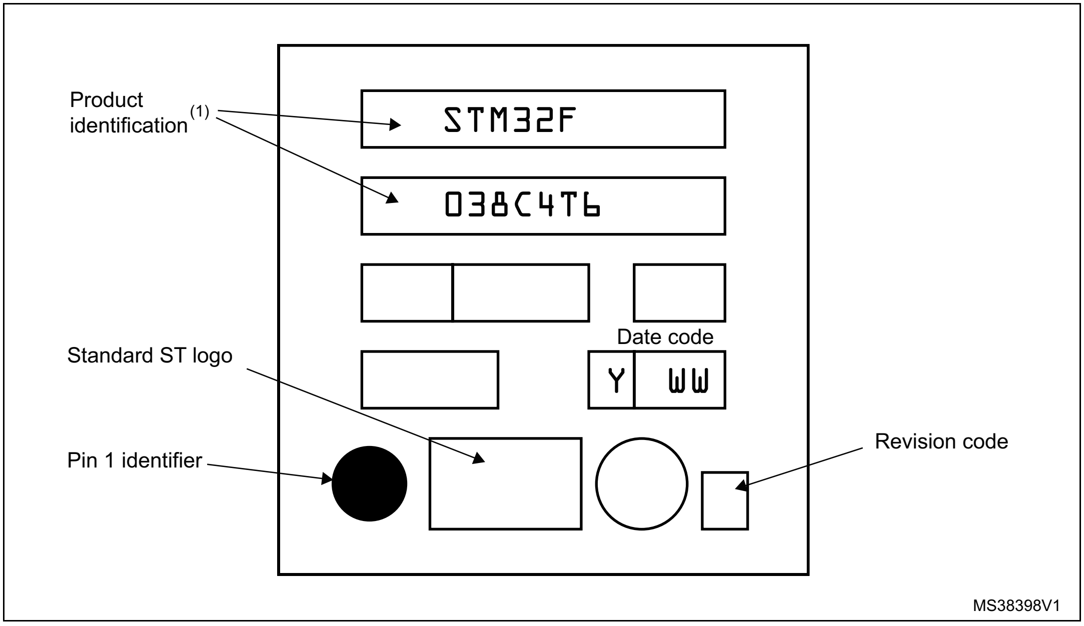


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

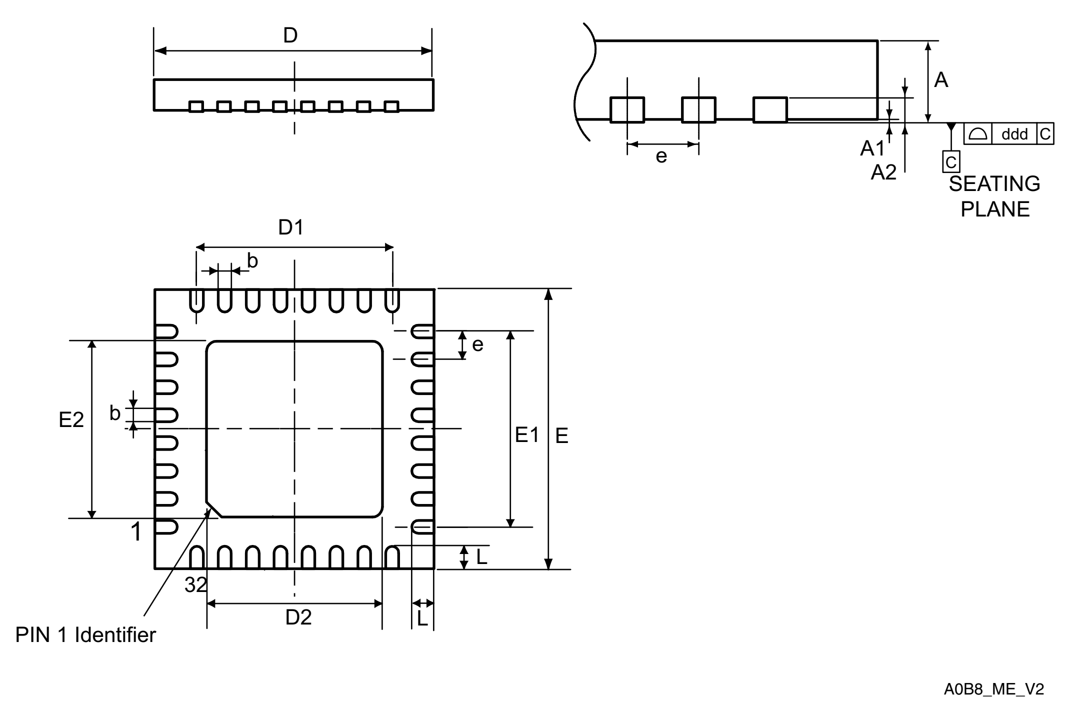
Figure 32. LQFP48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.2 UFQFPN32 package information

Figure 33. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline



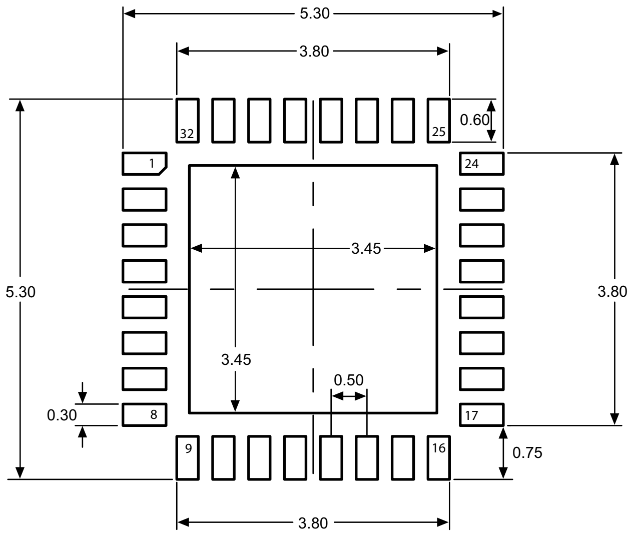
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table: Pin definitions*.

Table 60. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package recommended footprint

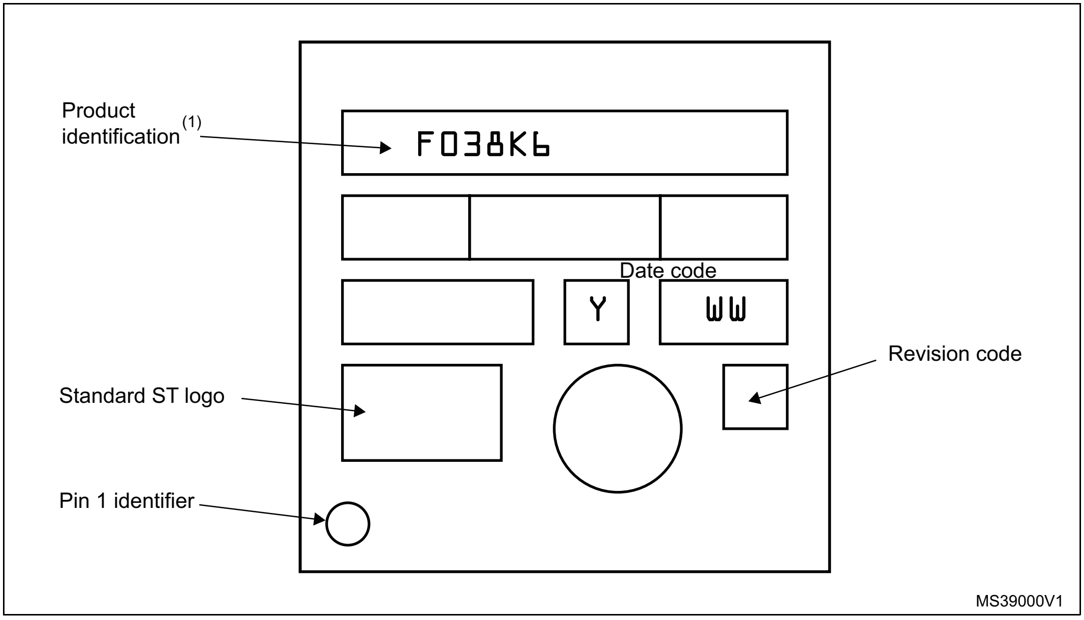


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

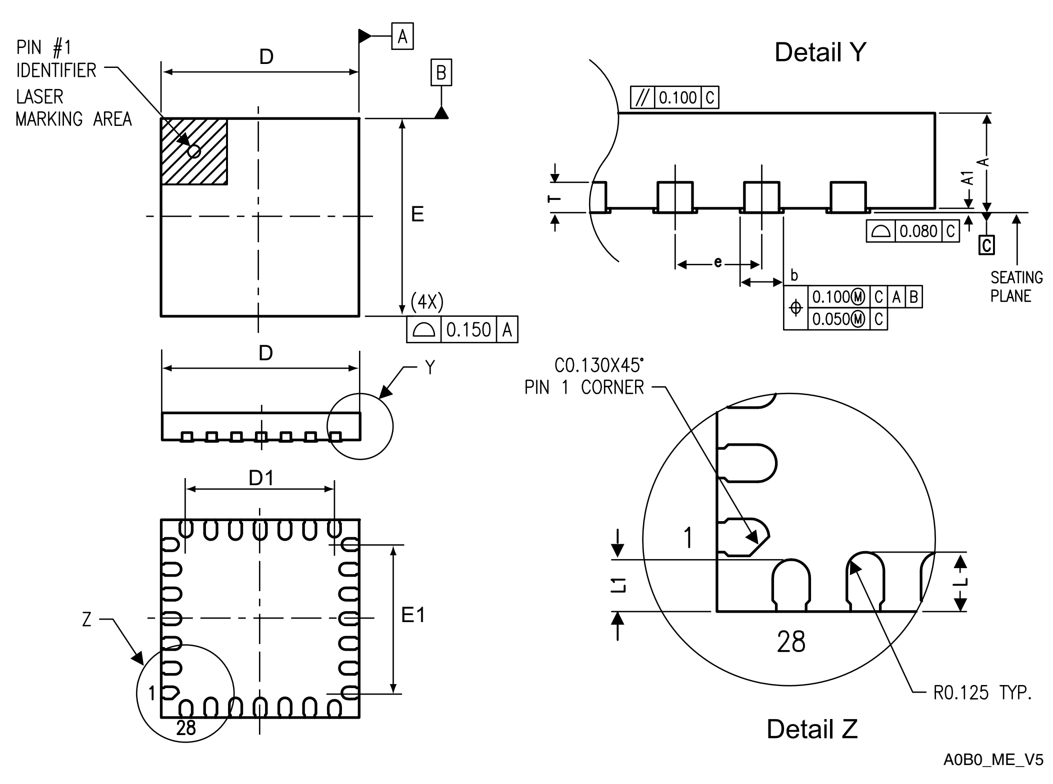
Figure 35. UFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 UFQFPN28 package information

Figure 36. UFQFPN28 - 28-lead, 4x4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



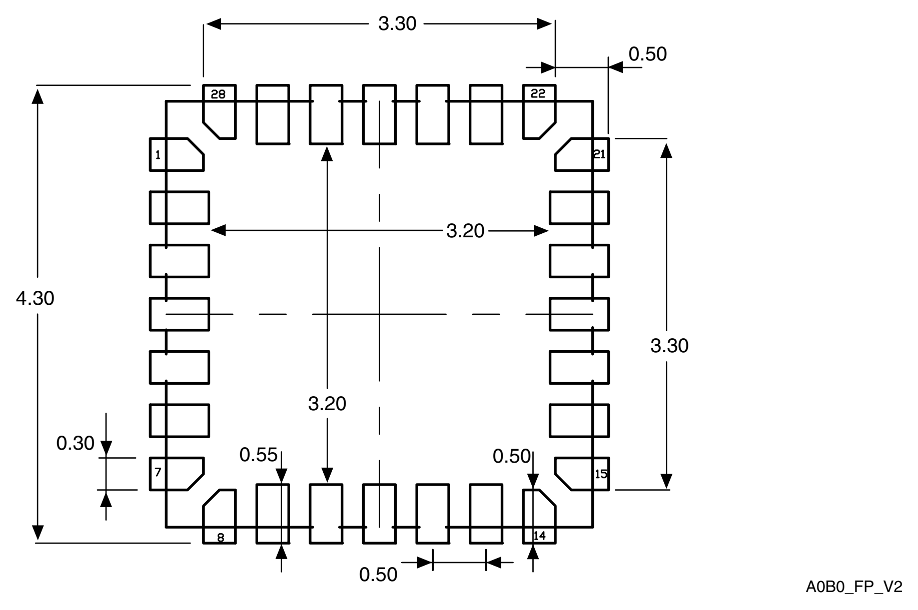
1. Drawing is not to scale.

Table 61. UFQFPN28 - 28-lead, 4x4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data[(1)]

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. UFQFPN28 - 28-lead, 4x4 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

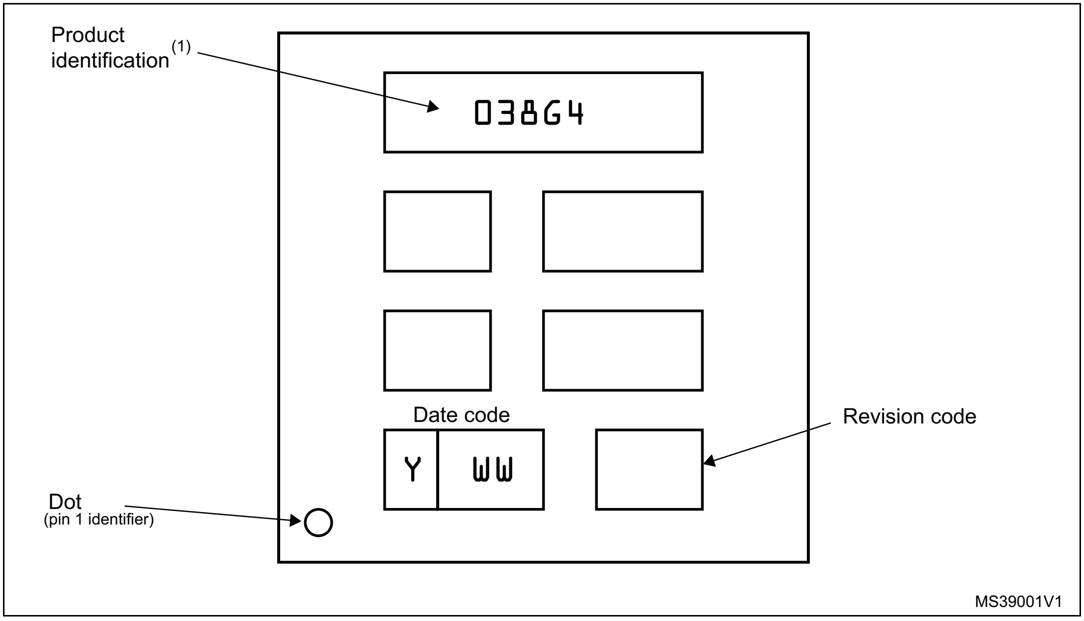


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

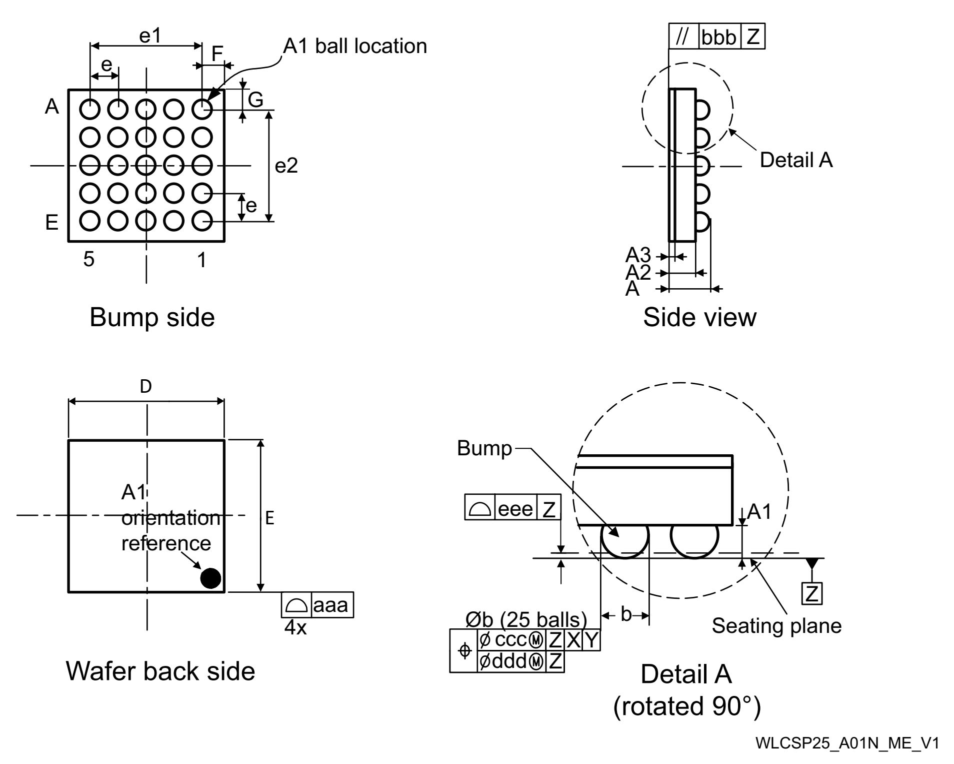
Figure 38. UFQFPN28 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.4 WLCSP25 package information

Figure 39. WLCSP25 - 25-ball, 2.423 x 2.325 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 62. WLCSP25 - 25-ball, 2.423 x 2.325 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3] [4]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.388	2.423	2.458	0.0940	0.0954	0.0968
E	2.29	2.325	2.36	0.0902	0.0915	0.0929
e	-	0.400	-	-	0.0157	-
e1	-	1.600	-	-	0.0630	-
e2	-	1.600	-	-	0.0630	-
F	-	0.4115	-	-	0.0162	-

Table 62. WLCSP25 - 25-ball, 2.423 x 2.325 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
G	-	0.3625	-	-	0.0143	-
aaa	-	0.100	-	-	0.0039	-
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
ddd	-	0.050	-	-	0.0020	-
eee	-	0.050	-	-	0.0020	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

Figure 40. WLCSP25 - 25-ball, 2.133 x 2.070 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

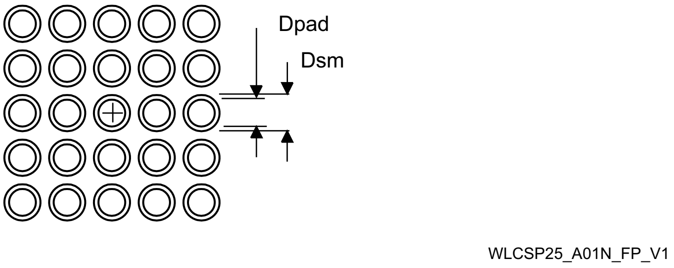


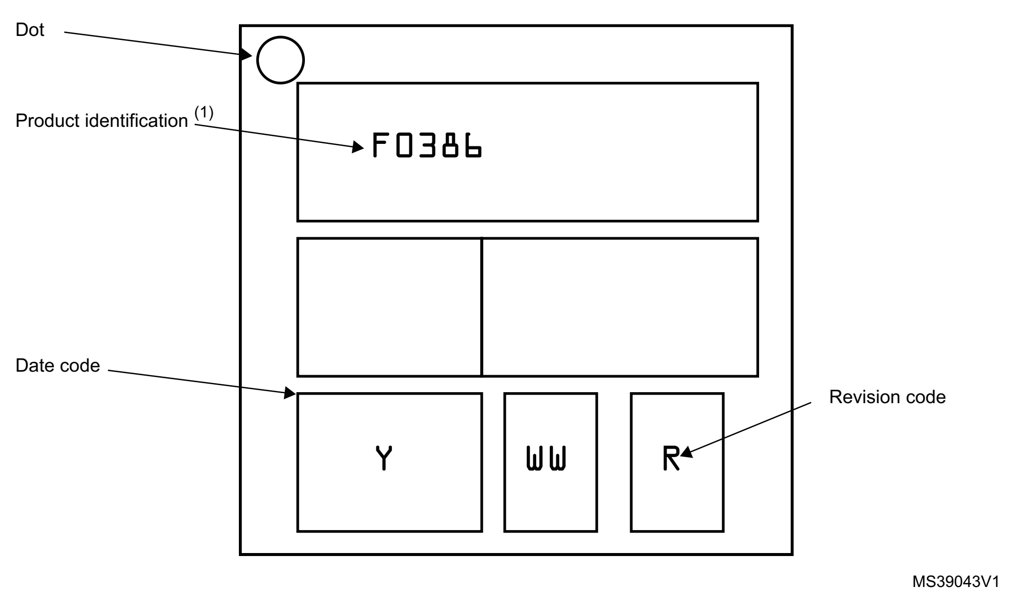
Table 63. WLCSP25 recommended PCB design rules (0.4 mm pitch)

Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

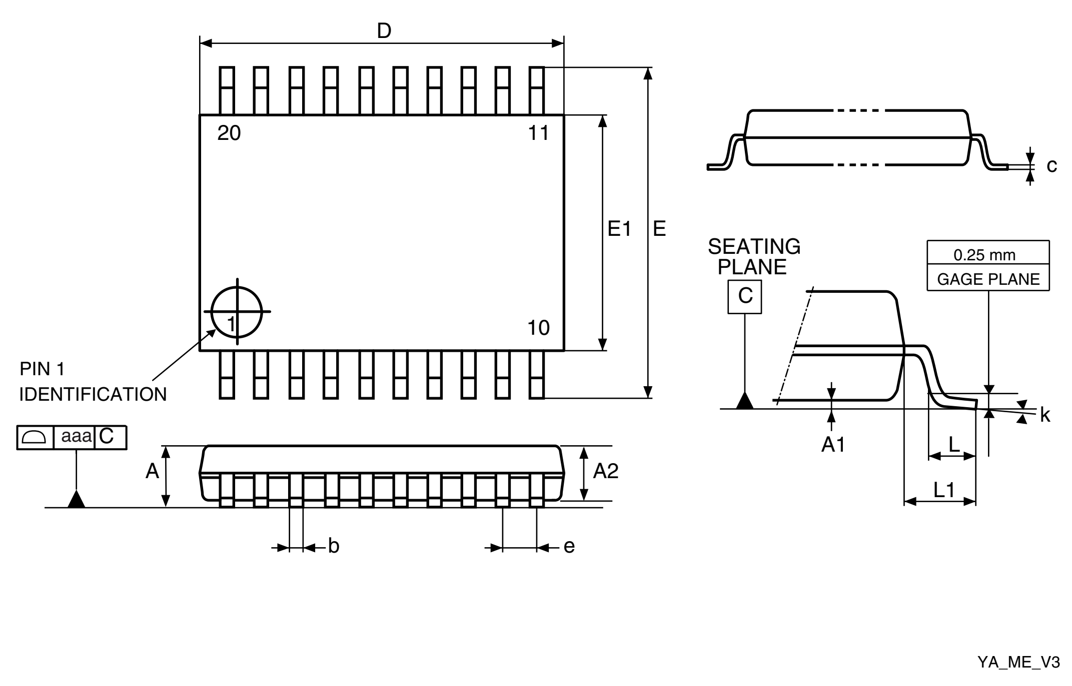
Figure 41. WLCSP25 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 TSSOP20 package information

Figure 42.TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package outline



1. Drawing is not to scale.

Table 64. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data

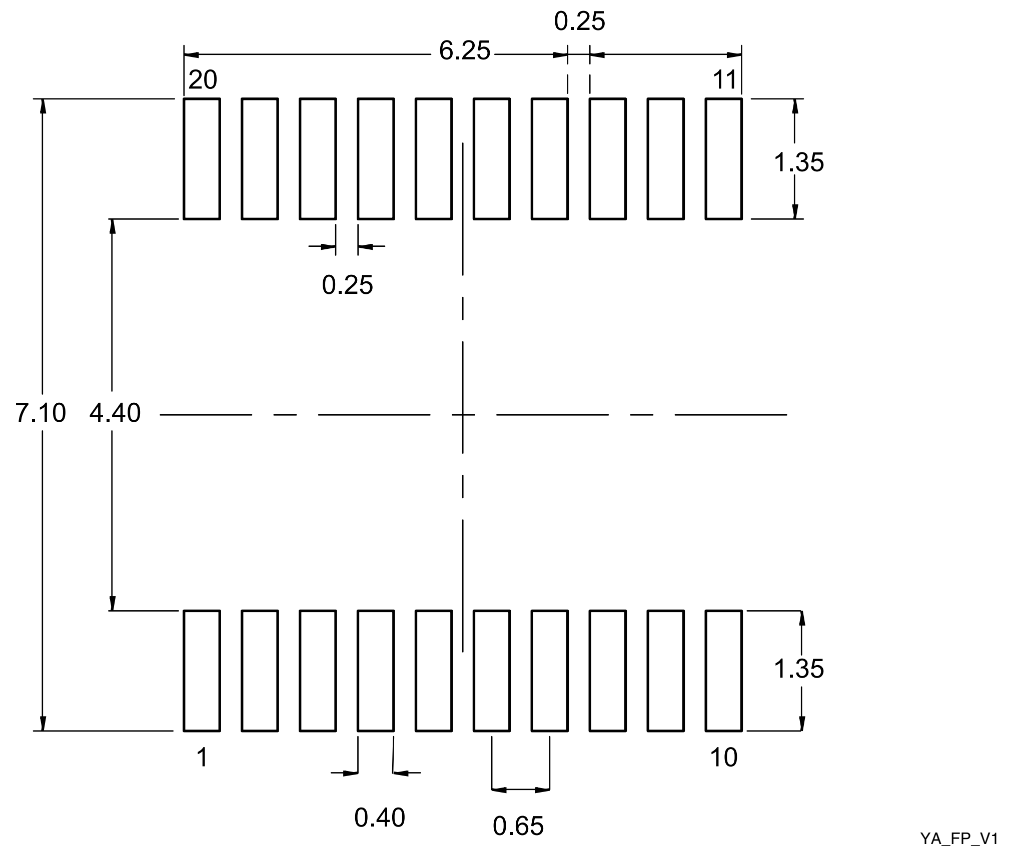
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D(2)	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1(3)	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-

Table 64. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 43. TSSOP20 – 20-lead thin shrink small outline, 6.5 x 4.4 mm, 0.65 mm pitch, package footprint

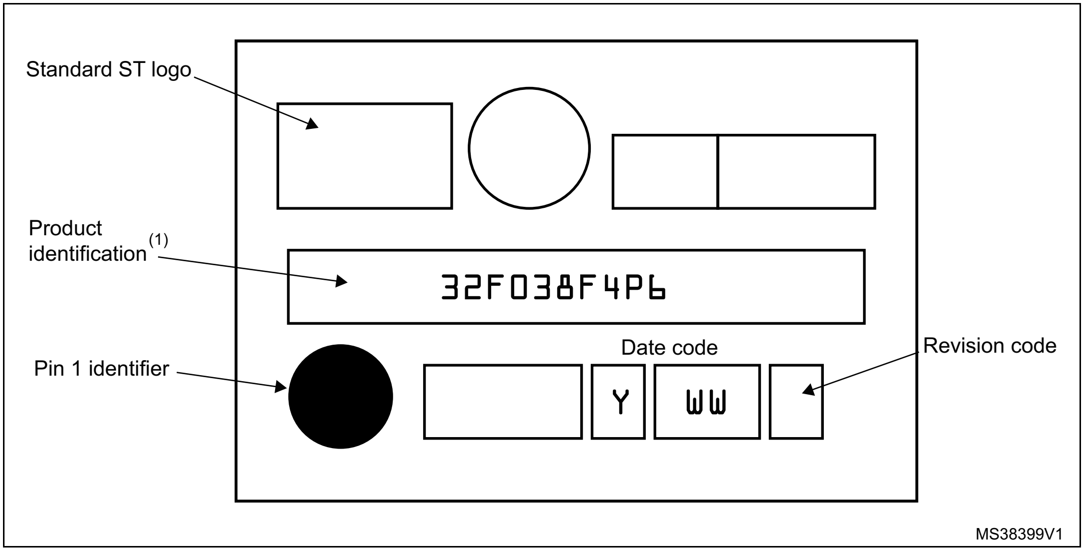


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 44. TSSOP20 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 17: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 65. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 × 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 × 4 mm	118	
	Thermal resistance junction-ambient WLCSP25 - 2.13 x 2.07 mm	74	
	Thermal resistance junction-ambient TSSOP20	110	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.6.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Part numbering*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F038x6 at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 80 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$

$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

$P_{Dmax} = 175 + 272 = 447\text{ mW}$

Using the values obtained in *Table 65* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

T_{Jmax} = 80 °C + (55°C/W × 447 mW) = 80 °C + 24.585 °C = 104.585 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C) see *Table 17: General operating conditions*.

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section 8: Part numbering*).

Note: With this given P_{Dmax} we can find the TAmax allowed for a given device temperature range (order code suffix 6 or 7).

Suffix 6: $T_{Amax} = T_{Jmax}$ - (55°C/W × 447 mW) = 105-24.585 = 80.415 °C

Suffix 7: $T_{Amax} = T_{Jmax}$ - (55°C/W × 447 mW) = 125-24.585 = 100.415 °C

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$P_{INTmax\,=}$ 20 mA × 3.5 V= 70 mW

$P_{IOmax\,=\,20}$ × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

$P_{Dmax\,=}$ 70 $_+$ 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 65* T_{Jmax} is calculated as follows:

– For LQFP48, 55 °C/W

T_{Jmax} = 100 °C + (55 °C/W × 134 mW) = 100 °C + 7.37 °C = 107.37 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 66. Ordering information scheme

Example: STM32 F 038 G 6 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

038 = STM32F038xx

Pin count

F = 20 pins
E = 25 pins
G = 28 pins
K = 32 pins
C = 48 pins

Code size

6 = 32 Kbytes of Flash memory

Package

P = TSSOP
U = UFQFPN
T = LQFP
Y = WLCSP

Temperature range

6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Options

xxx = programmed parts
TR = tape and reel

9 Revision history

Table 67. Document revision history

Date	Revision	Changes
28-May-2014	1	Initial release.

Table 67. Document revision history (continued)

Date	Revision	Changes
24-Sep-2015	2	Updated: – Table 2: STM32F038x6 family device features and peripheral counts – Figure 8: STM32F038x6 memory map, – AF1 alternate functions for PA0, PA1, PA2, PA3 and PA4 in Table 11: Alternate functions selected through GPIOA_AFR registers for port A, – the footnote for V_{IN} max value in Table 14: Voltage characteristics, – the footnote for max V_{IN} in Table 17: General operating conditions, – Table 20: Typical and maximum current consumption from VDD supply at VDD = 1.8 V – Table 21: Typical and maximum current consumption from the VDDA supply, – Table 23: Typical and maximum current consumption from the VBAT supply, – Table 19: Embedded internal reference voltage with the addition of t_{START} parameter, – Table 48: ADC characteristics, – Table 51: TS characteristics: removed the min. value for t_{START} parameter, – the typical value for R parameter in Table 52: VBAT monitoring characteristics, – $V_{ESD(CDM)}$ class and value in Table 40: ESD absolute maximum ratings, – the structure of Section 7: Package information. Added: – Figure 32: LQFP48 marking example (package top view), – Figure 35: UFQFPN32 marking example (package top view), – Figure 38: UFQFPN28 marking example (package top view), – Figure 44: TSSOP20 marking example (package top view).

Table 67. Document revision history (continued)

Date	Revision	Changes
24-Sep-2015	2 (continued)	Added WLCSP25 package, updates in the following: – *Table 1: Device summary*, – *Section 2: Description*, – *Table 2: STM32F038x6 family device features and peripheral counts*, – *Section 4: Pinouts and pin description*: addition of *Figure 6: WLCSP25 25-ball package ballout (bump side)* and update of *Table 10: Pin definitions*, – *Table 17: General operating conditions*, – *Section 7: Package information* with the addition of *Section 7.4: WLCSP25 package information*, – *Table 65: Package thermal characteristics*.