



Z0109NA0

4Q Triac

6 May 2015

Product data sheet

1. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Triggering in all four quadrants

2. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

3. Quick reference data

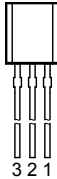
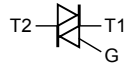
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	0.4	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	0.4	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	0.4	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	0.4	-	10	mA



4. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

5. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
Z0109NA0	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

6. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	12.5	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	13.8	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.78	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 20\text{ mA}$; T2+ G+	-	50	$A/\mu s$
		$I_G = 20\text{ mA}$; T2+ G-	-	50	$A/\mu s$
		$I_G = 20\text{ mA}$; T2- G+	-	20	$A/\mu s$
		$I_G = 20\text{ mA}$; T2- G-	-	50	$A/\mu s$
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}C$
T_j	junction temperature		-	125	$^{\circ}C$

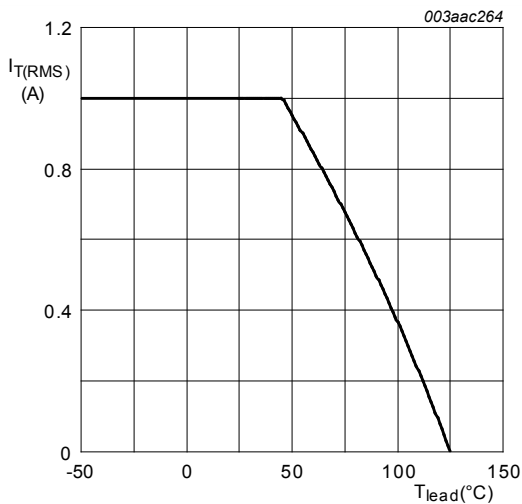
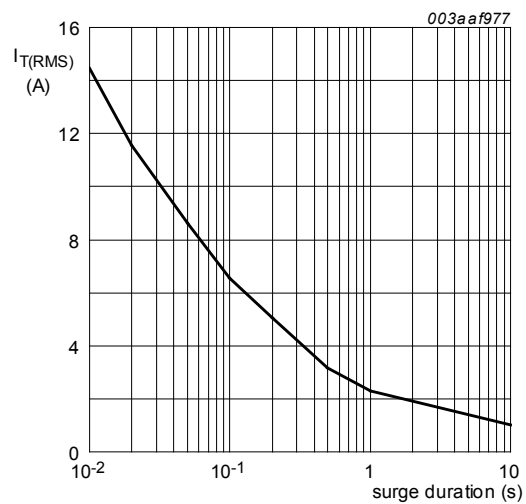


Fig. 1. RMS on-state current as a function of lead temperature; maximum values



$f = 50\text{ Hz}$; $T_{lead} = 45\text{ °C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

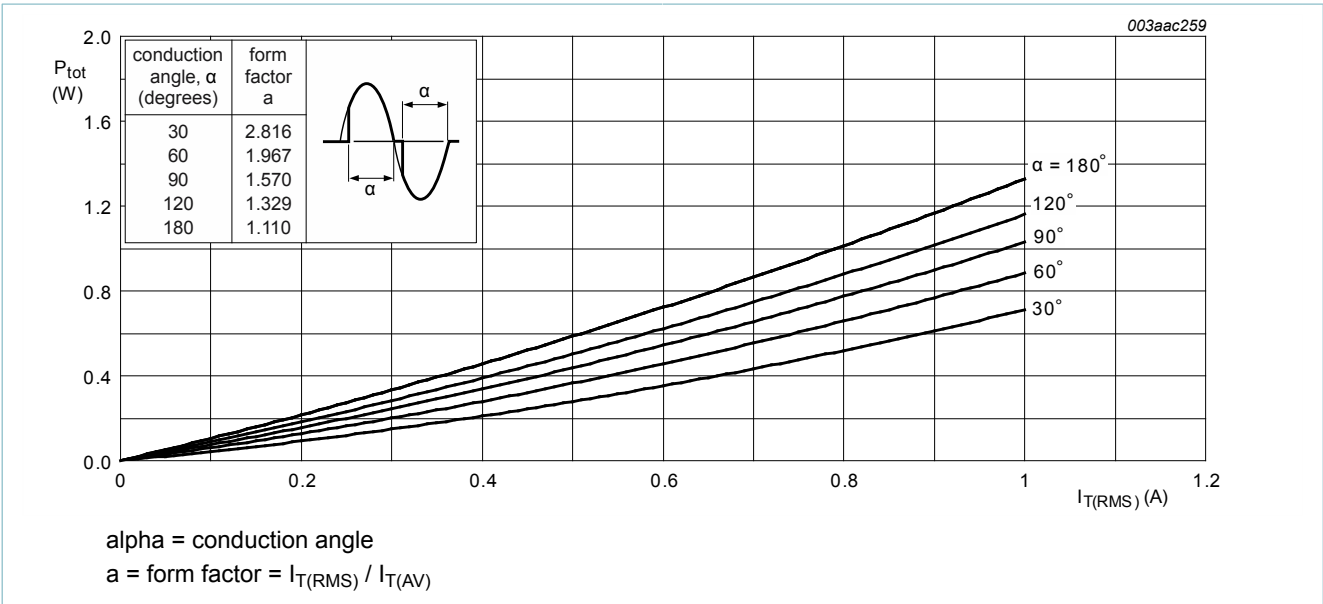


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

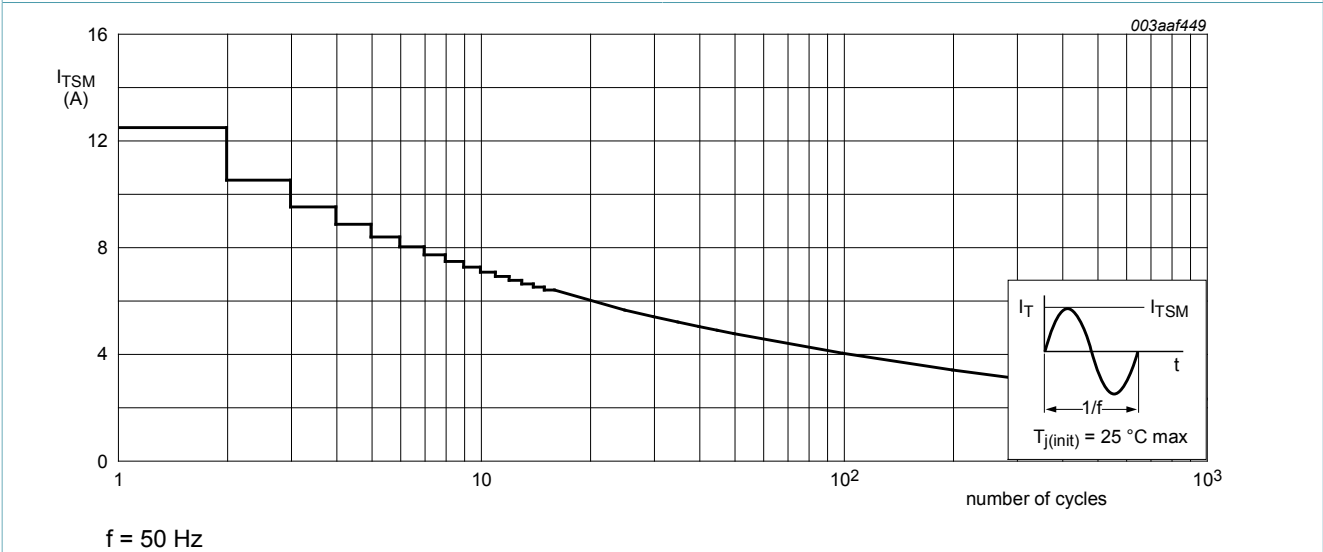


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

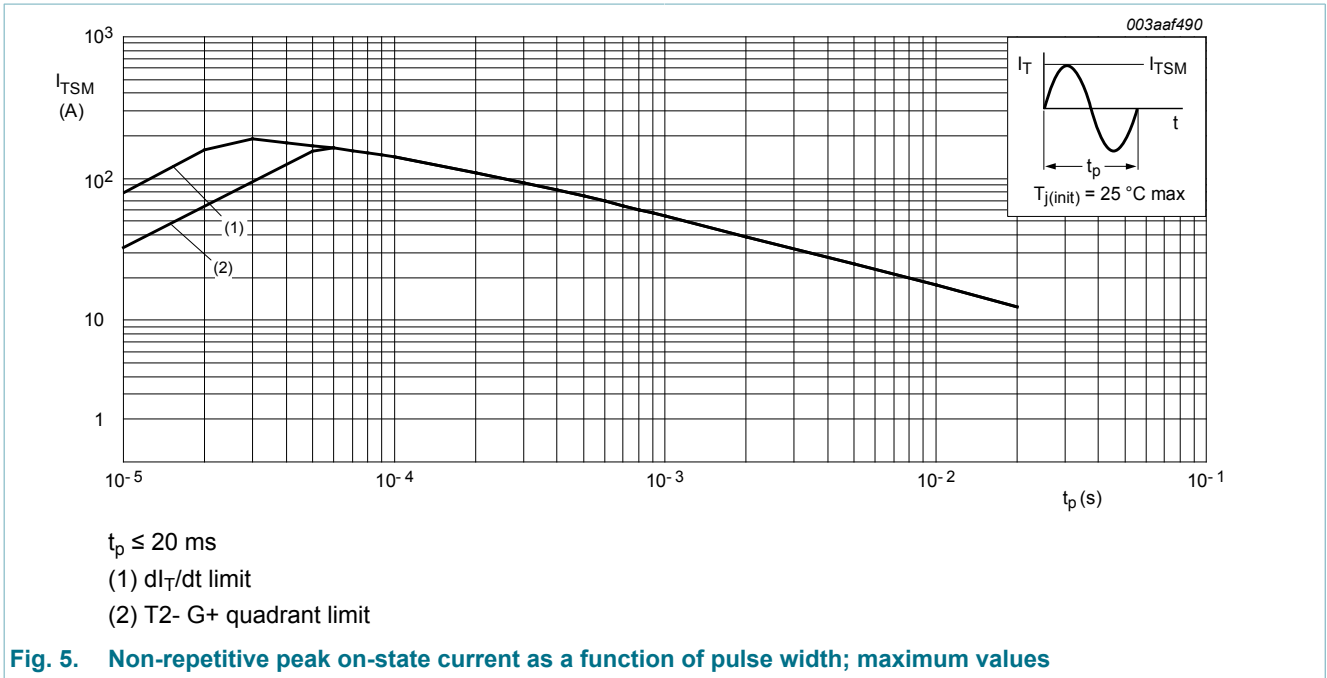
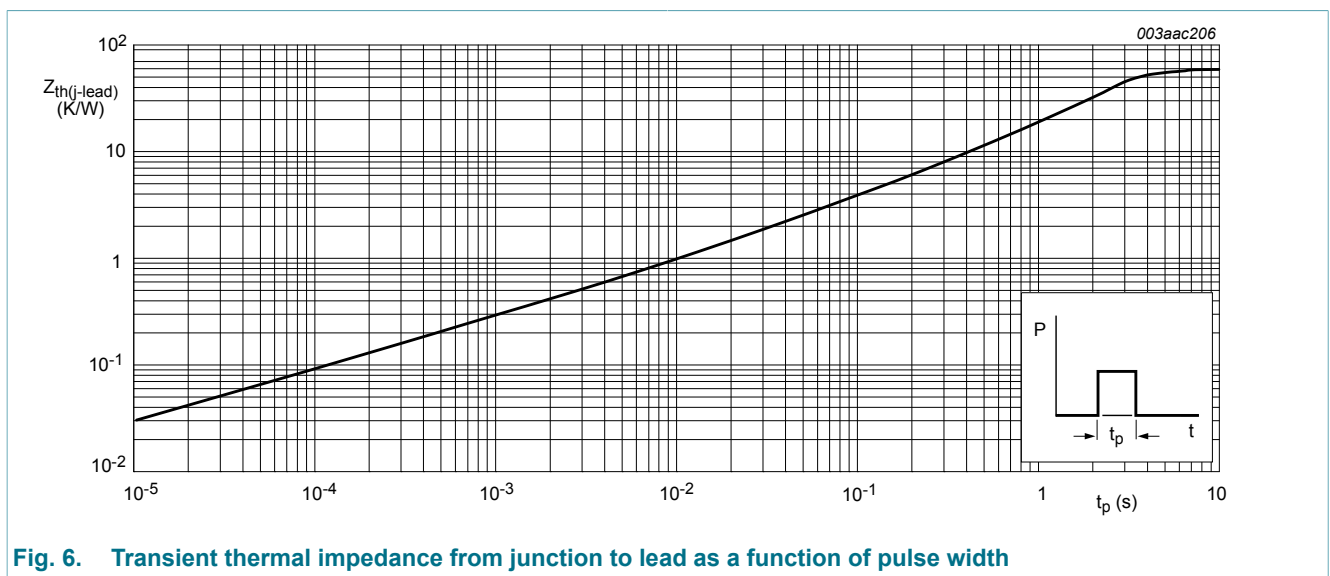


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

7. Thermal characteristics

Table 5. Thermal characteristics

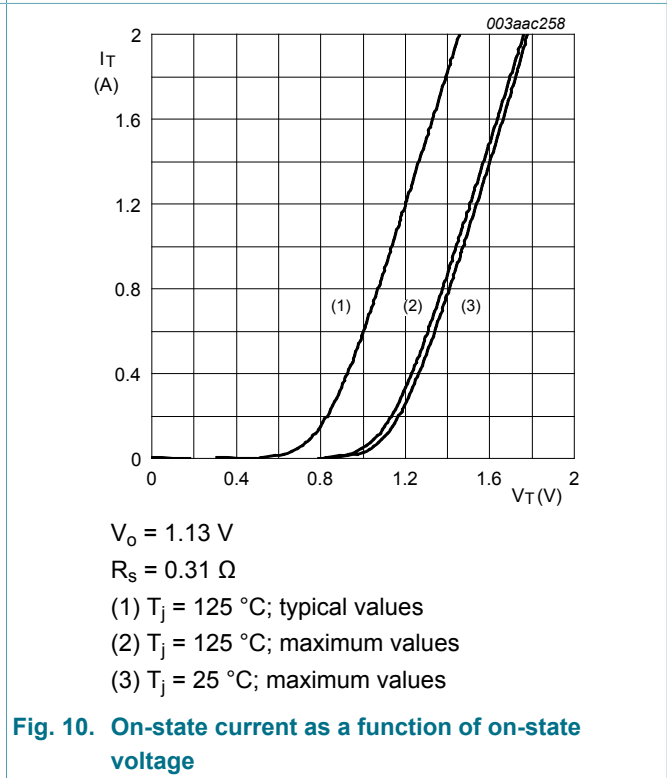
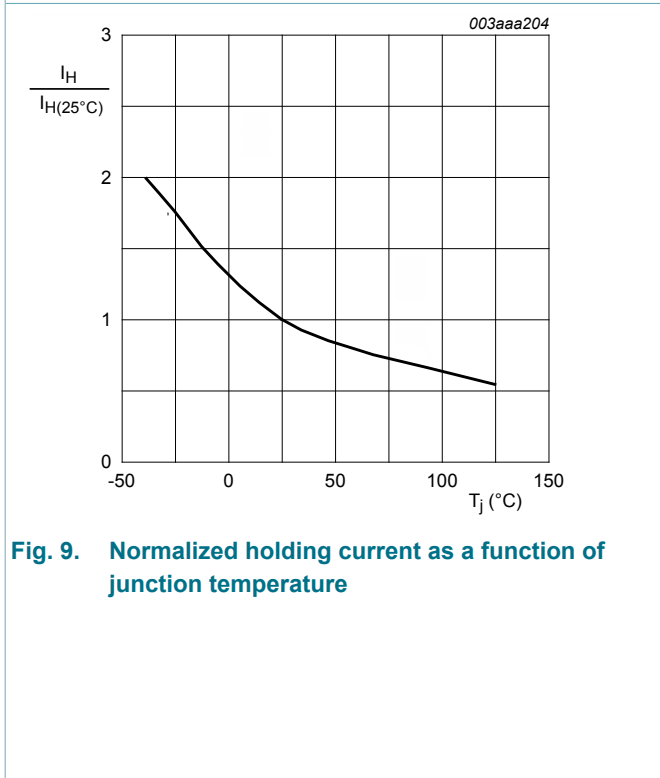
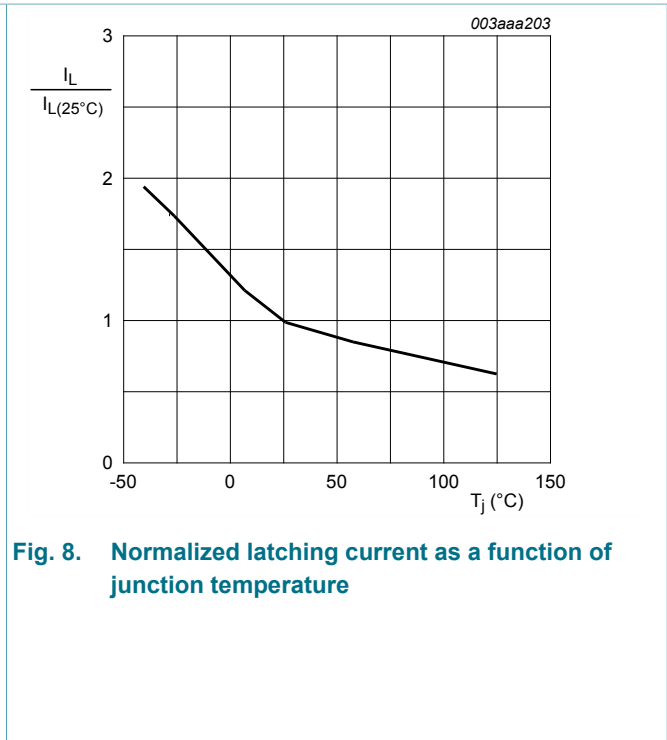
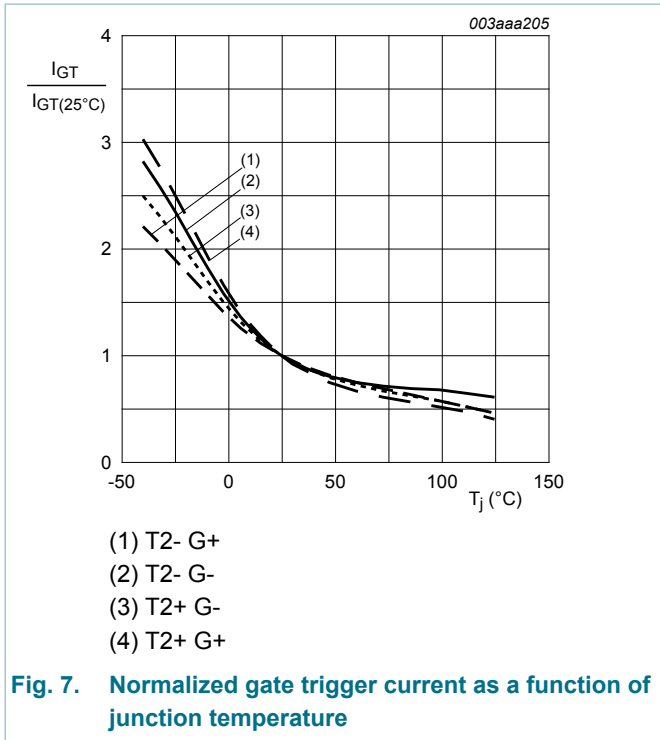
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length 4 mm	-	150	-	K/W



8. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	0.4	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G+; T _j = 25 °C; Fig. 7	0.4	-	10	mA
I _L	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8	-	-	15	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8	-	-	30	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8	-	-	15	mA
		V _D = 12 V; I _G = 0.1 A; T2- G+; T _j = 25 °C; Fig. 8	-	-	15	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 9	-	-	10	mA
V _T	on-state voltage	I _T = 1 A; T _j = 25 °C; Fig. 10	-	1.3	1.6	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11	-	-	1	V
		V _D = 800 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.2	-	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	-	0.5	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 110 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 12	120	-	-	V/μs
dV _{com} /dt	rate of change of commutating voltage	V _D = 400 V; T _j = 110 °C; dI _{com} /dt = 0.44 A/ms; gate open circuit	2	-	-	V/μs



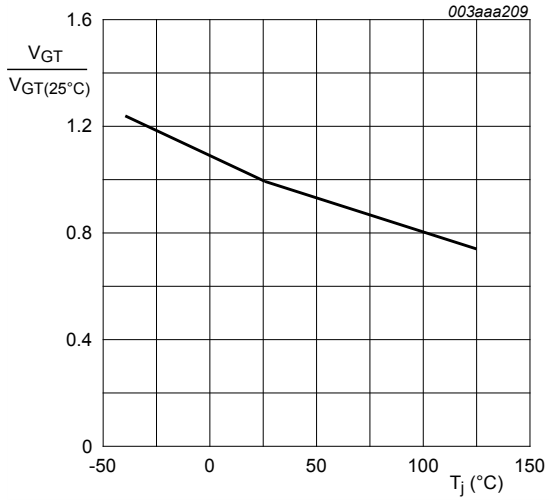


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

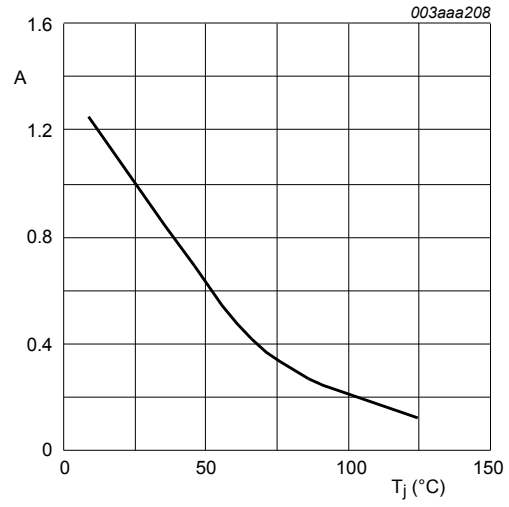


Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

$$A = \frac{dV_{D(T_j \text{ } ^\circ\text{C})} / dt}{dV_{D(25 \text{ } ^\circ\text{C})} / dt}$$

9. Package outline

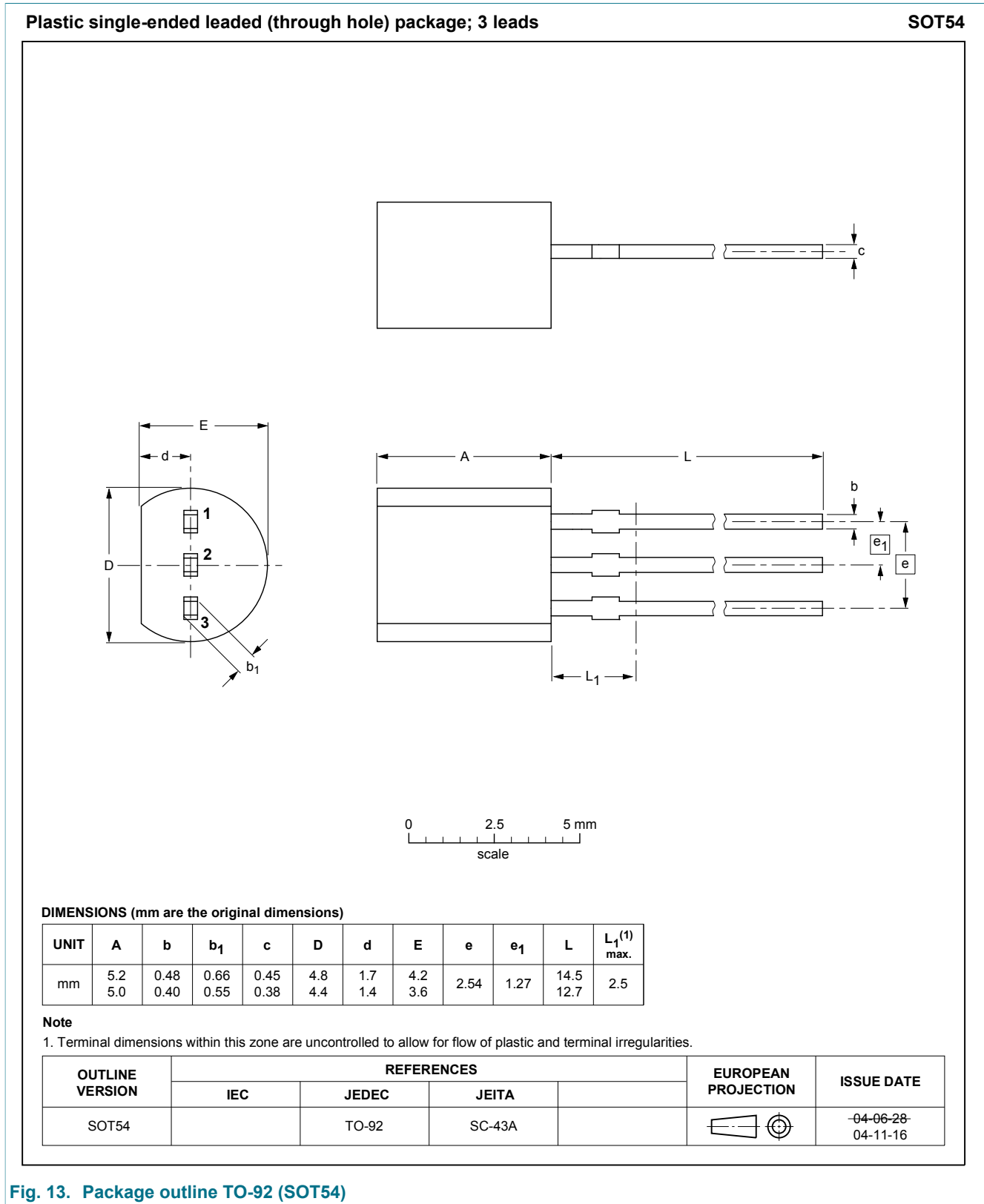


Fig. 13. Package outline TO-92 (SOT54)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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11. Contents

1	Features and benefits	1
2	Applications	1
3	Quick reference data	1
4	Pinning information	2
5	Ordering information	2
6	Limiting values	3
7	Thermal characteristics	6
8	Characteristics	7
9	Package outline	10
10	Legal information	11
10.1	Data sheet status	11
10.2	Definitions	11
10.3	Disclaimers	11
10.4	Trademarks	12

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Date of release: 6 May 2015