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QorIQ LS1043A Reference Design Board Quick Start

Contents

1 Introduction

This document describes the LS1043A reference design board (LS1043ARDB) and hardware kit containing the board. It also explains the basic board operations in a step-by-step manner.

This document describes the settings required to connect switches, connectors, jumpers, push buttons, and LEDs to the peripheral devices.

The LS1043ARDB functions with an integrated development environment (IDE), such as Freescale CodeWarrior. The instructions for working with the IDE are beyond the scope of this document.

The list of items included in the LS1043ARDB hardware kit is provided with the LS1043ARDB board support package (BSP). Optional hardware components that are not included in the LS1043ARDB hardware kit are:

- TDM modules
- PCIe/mini-PCIe cards
- CodeWarrior TAP (CWTAP)

2 Related documentation

The table below lists and explains the additional documents that you can refer to, for more information about LS1043ARDB.

Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

Table 1. Related documentation

Document	Description
QorIQ LS1043A Reference Manual (LS1043ARM)	Provides a detailed description on the LS1043A multicore processor and its features, such as memory map, serial interfaces, power supply, chip features, and clock information
QorIQ LS1043A Data Sheet	Contains information on LS1043A pin assignments, electrical characteristics, hardware design considerations, package information, and ordering information

3 LS1043ARDB system board interface

The figure below shows the front view of the LS1043ARDB.

Figure 1. LS1043ARDB front view

The figure below shows the rear view of the LS1043ARDB.

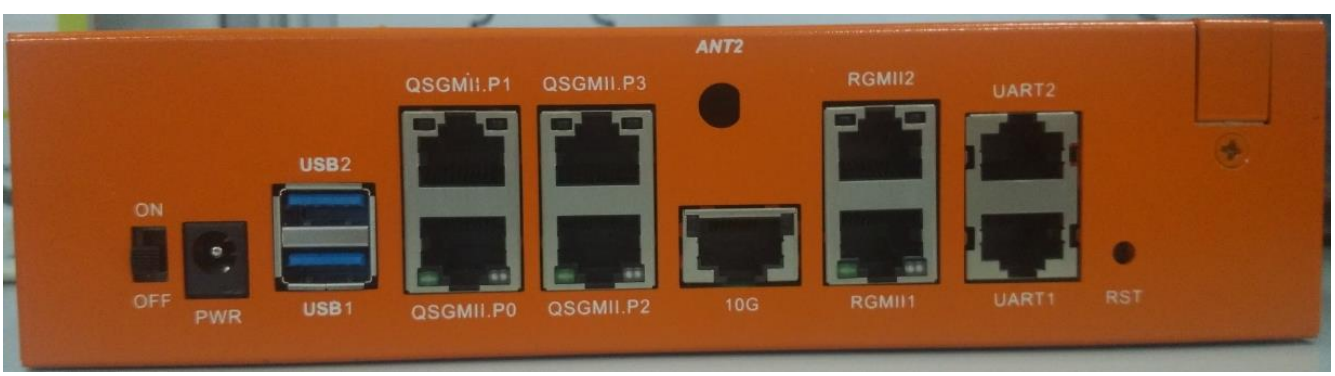

Figure 2. LS1043ARDB rear view

4 Getting started with LS1043ARDB

This section describes how to set up and use the LS1043ARDB.

4.1 Prepare board

To ensure correct board setup, prepare the board using the steps below:

1. Verify that the LS1043ARDB hardware kit contains all items mentioned in the kit contents list provided with the LS1043ARDB packing list.
2. Verify the LS1043ARDB dual inline package (DIP) switch settings. See Switch configurations for details.
3. Verify the LS1043ARDB jumper settings. See Jumper settings for details.
4. Attach the required devices to the LS1043ARDB connectors. See Connectors for details.
5. Optionally, connect the CodeWarrior TAP to the LS1043ARDB. See Setting up CodeWarrior TAP for details.
6. Install the DC power cord from the desktop power supply to the board power inlet.

4.2 Power up and use board

After the system has been properly set up, follow the steps below to power up and use the LS1043ARDB:

1. Turn ON the power switch (SW2).
2. The power LED (D1) on the printed circuit board (PCB) and the left LED (D13) of the chassis become green when the board is powered up. D3 LED on the PCB remains OFF while the boot code is fetched.
3. Connect the universal serial bus (USB) cable to the mini-USB port in the front panel used for console. You need to install the USB drivers on the host machine before using the serial terminal. You can download the latest drivers from https://developer.mbed.org/handbook/Windows-serial-configuration.
4. If you are using the RJ45 port, connect the RJ45 to UART cable to the J4 bottom port and set SW3[3] to OFF.

   You will see messages, similar to the ones shown below, on the console window (or in the CodeWarrior IDE, if using that):

```
U-Boot 2015.01-00055-g7aba6ad (Nov 19 2015 - 14:46:03)

Clock Configuration:
       CPU0(A53):1600 MHz  CPU1(A53):1600 MHz  CPU2(A53):1600 MHz
       CPU3(A53):1600 MHz
       Bus:      400  MHz  DDR:      1600 MT/s  FMAN:     500  MHz

Reset Configuration Word (RCW):
       00000000: 08100010 0a000000 00000000 00000000
       00000010: 14550002 80004012 e0025000 c1002000
       00000020: 00000000 00000000 00000000 00038800
       00000030: 00000000 00001101 00000096 00000001

Board: LS1043ARDB, boot from vBank 0
CPLD:  V1.4
PCBA:  V2.0

SERDES Reference Clocks:
SD1_CLK1 = 156.25MHZ, SD1_CLK2 = 100.00 MHz

I2C:   ready
DRAM:  2 GiB (DDR4, 32-bit, CL=12, ECC off)
Waking secondary cores to start from fff2a000
All (4) cores are up.
```

```
Using SERDES1 Protocol: 5205 (0x1455)
fman_port_enet_if:71: port(FM1_DTSEC3) is OK
fman_port_enet_if:77: port(FM1_DTSEC4) is OK
Flash: 128 MiB
NAND:  512 MiB
MMC:   FSL_SDHC: 0
EEPROM: NXID v1
PCIe1: disabled
PCIe2: Root Complex no link, regs @ 0x3500000
PCIe3: Root Complex no link, regs @ 0x3600000
In:    serial
Out:   serial
Err:   serial
Net:   Fman1: Uploading microcode version 108.4.15
FM1@DTSEC1, FM1@DTSEC2, FM1@DTSEC3, FM1@DTSEC4, FM1@DTSEC5, FM1@DTSEC6, FM1@TGEC1
Hit any key to stop autoboot:  0
=>
```

NOTE

U-Boot is updated frequently; therefore, the details given above may change slightly over a period of time.

4.3 Restart board

To restart or reset the system, use the reset button next to the UART port (RJ45 without LED).

5 Switch configurations

In the LS1043ARDB, the configuration switches are arranged along the edge of the board. Use the following figure as a reference.

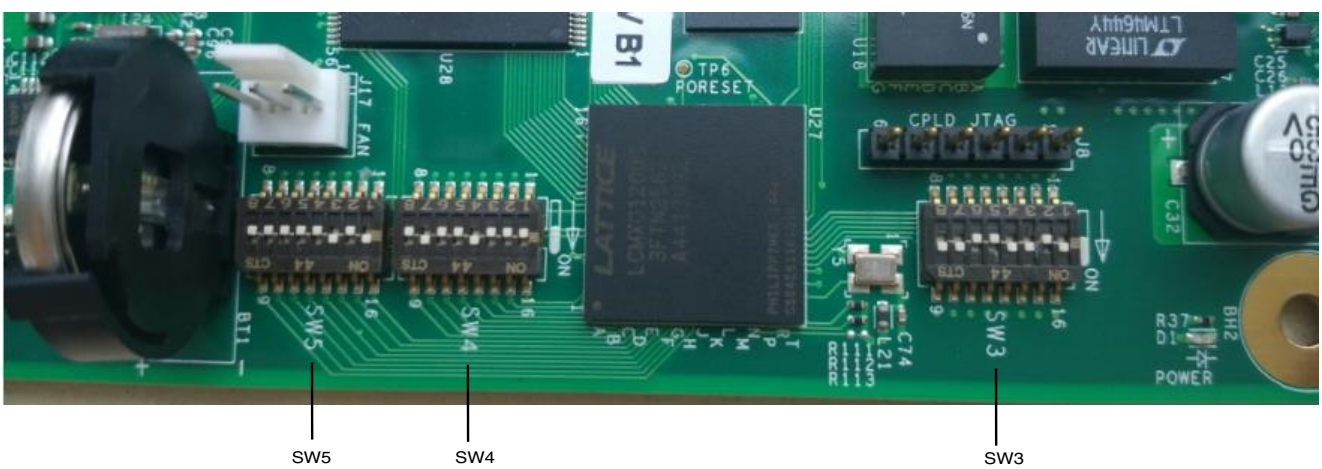

Figure 3. DIP switch locations

With the board positioned as shown above, switches read "SW5 SW4 SW3" moving from left to right. For these types of DIP switches:

- When a switch is up (OFF), the value is 0
- When a switch is down (ON), the value is 1

5.1 SW3 configuration

The figure below shows the SW3 switch on the LS1043ARDB.

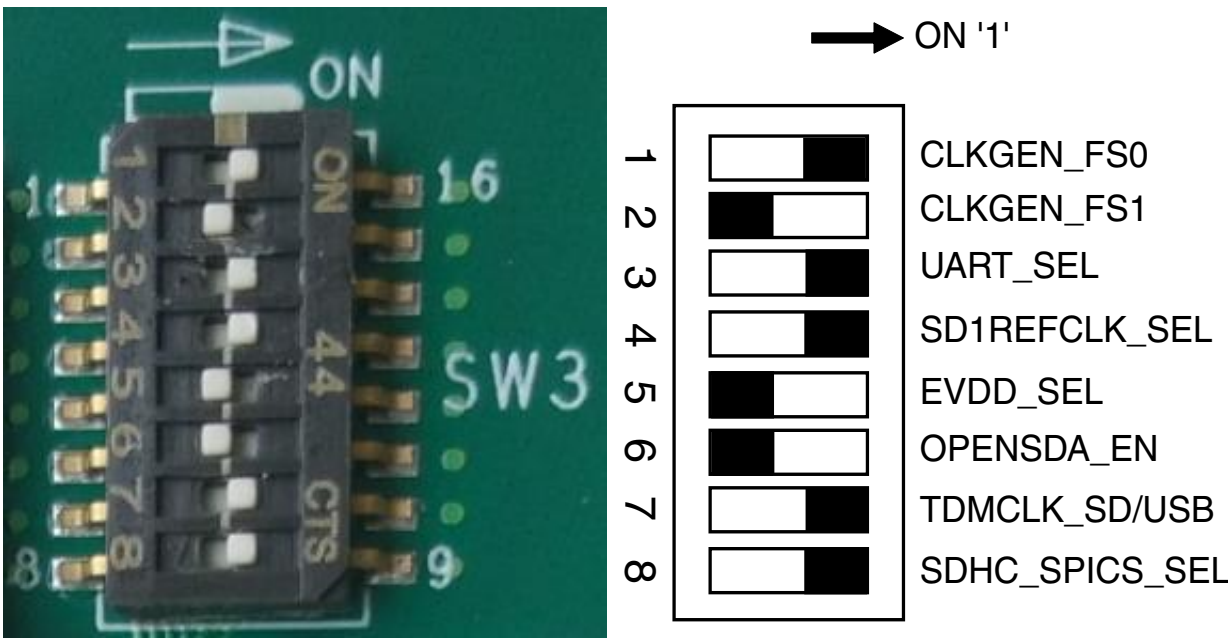

Figure 4. SW3 switch

The table below describes the SW3 configuration.

Table 2. SW3 configuration

Switch	Name	Description	ON (1) / OFF (0) setting
SW3[1]	CLKGEN_FS0	SYSCLK frequency select • 00: 66.66 MHz • 01: 80 MHz • 10: 100 MHz (default value) • 11: 83 MHz	1
SW3[2]	CLKGEN_FS1		0
SW3[3]	UART_SEL	UART1 output select • 0: RJ45, J4 lower one • 1: CMSISDAP, mini-USB port (default value)	1
SW3[4]	SD1REFCLK_SEL	SD1 REFCLK select • 0: 100 MHz (default value for the LS1021A interposer) • 1: 156.25 MHz (default value for the LS1043A processor)	1
SW3[5]	EVDD_SEL	EVDD voltage select • 0: 3.3 V (default value) • 1: 1.8 V	0

Table continues on the next page...

Table 2. SW3 configuration (continued)

Switch	Name	Description	ON (1) / OFF (0) setting
SW3[6]	OPENSDA_EN	CMSISDAP JTAG forced disable • 0: JTAG can be used by header or CMSISDAP (default value) • 1: CMSISDAP JTAG is forced to be disabled	0
SW3[7]	TDMCLK_SDHC/USB	TDM CLK or SDHC/USB select • 0: TDM CLK • 1: SDHC/USB (default value)	1
SW3[8]	SDHC_SPICS	SDHC_DAT[4:7] or SPI_CS select • 0: SDHC • 1: SPI_CS (default value)	1

5.2 SW4 configuration

The figure below shows the SW4 switch on the LS1043ARDB.

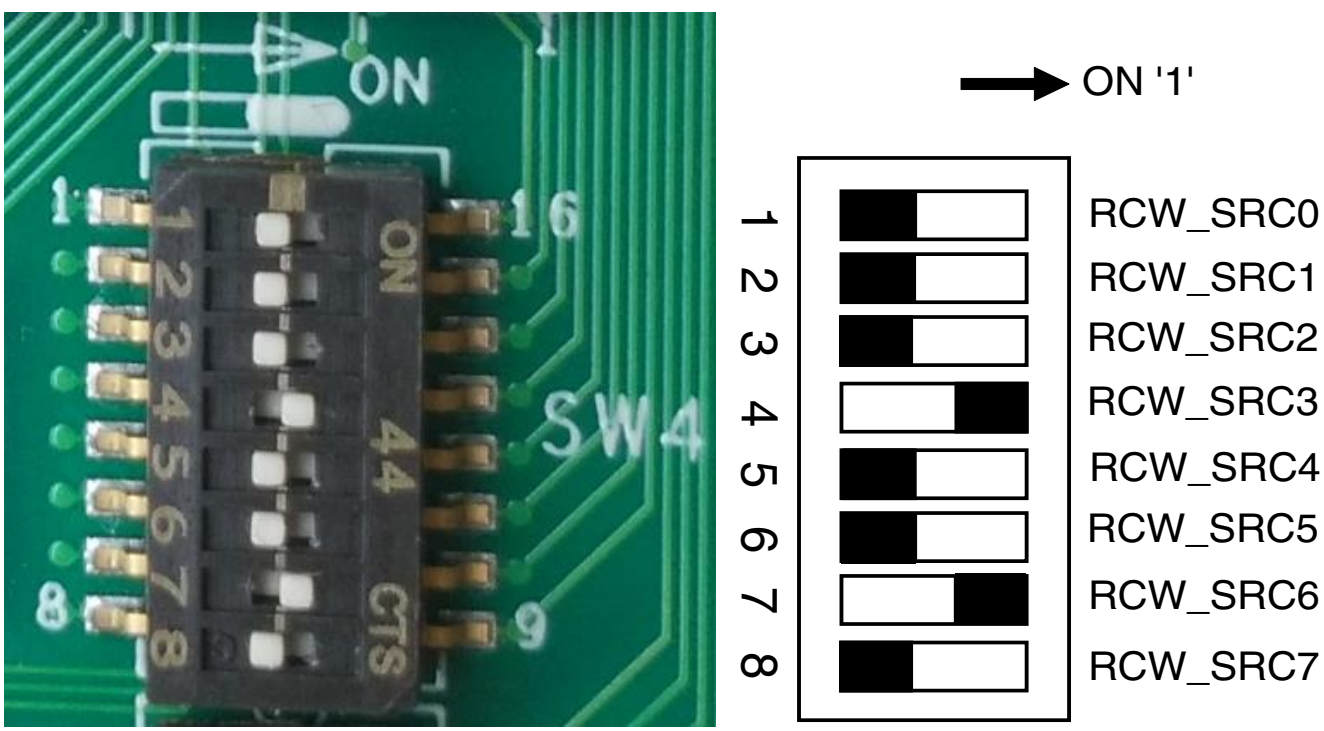

Figure 5. SW4 switch

The table below describes the SW4 configuration.

Table 3. SW4 configuration

Switch	Name	Description	ON (1) / OFF (0) setting
SW4[1]	RCW_SRC0	RCW_SRC[0:8] select • 0_0010_0101: 16-bit NOR (default value) • 0_0100_0000: SDHC/eMMC • 0_1001_1011: Hardcoded RCW • 1_0000_0110: 8-bit NAND flash, 2 KB page, 64 pages/block **NOTE:** The RCW_SRC field (9 bits) is spread over SW4 and SW5.	0
SW4[2]	RCW_SRC1		0
SW4[3]	RCW_SRC2		0
SW4[4]	RCW_SRC3		1
SW4[5]	RCW_SRC4		0
SW4[6]	RCW_SRC5		0
SW4[7]	RCW_SRC6		1
SW4[8]	RCW_SRC7		0
SW5[1]	RCW_SRC8		1

5.3 SW5 configuration

The figure below shows the SW5 switch on the LS1043ARDB.

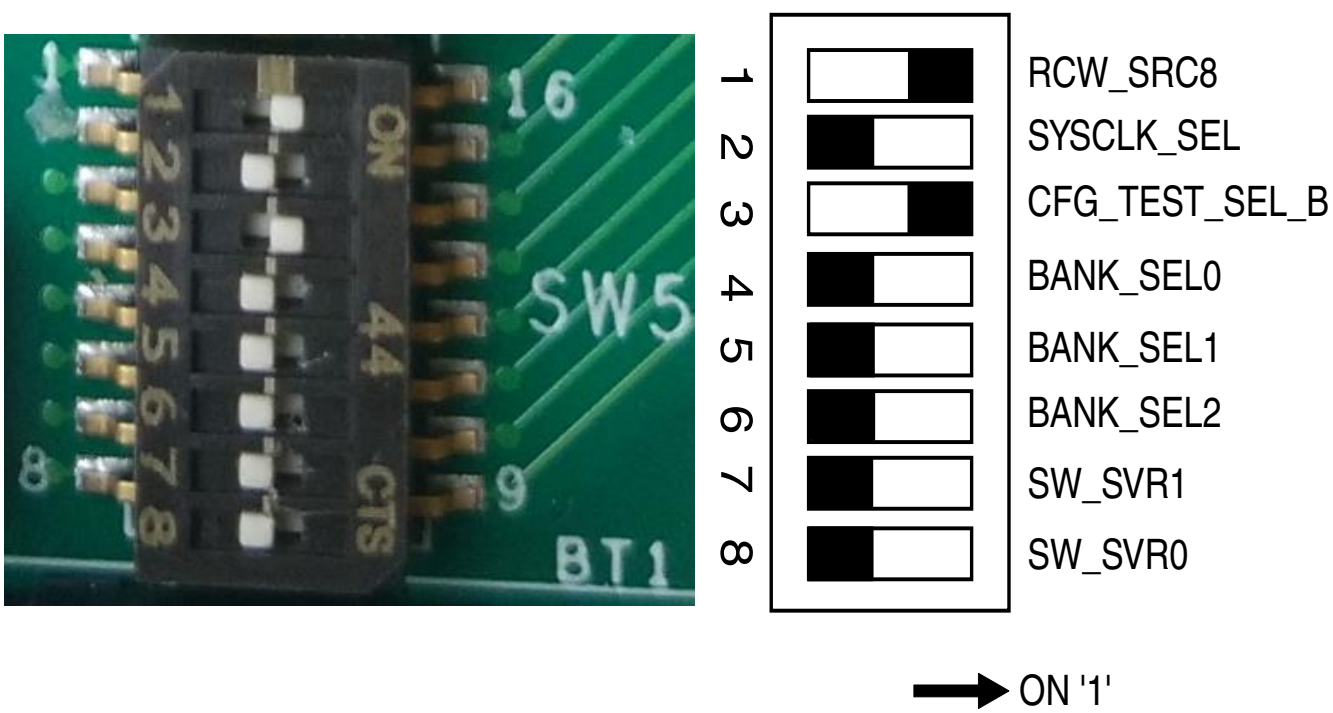

Figure 6. SW5 switch

The table below describes the SW5 configuration.

Table 4. SW5 configuration

Switch	Name	Description	ON (1) / OFF (0) setting
SW5[2]	SYSCLK_SEL	Differential SYSCLK select • 0: Differential SYSCLK (default value) • 1: Single-end system clock	0
SW5[3]	CFG_TEST_SEL_B	CFG_TEST_SEL for the LS1043A processor • 0: Disables cores 3 and 4 • 1: Enables all cores (default value)	1
SW5[4]	BANK_SEL0	Virtual bank select • 000: No change (default value) • 001: Virtual bank #1 • … … • 111: Virtual bank #7	0
SW5[5]	BANK_SEL1		0
SW5[6]	BANK_SEL2		0
SW5[7]	SW_SVR1	SVR[1:0] • 00: Reserved (default value for LS1043A)	0
SW5[8]	SW_SVR0		0

6 Jumper settings

The table below lists the factory default jumper settings for the LS1043ARDB.

Table 5. LS1043ARDB jumper settings

Jumper	Size	Name/function	Description
J5	1x2 pin	Remote reset	• Open: No activity (default value) • Shorted: Reset the board
J6	1x2 pin	Power switch	• Open: Power switch is functional (default value) • Shorted: Power switch is disabled
J9[1]	1x3 pin	SPICS and SDHC Dat[4:7] voltage selection	• 1-2 shorted: 1.8 V (default value) • 2-3 shorted: 3.3 V
J10	1x2 pin	FA_VL pin voltage setting	• Open: GND • Shorted: 1.0 V (default value)
J12	1x2 pin	PWR_PROG_MTR voltage setting	• Open: GND (default value) • Shorted: 1.8 V
J13	1x2 pin	PWR_PROG_SFP voltage setting	• Open: GND (default value) • Shorted: 1.8 V
J14	1x2 pin	TA_BB_VDD voltage setting	• Open: GND • Shorted: 1.0 V (default value)
J15[1]	1x3 pin	SPI bus voltage setting	• 1-2 shorted: 1.8 V (default value) • 2-3 shorted: 3.3 V
J22	1x3 pin	External power for power amplifier (PA) voltage for some Wi-Fi cards	• 1-2 shorted: 3.3 V (default value) • 2-3 shorted: 5.0 V

1. J9 and J15 only exist on the SCH-28529 Rev. A1 board.

The figure below shows the jumper locations.

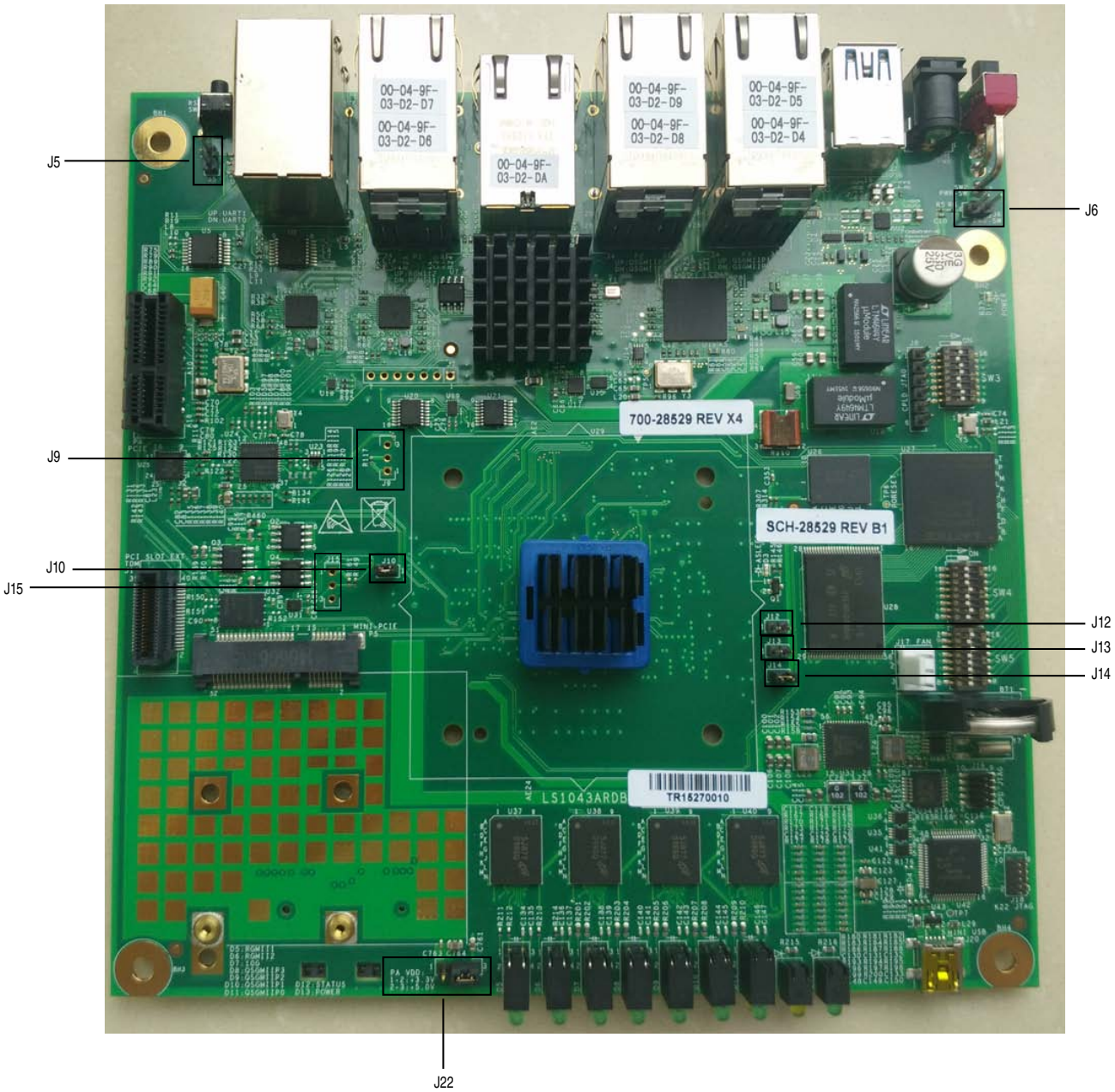

Figure 7. LS1043ARDB jumper locations

7 Interfaces

This section describes the interfaces for the LS1043ARDB.

7.1 UART interfaces

The LS1043ARDB supports two UART interfaces, UART1 and UART2. You can use UART1 as a console port. On the LS1043ARDB, you can use UART1 in two ways:

- Route UART1 to the RJ45 connector
- Route UART1 to the CMSISDAP circuit, which can be used on the mini-USB port

SW3[3] is used to select UART1. The figure below shows UART1 connection using the RJ45 connector when SW3[3] is OFF.

Figure 8. UART1 connection using RJ45 connector

The figure below shows UART1 connection using mini-USB when SW3[3] is ON.

Figure 9. UART1 connection using mini-USB

7.2 Ethernet interfaces

The LS1043ARDB has six 100M/1G Ethernet ports (four QSGMII ports and two RGMII ports) and one 10G Ethernet port. Connection is made directly using an RJ45 connector. Connect an appropriate cable (CAT 5E or better) between the RJ45 and target system. Auto-crossover is supported so that loopback testing between any two ports can be done.

The figure below shows the Ethernet ports available on the LS1043ARDB.

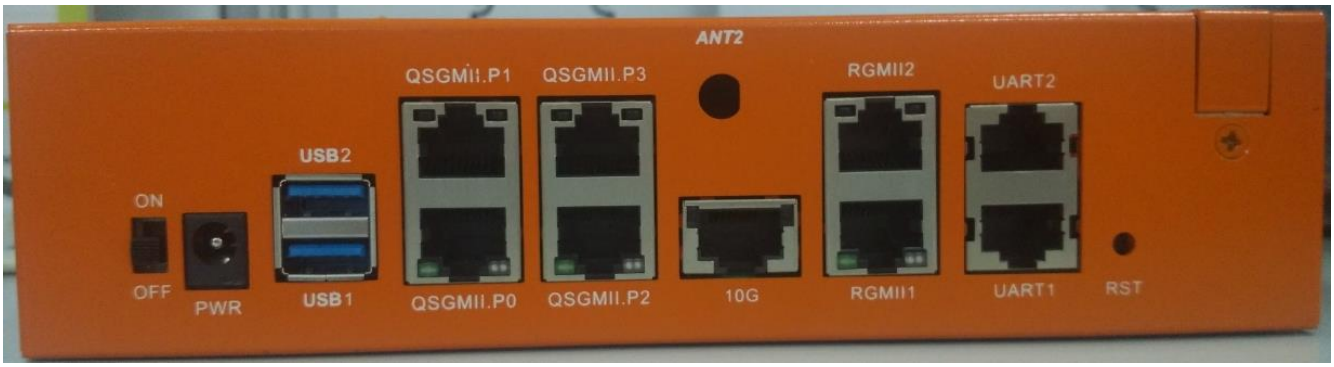

Figure 10. Ethernet connection

The table below shows a mapping between the Ethernet port names printed on the chassis and port names used in Linux.

Table 6. Ethernet port mapping

Port name on chassis	Port name in Linux
QSGMII.P0	eth0
QSGMII.P1	eth1
QSGMII.P2	eth4
QSGMII.P3	eth5
RGMII1	eth2
RGMII2	eth3
10G	eth6

7.3 PCI express cards

The LS1043ARDB supports one peripheral component interconnect (PCI) express slot and one mini-PCI express slot. Install the desired device in the appropriate slot.

NOTE

The PCI express card images shown in this section are only for demonstration purposes. These cards are not provided with the LS1043ARDB hardware kit.

7.3.1 Standard PCI express card installation

The figure below shows how to install a standard PCI express card on the LS1043ARDB.

Figure 11. Standard PCI express card installation

7.3.2 Mini-PCI express card installation

To install a mini-PCI express card on the LS1043ARDB, perform these steps:

1. Add the soft thermal pad, available in the LS1043ARDB hardware kit, on the LS1043ARDB, before you install a Wi-Fi card on the board (see figure below).

Figure 12. Soft thermal pad installation

2. Attach the mini-PCI express card to the LS1043ARDB, as shown in the figure below.

Figure 13. Mini-PCI express card installation

7.4 TDM riser card

The LS1043ARDB supports the Freescale time-division multiplexing (TDM) riser card (part number: TDM-DS26522). You need to use an adapter board (part number: X-TDM-ADP) to install the TDM riser card on the LS1043ARDB.

NOTE

The TDM riser card and adapter board are not provided with the LS1043ARDB hardware kit. To order them, contact your Freescale representative.

The figure below shows how to install a TDM riser card on the LS1043ARDB.

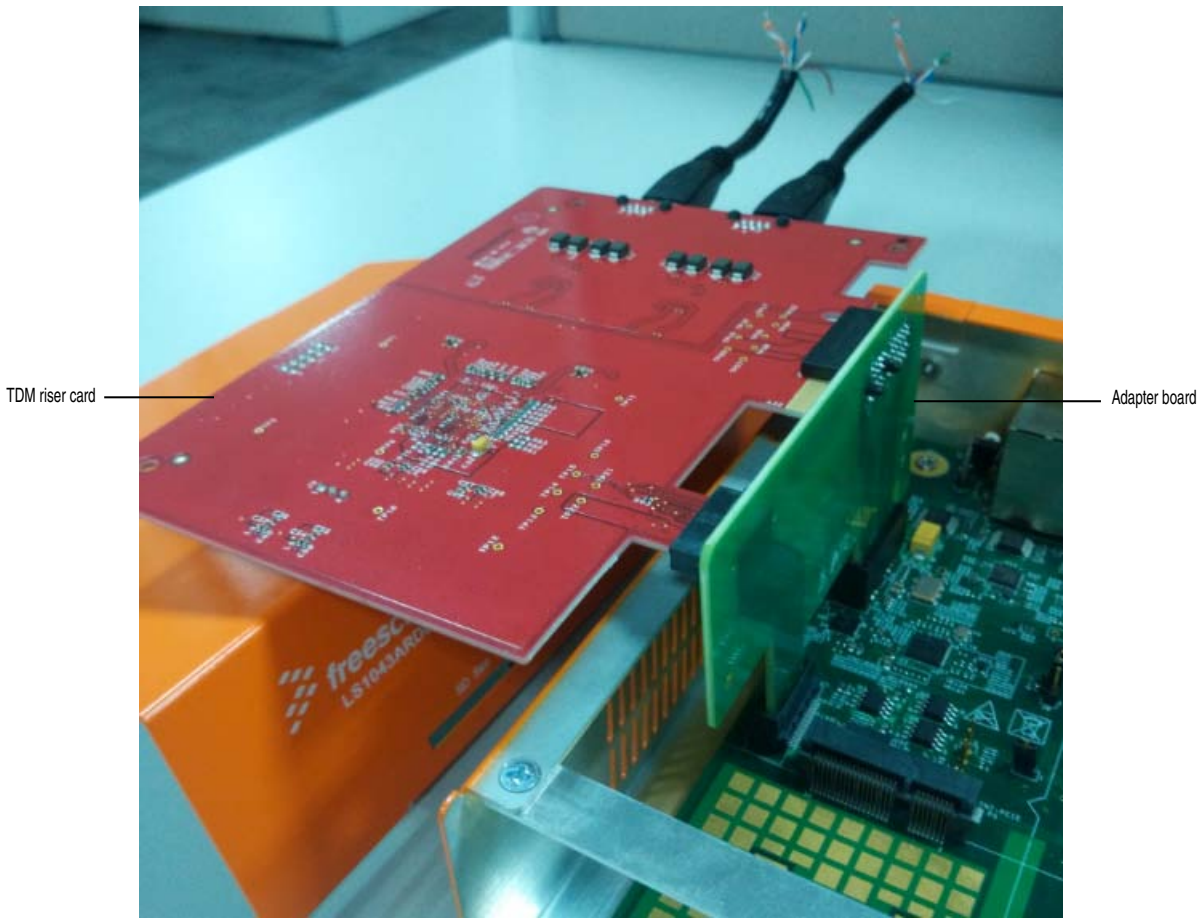

Figure 14. TDM card installation

8 Connectors

The table below lists the connectors available on the LS1043ARDB.

Table 7. LS1043ARDB connectors

Connector	Description	Connector type	Typical connection
SW2	DC power switch	3-pin ON/OFF switch	Turns power ON/OFF
J1	12 V power jack	DC power jack	Connects to 12 V, 5 A power supply
J8	CPLD JTAG	6-pin JTAG header	Connects to the CPLD programmer
J16	CPU JTAG	2x5-pin ARM JTAG header	Connects to the CodeWarrior TAP
J18	K22 MCU JTAG	2x5-pin ARM JTAG header	Connects to the JLINK emulation
P5	Mini-PCIe slot	52-pin mini-PEX socket	-open-
P4	PCIe slot	36-pin X1 PEX socket	-open-

Table continues on the next page...

Table 7. LS1043ARDB connectors (continued)

Connector	Description	Connector type	Typical connection
J20	Mini-USB to UART1	5-pin mini-USB port	Connects to the computer
J21	SD slot. SD slot is located on the bottom side of the PCB.	28-pin full SD slot	-open-
J17	Chassis fan	1x3-pin header	-open-
J11	TDM slot	2x20-pin connector	-open-
SW1	Reset key	4-pin reset switch	-open-
J4	DUART	2x8-pin RJ45 connector • UART2: Top • UART1: Bottom	Connects to the RJ45 to DB9 serial cable
P1	10/100/1000M Ethernet ports	2x8-pin RJ45 connector • RGMII2: Top • RGMII1: Bottom	-open-
J3	10G Ethernet port	19-pin RJ46 connector	-open-
P2	QSGMII Ethernet ports	2x8-pin RJ45 connector • Port 3: Top • Port 2: Bottom	-open-
P3	QSGMII Ethernet ports	2x8-pin RJ45 connector • Port 1: Top • Port 0: Bottom	-open-
J2	USB3.0 ports	18-pin dual USB3.0 connector • USB1: Top • USB2: Bottom	-open-
BT1	RTC battery	3-pin battery holder	Connects to 3 V coin battery

The figure below shows the connector locations on the LS1043ARDB.

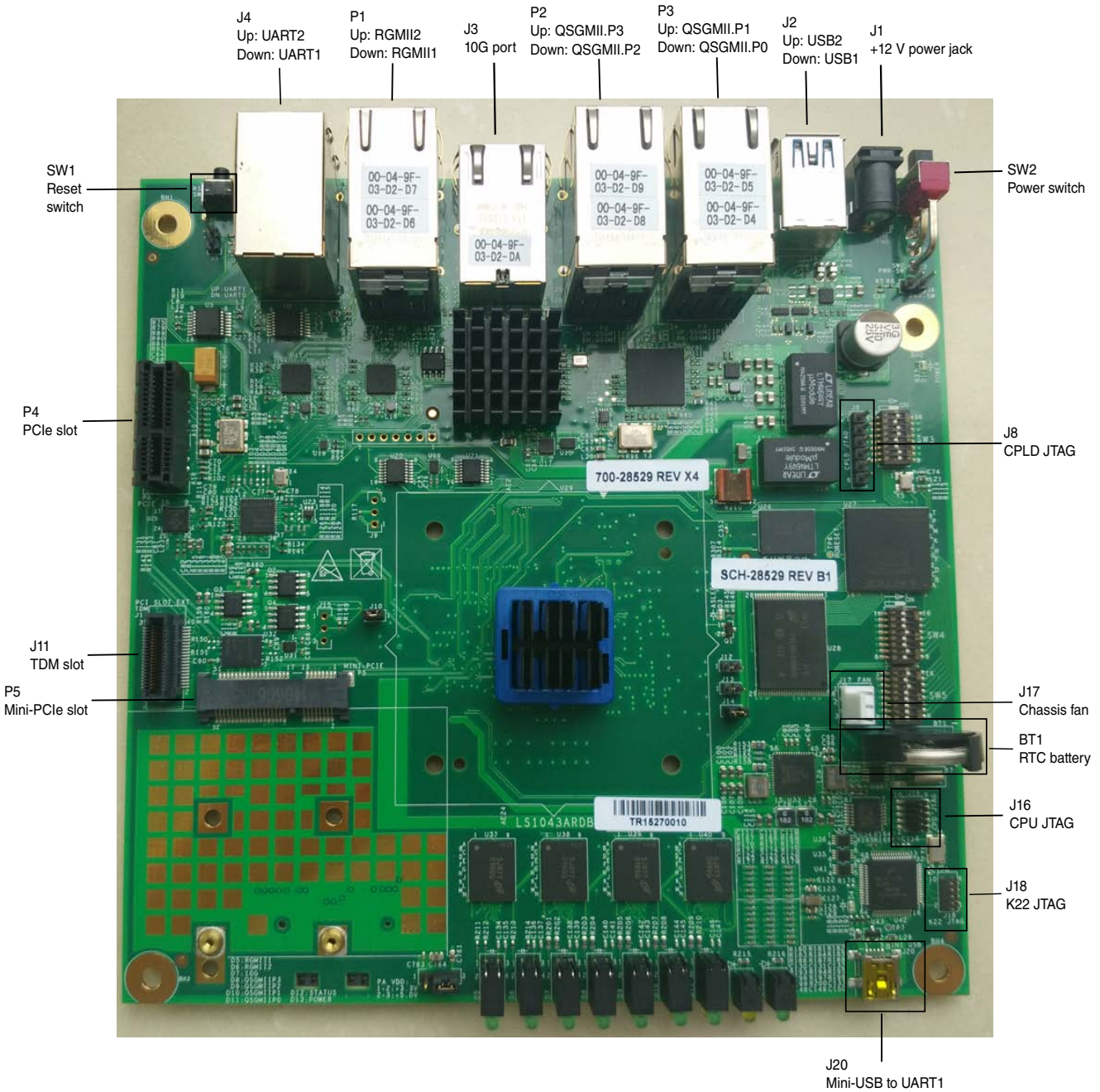

Figure 15. Connector locations on LS1043ARDB

9 Push and slide buttons

The table below describes the functions of the LS1043ARDB push button and slide switch.

Table 8. LS1043ARDB push and slide buttons

Push/slide button	Label	Function	Description
SW1	RESET	System reset	Press SW1 to reset the system, including the device and all attached peripherals.
SW2	PWR	Power cycle	Slide SW2 to turn the power on or off. **NOTE:** If J6 is shorted, to force power on, then SW2 will have no effect.

The figure below shows the push/slide button locations.

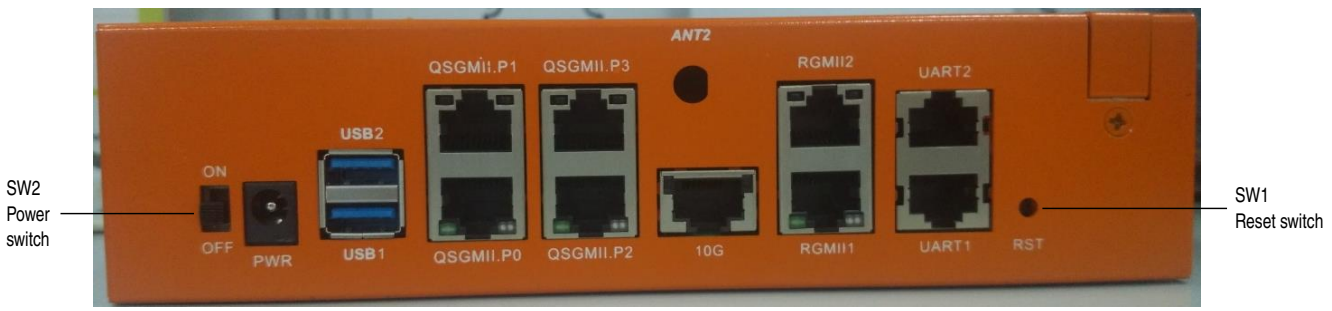

Figure 16. LS1043ARDB buttons

10 LED indicators

The table below explains the light emitting diodes (LEDs) on the LS1043ARDB.

Table 9. LS1043ARDB LEDs

LED	Color	Positioned on	Name	Description
D1	Green	PCB	Power LED (3.3 V)	• OFF: 3.3 V power is OFF • ON: 3.3 V power is supplied
D2	RED	PCB	AQR105 GPIO	TBD
D3	Green	PCB	ASLEEP	• ON: If the processor is not configured properly, or if the RCW contents are not correct • OFF: RCW is fetched
D4	Green	PCB	K22	• ON: CMSISDAP firmware is loaded • OFF: CMSISDAP firmware is not loaded
D5	Yellow/Green	Chassis	RGMII1	• Green: RGMII1 link • Yellow: RGMII1 activity
D6	Yellow/Green	Chassis	RGMII2	• Green: RGMII2 link • Yellow: RGMII2 activity
D7	Yellow/Green	Chassis	10G	• Green: AQR105 10G PHY link • Yellow: AQR105 10G PHY activity
D8	Yellow/Green	Chassis	QSGMII.P3	• Green: QSGMII P3 link • Yellow: QSGMII P3 activity

Table continues on the next page...

Table 9. LS1043ARDB LEDs (continued)

LED	Color	Positioned on	Name	Description
D9	Yellow/Green	Chassis	QSGMII.P2	• Green: QSGMII P2 link • Yellow: QSGMII P2 activity
D10	Yellow/Green	Chassis	QSGMII.P1	• Green: QSGMII P1 link • Yellow: QSGMII P1 activity
D11	Yellow/Green	Chassis	QSGMII.P0	• Green: QSGMII P0 link • Yellow: QSGMII P0 activity
D12	Yellow	Chassis	Status LED	Defined in the CPLD register
D13	Green	Chassis	Power LED (3.3 V)	• OFF: 3.3 V power is OFF • ON: 3.3 V power is supplied

The figure below shows the LED locations on the LS1043ARDB.

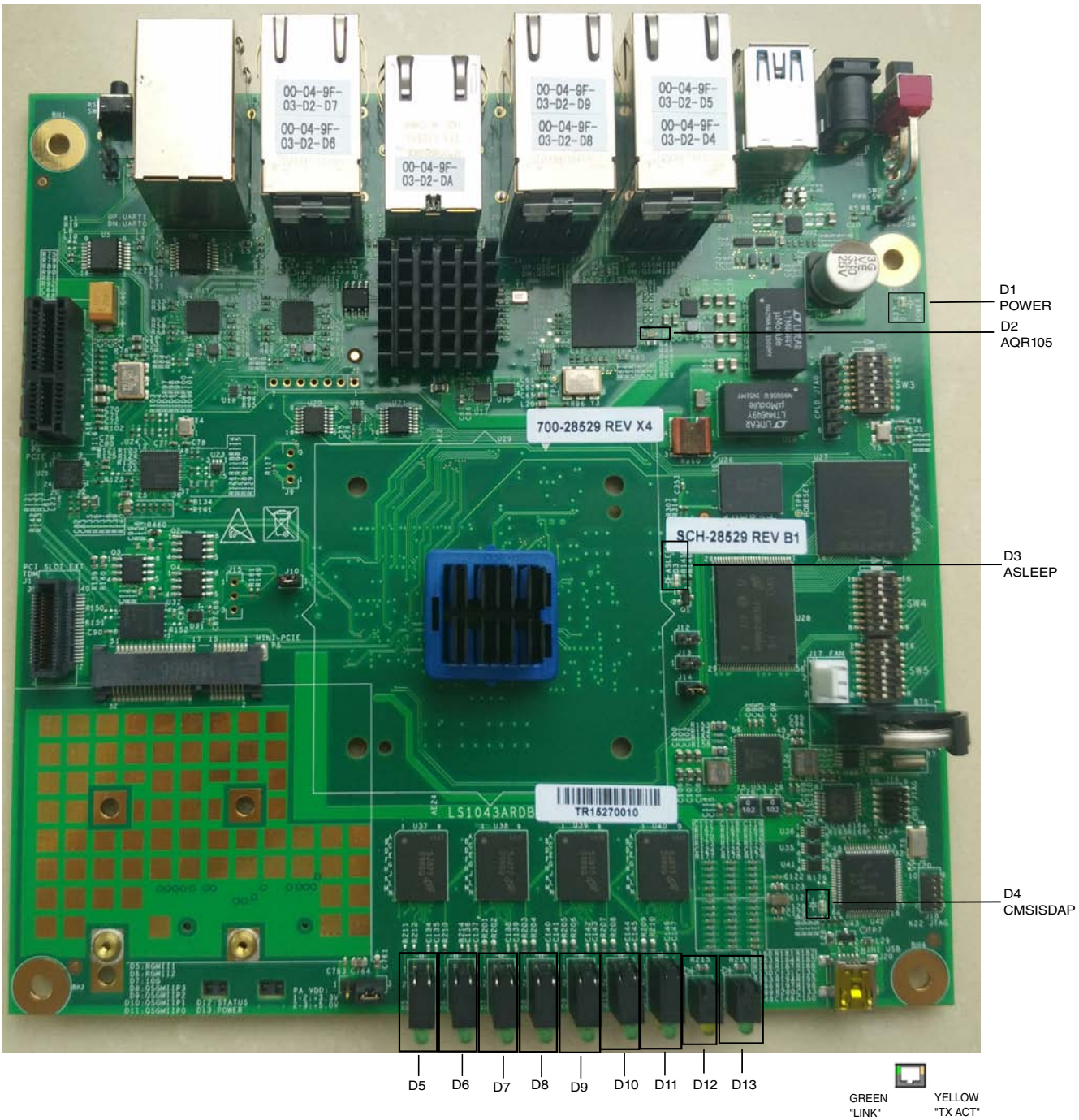

Figure 17. LS1043ARDB LED locations

11 Setting up CodeWarrior TAP

The CodeWarrior TAP allows you to debug and control of the LS1043ARDB system using the CodeWarrior IDE.

NOTE

No CodeWarrior TAP is included in the LS1043ARDB hardware kit.

Follow the instructions provided with the CodeWarrior package to set up the environment and attach the host (for example, USB or Ethernet)

To attach the CodeWarrior TAP to the LS1043ARDB, follow the steps below:

1. Install the 10-pin micro adapter provided with the CodeWarrior TAP (CWH-CTP-CTX10-YE).
2. Connect the 10-wire cable as shown in the figure below (both ends are keyed and can be installed on either side).

Figure 18. CodeWarrior installation

3. Install the free end of the cable to J16 on the LS1043ARDB.

NOTE

The connector is keyed to prevent reversal. When properly aligned, the red stripe will be nearest to the board edge.

The CodeWarrior TAP is now ready to be used. Follow the instructions provided with the CodeWarrior package to complete the IDE setup.

12 LS1043ARDB operating configurations

The table below shows the default LS1043ARDB operating voltages.

Table 10. LS1043ARDB operating voltages

Supply voltages	Description	Voltage value
AVDD_CGA1, AVDD_CGA2, AVDD_PLAT, AVDD_D1	Supply voltages (core/platform/DDR) for PLLs	1.8 V

Table continues on the next page...

Table 10. LS1043ARDB operating voltages (continued)

Supply voltages	Description	Voltage value
AVDD_SD1_PLL1, AVDD_SD1_PLL2	Supply voltages (filtered from XVDD) for SerDes PLLs 1 and 2	1.35 V
G1VDD voltage	I/O supply voltage for DDR DRAM	1.2 V
S1VDD voltage	Core power supply for the SerDes transceivers	1.0 V
X1VDD voltage	Pad power supply for the SerDes transceivers	1.35 V
OVDD voltage	General I/O supply: Used for GPIO1, GPIO2, DSPI, eSDHC[4:7], SYSCLK, DDRCLK, and IFC system control and power management, clocking, debug, and JTAG I/O	1.8 V
LVDD voltage	Ethernet supply voltage	1.8 V
DVDD voltage	Supply voltage for DUART, I2C, DMA, QE, GPIO1, GPIO4, and USB control	3.3 V
EVDD voltage	Supply voltage for eSDHC[0:3]/CLK/CMD and GPIO2	3.3 V / 1.8 V
TVDD voltage	Supply voltage for Ethernet management interface 2 (EMI2) and GPIO4	1.2 V
2V5 voltage	AQR105 VDD_IO supply voltage	2.5 V
FA_VL voltage	Reserved for internal use	0 V / (1.0 V - optional)
PROG_MTR	Reserved for internal use	0 V / (1.8 V - optional)
PROG_SFP	Security fuse programming override supply	0 V / (1.8 V - optional)
TH_VDD	Thermal monitor unit supply	1.8 V
TA_BB_VDD voltage	Low power security monitor supply	1.0 V
VDD	Core and platform supply	1.0 V
USB_SVDD1 and 2	USB PHY analog supply	1.0 V
USB_SDVDD1 and 2	USB PHY digital supply	1.0 V
USB_HVDD1 and 2	USB PHY transceiver supply	3.3 V
VPP voltage	DDR1, 2, and 3 activating power supply	2.5 V
VREF (DDR VREF voltage)	DDR VREF voltage power supply	0.6 V
VTT1 (DDR3_VTT voltage)	DDR3 termination voltage power supply	0.6 V

The table below shows the default LS1043ARDB clock rates.

Table 11. LS1043ARDB clock rates

Clock	Description	Frequency
Core clock	Depends on RCW	1600 MHz
Platform clock	Depends on RCW	400 MHz
SYSCLK (differential or single-end SYSCLK)	System clock	100 MHz
RTC CLK	Real-time clock	32.768 kHz
DDR CLK	DDR clock	100 MHz
SD1_REF1 CLK	SerDes1 reference clock 1	156.25 MHz
SD1_REF2 CLK	SerDes1 reference clock 2	100 MHz

13 NOR flash memory map

The table below shows the NOR flash memory map.

Table 12. NOR flash memory map

Memory address range	Device	Memory size
0x0_6000_0000 - 0x0_600F_FFFF	RCW + PBI	1 MB
0x0_6010_0000 - 0x0_601F_FFFF	U-Boot	1 MB
0x0_6020_0000 - 0x0_602F_FFFF	U-Boot environment	1 MB
0x0_6030_0000 - 0x0_603F_FFFF	FMan microcode	1 MB
0x0_6040_0000 - 0x0_604F_FFFF	UEFI	1 MB
0x0_6050_0000 - 0x0_605F_FFFF	PPA	1 MB
0x0_6060_0000 - 0x0_606F_FFFF	QE firmware	1 MB
0x0_6070_0000 - 0x0_60EF_FFFF	Reserved	8 MB
0x0_60F0_0000 - 0x0_60FF_FFFF	PHY firmware	1 MB (not used)
0x0_6100_0000 - 0x0_610F_FFFF	Reserved	1 MB
0x0_6110_0000 - 0x0_638F_FFFF	FIT image	40 MB
0x0_6390_0000 - 0x0_63FF_FFFF	Unused	7 MB
0x0_6400_0000 - 0x0_640F_FFFF	RCW + PBI	1 MB
0x0_6410_0000 - 0x0_641F_FFFF	U-Boot	1MB
0x0_6420_0000 - 0x0_642F_FFFF	U-Boot environment	1 MB
0x0_6430_0000 - 0x0_646F_FFFF	FMan microcode	1 MB
0x0_6440_0000 - 0x0_644F_FFFF	UEFI	1 MB
0x0_6450_0000 - 0x0_645F_FFFF	PPA	1 MB
0x0_6460_0000 - 0x0_646F_FFFF	QE firmware	1 MB
0x0_6470_0000 - 0x0_64EF_FFFF	Reserved	14 MB
0x0_64F0_0000 - 0x0_64FF_FFFF	PHY firmware	1 MB (not used)
0x0_6500_0000 - 0x0_650F_FFFF	Reserved	1 MB
0x0_6510_0000 - 0x0_678F_FFFF	FIT image	40 MB
0x0_6790_0000 - 0x0_67FF_FFFF	Unused	7 MB

14 Revision history

The table below summarizes revisions to this document.

Table 13. Revision history

Revision	Date	Topic cross-reference	Change description
Rev. 1	11/2015	Power up and use board	Updated console output
		TDM riser card	Added as a new section

Table continues on the next page...

Table 13. Revision history (continued)

Revision	Date	Topic cross-reference	Change description
		LS1043ARDB operating configurations	Changed core clock frequency from 1500 MHz to 1600 MHz in Table 11
Rev. 0	08/2015		Initial public release

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