MAX32620/MAX32621 High-Performance, Ultra-Low Power Cortex-M4F Microcontroller for Rechargeable Devices

General Description

The MAX32620/MAX32621 is a 32-bit RISC ARM® Cortex®-M4F (M4 plus Floating Point Unit) microcontroller. It is ideally suited for the emerging category of medical and fitness applications. The architecture combines high-efficiency, signal-processing functionality with low cost, and ease of use. The device features 4 powerful & flexible power modes. Built-in dynamic clock gating and firmware controlled power gating minimize power consumption for any application. Multiple SPI, UART, and I2C serial interfaces, as well as a 1-Wire® master and USB, allow for interconnection to a wide variety of external sensors. A four-input, 10-bit ADC with selectable references is provided.

The MAX32621 is a secure version of the MAX32620, incorporating a trust protection unit (TPU) with encryption and advanced security features.

Applications

- Sport Watches
- Fitness Monitors
- Wearable Medical Patches
- Portable Medical Devices
- Sensor Hub

Benefits and Features

- High-Efficiency Microcontroller for Rechargeable Devices
  - Internal Oscillator Operates Up to 96MHz
  - Floating Point Unit
  - Memory Protection Unit
  - 2MB Flash Memory
  - 256KB SRAM
  - 8KB Instruction Cache
  - 1.2V ±5% Core Supply Voltage
  - 1.8V ±5% I/O and Analog Supply Voltage
  - Optional 3.3V ±5% USB Supply Voltage
- Tiny 81-Ball WLP Minimizes Board Space (3.9mm x 3.9 mm WLP, 0.4 mm Pitch)
- Power Management Maximizes Uptime for Battery Applications
  - 95µA/MHz Active Executing from Flash
  - 600nA Low Power (LP0) Mode with RTC Enabled
  - 2.5µA Ultra-Low Power Data Retention Mode (LP1) with Fast 5µs (typ) Wakeup to 96MHz
  - Peripheral Management Unit (PMU) Reduces Power Consumption in Measurement Mode (LP2)
- Optimal Peripheral Mix Provides Platform Scalability
  - Three SPI Masters, Four UARTs, Three I2C Masters, and One 1-Wire Master
  - 49 General-Purpose I/O Pins
  - SPI Execute in Place Engine for Memory Expansion with Minimal Footprint
  - Full-Speed USB 2.0 with Internal Transceiver
  - Sixteen Pulse Train Engines
  - Four-Input, 10-Bit Sigma-Delta ADC Operating at 7.8 kS/s
- Trust Protection Unit (TPU) Secures Valuable IP and Data (MAX32621 Only)
  - Robust Hardware Internal Security
  - High-Speed Modular Arithmetic Accelerator (MAA) Supports Fast ECDSA
  - AES Hardware Engine
  - Hardware PRNG Entropy Generator
  - Secure Boot Loader

***Ordering Information*, and *Additional Features* appear at end of data sheet.**

19-7679; Rev 0; 6/15

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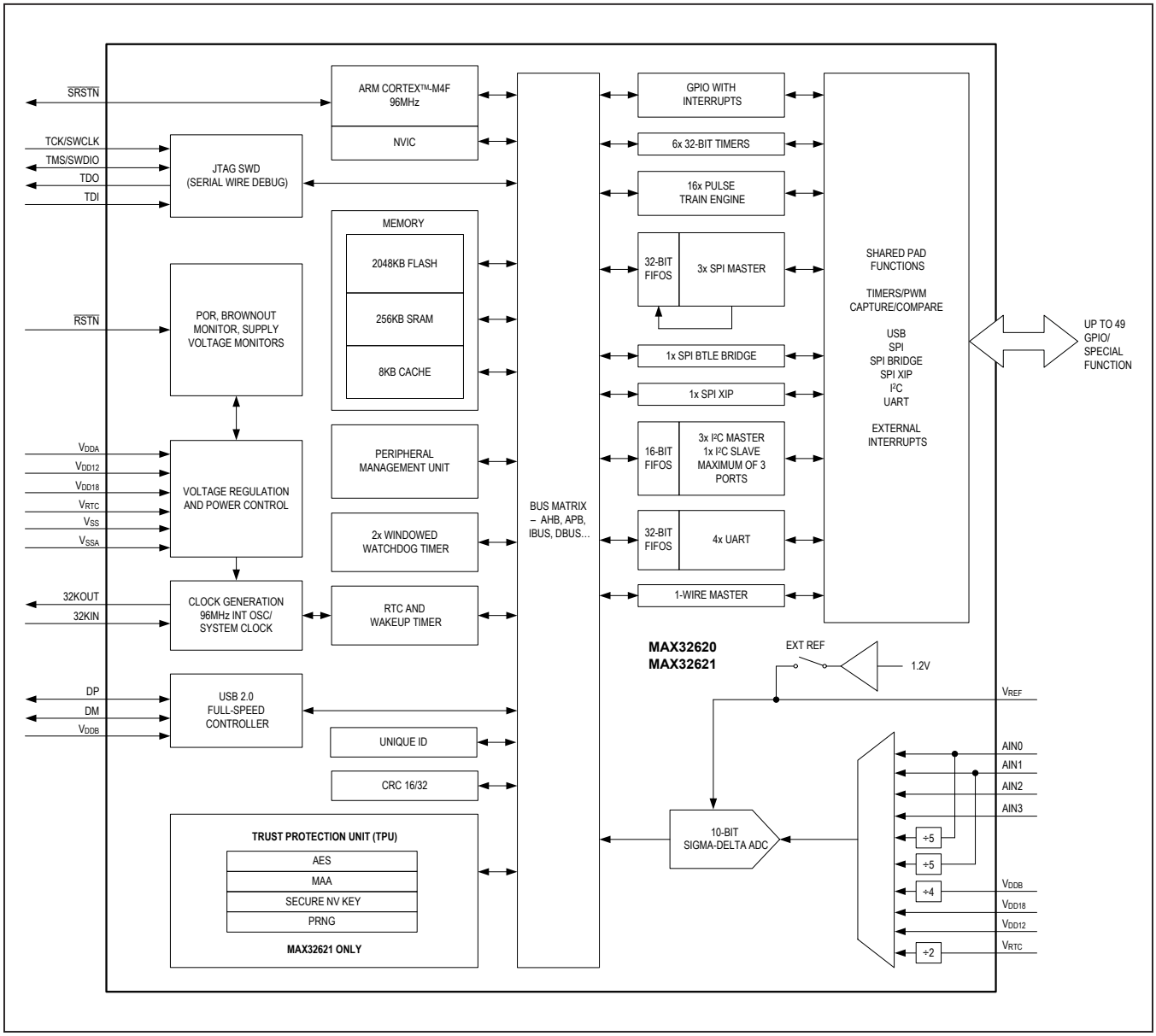
MAX32620/MAX32621 Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.)

V_{DD18} .....-0.3V to +1.89V
V_{DD12} .....-0.3V to +1.26V
V_{DDA} with respect to $V_{SS\backslash A}$ .....-0.3V to +1.89V
V_{RTC}.....-0.3V to +3.6V
V_{DDB} .....-0.3V to +3.6V
V_{REF}.....-0.3V to +3.6V
32KIN, 32KOUT.....-0.3V to +3.6V
RSTN, SRSTN, GPIO .....-0.3V to +3.6V
AIN[1:0].....-0.3V to +5.5V
AIN[3:2].....-0.3V to +3.6V

Total current into V_{DD18} (sink) 100mA
Total current into V_{SS}.....100mA
Output current (sink) by Any I/O pin..... 25mA
Output current (source) by Any I/O pin .....-25mA
Continuous Power Dissipation (T_A = +70°C)
TQFP (multilayer board)
(derate 45.5mW/°C above +70°C) 3636.4mW
Operating Temperature Range..... -20°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Package Thermal Characteristics (Note 1)

TQFP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....22°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD18}		1.71	1.8	1.89	V
	V_{DD12}		1.14	1.2	1.26	
	V_{DDA}		1.71	1.8	1.89	
	V_{RTC}		1.71	1.8	1.89	
	V_{DDB}		3.04	3.3	3.60	
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD18}	1.62		1.70	V
Power On Reset Voltage	V_{POR}	Monitors V_{DD18}		1.5		V
RAM Data Retention Voltage	V_{DRV}			0.94		V
V_{DD12} Dynamic Current, LP3 Mode	I_{DD12_DLP3}	Executing code from cache memory,		95		µA/MHz
V_{DD12} Current, LP3 Mode	I_{DD12_LP3}	System clock stopped		490		µA
V_{DD18} Current, LP3 Mode	I_{DD18_LP3}	Executing code from cache memory, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		360		µA

Electrical Characteristics (continued)

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{RTC} Current, LP3 Mode	I_{RTC_LP3}	RTC disabled		105		nA
		RTC enabled		805		nA
V_{DD12} Dynamic Current, LP2 Mode	I_{DD12_DLP2}	ARM in sleep mode, PMU with two channels active		27		µA/MHz
V_{DD12} Current, LP2 Mode	I_{DD12_LP2}	ARM in sleep mode, system clock stopped		490		µA
V_{DD18} Current, LP2 Mode	I_{DD18_LP2}	ARM in sleep mode, PMU with two channels active, all inputs are tied to V_{SS} or V_{DD18}, outputs do not source/sink any current		360		µA
V_{RTC} Current, LP2 Mode	I_{RTC_LP2}	RTC disabled		105		nA
		RTC enabled		805		nA
V_{DD12} Current, LP1 Mode	I_{DD12_LP1}	Standby state with full data retention		0		µA
V_{DD18} Current, LP1 Mode	I_{DD18_LP1}	Standby state with full data retention		2.5		µA
V_{RTC} Current, LP1 Mode	I_{RTC_LP1}	RTC disabled		105		nA
		RTC enabled		505		nA
V_{DD12} Current, LP0 Mode	I_{DD12_LP0}			0		nA
V_{DD18} Current, LP0 Mode	I_{DD18_LP0}			120		nA
V_{RTC} Current, LP0 Mode	I_{RTC_LP0}	RTC disabled		105		nA
		RTC enabled		505		nA
LP2 Mode Resume Time	t_{LP2_ON}			0		µs
LP1 Mode Resume Time	t_{LP1_ON}			5		µs
LP0 Mode Resume Time	t_{LP0_ON}			15		µs
CLOCKS						
Internal Relaxation Oscillator Frequency	f_{INTCLK}	Factory default	94.08	96.0	97.92	MHz
		Firmware trimmed, required for USB compliance	95.76	96.0	96.24	MHz
System Clock Frequency	f_{CK}		0.371		97.92	MHz
System Clock Period	t_{CK}			$1/f_{CK}$		

Electrical Characteristics (continued)

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RTC Input Frequency	f_{32KIN}	32kHz watch crystal (6pF)		32.768		kHz
RTC Power Up Time	t_{RTC_ON}			250		ms
GENERAL PURPOSE I/O						
Input Low Voltage for $\overline{RSTN}$, $\overline{SRSTN}$, and All Port Pins	V_{IL}				0.3 x V_{DD18}	V
Input High Voltage for $\overline{RSTN}$, $\overline{SRSTN}$, and All Port Pins	V_{IH}		0.7 x V_{DD18}			V
Input Hysteresis (Schmitt)	V_{IHYS}			100		mV
Output Low Voltage for All Port Pins	V_{OL}	I_{OL} = 4mA (normal drive)		0.2	0.4	V
		I_{OL} = 24mA (high drive)		0.2	0.4	V
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All Port Pins	V_{OH}	I_{OH} = -2mA (normal drive)	V_{DD18} - 0.4			V
		I_{OH} = -8mA (high drive)	V_{DD18} - 0.4			V
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				48	mA
Input/Output Pin Capacitance for All Port Pins	C_{IO}			5		pF
Input Leakage Current Low	I_{IL}	V_{DD18} = 1.89V V_{IN} = 0V, internal pullup disabled	-100		+100	nA
Input Leakage Current High	I_{IH}	V_{DD18} = 1.89V, V_{IN} = 1.89V, internal pulldown disabled	-100		+100	nA
	I_{OFF}	V_{DD18} = 0V, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DD18} = 1.71V, V_{IN} = 3.60V	-1		+1	µA
Input Pullup Resistor $\overline{RSTN}$, $\overline{SRSTN}$, TMS, TCK, TDI	R_{PU}			25		kΩ
Input Pullup/Pulldown All GPIO	R_{PU_GPIO}	Normal resistance mode		25		kΩ
		Highest resistance mode		1		MΩ
FLASH MEMORY						
Page Size				8		kB
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		ms
Flash Programming Time Per Word	t_{PROG}			60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years

USB Electrical Characteristics

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input High Voltage DP, DM	V_{IHD}		2.0			V
Single-Ended Input Low Voltage DP, DM	V_{ILD}				0.8	V
Output Low Voltage DP, DM	V_{OLD}	R_L = 1.5kΩ from DP to 3.6V			0.3	V
Output High Voltage DP, DM	V_{OHD}	R_L = 15kΩ from DP and DM to V_{SS}	2.8			V
Differential Input Sensitivity DP, DM	V_{DI}	DP to DM	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Single-Ended Receiver Threshold	V_{SE}		0.8		2.0	V
Single-Ended Receiver Hysteresis	V_{SEH}			200		mV
Differential Output Signal Cross-Point Voltage	V_{CRS}	C_L = 50pF, GBD	1.3		2.0	V
DP, DM Off-State Input Impedance	R_{LZ}		300			kΩ
Driver Output Impedance	R_{DRV}	Steady-state drive	28		44	Ω
DP Pullup Resistor	R_{PU}	Idle	0.9		1.575	kΩ
		Receiving	1.425		3.090	
USB TIMING						
DP, DM Rise Time (Transmit)	t_R	C_L = 50pF, GBD	4		20	ns
DP, DM Fall Time (Transmit)	t_F	C_L = 50pF, GBD	4		20	ns
Rise/Fall Time Matching (Transmit)	t_R, t_F	C_L = 50pF, GBD	90		110	%

ADC Electrical Characteristics

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

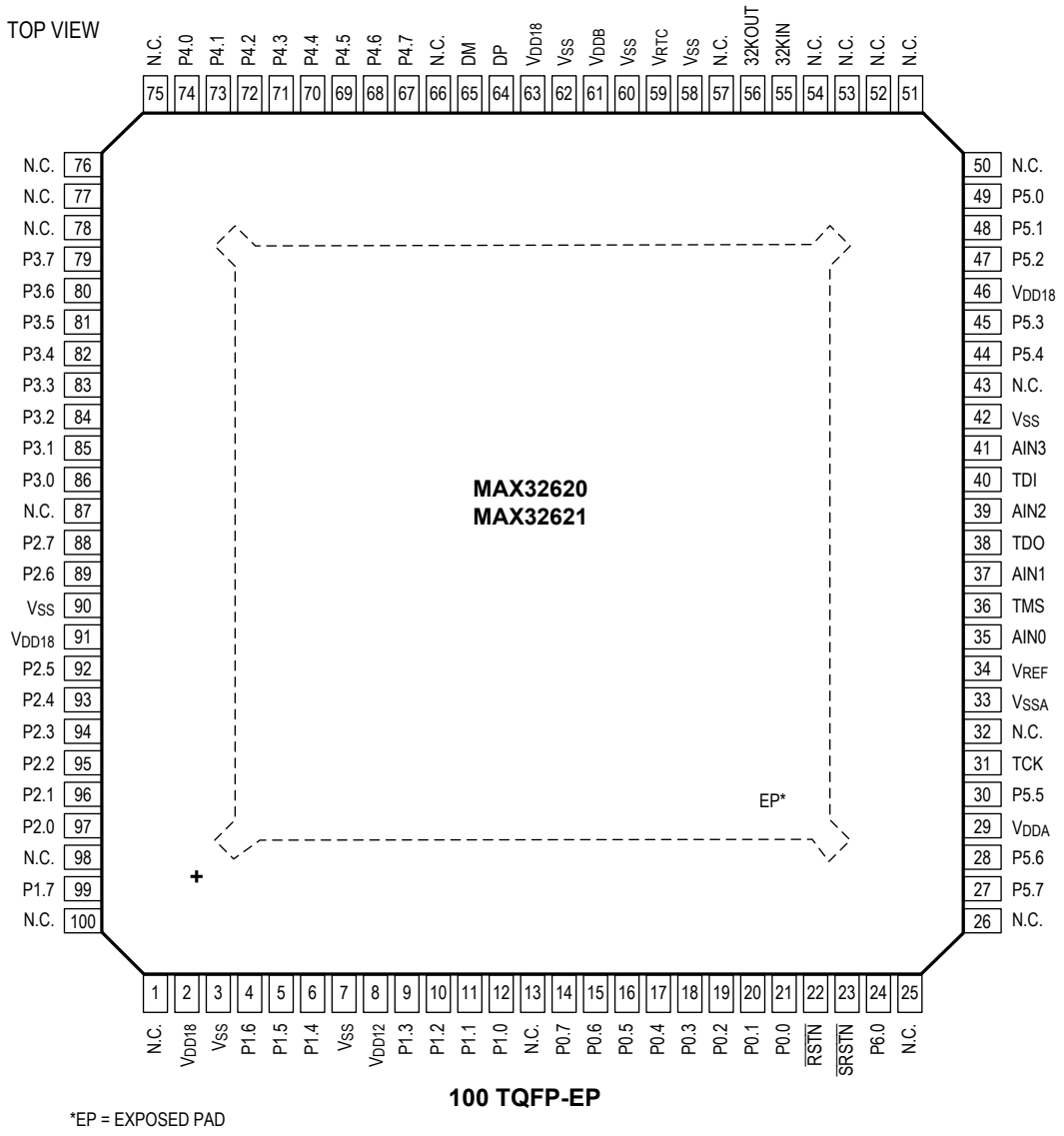
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution				10		bits
ADC Clock Rate	f_{ACLK}		0.1		8	MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 1	V_{SS}		V_{DDA}	V
		AIN[1:0], ADC_CHSEL = 4–5, BUF_BYPASS = 1	V_{SS}		5.5V	
		AIN[3:0], ADC_CHSEL = 0–3, BUF_BYPASS = 0	50mV		V_{DDA} - 50mV	
		AIN[1:0], ADC_CHSEL = 4-5, BUF_BYPASS = 0	50mV		5.5V	

ADC Electrical Characteristics (continued)

(Limits are tested at T_A = +20°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	R_{AIN}	AIN[1:0], ADC_HSEL = 4–5, ADC active		45		kΩ
Input Dynamic Current, Switched Capacitance	I_{AIN}	ADC active, ADC buffer bypassed		4.5		µA
		ADC active, ADC buffer enabled		50		nA
Analog Input Capacitance	C_{AIN}	Fixed capacitance to ground		1		pF
		Dynamically switched capacitance		250		nF
Integral Nonlinearity	INL				±2	LSb
Differential Nonlinearity	DNL				±1	LSb
Offset Error	V_{OS}			±1		LSb
Gain Error	GE			±2		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		240		µA
Input Buffer Active Current	I_{INBUF}			53		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of: ADC clock, ADC bias, reference buffer, or input buffer to CpuAdcStart			10	µs
		Any power-up of: ADC clock or ADC bias to CpuAdcStart			48	t_{ACLK}
ADC Output Latency	t_{ADC}			1025		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.80	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.12	4	nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.02	1.0	nA
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.200		V
Signal to Noise Ratio	SNR			58.5		dB
Signal to Noise and Distortion	SINAD			58.5		dB
Total Harmonic Distortion	THD			-68.5		dB
Spurious Free Dynamic Range	SFDR			74		dB
Bandgap Temperature Coefficient	V_{TEMPCO}	Box method		30		ppm/°C
Reference Input Capacitance	C_{REF_IN}	Dynamically switched capacitance, ADC_XREF=1, ADC active		250		fF
External Reference Voltage	V_{REF_EXT}	ADC_XREF = 1	1.17	1.23	1.29	V
Reference Dynamic Current	I_{REF_EXT}	ADC_XREF=1, ADC active		4.1		µA

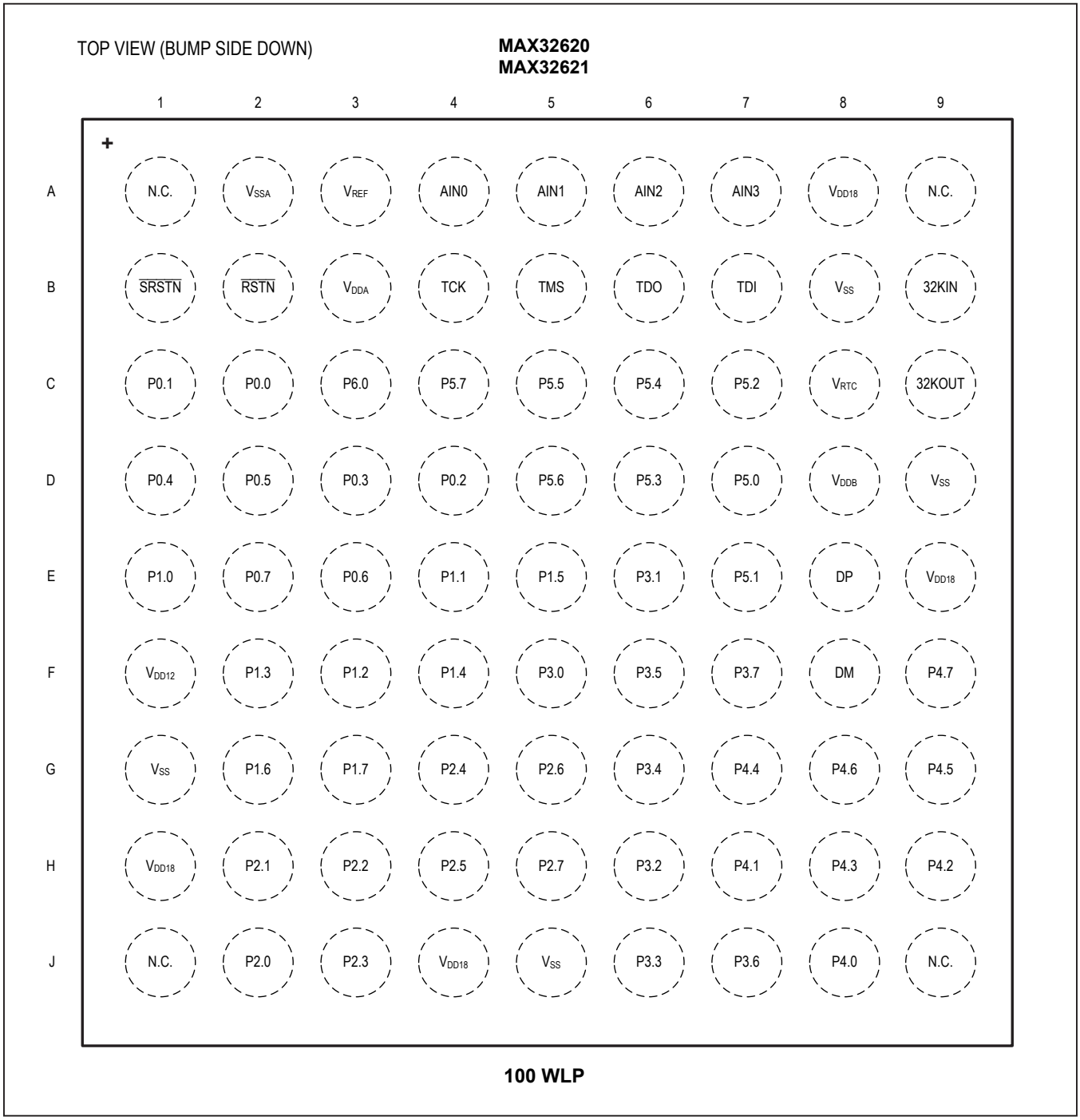
Pin Configuration



100 TQFP-EP

*EP = EXPOSED PAD

Pin Configuration (continued)



Pin Description

PIN		NAME	FUNCTION
TQFP	WLP		
POWER			
61	D8	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close to this pin as possible.
8	F1	V_{DD12}	1.2V Supply Voltage. This pin must be bypassed to V_{SS} with a 100nF capacitor as close to this pin as possible.
59	C8	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close to this pin as possible.
29	B3	V_{DDA}	Analog Supply Voltage. This pin must be bypassed to V_{SSA} with a 1.0µF capacitor as close to this pin as possible
2, 46, 63, 91	A8, E9, H1, J4	V_{DD18}	1.8V Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close to this pin as possible.
34	A3	V_{REF}	ADC Reference. This pin should be left unconnected if an external reference is not used.
3, 7, 42, 58, 60, 62, 90	B8, D9, G1, J5	V_{SS}	Digital Ground.
33	A2	V_{SSA}	Analog Ground. This pin must be connected to V_{SS}.
—	—	EP	Exposed Pad (TQFP Only). This pad must be connected to V_{SS}. Refer to Application Note 3273: Exposed Pads: A Brief Introduction for additional information.
CLOCKS			
55	B9	32KIN	32kHz Crystal Oscillator Input/Output. Connect a 6pF 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected. A 32kHz crystal or external clock source is required for proper USB operation.
56	C9	32KOUT	
USB			
64	E8	DP	USB D+ Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
65	F8	DM	USB D- Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
JTAG			
31	B4	TCK	JTAG Clock or Serial Wire Debug Clock. This pin has an internal 25kΩ pullup to V_{DD18}.
36	B5	TMS	JTAG Test Mode Select or Serial Wire Debug I/O. This pin has an internal 25kΩ pullup to V_{DD18}.
38	B6	TDO	JTAG Test Data Output
40	B7	TDI	JTAG Test Data Input. This pin has an internal 25kΩ pullup to V_{DD18}.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
RESET			
22	B2	$\overline{\text{RSTN}}$	Hardware Reset, Active-Low Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal 25kΩ pullup to the V_{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
23	B1	$\overline{\text{SRSTN}}$	Software Reset, Active-Low Input/Output. The device remains in software reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a reset to the ARM core, digital registers and peripherals (resetting most of the core logic on the V_{DD12} supply). This reset does not affect the POR only registers, RTC logic, ARM debug engine or JTAG debugger allowing for a soft reset without having to reconfiguring all registers. After the device senses $\overline{\text{SRSTN}}$ as a logic 0, the pin automatically reconfigures as an output sourcing a logic 0. The device continues to output for 6 system clock cycles and then repeats the input sensing/output driving until $\overline{\text{SRSTN}}$ is sensed inactive. This pin is internally connected with an internal 25kΩ pullup to the V_{RTC} supply. This pin should be left unconnected if the system design does not provide a reset signal to the device.
GENERAL-PURPOSE I/O AND SPECIAL FUNCTIONS			
21	C2	P0.0	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 1 for details.
20	C1	P0.1	
19	D4	P0.2	
18	D3	P0.3	
17	D1	P0.4	
16	D2	P0.5	
15	E3	P0.6	
14	E2	P0.7	
12	E1	P1.0	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 1 for details.
11	E4	P1.1	
10	F3	P1.2	
9	F2	P1.3	
6	F4	P1.4	
5	E5	P1.5	
4	G2	P1.6	
99	G3	P1.7	

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
97	J2	P2.0	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 1 for details.
96	H2	P2.1	
95	H3	P2.2	
94	J3	P2.3	
93	G4	P2.4	
92	H4	P2.5	
89	G5	P2.6	
88	H5	P2.7	
86	F5	P3.0	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 1 for details.
85	E6	P3.1	
84	H6	P3.2	
83	J6	P3.3	
82	G6	P3.4	
81	F6	P3.5	
80	J7	P3.6	
79	F7	P3.7	
74	J8	P4.0	General-Purpose I/O, Port 4. Most port pins have multiple special functions. See Table 1 for details.
73	H7	P4.1	
72	H9	P4.2	
71	H8	P4.3	
70	G7	P4.4	
69	G9	P4.5	
68	G8	P4.6	
67	F9	P4.7	
49	D7	P5.0	General-Purpose I/O, Port 5. Most port pins have multiple special functions. See Table 1 for details.
48	E7	P5.1	
47	C7	P5.2	
45	D6	P5.3	
44	C6	P5.4	
30	C5	P5.5	
28	D5	P5.6	
27	C4	P5.7	
24	C3	P6.0	General-Purpose I/O, Port 6.0. Most port pins have multiple special functions. See Table 1 for details.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	WLP		
ANALOG INPUT PINS			
35	A4	AIN0	ADC Input 0. 5V-tolerant input.
37	A5	AIN1	ADC Input 1. 5V-tolerant input.
39	A6	AIN2	ADC Input 2
41	A7	AIN3	ADC Input 3
NO CONNECTS			
1, 13, 25, 26, 32, 43, 50–54, 57, 66, 75–78, 87, 98, 100	A1, A9, J1, J9	N.C.	No Connection

Table 1. MAX326320/MAX32621 GPIO Special Function Cross Reference

GPIO	SPECIAL FUNCTIONS						
P0.0	UART0A_RX	UART0B_TX	PT_PT0	TIMER_TMR0	GPIO_INT(P0)		
P0.1	UART0A_TX	UART0B_RX	PT_PT1	TIMER_TMR1	GPIO_INT(P0)		
P0.2	UART0A_CTS	UART0B_RTS	PT_PT2	TIMER_TMR2	GPIO_INT(P0)		
P0.3	UART0A_RTS	UART0B_CTS	PT_PT3	TIMER_TMR3	GPIO_INT(P0)		
P0.4	SPIM0_SCK	PT_PT4	TIMER_TMR4	GPIO_INT(P0)			
P0.5	SPIM0_MOSI/ SDIO0	PT_PT5	TIMER_TMR5	GPIO_INT(P0)			
P0.6	SPIM0_MISO/ SDIO1	PT_PT6	TIMER_TMR0	GPIO_INT(P0)			
P0.7	SPIM0_SS0	PT_PT7	TIMER_TMR1	GPIO_INT(P0)			
P1.0	SPIM1_SCK	SPIX_SCK	PT_PT8	TIMER_TMR2	GPIO_INT(P1)		
P1.1	SPIM1_MOSI/ SDIO0	SPIX_SDIO0	PT_PT9	TIMER_TMR3	GPIO_INT(P1)		
P1.2	SPIM1_MISO/ SDIO1	SPIX_SDIO1	PT_PT10	TIMER_TMR4	GPIO_INT(P1)		
P1.3	SPIM1_SS0	SPIX_SS	PT_PT11	TIMER_TMR5	GPIO_INT(P1)		
P1.4	SPIM1_SDIO2	SPIX_SDIO2	PT_PT12	TIMER_TMR0	GPIO_INT(P1)		
P1.5	SPIM1_SDIO3	SPIX_SDIO3	PT_PT13	TIMER_TMR1	GPIO_INT(P1)		
P1.6	I2CM0/SA_SDA	PT_PT14	TIMER_TMR2	GPIO_INT(P1)			
P1.7	I2CM0/SA_SCL	PT_PT15	TIMER_TMR3	GPIO_INT(P1)			
P2.0	UART1A_RX	UART1B_TX	PT_PT0	TIMER_TMR4	GPIO_INT(P2)		
P2.1	UART1A_TX	UART1B_RX	PT_PT1	TIMER_TMR5	GPIO_INT(P2)		

Table 1. MAX326320/MAX32621 GPIO Special Function Cross Reference (continued)

GPIO	SPECIAL FUNCTIONS						
P2.2	UART1A_CTS	UART1B_RTS	PT_PT2	TIMER_TMR0	GPIO_INT(P2)		
P2.3	UART1A_RTS	UART1B_CTS	PT_PT3	TIMER_TMR1	GPIO_INT(P2)		
P2.4	SPIM2A_SCK	PT_PT4	TIMER_TMR2	GPIO_INT(P2)			
P2.5	SPIM2A_MOSI/ SDIO0	PT_PT5	TIMER_TMR3	GPIO_INT(P2)			
P2.6	SPIM2A_MISO/ SDIO1	PT_PT6	TIMER_TMR4	GPIO_INT(P2)			
P2.7	SPIM2A_SS0	PT_PT7	TIMER_TMR5	GPIO_INT(P2)			
P3.0	UART2A_RX	UART2B_TX	PT_PT8	TIMER_TMR0	GPIO_INT(P3)		
P3.1	UART2A_TX	UART2B_RX	PT_PT9	TIMER_TMR1	GPIO_INT(P3)		
P3.2	UART2A_CTS	UART2B_RTS	PT_PT10	TIMER_TMR2	GPIO_INT(P3)		
P3.3	UART2A_RTS	UART2B_CTS	PT_PT11	TIMER_TMR3	GPIO_INT(P3)		
P3.4	I2CM1/SB_SDA	SPIM2A_SS1	PT_PT12	TIMER_TMR4	GPIO_INT(P3)		
P3.5	I2CM1/SB_SCL	SPIM2A_SS2	PT_PT13	TIMER_TMR5	GPIO_INT(P3)		
P3.6	SPIM1_SS1	SPIX_SS1	PT_PT14	TIMER_TMR0	GPIO_INT(P3)		
P3.7	SPIM1_SS2	SPIX_SS2	PT_PT15	TIMER_TMR1	GPIO_INT(P3)		
P4.0	OWM_I/O	SPIM2A_SR0	PT_PT0	TIMER_TMR2	GPIO_INT(P4)		
P4.1	OWM_PUPEN	SPIM2A_SR1	PT_PT1	TIMER_TMR3	GPIO_INT(P4)		
P4.2	SPIM0_SDIO2	PT_PT2	TIMER_TMR4	GPIO_INT(P4)			
P4.3	SPIM0_SDIO3	PT_PT3	TIMER_TMR5	GPIO_INT(P4)			
P4.4	SPIM0_SS1	PT_PT4	TIMER_TMR0	GPIO_INT(P4)			
P4.5	SPIM0_SS2	PT_PT5	TIMER_TMR1	GPIO_INT(P4)			
P4.6	SPIM0_SS3	PT_PT6	TIMER_TMR2	GPIO_INT(P4)			
P4.7	SPIM0_SS4	PT_PT7	TIMER_TMR3	GPIO_INT(P4)			
P5.0	SPIB_SCK	SPIM2B_SCK	PT_PT8	TIMER_TMR4	GPIO_INT(P5)		
P5.1	SPIB_SDIO0	SPIM2B_ MOSI/SDIO0	PT_PT9	TIMER_TMR5	GPIO_INT(P5)		
P5.2	SPIB_SDIO1	SPIM2B_ MISO/SDIO1	PT_PT10	TIMER_TMR0	GPIO_INT(P5)		
P5.3	SPIB_SSN0	SPIM2B_SS0	UART3A_RX	UART3B_TX	PT_PT11	TIMER_TMR1	GPIO_INT(P5)
P5.4	SPIB_SDIO2	SPIM2B_ SDIO2	UART3A_TX	UART3B_RX	PT_PT12	TIMER_TMR2	GPIO_INT(P5)
P5.5	SPIB_SDIO3	SPIM2B_ SDIO3	UART3A_CTS	UART3B_RTS	PT_PT13	TIMER_TMR3	GPIO_INT(P5)
P5.6	SPIB_SRN	SPIM2B_SR	UART3A_RTS	UART3B_CTS	PT_PT14	TIMER_TMR4	GPIO_INT(P5)
P5.7	I2CM2/SC_SDA	SPIM2B_SS1	PT_PT15	TIMER_TMR5	GPIO_INT(P5)		
P6.0	I2CM2/SC_SCL	SPIM2B_SS2	PT_PT0	TIMER_TMR0	GPIO_INT(P5)		

MAX32620/MAX32621 Detailed Description

The MAX32620/MAX3261 is a low-power, mixed signal microcontroller based on the ARM Cortex-M4F 32-bit core with a maximum operating frequency of 96MHz. The MAX32621 is a secure version, incorporating a trust protection unit (TPU) with encryption and advanced security features.

Application code executes from an onboard 2MB program flash memory, with 256KB SRAM available for general application use. An 8KB instruction cache improves execution throughput, and a transparent code scrambling scheme protects customer intellectual property residing in the program flash memory. Additionally, a SPI execute in place (XIP) external memory interface allows application code and data (up to 16MB) to be accessed from an external SPI memory device.

A 10-bit sigma-delta ADC is provided with a multiplexer front end for four external input channels (two of which are 5.5V tolerant) and six internal channels. Dedicated divided supply input channels allows direct monitoring of onboard power supplies V_{DD12}, V_{DD18}, V_{DDB} and V_{RTC} by the ADC. Built-in limit monitors allow converted input samples to be compared against user-configurable high and low limits, with an option to trigger an interrupt and wake the CPU from a low power mode if attention is required.

A wide variety of communications and interface peripherals are provided, including a USB 2.0-compliant slave interface, three master SPI interfaces, four UART interfaces with multidrop support, three master I^2C interfaces, and a slave I^2C interface.

ARM Cortex-M4F Architecture

The ARM Cortex-M4F processor is ideal for the emerging category of wearable medical and wellness applications. The architecture combines high-efficiency signal processing functionality with low power, low cost, and ease of use.

- Floating Point Unit (FPU)
- Memory Protection Unit
- Full debug support level
  - Debug Access Port (DAP)
  - Breakpoints
  - DWT
  - Flash patch
  - Halting debug
- Debug access port : JTAG or serial wire
- NVIC support
  - 52 interrupts to be grouped by firmware into 8 levels of priority
- Cortex-M4F DSP supports Single Instruction Multiple Data (SIMD) Path DSP extensions, providing:
  - 4 parallel 8 bit add/sub
  - 2 parallel 16 bit add/sub
  - 2 parallel MACs
  - 32 or 64 bit accumulate
  - Signed, unsigned, data with or without saturation

Analog to Digital Converter (ADC)

The 10-bit sigma-delta ADC provides 4 external inputs and can also be configured to measure all internal power supplies. It operates at a maximum of 7.8ksps. AIN0 and AIN1 are 5.5V tolerant, making them suitable for monitoring batteries.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low-power mode.

The ADC reference is selectable:

- Internal bandgap
- External reference

Pulse Train Engine

Sixteen independent pulse train generators provide either a square wave or a repeating pattern from 2 bits to 32 bits in length. The frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, etc.) of the input pulse train module clock.

Any single pulse train generator or any desired group of pulse train generators can be restarted at the beginning of their patterns and synchronized with one another ensuring simultaneous startup. Additionally, each pulse train can operate in a single shot mode.

Clocking Scheme

The high-frequency internal relaxation oscillator operates at a nominal frequency of 96MHz. It is the primary clock source for the digital logic and peripherals.

An external 32.766kHz timebase is required when using the RTC or USB features of the device. The time base can be generated by attaching a 32kHz crystal. An external clock source can also be applied to the 32KIN pin. The external clock source must meet the electrical/timing requirements in the EC table. The 32kHz output can be directed out to pin P1.7 for observation and use.

Interrupt Sources

The ARM nested vector interrupt controller (NVIC) provides high speed, deterministic interrupt response, interrupt masking, and multiple interrupt sources. Each peripheral is connected to the NVIC and can have multiple interrupt flags to indicate the specific source of the interrupt within the peripheral. 52 interrupts can be grouped by firmware into 8 levels of priority (including internal and external interrupts).

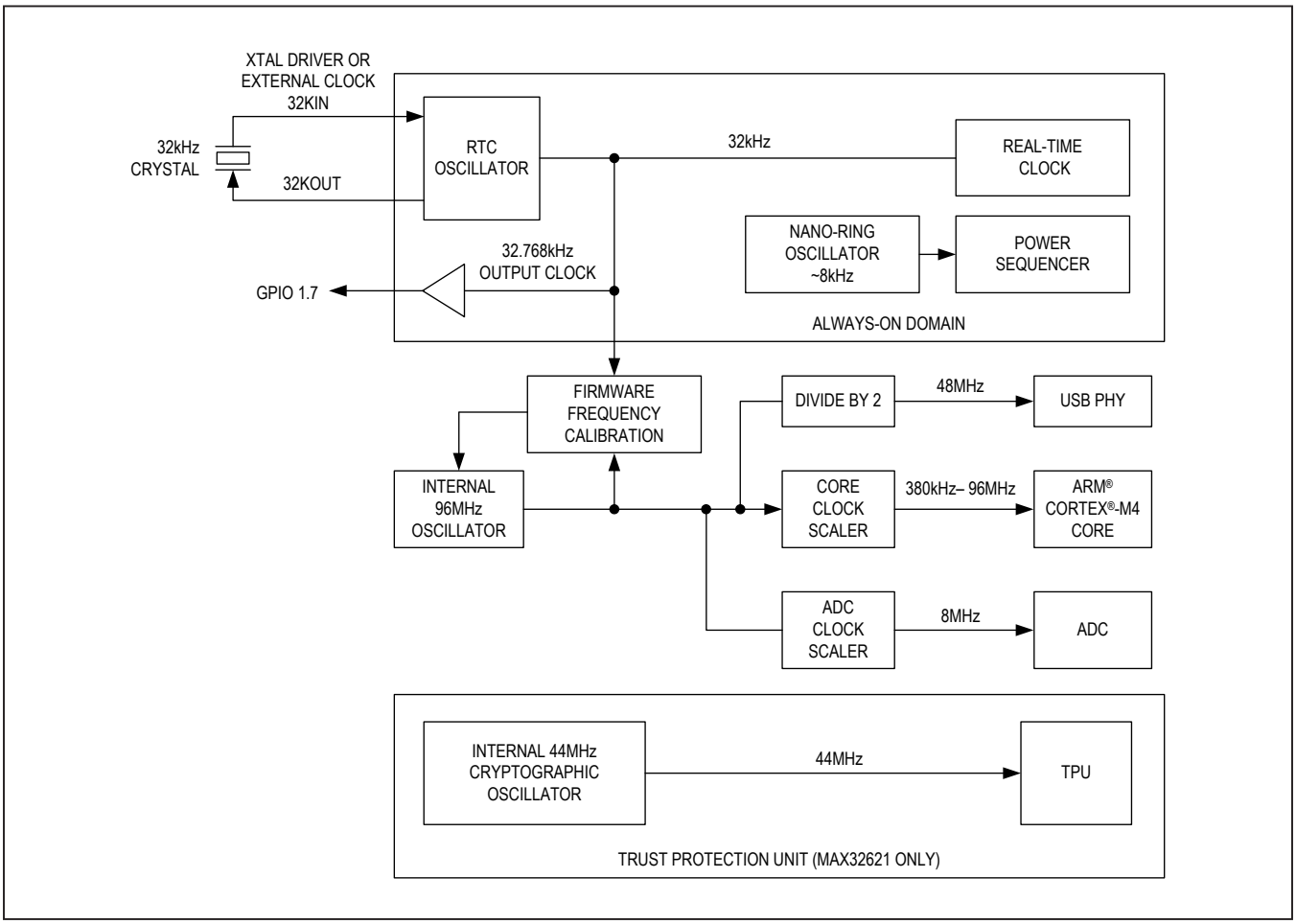


Figure 1. Clock Diagram

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software. A time-of-day alarm and independent subsecond alarm can cause an interrupt or wake the device from stop mode.

The minimum wake-up interval is 244µs.

CRC Module

The CRC hardware module provides fast calculations and data integrity checks by application software. The CRC module supports both the CRC-16-CCITT and CRC-32 ($X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X^{1}+1$)polynomials.

Watchdog Timers

Two independent watchdog timers (WDT) with window support are provided. The WDT has multiple clock source options to ensure system security. It uses a 32-bit timer with prescaler to generate the watchdog reset. When enabled, the WDT must be reset prior to timeout or within a window of time if window mode is enabled. Failure to reset the WDT during the programmed timing window results in a watchdog timeout. WTD resets can cause firmware or power-on resets. The WDT1 or WDT2 flags are set on reset if a watchdog expiration caused the system reset. The clock source options for the WDT include:

- Scaled-system clock
- RTC clock
- Nano-ring management clock

Programmable Timers

Six 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals. Each timer can be split into 2 16-bit timers, enabling 12 standard 16-bit timers.

32-bit timer features:

- 32-bit up/down auto-reload
- Programmable 16-bit prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- GPIOs can be assigned as external timer inputs, clock gating or capture, limited to an input frequency of 1/4 of the peripheral clock frequency
- Timer output pin
- Configurable as 2x 16-bit general purpose timers
- Timer interrupt

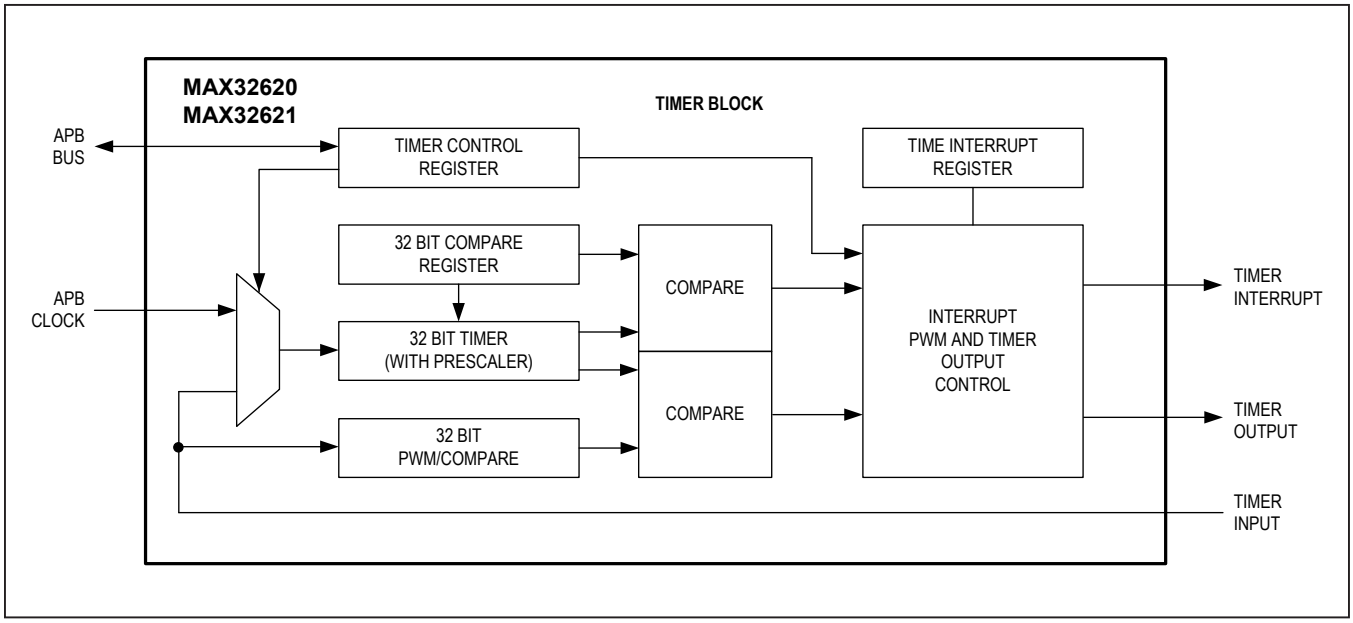


Figure 2. Timer Block Diagram, 32-Bit Mode

Serial Peripherals

USB Controller

The integrated USB controller is compliant with the full-speed (12Mb/s) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator allows for smart switching between the main supply and V_{DDB} when connected to a USB host controller.

The USB controller supports DMA for the endpoint buffers. A total of 7 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.

An external 32kHz crystal or clock source is required for USB operation, even if the RTC function is not used. Although the USB timing is derived from the internal 96MHz oscillator, the default accuracy is not sufficient for USB operation. Firmware trimming of the 96MHz oscillator, using the 32kHz timebase as a reference, is necessary to comply with USB timing requirements.

I²C Master and Slave Ports

The I²C interface is a bidirectional, 2-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. Three I²C master engines and one I²C-selectable slave engine interface to a wide variety of I²C-compatible peripherals. These engines support both standard mode and fast mode I²C standards. The slave engine shares the same I/O port as the master engines and is selectable through the I/O configuration settings. It provides the following features:

- Master or slave mode operation
- Information transferal over a serial data circuit (SDA) and serial clock circuit (SCL)
- Supports standard (7-bit) addressing
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates:
  - Standard mode: 100kbps
  - Fast mode: 400kbps
- On-chip filter to reject spikes on the data circuit
- Receiver FIFO depth of 16 bytes
- Transmitter FIFO depth of 16 bytes

Serial Peripheral Interface Master Interface

The SPI master-mode-only interface operates independently in a single or multiple slave system and is fully accessible to the user application.

The SPI ports provide a highly configurable, flexible and efficient interface to communicate with a wide variety of SPI slave devices. The three SPI master ports (SPI0, SPI1, SPI2) support the following features:

- Supports all four SPI modes (0,1,2,3) for single-bit communication
- 3 or 4 wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad I/O supported
- Up to 5 slave select lines per port
- Up to 2 slave ready lines
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- Programmable SCK alternate timing
- SS (slave select) assertion and deassertion timing with respect to leading/trailing SCK edge

Serial Peripheral Interface Execute in Place (XIP) Master

The SPI execute in place (XIP) master allows the CPU to transparently execute instructions stored in an external SPI flash. Instructions fetched through the SPI XIP master are cached just like instructions fetched from internal program memory. The SPI XIP master can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

UART

All four universal asynchronous receiver-transmitter (UART) interfaces support full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry-standard request to send (RTS) and clear to send (CTS) methodology. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 2x 32-byte send/receive FIFOs, one for transmit and receive
- Full-duplex operation for asynchronous data transfers
- Programmable interrupt for receive and transmit
- Independent baud-rate generator
- Programmable 9th bit parity support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Maximum baud rate 460.8kB

Trust Protection Unit (TPU) (MAX32621 Only)

The TPU enhances cryptographic data security for valuable intellectual property (IP) and data. A high-speed, dedicated, hardware-based math accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms including:

- AES-128
- AES-192
- AES-256
- 1024-bit DSA
- 2048-bit (CRT)

The device provides a pseudo-random number generator which can be used to create cryptographic keys for any application. A user-selectable entropy source further increases the randomness and key strength.

The secure bootloader protects against unauthorized access to program memory.

Peripheral Management Unit (PMU)

The PMU is a DMA-based link list processing engine that performs operations and data transfers involving memory and/or peripherals in the advanced peripheral bus (APB) and advanced high-performance bus (AHB) peripheral memory space while the main CPU is in a sleep state. This allows low-overhead peripheral operations to be performed without the CPU, significantly reducing overall power consumption. Using the PMU with the CPU in a sleep state provides a lower-noise environment critical for obtaining optimum ADC performance.

Key features of the PMU engine include:

- Six independent channels with round-robin scheduling allows for multiple parallel operations
- Programmed using SRAM-based PMU opcodes
- PMU action can be initiated from interrupt conditions from peripherals without CPU
- Integrated AHB bus master
- Coprocessor-like state machine

Additional Documentation

Engineers must have the following documents to fully use this device:

- This data sheet, containing pin descriptions, feature overviews, and electrical specifications
- The device-appropriate user guide, containing detailed information and programming guidelines for core features and peripherals
- Errata sheets for specific revisions noting deviations from published specifications.

For information regarding these documents, visit Technical Support at **support.maximintegrated.com/micro**.

Development and Technical Support

Contact technical support for information about highly versatile, affordable development tools, available from Maxim Integrated and third-party vendors.

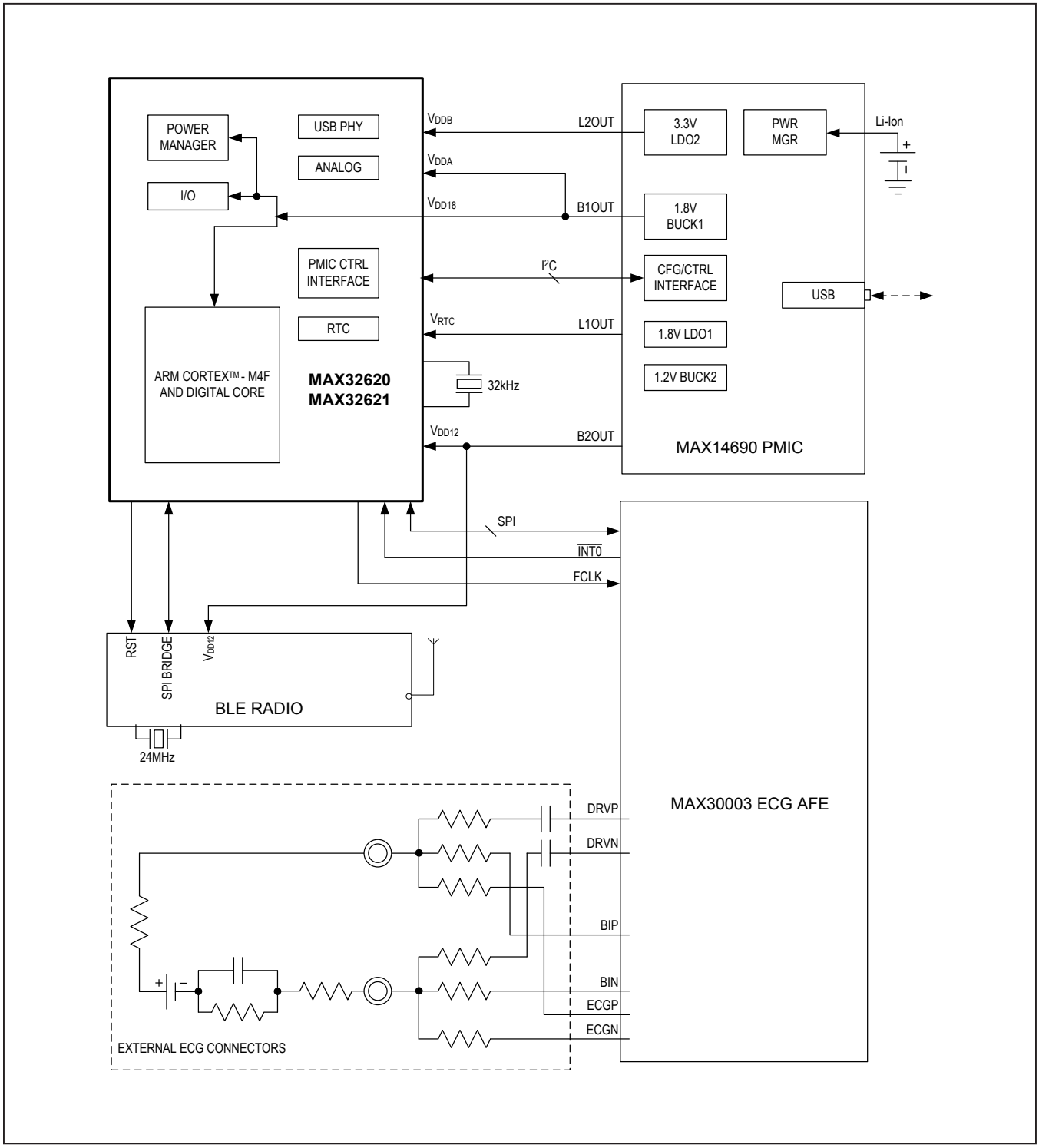
- Evaluation kits
- Software development kit
- Compilers
- Integrated development environments (IDEs)
- USB interface modules for programming and debugging

For technical support, go to **support.maximintegrated.com/micro**.

Additional Features

- ARM® Cortex®-M4F 32 Bit RISC CPU
  - Internal 96MHz Oscillator Saves Board Space and Cost
  - Memory Protection Unit
  - Floating Point Unit
- Ultra-Low Power
  - 95µA/MHz Dynamic Power Executing from Flash
  - 600nA (typ) Low Power Mode LP0 Current with RTC Enabled
  - 2.5µA Ultra-Low Power Data Retention Mode LP1 with Fast 5µs (typ) Wakeup
  - Dynamic Clock Disables Unused Peripherals/Logic
  - Wake Up from RTC, USB, GPIO, Multiple/Single Events
- Peripherals
  - 3x SPI Master Engines (1/2/4-bit Width)
  - 1x SPI Master XiP Engine for External Flash Execution
  - 3x I2C Master Engines (Fast/Standard Mode)
  - 1x I2C Slave Engine (Shared Pins with Master Engines)
  - 4x UART with Optional Hardware Flow Control
  - 1x 1-Wire Master
  - 16x Pulse Train Engines
  - USB 2.0-Compliant Peripheral, Full Speed (12Mb/s)
  - 6x 32-Bit Timers (Reconfigurable as 12 x 16-Bit Timers)
  - 32 Bit Real-Time Clock (RTC) with Time of Day Alarm
  - Supports 1149.1 JTAG with Serial Wire Debug
- Memory
  - 2MB Flash Memory
  - 8KB Instruction Cache
  - 256KB SRAM
- Supply Voltage
  - 1.2V ±5% Core Supply Voltage
  - 1.8V ±5% I/O and Analog Supply Voltage
  - Optional 3.3V ±5% USB Supply Voltage
- Other Features:
  - 49 General Purpose I/O (GPIO)
  - 2x Programmable Watchdog Timers with Independent Clock Sources
- Analog Components
  - Four-Input, 10-Bit Sigma-Delta ADC Operating at 7.8 kS/s
  - 5.5V, 1.2V-Tolerant Inputs
  - Internal or External Reference
- Peripheral Management Unit (PMU) Reduces Power Consumption in Sleep Mode
- Trust Protection Unit for Data Integrity and IP Protection
  - AES Hardware Engine
  - MAA for ECDSA and Modular Arithmetic
  - Trust Protection Unit (TPU) for End-to-End Security
  - Hardware PRNG Entropy Generator
  - Secure Boot Loader
  - CRC16/32 Engine
  - Factory-Programmed Unique ID

Typical Application Circuit—Electrocardiogram (ECG) Patch



Ordering Information

PART	FLASH (MB)	SRAM (KB)	TRUST PROTECTION UNIT	PIN-PACKAGE
MAX32620ICQ+	2	256	No	100 TQFP
MAX32620IWG+	2	256	No	81 WLP
MAX32620IWG+T	2	256	No	81 WLP
MAX32621ICQ+	2	256	Yes	100 TQFP
MAX32621IWG+	2	256	Yes	81 WLP
MAX32621IWG+T	2	256	Yes	81 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
81 WLP	W813D3+1	**21-0776**	Refer to **Application Note 1891**
100 TQFP-EP	C100E+3	**21-0116**	**90-0154**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—