TEXAS INSTRUMENTS

LP8862-Q1

SNVSA75A – NOVEMBER 2015 – REVISED NOVEMBER 2015

LP8862-Q1 High-Performance 2-Channel LED Driver for Automotive Lighting

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Input Voltage Operating Range 4.5 V to 40 V
- Two High-Precision Current Sinks
  - Current Matching 1% (Typical)
  - Output Current up to 160 mA/Channel
  - Dimming Ratio 10 000:1 at 200 Hz
- Integrated DC-DC for LED String Power
  - Boost and SEPIC Modes Supported
  - Output Voltage up to 45 V
  - Switching Frequency 300 kHz to 2.2 MHz
- EMI Minimization With Optional DC-DC Synchronization Input or Spread Spectrum
- Power-Line FET Control for Inrush Current Protection and Standby Energy Saving
- Extensive Fault Detection Features
  - Fault Output
  - Input Voltage OVP, UVLO, and OCP
  - Open and Shorted LED Fault Detection
  - Thermal Shutdown
- Minimum Number of External Components

2 Applications

Automotive Infotainment, Instrument Cluster and Backlighting Systems

3 Description

The LP8862-Q1 is an automotive high-efficiency, low-EMI, easy-to-use LED driver with integrated DC-DC converter. The DC-DC supports both boost and SEPIC modes of operation. The device has two high-precision current sinks that can provide high dimming ratio brightness control with a PWM input signal.

The DC-DC converter has an adaptive output voltage control based on the LED current sink headroom voltages. This feature minimizes power consumption by adjusting the voltage to the lowest sufficient level in all conditions. DC-DC supports spread spectrum for switching frequency and an external synchronization with a dedicated pin. The high switching frequency allows the LP8862-Q1 to avoid disturbance for AM radio band.

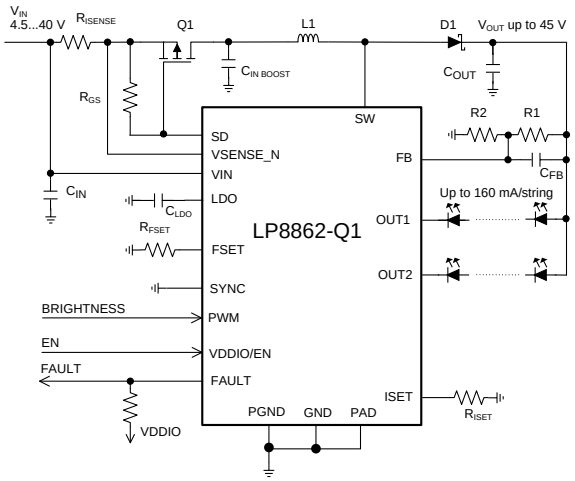
The input voltage range for the LP8862-Q1 is from 4.5 V to 40 V to support automotive stop/start and load dump conditions. The device supports PWM brightness dimming ratio 10 000:1 for 200-Hz input PWM frequency. The LP8862-Q1 integrates extensive fault detection features. The device has an option to drive an external p-FET to disconnect the input supply from the system in the event of a fault. This feature also reduces inrush current and standby power consumption.

Device Information(1)

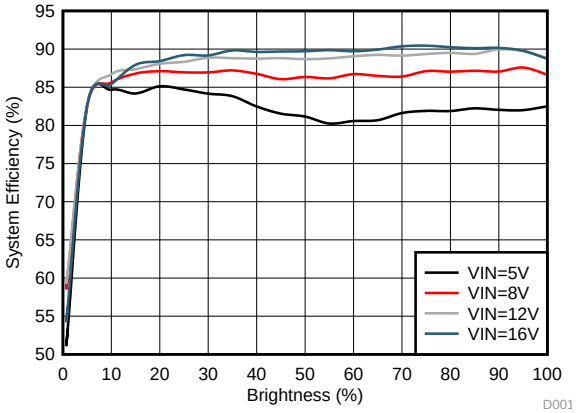
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP8862-Q1	HTSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



System Efficiency



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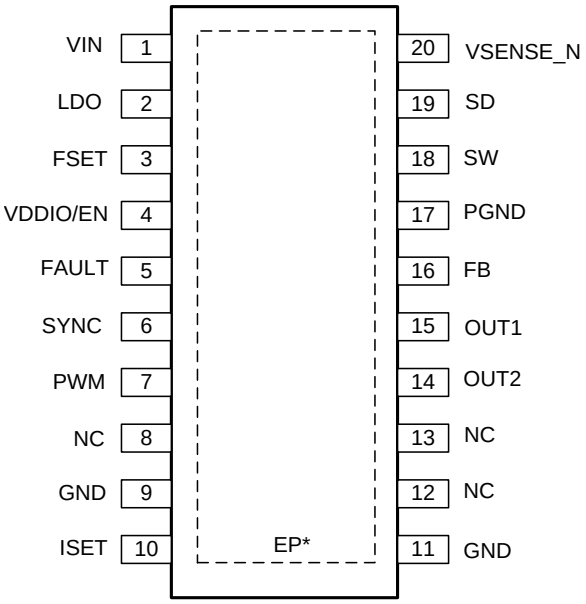
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2015) to Revision A	Page
• Changed device from product preview to production data	1

5 Pin Configuration and Functions

PWP Package
20-Pin TSSOP
Top View



*EXPOSED PAD

Table 1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	VIN	A	Input power pin as well as the positive input for an optional current sense resistor.
2	LDO	A	Output of internal LDO; connect a 1-µF decoupling capacitor between this pin and noise-free ground.
3	FSET	A	DC-DC (boost or SEPIC) switching-frequency-setting resistor.
4	VDDIO/EN	I	Enable input for the device as well as supply input (VDDIO) for digital pins
5	FAULT	OD	Fault signal output. If unused, this pin may be left floating.
6	SYNC	I	Input for synchronizing boost. If synchronization is not used, connect this pin to GND to disable spread spectrum or to VDDIO/EN to enable spread spectrum.
7	PWM	I	PWM dimming input.
8	NC		No internal connection
9	GND	G	Ground.
10	ISET	A	LED current setting resistor
11	GND	G	Ground.
12	NC	—	No internal connection
13	NC	—	No internal connection
14	OUT2	A	Current sink output. This pin must be connected to GND if not used.
15	OUT1	A	Current sink output. This pin must be connected to GND if not used.
16	FB	A	DC-DC (boost or SEPIC) feedback input.
17	PGND	G	DC-DC (boost or SEPIC) power ground.
18	SW	A	DC-DC (boost or SEPIC) switch pin.
19	SD	A	Power-line FET control.
20	VSENSE_N	A	Input current sense pin.

(1) A: Analog pin, G: Ground pin, P: Power pin, I: Input pin, I/O: Input/Output pin, O: Output pin, OD: Open Drain pin

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage on pins	VIN, VSENSE_N, SD, SW, FB	–0.3	50	V
	OUT1, OUT2	–0.3	45	
	LDO, SYNC, FSET, ISET, PWM, VDDIO/EN, FAULT	–0.3	5.5	
Continuous power dissipation(3)		Internally Limited		
Ambient temperature range T_A(4)		–40	125	ºC
Junction temperature range T_J(4)		–40	150	ºC
Maximum lead temperature (soldering)			See(5)	ºC
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 165°C (typical) and disengages at T_J = 145°C (typical).
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 150°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.
(5) For detailed soldering specifications and information, please refer to the *PowerPAD™ Thermally Enhanced Package Application Note* (SLMA002).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 10, 11, 20)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VIN	4.5	45	V
	VSENSE_N, SD, SW	0	45	
	OUT1, OUT2	0	40	
	FB, FSET, LDO, ISET, VDDIO/EN, FAULT	0	5.25	
	SYNC, PWM	0	VDDIO/EN	

(1) All voltages are with respect to the potential at the GND pins.

6.4 Thermal Information

THERMAL METRIC[1]		LP8862-Q1 PWP (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	44.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

6.5 Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted)[1][2].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Standby supply current	Device disabled, $V_{VDDIO/EN}$ = 0 V, V_{IN} = 12 V		4.5	20	µA
	Active supply current	V_{IN} = 12 V, V_{OUT} = 26 V, output current 160 mA/channel, converter f_{SW} = 300 kHz		5	12	mA
V_{POR_R}	Power-on reset rising threshold	LDO pin voltage. Output of the internal LDO or an external supply input (V_{DD}).			2.7	V
V_{POR_F}	Power-on reset falling threshold	LDO pin voltage. Output of the internal LDO or an external supply input (V_{DD}).	1.5			
T_{TSD}	Thermal shutdown threshold		150	165	175	°C
T_{TSD_HYST}	Thermal shutdown hysteresis			20		

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are specified by design, test, or statistical analysis.

6.6 Internal LDO Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LDO}	Output voltage	V_{IN} = 12 V	4.15	4.3	4.45	V
V_{DR}	Dropout voltage		120	220	430	mV
I_{SHORT}	Short circuit current			50		mA

6.7 Protection Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	VIN OVP threshold voltage		41	42	44	V
I_{OCP}	VIN OCP current	R_{SENSE} = 50 mΩ	2.7	3.2	3.7	A
V_{UVLO}	VIN UVLO			4.0		V
V_{UVLO_HYST}	VIN UVLO hysteresis			100		mV
	LED short detection threshold		5.6	6	7	V

6.8 Power Line FET Control Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSENSE_N pin leakage current	V_{VSENSE_N} = 45 V		0.1	3	µA
SD leakage current	V_{SD} = 45 V		0.1	3	µA
SD pulldown current		185	230	283	µA

6.9 Current Sinks Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LEAKAGE}$	Leakage current	Outputs OUT1 and OUT2, $V_{OUT\#}$ = 45 V		0.1	5	µA
I_{MAX}	Maximum current	OUT1, OUT2		160		mA
I_{OUT}	Output current accuracy	I_{OUT} = 160 mA	−5%		5%	
I_{MATCH}	Output current matching (1)	I_{OUT} = 160 mA, PWM duty =100%		1%	5%	
V_{SAT}	Saturation voltage (2)	I_{OUT} = 160 mA , V_{LDO} = 4.3 V		0.4	0.7	V

(1) Output Current Accuracy is the difference between the actual value of the output current and programmed value of this current. Matching is the maximum difference from the average. For the constant current sinks on the part (OUT1, OUT2), the following are determined: the maximum output current (MAX), the minimum output current (MIN), and the average output current of all outputs (AVG). Matching number is calculated: (MAX-MIN)/AVG. The typical specification provided is the most likely norm of the matching figure for all parts. LED current sinks were characterized with 1-V headroom voltage. Note that some manufacturers have different definitions in use.
(2) Saturation voltage is defined as the voltage when the LED current has dropped 10% from the value measured at 1 V.

6.10 PWM Brightness Control Electrical Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{PWM}	PWM input frequency		100		20 000	Hz
$t_{ON/OFF}$	Minimum on/off time	I_{OUT} = 100 mA			0.5	µs

6.11 Boost or SEPIC Converter Characteristics

T_J = −40°C to 125°C (unless otherwise noted).
Unless otherwise specified: V_{IN} = 12 V, EN/VDDIO = 3.3 V, L = 22 µH, C_{IN} = 2 × 10 µF ceramic and 33 µF electrolytic, C_{OUT} = 2 × 10-µF ceramic and 33-µF electrolytic, D = NRVB460MFS, f_{SW} = 300 kHz.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5		40	V
V_{OUT}	Output voltage		6		45	V
f_{SW_MIN}	Minimum switching frequency (central frequency if spread spectrum is enabled)	Defined by R_{FSET} resistor		300		kHz
f_{SW_MAX}	Maximum switching frequency (central frequency if spread spectrum is enabled)			2 200		kHz
V_{OUT}/V_{IN}	Conversion ratio				10	
T_{OFF}	Minimum switch OFF time	f_{SW} ≥ 1.15 MHz			55	ns
I_{SW_MAX}	SW current limit		1.8	2	2.2	A
R_{DSON}	FET R_{DSON}	Pin-to-pin		240	400	mΩ
f_{SYNC}	External SYNC frequency		300		2 200	kHz
$t_{SYNC\_ON\_MIN}$	External SYNC minimum on time			150		ns
$t_{SYNC\_OFF\_MIN}$	External SYNC minimum off time			150		ns

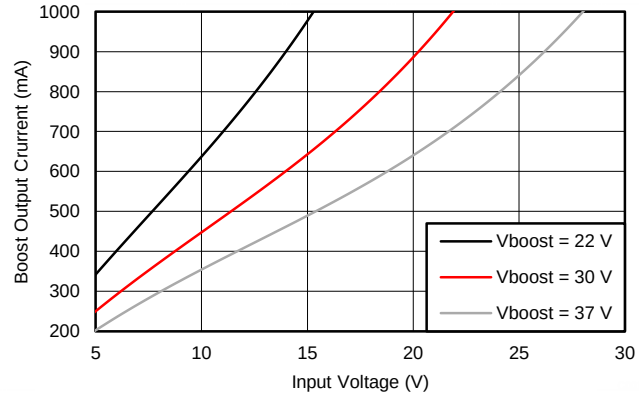
6.12 Logic Interface Characteristics

T_J = −40°C to 125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT VDDIO/EN						
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		1.65			
I_I	Input current		−1	5	30	µA
LOGIC INPUT SYNC/FSET, PWM						
V_{IL}	Input low level				0.2 × VDDIO/EN	V
V_{IH}	Input high level		0.8 × VDDIO/EN			
I_I	Input current		−1		1	µA
LOGIC OUTPUT FAULT						
V_{OL}	Output low level	Pullup current 3 mA		0.3	0.5	V
$I_{LEAKAGE}$	Output leakage current	V = 5.5 V			1	µA

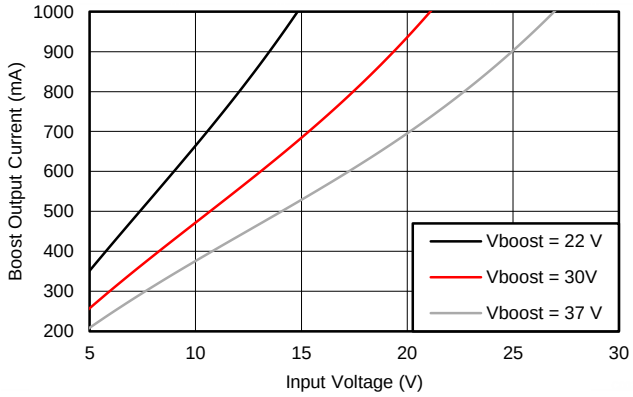
6.13 Typical Characteristics

Unless otherwise specified: D = NRVB460MFS, T = 25ºC



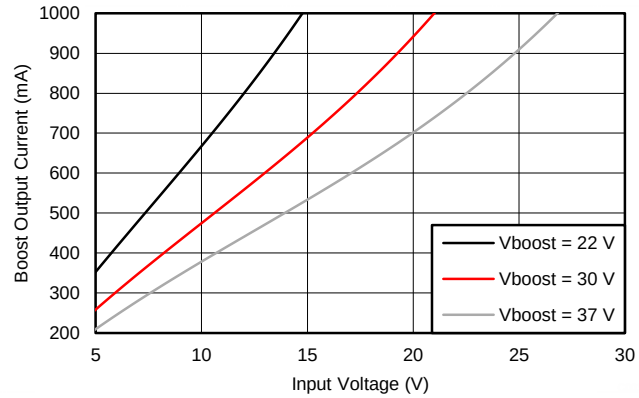
f_{SW} = 300 kHz L = 33 µH DC load (PWM = 100%)
C_{IN} and C_{OUT} = 33 µF + 2 × 10 µF (ceramic)

Figure 1. Maximum Boost Current



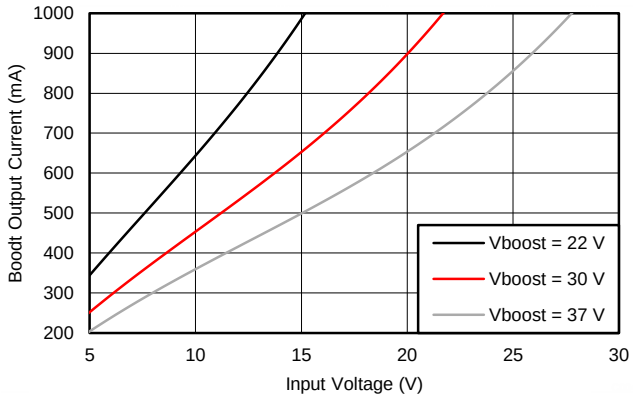
f_{SW} = 800 kHz L = 15 µH DC load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 2. Maximum Boost Current



f_{SW} = 1.5 MHz L = 8.2 µH DC load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 3. Maximum Boost Current



f_{SW} = 2.2 MHz L = 4.7 µH DC load (PWM = 100%)
C_{IN} and C_{OUT} = 2 × 10 µF (ceramic)

Figure 4. Maximum Boost Current

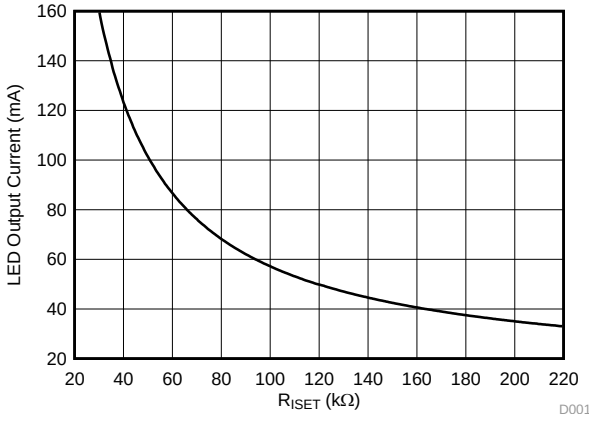


Figure 5. LED Current vs R_{ISET}

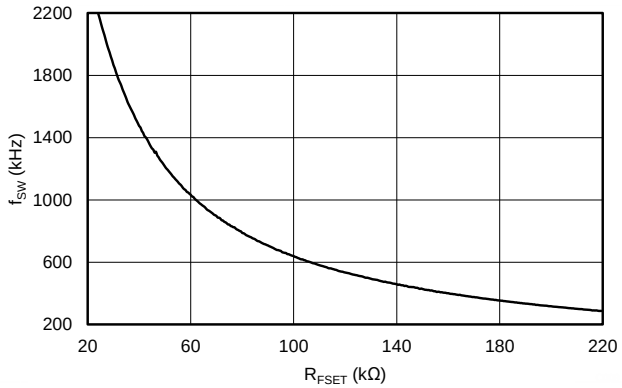


Figure 6. Boost Switching Frequency f_{SW} vs R_{FSET}

7 Detailed Description

7.1 Overview

The LP8862-Q1 is a highly integrated LED driver for automotive infotainment, lighting systems, and medium-sized LCD backlight applications. It includes a DC-DC with an integrated FET, supporting both boost and SEPIC modes, an internal LDO enabling direct connection to battery without need for a pre-regulated supply, and two LED current sinks. A VDDIO/EN pin provides the supply voltage for digital IOs (PWM and SYNC inputs) and at the same time enables the device.

The switching frequency on the DC-DC regulator is set by a resistor connected to the FSET pin. The maximum output voltage of the DC-DC is set by a resistive divider connected to the FB pin. For best efficiency the output voltage is adapted automatically to the minimum necessary level needed to drive the LED strings. This is done by monitoring LED output voltage drop in real time. For EMI reduction and control two optional features are available:

- Spread spectrum, which reduces EMI noise around the switching frequency and its harmonic frequencies
- DC-DC can be synchronized to an external frequency connected to SYNC pin

The two constant current sinks OUT1 and OUT2 provide LED current up to 160 mA. Value for the current per OUT pin is set with a resistor connected to ISET pin. Unused current sink must be connected to ground. Grounded sink is disabled and excluded from adaptive output voltage control and LED string fault detection.

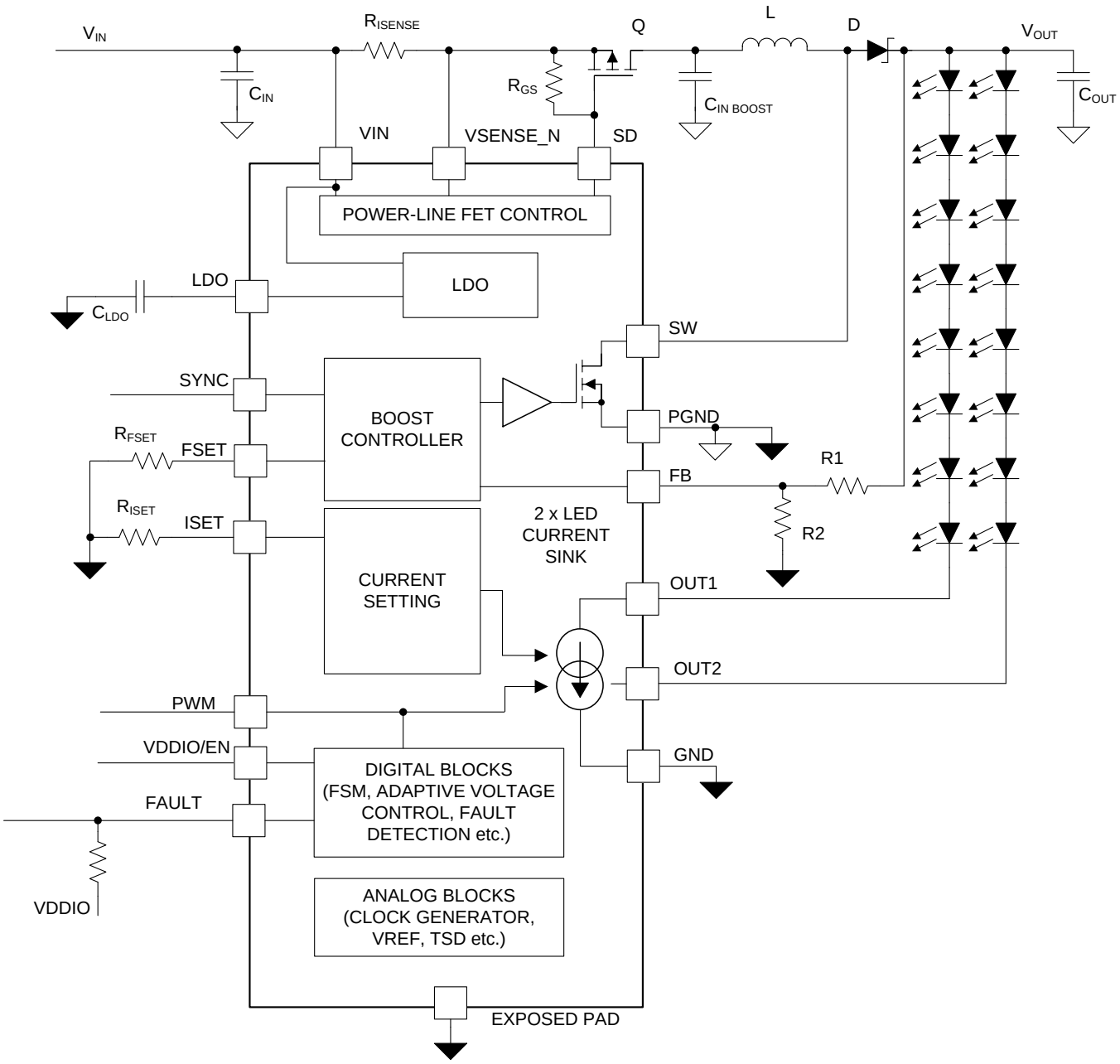
Brightness is controlled with the PWM input. Frequency range for the input PWM is from 100 Hz to 20 kHz. LED output PWM follows the input PWM so the output frequency is equal to the input frequency.

The LP8862-Q1 has extensive fault detection features:

- Open-string and shorted LED detections
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- V_{IN} input overvoltage protection
  - Threshold sensing from VIN pin
- V_{IN} input undervoltage protection
  - Threshold sensing from VIN pin
- V_{IN} input overcurrent protection
  - Threshold sensing across R_{ISENSE} resistor
- Thermal shutdown in case of die overtemperature

Fault condition is indicated with the FAULT output pin. Additionally, the LP8862-Q1 supports control for an optional power-line FET allowing further protection by disconnecting the device from power-line in fault condition. With the power-line FET control it possible to protect device itself, DC-DC external components and LEDs in case of shorted V_{OUT} and too-high V_{IN} voltage. Power-line FET control also features soft-start which reduces the peak current from the power-line during start-up.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Integrated DC-DC Converter

The LP8862-Q1 DC-DC converter generates supply voltage for the LEDs and can operate in boost mode or in SEPIC mode. The maximum output voltage V_{OUT_MAX} is defined by an external resistive divider (R1, R2).

V_{OUT_MAX} must be chosen based on the maximum voltage required for LED strings. Recommended maximum voltage is about 30% higher than maximum LED string voltage. Initial output voltage is about 88% of V_{OUT_MAX}. DC-DC output voltage is adjusted automatically based on LED current sink headroom voltage. Maximum output voltage can be calculated with Equation 1:

$$V_{OUT\_MAX} = \left(\frac{V_{BG}}{R2} + 0.0387\right) \times R1 + V_{BG} \quad (1)$$

where

- V_{BG} = 1.2 V
- R2 recommended value is 130 kΩ
- Resistor values are in kΩ

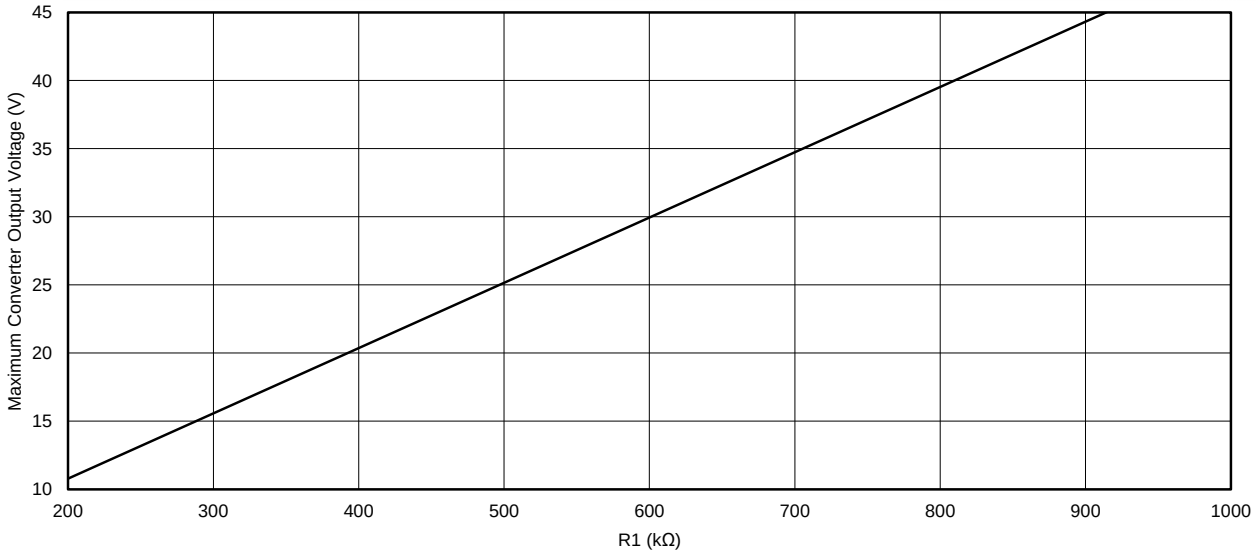


Figure 7. Maximum Converter Output Voltage vs R1 Resistance

The converter is a current mode DC-DC converter, where the inductor current is measured and controlled with the feedback. Switching frequency is adjustable between 300 kHz and 2.2 MHz with R_{FSET} resistor as shown in Equation 2:

$$f_{SW} = 67600 / (R_{FSET} + 6.4) \quad (2)$$

where

- f_{SW} is switching frequency, kHz
- R_{FSET} is frequency setting resistor, kΩ

In most cases lower frequency has higher system efficiency. DC-DC parameters are chosen automatically according to the selected switching frequency (see Table 3). In boost mode a 15-pF capacitor C_{FB} must be placed across resistor R1 when operating in 300-kHz to 500-kHz range (see Figure 19). When operating in 1.8-MHz to 2.2-MHz range C_{FB} = 4.7 pF.

Feature Description (continued)

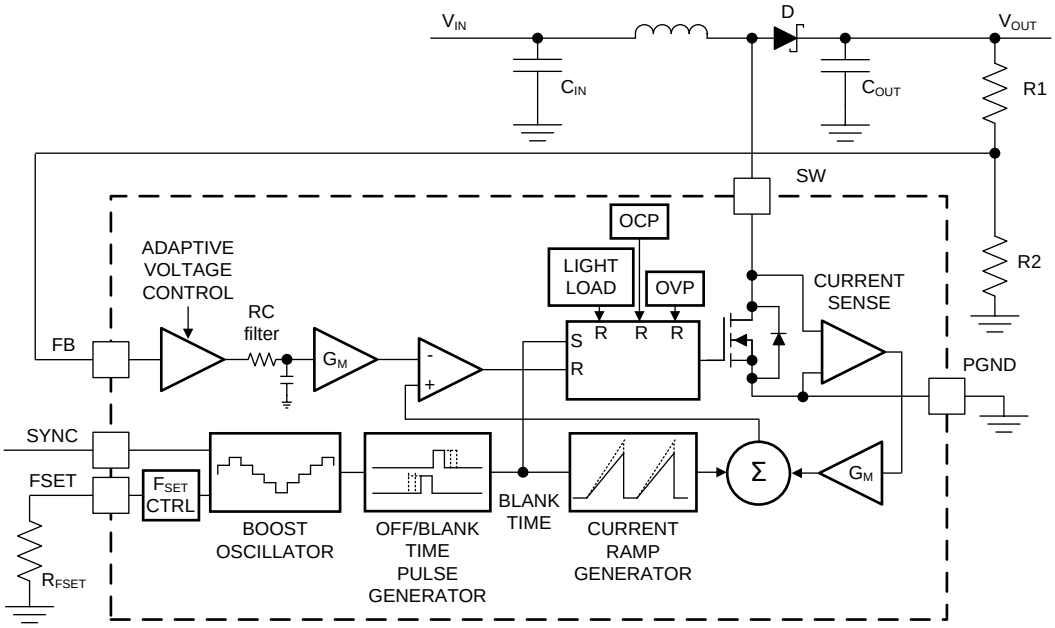


Figure 8. Boost Block Diagram

DC-DC can be driven by an external SYNC signal between 300 kHz…2.2 MHz (Table 2). If the external synchronization input disappears, DC-DC continues operation at the frequency defined by R_{FSET} resistor. When external frequency disappears and SYNC pin level is low, DC-DC continues operation without spread spectrum immediately. If SYNC remains high, DC-DC continues switching with spread spectrum enabled after 256 µs.

External SYNC frequency must be 1.2…1.5 times higher than the frequency defined by R_{FSET} resistor. Minimum frequency setting with R_{FSET} is 250 kHz to support a 300-kHz external clock.

The optional spread spectrum feature (±3% from central frequency, 1-kHz modulation frequency) reduces EMI noise at the switching frequency and its harmonic frequencies. When external synchronization is used, internal spread spectrum feature is not available.

Table 2. DC-DC Synchronization Mode

SYNC PIN INPUT	MODE
Low	Spread spectrum disabled
High	Spread spectrum enabled
300...2200 kHz frequency	Spread spectrum disabled, external synchronization mode

Table 3. DC-DC Parameters(1)

RANGE	FREQUENCY (kHz)	TYPICAL INDUCTANCE (µH)	TYPICAL INPUT AND OUTPUT CAPACITORS (µF)	MINIMUM SWITCH OFF TIME (ns)(2)	BLANK TIME (ns)	CURRENT RAMP (A/s)	CURRENT RAMP DELAY (ns)
1	300...480	33	2 × 10 (ceramic) + 33 (electrolytic)	150	95	24	550
2	480...1150	15	10 (ceramic) + 33 (electrolytic)	60	95	43	300
3	1150...1650	10	3 × 10 (ceramic)	40	95	79	0
4	1650...2200	4.7	3 × 10 (ceramic)	40	70	145	0

(1) Parameters are for reference only
(2) Due to current-sensing comparator delay the actual minimum off time is 6 ns (typical) longer than in the table.

The converter SW pin DC current is limited to 2 A (typical). To support warm start transient condition the current limit is automatically increased to 2.5 A for a short period of 1.5 seconds when a 2-A limit is reached.

NOTE

Application condition where the 2-A limit is exceeded continuously is not allowed. In this case the current limit would be 2 A for 1.5 seconds followed by 2.5-A limit for 1.5 seconds, and this 3-second period repeats.

7.3.2 Internal LDO

The internal LDO regulator converts the input voltage at VIN to a 4.3-V output voltage for internal use. Connect LDO output with a minimum of 1-µF ceramic capacitor to ground as close to the LDO pin as possible. If an external voltage higher than 4.5 V is connected to LDO pin, the internal LDO is disabled, and the internal circuitry is powered from the external power supply. VIN and VSENSE_N pins must be connected to the same external voltage as LDO pin. For an application example schematic refer to the LP8861-Q1 data sheet (SNVSA50).

7.3.3 LED Current Sinks

7.3.3.1 Current Sink Configuration

The LP8862-Q1 detects LED current sink configuration during start-up. A current sink connected to ground is disabled and excluded from the adaptive DC-DC control and fault detection.

7.3.3.2 Current Setting

Maximum current for the LED current sinks is controlled with external R_{ISET} resistor. Resistor value for targeted LED string current can be calculated using Equation 3:

$$R_{ISET} = 4422 / (I_{LED} – 13) \quad (3)$$

where

- R_{ISET} is current setting resistor, kΩ
- I_{LED} is output current per output, mA

7.3.3.3 Brightness Control

The LP8862-Q1 controls the brightness of the display with conventional PWM. Output PWM directly follows the input PWM. Input PWM frequency can be in the range of 100 Hz to 20 kHz. Dimming ratio is calculated as ratio between the input PWM period and minimum on/off time (0.5 µs).

7.3.4 Power Line FET Control

The LP8862-Q1 has a control pin (SD) for driving the gate of an external power-line FET. Power-line FET is an optional feature. Power-line FET limits inrush current by turning on gradually when the device is enabled (VDDIO/EN = high, $V_{IN} > V_{GS}$). Inrush current is controlled by increasing sink current for the FET gradually to 230 µA. In shutdown the LP8862-Q1 turns off the power-line FET and prevents possible DC-DC and LEDs leakage. The power switch also turns off in case of any fault which causes the device to enter FAULT RECOVERY state.

7.3.5 Fault Detections

The LP8862-Q1 has fault detection for LED open and short, V_{IN} input overvoltage (VIN_OVP), V_{IN} undervoltage lockout (VIN_UVLO), power-line overcurrent (VIN_OCP), and thermal shutdown (TSD).

7.3.5.1 Adaptive DC-DC Voltage Control and Functionality of LED Fault Comparators

Adaptive voltage control function adjusts the DC-DC output voltage to the minimum sufficient voltage for proper LED current sink operation. The current sink with highest V_F LED string is detected and DC-DC output voltage adjusted accordingly. DC-DC adaptive control voltage step size is defined by maximum voltage setting, $V_{STEP} = (V_{OUT\_MAX} – V_{OUT\_MIN)} /256$. Periodic down pressure is applied to the target voltage to achieve better system efficiency.

Every LED current sink has 3 comparators for the adaptive DC-DC control and LED-fault detections. Comparator outputs are filtered; filtering time is 1 µs.

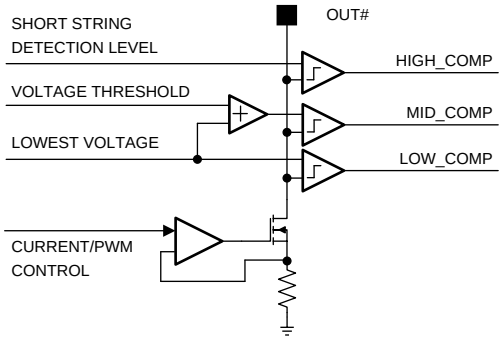


Figure 9. Comparators for Adaptive Voltage Control and LED Fault Detection

Figure 10 illustrates different cases which cause DC-DC voltage increase, decrease, or generate faults. In normal operation, voltage at the OUT1 and OUT2 pins is between LOW_COMP and MID_COMP levels, and V_{OUT} voltage stays constant. LOW_COMP level is the minimum for proper LED current sink operation, 1.1 × V_{SAT} + 0.2 V (typical). MID_COMP level is 1.1 × V_{SAT} + 1.2 V (typical) so typical headroom window is 1 V.

When voltage at OUT1 and OUT2 pin increases above MID_COMP level, DC-DC voltage adapts downwards.

When voltage at OUT1 or OUT2 pin falls below LOW_COMP threshold, DC-DC voltage adapts upwards. In the condition where V_{OUT} reaches the maximum and there are one or more outputs still below LOW_COMP level, an open LED fault is detected.

HIGH_COMP level, 6 V typical, is the threshold for shorted LED detection. When the voltage of OUT1 or OUT2 pin increases above HIGH_COMP level and the other output is within the normal headroom window, shorted LED fault is detected.

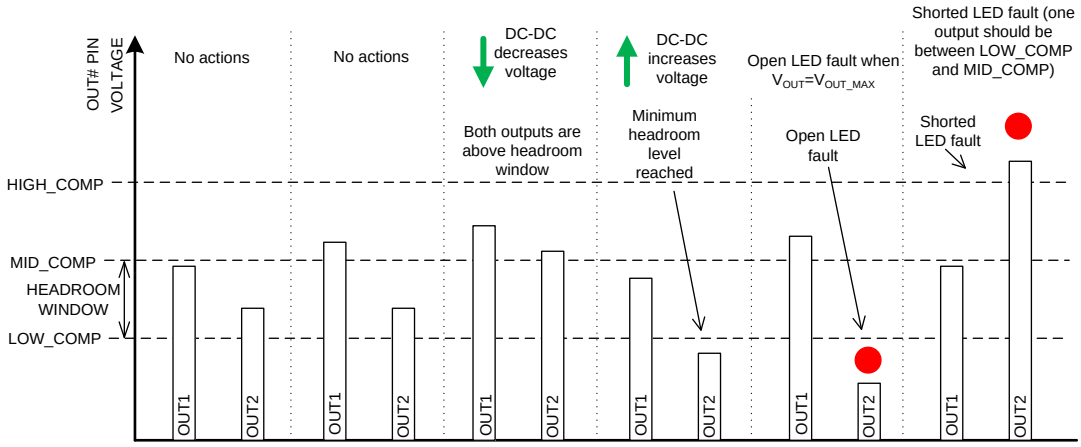


Figure 10. DC-DC Adaptation and LED Fault Detection Algorithms

7.3.5.2 Overview of the Fault/Protection Schemes

Summary of LP8862-Q1 fault detection behavior is shown in Table 4. Detected faults (excluding LED open or short) cause device to enter FAULT_RECOVERY state. In FAULT_RECOVERY the DC-DC and LED current sinks of the device are disabled, power-line FET is turned off, and the FAULT pin is pulled low. The device recovers automatically and enters normal operating mode (ACTIVE) after a recovery time of 100 ms if the fault condition has disappeared. When recovery is succesful, FAULT pin is released.

In case a LED fault is detected, device continues normal operation and only the faulty string is disabled. Fault is indicated via FAULT pin which can be released by toggling VDDIO/EN pin low for a short period of 2…20 µs. LEDs are turned off for this period but device stays in ACTIVE mode. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.

Table 4. Fault Detections

FAULT/ PROTECTION	FAULT NAME	THRESHOLD	FAULT PIN	FAULT_ RECOVERY STATE	ACTION
VIN overvoltage protection	VIN_OVP	1. V_{IN} > 42 V 2. V_{OUT} > V_{SET_DCDC} + 6..10 V. V_{SET_DCDC} is voltage value defined by logic during adaptation	Yes	Yes	1. Overvoltage is monitored from the beginning of soft start. Fault is detected if the duration of over-voltage condition is 100 µs minimum. 2. Overvoltage is monitored from the beginning of normal operation (ACTIVE mode). Fault is detected if over-voltage condition duration is 560 ms minimum (t_{filter}). After the first fault detection filter time is reduced to 50 ms for following recovery cycles. When device recovers and has been in ACTIVE mode for 160 ms, filter time is increased back to 560 ms .
VIN undervoltage lockout	VIN_UVLO	Falling 3.9 V Rising 4 V	Yes	Yes	Detects undervoltage condition at VIN pin. Sensed in all operating modes. Fault is detected if undervoltage condition duration is 100 µs minimum.
VIN overcurrent protection	VIN_OCP	3 A (50-mΩ current sensor resistor)	Yes	Yes	Detects over current by measuring voltage of the R_{ISENSE} resistor connected between VIN and VSENSE_N pins. Sensed from the beginning of soft start. Fault is detected if undervoltage condition duration is 10 µs minimum.
Open LED fault	OPEN_LED	LOW_COMP threshold	Yes	No	Detected if the voltage of OUT1 pin or OUT2 pin is below threshold level, and DC-DC adaptive control has reached maximum voltage. Open string(s) is removed from the adaptive voltage control loop and current sink is disabled. Fault pin is released by toggling VDDIO/EN pin. If VDDIO/EN is low for a period of 2…20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Shorted LED fault	SHORT_LED	Shorted string detection level 6 V	Yes	No	Detected if the voltage of OUT1 pin or OUT2 pin is above shorted string detection level, and the voltage of the other OUT pin is within headroom window. Shorted string is removed from the adaptive voltage control loop and current sink is disabled. Fault pin is released by toggling the VDDIO/EN pin. If VDDIO/EN is low for a period of 2…20 µs, LEDs are turned off for this period but device stays ACTIVE. If VDDIO/EN is low longer, device goes to STANDBY and restarts when EN goes high again.
Thermal protection	TSD	165ºC Thermal Shutdown Hysteresis 20ºC	Yes	Yes	Thermal shutdown is monitored from the beginning of soft start. Die temperature must decrease by 20°C for device to recover.

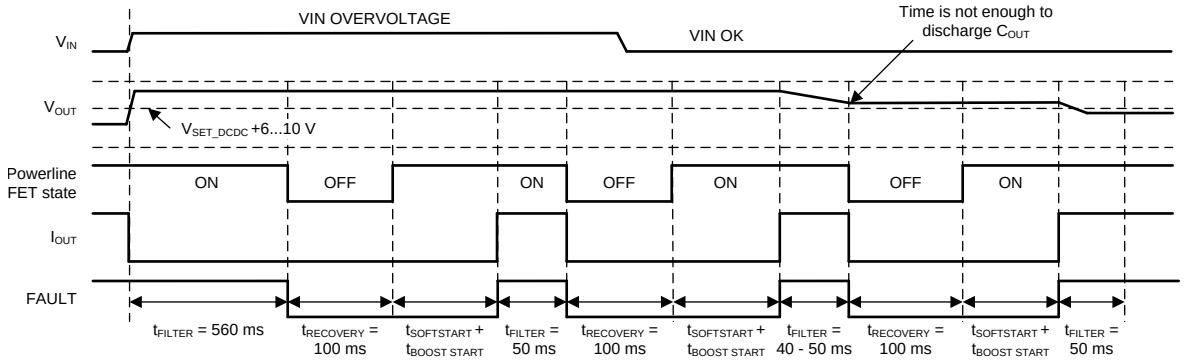


Figure 11. VIN Overvoltage Protection (DC-DC OVP)

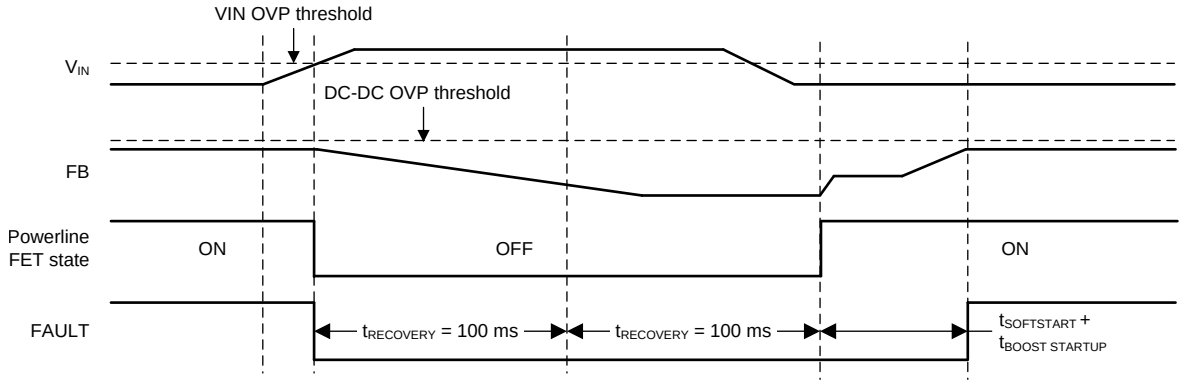


Figure 12. VIN Overvoltage Protection (VIN OVP)

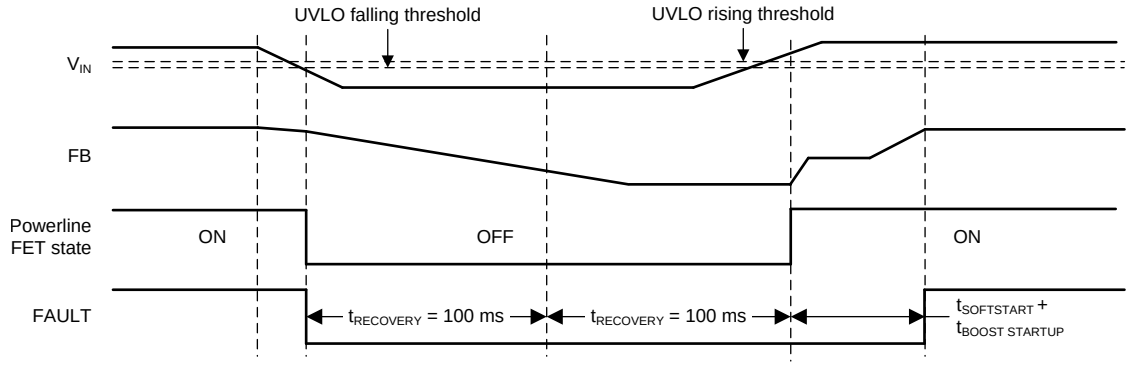


Figure 13. VIN Undervoltage Lockout

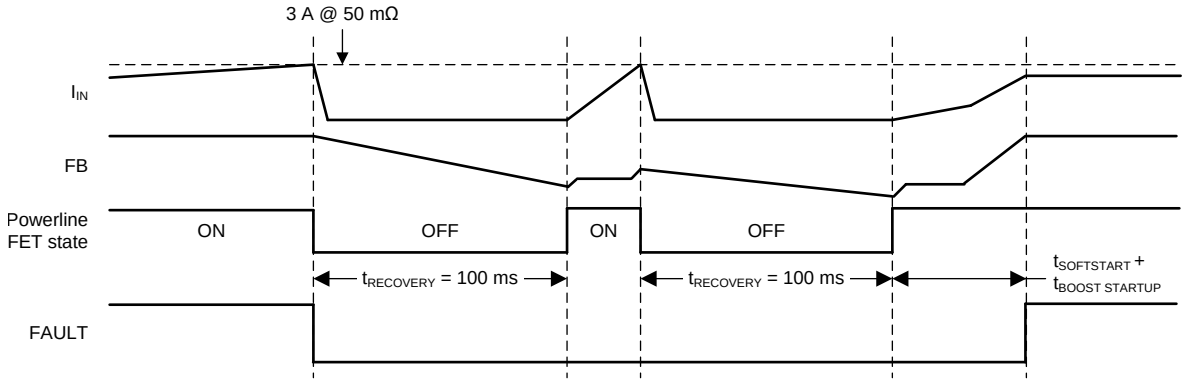


Figure 14. Input Voltage Overcurrent Protection

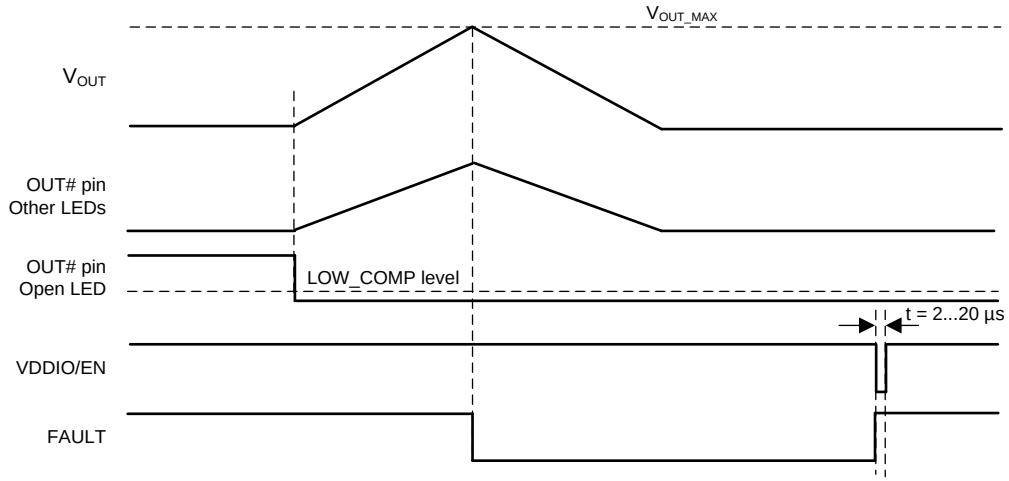


Figure 15. LED Open Fault

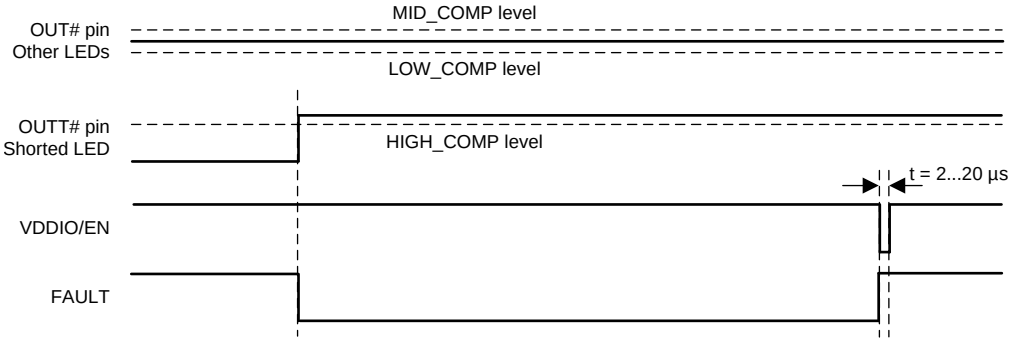


Figure 16. LED Short Fault

7.4 Device Functional Modes

7.4.1 Device States

The LP8862-Q1 enters STANDBY mode when the internal LDO output rises above the power-on reset level, $V_{LDO} > V_{POR}$. In STANDBY mode the device is able to detect the VDDIO/EN signal. When VDDIO/EN is pulled high, the device powers up. During soft start the external power-line FET is opened gradually to limit inrush current. Soft start is followed by boost (SEPIC) start, during which time V_{OUT} is ramped to the initial value. After boost (SEPIC) start LED outputs are sensed to detect grounded outputs. Grounded outputs are disabled and excluded from the adaptive boost (SEPIC) voltage control loop.

If a fault condition is detected, the LP8862-Q1 enters FAULT_RECOVERY state. In this state power line FET is switched off and both the boost (SEPIC) and LED current sinks are disabled. Faults that cause the device to enter FAULT_RECOVERY are shown in Figure 17. When LED open or short is detected, faulty string is disabled but the device stays in ACTIVE mode.

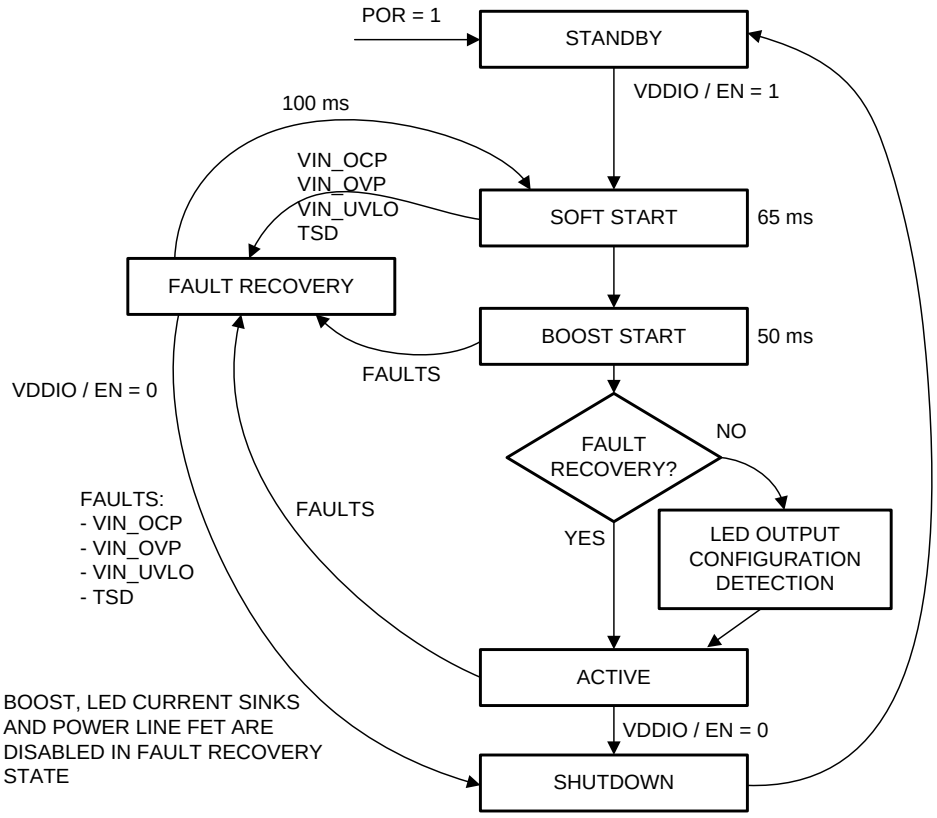


Figure 17. State Diagram

Device Functional Modes (continued)

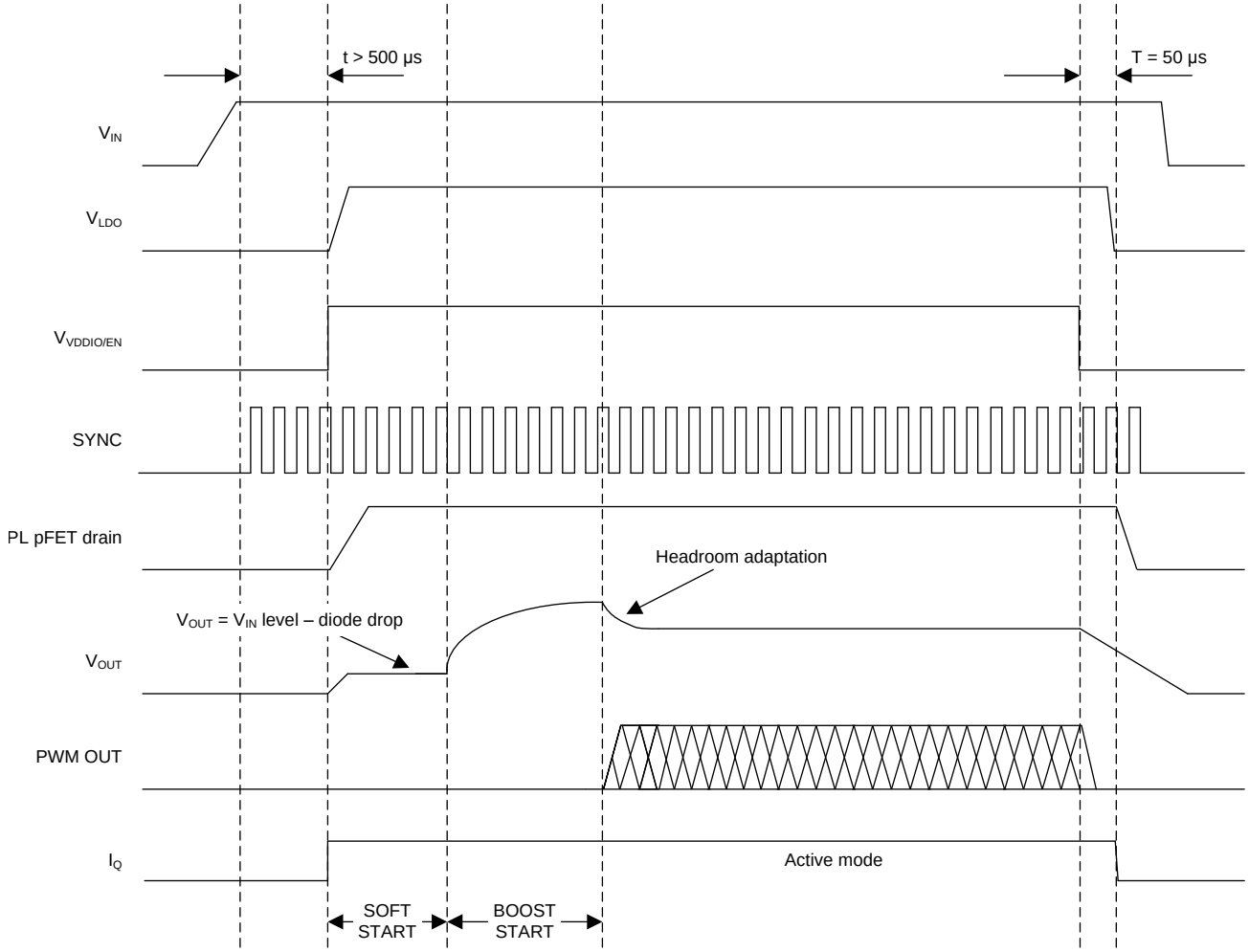


Figure 18. Timing Diagram for Typical Start-Up and Shutdown

8 Application and Implementation

8.1 Application Information

The LP8862-Q1 is designed for automotive applications, and an input voltage V_{IN} is intended to be connected to the automotive battery. Device circuitry is powered from the internal LDO, which can alternatively be used as an external VDD voltage — in this case external voltage should be in 4.5-V to 5.5-V range.

The LP8862-Q1 uses a simple four-wire control:

- VDDIO/EN for enable
- PWM input for brightness control
- SYNC pin for boost synchronisation (optional)
- FAULT output to indicate fault condition (optional)

8.2 Typical Applications

8.2.1 Typical Application for 2 LED Strings

Figure 19 shows typical application for the LP8862-Q1 which supports 2 LED strings with maximum current 160 mA per string. Boost switching frequency in this example is is 400 kHz.

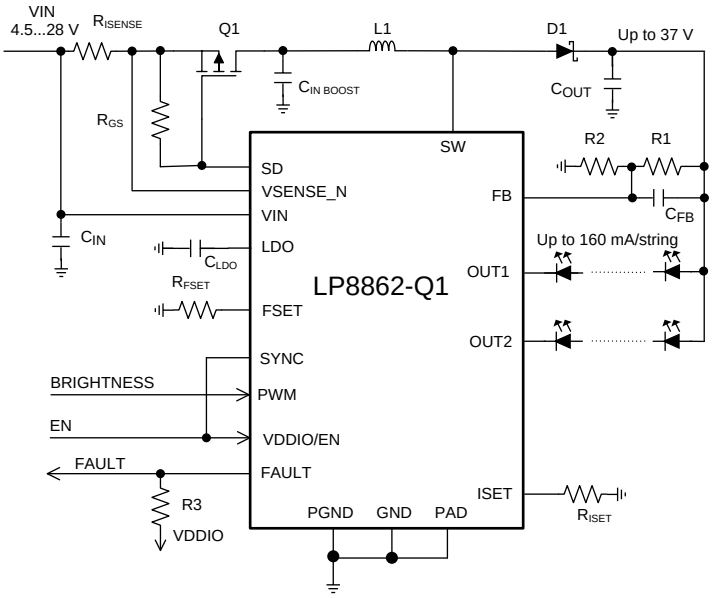


Figure 19. LP8862-Q1 Boost Mode, Two Strings, 160-mA String Configuration

Typical Applications (continued)

8.2.1.1 Design Requirements

Typical design parameters for a boost-mode two-string configuration are shown in Table 5:

Table 5. Boost Mode Design Parameters

DESIGN PARAMETER	VALUE
VIN voltage range	4.5…28 V
LED string	2 × 8 LEDs (30 V)
LED string current	160 mA
Max boost voltage	37 V
Boost switching frequency	400 kHz
External boost sync	not used
Boost spread spectrum	enabled
L1	22 µH
C_{IN}	10 µF, 50 V
$C_{IN\ BOOST}$	2 × (10-µF 50-V ceramic) + 33-µF 50-V electrolytic
C_{OUT}	2 × (10-µF 50-V ceramic) + 33-µF 50-V electrolytic
C_{FB}	15 pF
C_{LDO}	1 µF, 10 V
R_{ISET}	30 kΩ
R_{FSET}	160 kΩ
R_{ISENSE}	50 mΩ
R1	750 kΩ
R2	130 kΩ
R3	10 kΩ
R_{GS}	20 kΩ

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

There are two main considerations when choosing an inductor; the inductor must not saturate, and the inductor current ripple must be small enough to achieve the desired output voltage ripple. Different saturation current rating specifications are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C. However, ratings at the maximum ambient temperature of application should be requested from the manufacturer. Shielded inductors radiate less noise and are preferred. The saturation current must be greater than the sum of the maximum load current and the worst case average-to-peak inductor current. Equation 4 shows the worst-case conditions:

$$I_{SAT} > \frac{I_{OUTMAX}}{D'} + I_{RIPPLE} \quad \text{For Boost}$$

$$\text{Where } I_{RIPPLE} = \frac{(V_{OUT} - V_{IN})}{(2 \times L \times f)} \times \frac{V_{IN}}{V_{OUT}}$$

$$\text{Where } D = \frac{(V_{OUT} - V_{IN})}{(V_{OUT})} \text{ and } D' = (1 - D)$$

- I_{RIPPLE} - peak inductor current
- I_{OUTMAX} - maximum load current
- V_{IN} - minimum input voltage in application
- L - min inductor value including worst case tolerances
- f - minimum switching frequency
- V_{OUT} - output voltage
- D - Duty Cycle for CCM Operation
- V_{OUT} - Output Voltage

(4)

As a result the inductor must be selected according to the I_{SAT}. A more conservative and recommended approach is to choose an inductor that has a saturation current rating greater than the maximum current limit. A saturation current rating of at least 3 A is recommended for most applications. See Table 3 for inductance recommendations for the different switching frequency ranges. Resistance of the inductor must be less than 300 mΩ for good efficiency.

See detailed information in *Understanding Boost Power Stages in Switch Mode Power Supplies*. "Power Stage Designer™ Tools" can be used for the boost calculation: http://www.ti.com/tool/powerstage-designer.

8.2.1.2.2 Output Capacitor Selection

A ceramic capacitor with 2 × $V_{MAX\ BOOST}$ or more voltage rating is recommended for the output capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different boost switching frequencies are shown in Table 3. To minimize audible noise of ceramic capacitors their geometric size must typically be minimized.

8.2.1.2.3 Input Capacitor Selection

A ceramic capacitor with 2 × $V_{VIN\ MAX}$ or more voltage rating is recommended for the input capacitor. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Capacitance recommendations for different boost switching frequencies are shown in Table 3.

8.2.1.2.4 LDO Output Capacitor

A ceramic capacitor with at least 10-V voltage rating is recommended for the output capacitor of the LDO. The DC-bias effect can reduce the effective capacitance by up to 80%, which needs to be considered in capacitance value selection. Typically a 1-µF capacitor is sufficient.

8.2.1.2.5 Diode

A Schottky diode should be used for the boost output diode. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer. Diode rating for peak repetitive current should be greater than inductor peak current (up to 3 A) to ensure reliable operation. Average current rating must be greater than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. Choose a reverse breakdown voltage of the Schottky diode significantly larger than the output voltage.

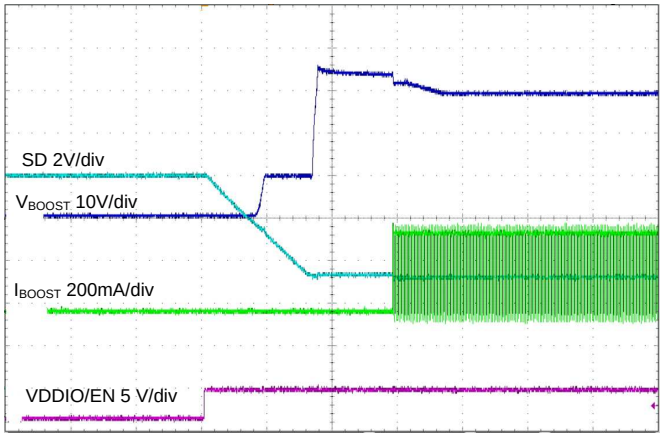
8.2.1.2.6 Power Line Transistor

A pFET transistor with necessary voltage rating (V_{DS} at least 5 V higher than max input voltage) must be used. Current rating for the FET must be the same as input peak current or greater. Transfer characteristic is very important for pFET. V_{GS} for open transistor must be less then V_{IN}. A 20-kΩ resistor between pFET gate and source is sufficient.

8.2.1.2.7 Input Current Sense Resistor

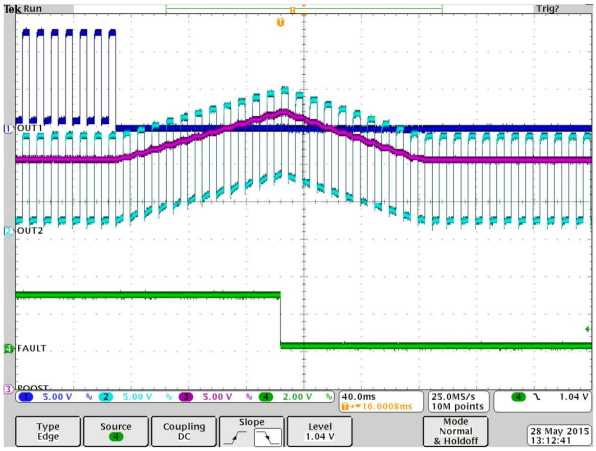
A high-power 50 mΩ resistor must be used for sensing the boost input current. Power rating can be calculated from the input current and sense resistor resistance value. Increasing R_{ISENSE} decreases VIN_OCP current proportionally.

8.2.1.3 Application Curves



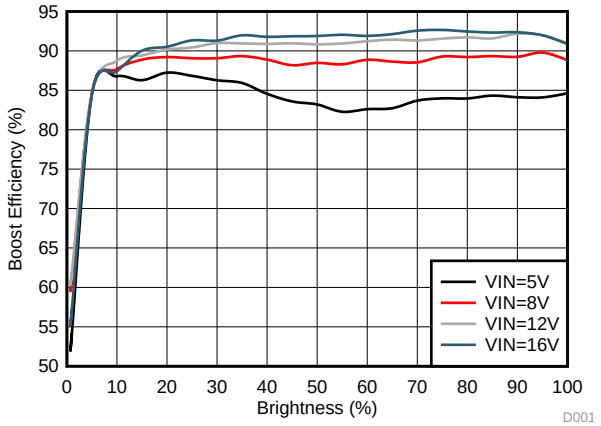
f_{SW} = 300 kHz V_{IN} = 10 V
Brightness PWM 50% 100 Hz

Figure 20. Typical Start-Up



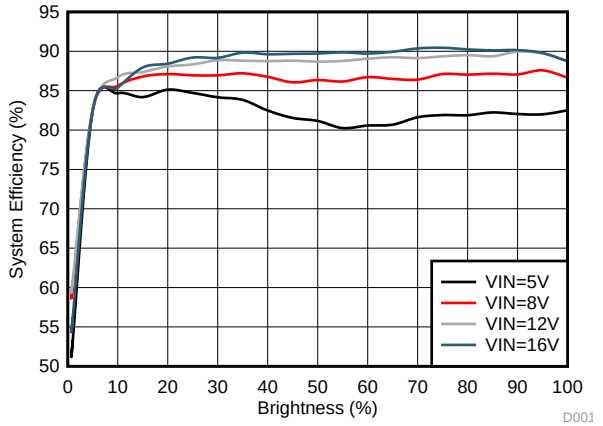
Open string connected to OUT1

Figure 21. Open LED Fault



Two strings, 8 LEDs per string f_{SW} = 400 kHz
160 mA/string for V_{IN} = 12 V and V_{IN} = 16 V
130 mA/string for V_{IN} = 8 V
90 mA/string for V_{IN} = 5 V

Figure 22. Boost Efficiency



Two strings, 8 LEDs per string f_{SW} = 400 kHz
160 mA/string for V_{IN} = 12 V and V_{IN} = 16 V
130 mA/string for V_{IN} = 8 V
90 mA/string for V_{IN} = 5 V

Figure 23. System Efficiency

8.2.2 SEPIC Mode Application

When LED string voltage can be above or below V_{IN} voltage, SEPIC configuration can be used. In Figure 24 an external frequency is used to synchronize SEPIC switching frequency. External frequency can be modulated to spread switching frequency spectrum.

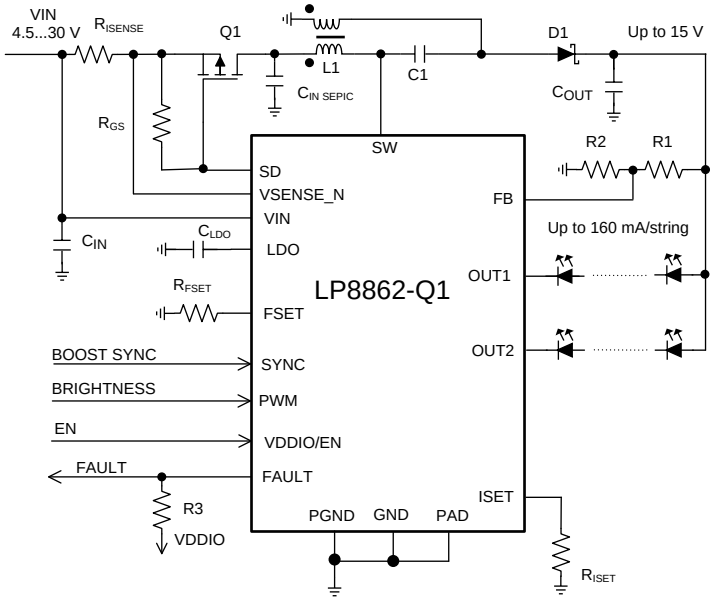


Figure 24. SEPIC Mode, 2 Strings, 160-mA String Configuration

Typical design parameters for a SEPIC-mode two-string configuration are shown in Table 6:

Table 6. SEPIC Mode Design Parameters

DESIGN PARAMETER	VALUE
VIN voltage range	4.5…30 V
LED string	2 × 2 LEDs (9 V)
LED string current	160 mA
Max output voltage	15 V
SEPIC switching frequency	300 kHz
External boost sync	used
Spread spectrum	Internal spread spectrum not available, external frequency input can be modulated
L1	22 µH
C_{IN}	10 µF, 50 V
$C_{IN\ SEPIC}$	2 × (10-µF 50-V ceramic) + 33-µF 50-V electrolytic
C_{OUT}	2 × (10-µF 50-V ceramic) + 33-µF 50-V electrolytic
C_{LDO}	1 µF, 10 V
R_{ISET}	30 kΩ
R_{FSET}	210 kΩ
R_{ISENSE}	50 mΩ
R1	300 kΩ
R2	130 kΩ
R3	10 kΩ
R_{GS}	20 kΩ

8.2.2.1 Detailed Design Procedure

In SEPIC mode the maximum voltage at the SW pin is equal to the sum of the input voltage and the output voltage. Because of this, the maximum sum of input and output voltage must be limited below 50 V. See Detailed Design Procedure for general external component guidelines. The main differences of SEPIC compared to boost are described below.

Power Stage Designer™ Tool can be used for modeling SEPIC behavior: http://www.ti.com/tool/powerstage-designer. For detailed explanation on SEPIC see Texas Instruments Analog Applications Journal *Designing DC/DC Converters Based on SEPIC Topology* (SLYT309).

8.2.2.1.1 Inductor

In SEPIC mode, coupled coil saturation rating should be higher than input side inductor peak current. Current values can be estimated using *Power Stage Designer™ Tool* or using equations in SLYT309.

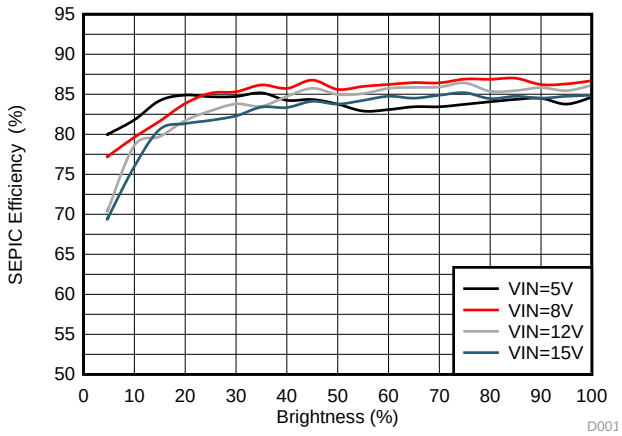
8.2.2.1.2 Diode

In SEPIC mode diode peak current is equal to the sum of input and output currents. Diode rating for peak repetitive current must be greater than SW pin current limit (up to 3 A for transients) to ensure reliable operation. Average current rating must be greater than the maximum output current. Voltage rating must be higher than sum of input and output voltages.

8.2.2.1.3 Capacitor C1

A ceramic capacitor with low ESR is recommended. Voltage rating must be higher than maximum input voltage.

8.2.2.2 Application Curves

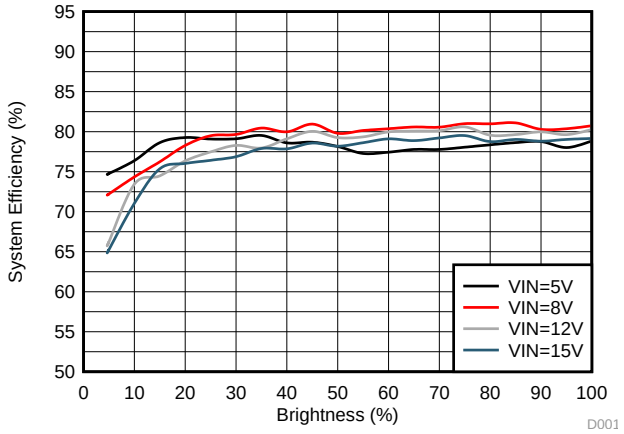


Two strings, 2 LEDs per string

160 mA/string

f_{SW} = 300 kHz

Figure 25. SEPIC Efficiency



Two strings, 2 LEDs per string

160 mA/string

f_{SW} = 300 kHz

Figure 26. System Efficiency

9 Power Supply Recommendations

The LP8862-Q1 device is designed to operate from an automotive battery. The device must be protected from reversal voltage and voltage dump over 50 V. The resistance of the input supply rail must be low enough so that the input current transient does not cause too-high drop at the LP8862-Q1 VIN pin. If the input supply is connected by using long wires additional bulk capacitance may be required in addition to the ceramic bypass capacitors in the V_{IN} line.

10 Layout

10.1 Layout Guidelines

Figure 27 shows a recommended layout for the LP8862-Q1 used to demonstrate the principles of a good layout. This layout can be adapted to the actual application layout if or where possible. It is important that all boost components are close to the chip, and the high current traces must be wide enough. By placing boost components on one side of the chip it is easy to keep the ground plane intact below the high current paths. This way other chip pins can be routed more easily without splitting the ground plane. Place LDO capacitor as close to LDO pin as possible.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to the SW and PGND pins. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents try to find route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
- The GND plane needs to be intact under the high current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting need to be on the same direction in optimal case.
- Inductor placement should be so that the current flows in the same direction as in the current loops. Rotating inductor 180° changes current direction.
- Use separate power and noise free grounds. The power ground is used for boost converter return current and noise-free ground for more sensitive signals, like LDO bypass capacitor grounding as well as grounding the GND pin of LP8862-Q1 device itself.
- Boost output feedback voltage to LEDs needs to be taken out *after* the output capacitors, not straight from the diode cathode.
- Place LDO 1-µF bypass capacitor as close as possible to the LDO pin.
- Input and output capacitors need strong grounding (wide traces, many vias to GND plane).
- If two output capacitors are used they need symmetrical layout to get both capacitors working ideally.
- Output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable on some loads and this increases EMI. DC bias characteristics need to be obtained from the component manufacturer; it is not taken into account on component tolerance. X5R/X7R capacitors are recommended.

10.2 Layout Example

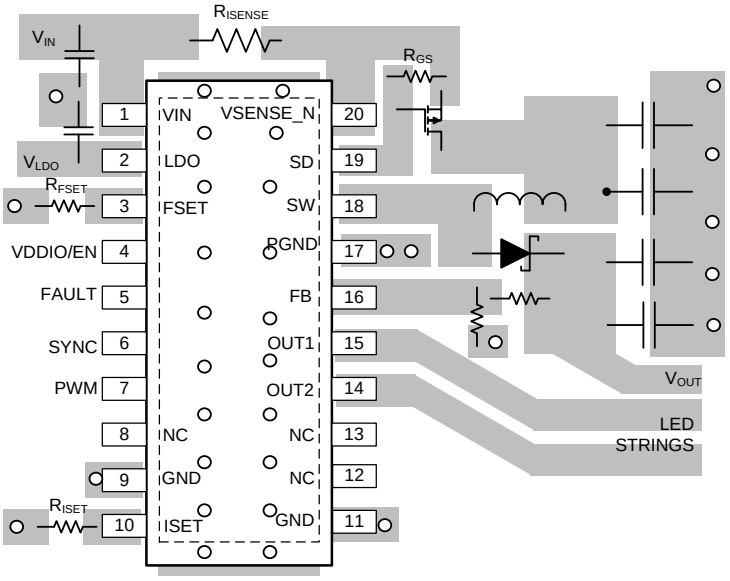


Figure 27. LP8862-Q1 Boost Layout

11 Device and Documentation Support

11.1 Third-Party Products Disclaimer

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Using the LP8862-Q1EVM Evaluation Module* (SNVU478)
- *PowerPAD™ Thermally Enhanced Package Application Note* (SLMA002)
- Texas Instruments Application Report *Understanding Boost Power Stages in Switch Mode Power Supplies* (SLVA061
- Texas Instruments Analog Applications Journal *Designing DC/DC Converters Based on SEPIC Topology* (SLYT309)
- Power Stage Designer™ Tool can be used for both boost and SEPIC: http://www.ti.com/tool/powerstage-designer

11.3 Trademarks

All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP8862QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LP8862Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

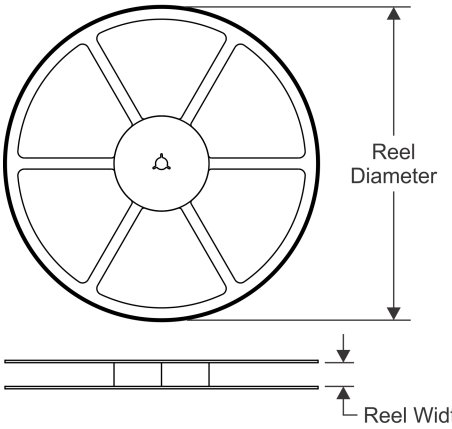
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

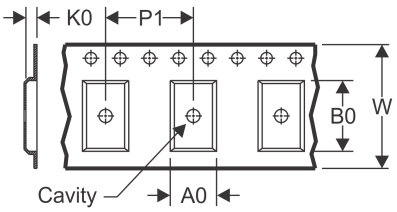
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

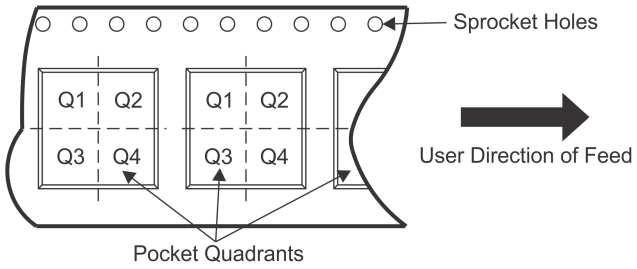


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

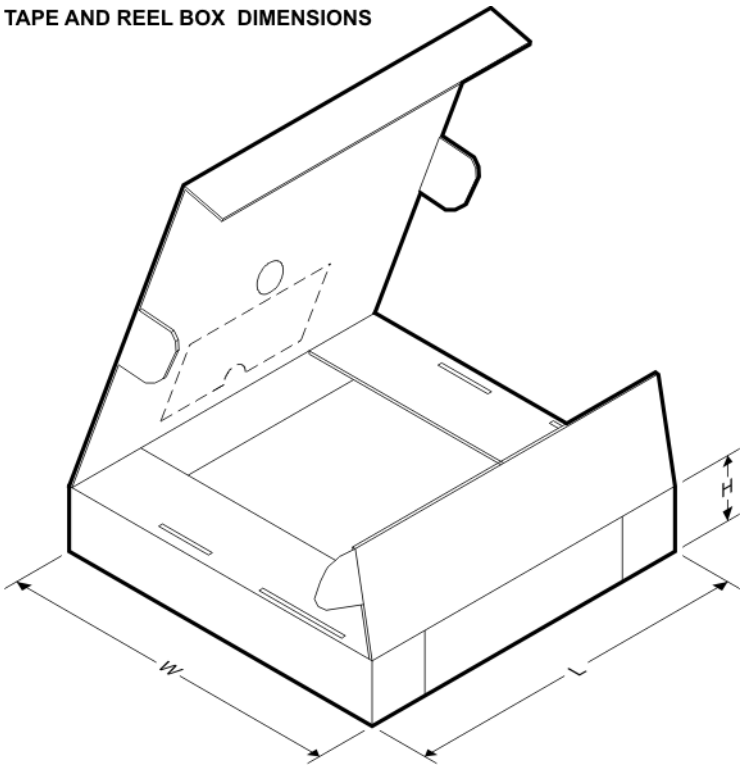
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8862QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8862QPWPRQ1	HTSSOP	PWP	20	2000	367.0	367.0	38.0

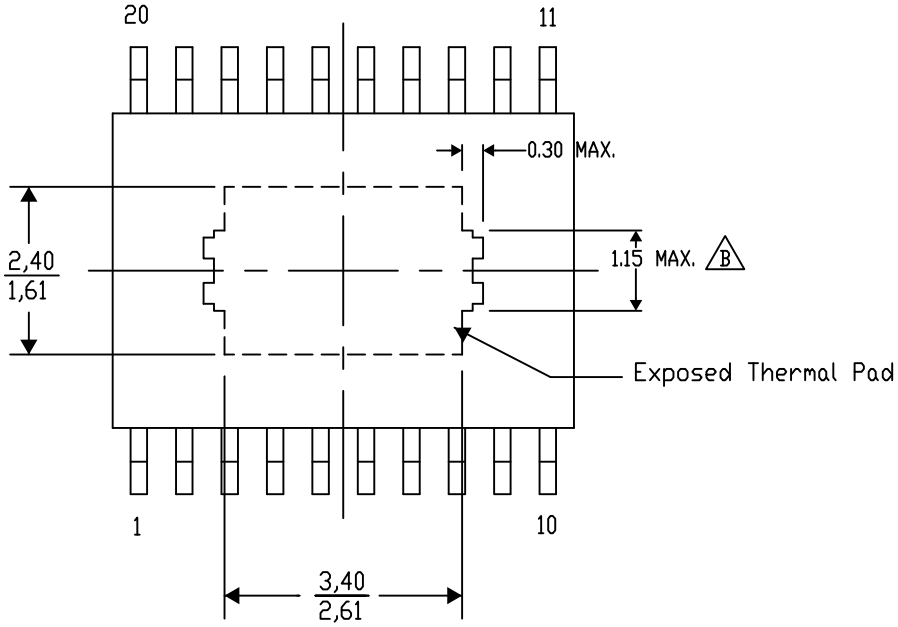
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

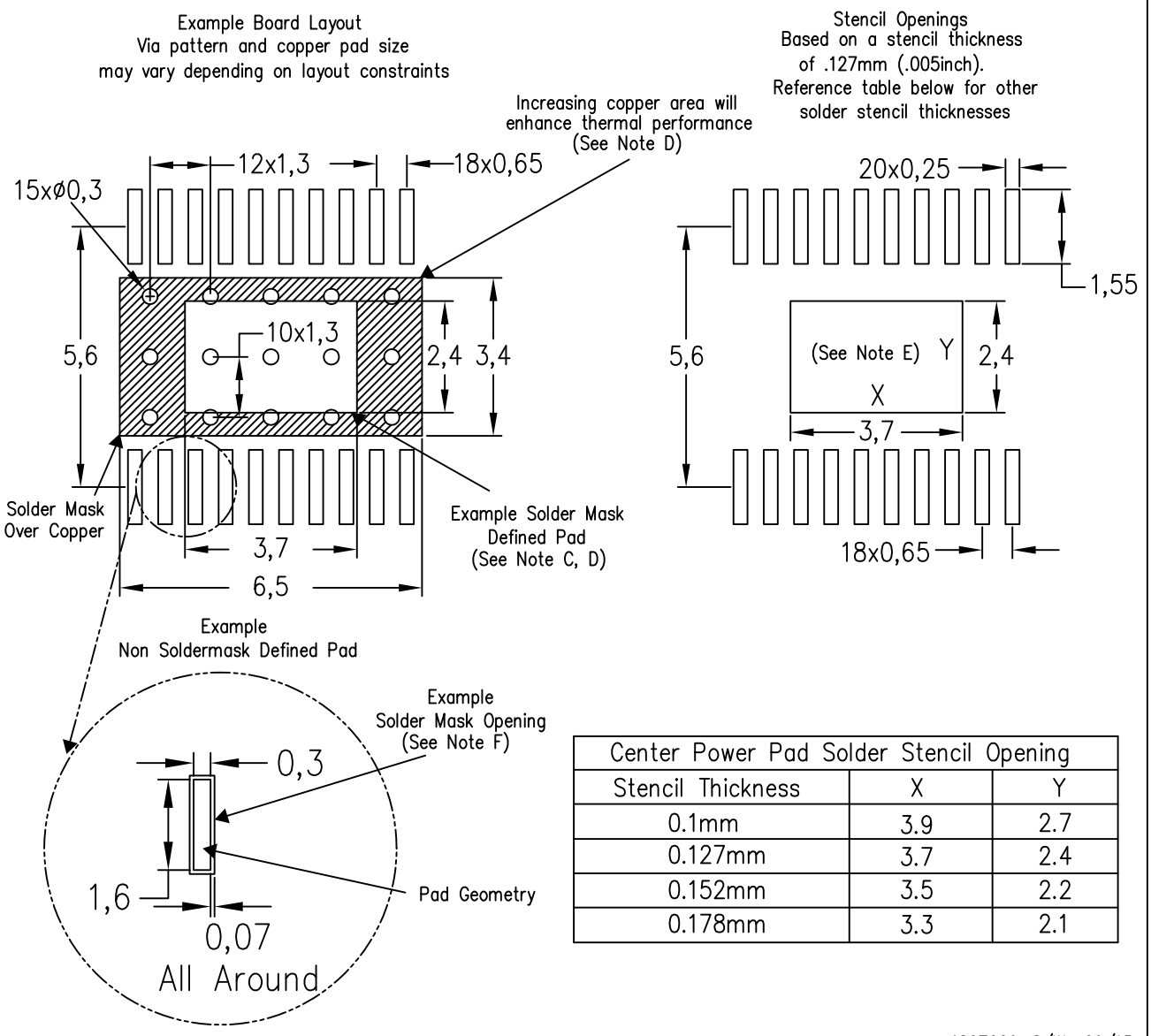
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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