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**PRODUCT BULLETIN**

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**ISSUE DATE:** 04-Mar-2016

**NOTIFICATION:** 17117

**TITLE:** Kinetis V Update RM, DS and Errata to Reflect Changes and Added KMS

**EFFECTIVE DATE:** 08-Mar-2016

**DEVICE(S)**

MPN
MKV30F128VFM10
MKV30F128VLF10
MKV30F128VLH10
MKV30F64VFM10
MKV30F64VLF10
MKV30F64VLH10
MKV31F128VLH10
MKV31F128VLH10P
MKV31F128VLL10
MKV31F256VLH12
MKV31F256VLH12P
MKV31F256VLL12
MKV31F512VLH12
MKV31F512VLL12
MKV31F512VLL12P

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**AFFECTED CHANGE CATEGORIES**

- DATASHEET
- ERRATA
- REFERENCE MANUAL

**DESCRIPTION OF CHANGE**

## REFERENCE MANUAL

Kinetis KV30: 100MHz Cortex-M4F 64/128KB Flash 32-64pin at

[http://cache.nxp.com/files/microcontrollers/doc/ref\\_manual/KV30P64M100SFARM.pdf](http://cache.nxp.com/files/microcontrollers/doc/ref_manual/KV30P64M100SFARM.pdf)

Kinetis KV31: 100MHz Cortex-M4F 128KB Flash (64/100pin) at

[http://cache.nxp.com/files/microcontrollers/doc/ref\\_manual/KV31P100M100SF9RM.pdf](http://cache.nxp.com/files/microcontrollers/doc/ref_manual/KV31P100M100SF9RM.pdf)

Kinetis KV31: 120MHz Cortex-M4F 512KB Flash (64/100pin) at

[http://cache.nxp.com/files/microcontrollers/doc/ref\\_manual/KV31P100M120SF7RM.pdf](http://cache.nxp.com/files/microcontrollers/doc/ref_manual/KV31P100M120SF7RM.pdf)

Kinetis KV31: 120MHz Cortex-M4F 256KB Flash (64/100pin) at

[http://cache.nxp.com/files/microcontrollers/doc/ref\\_manual/KV31P100M120SF8RM.pdf](http://cache.nxp.com/files/microcontrollers/doc/ref_manual/KV31P100M120SF8RM.pdf)

### Updates Include:

Added KMS Module Functional Categories and KMS orderable part number.

Other minor changes to Reference Manual to correct documentation errors.

Updated "Flash Memory Sizes" Section.

Updated MDM-AP Status register assignments and MDM-AP Control register assignments

Updated Debug and Security section

In Pin Control Register (PCRN), added additional details to Interrupt Configuration field (IRQC) description.

Flash Bootloader section updates

SMC - removed RAM2 content.

Crossbar Corrected errors in features, and memory map/ register definitions

**DMAMUX** - Updated the offset address of the registers nad in code examples

**eDMA** - Add notes to fault Reporting and handling, peak transfer rates, removed two feature bullets, Changed name descriptions in registers

**EWM** updated block diagram, update EWM refresh mechanism table

**MCG** - updated bitfiled access in the MCG\_SC register and the reset value of MCG\_C2 [FCTRIM] to x

**FMC** - corrected FMC\_PFAPR reset value

FTFA - Modify FSEC[MEEN] register field description

FTFA - Modify Flash Commands by Mode table entries for Read 1s All Blocks and Erase All Blocks commands

FTFA - Add Read 1s All Execute-only Segments and Erase All Execute-only Segments commands; modify list of Margin Read Commands

FTFA - Add reference to AN5112 in Flash Access Protection

FTFA - Add ACCERR check for mode/security in Error Handling table for Verify Backdoor Access Key and Read 1s All Blocks commands

FTFA - Change column heading from Byte to Offset Address in configuration field description table

FTFA - Add suggestion to bit poll FSTAT[CCIF] for command completion in Generic flash command write sequence flowchart

FTFA - Clarify that ACCERR and FPVIOL flags must be clear before ERSSUSP can be set in Suspending an Erase Flash Sector Operation

FTFA - Remove erroneous reference to the flash configuration field in Suspending an Erase Flash Sector Operation

FTFA - Specify minimum time of 4.3 msec between request to resume and suspend erase in Resuming an Erase Flash Sector Operation

FTFA - Correct FPROT register description when supporting 2KB sectors

FTFA - Add list of specific commands impacted by Flash Access Protection

FTFA - Clarify writability of ACCERR and FPVIOL while CCIF is set in FSTAT register description

EZPORT - In "EzPort commands" table, modified footnote in BE row from "Bulk Erase is accepted when security is set and only when the BEDIS status field is not set," to "Bulk Erase is accepted when the BEDIS status field is not set."

EZPORT - In In "EzPort status register field description," in BEDIS row:

EZPORT - In Modified field description from "Indicates whether bulk erase (BE) is disabled when flash is secure," to "Indicates whether bulk erase (BE) is disabled."

EZPORT - In Modified first sentence of bit setting description for '1', from "1 = BE is disabled if FS is also set," to "1 = BE is disabled."

FLEXBUS - clarified Set/Clear in RDAH bitfield of CSCR register, added note to "Initializing chip-select" section, update color to diagram,

FLEXBUS - All Timing Diagrams added TIP waveform, state variables and other information

CRC- Wording change to Intro

ADC - changed bitfield access of ADC\_SC3[CALF] to w1c.

CMP - Update field description of CFF and CFR in CMP status and control register

VREF - Added internal Voltage Regulator topic to the chapter.

PDB - added pulse-out diagram, clarified SC[LDOK], added a note to multiple registers about SC[LDOK]

FTM - added note to block diagram, add a feature in list, clarify SC register clock source.

FTM - clarified external trigger in Channel Trigger output, add cross-reference

FTM - update bitfield FTM\_SC[CLKS] description,

FTM - Updated Edge-Aligned PWM mode description, clarified counter clock source references, added detail about input capture.

SPI - added two topics, update section Continuous Serial Communication clock, update reset value of Status register, fix errors in SMSZ bitfield.

SPI - added RXFRn to statements about transfer error, updated bit field descriptions, added notes,

SPI - previous errata moved into RM - In Module Configuration Register(SPI\_MCR) note to the [CLR\_RXF] bit field.

I2C - corrected figure Typical I2C interrupt routine, added notes

UART - added notes to bitfield MODEM[TXRTSE], added overbar to CTS signal in table.

LPUART - update field descriptions of WATER[RXWATER] and STAT[RDRF]

GPIO - update features

### ERRATA:

Mask Set Errata for Mask 0N36M-Errata at [http://cache.nxp.com/files/32bit/doc/errata/KINETIS\\_V\\_0N36M.pdf](http://cache.nxp.com/files/32bit/doc/errata/KINETIS_V_0N36M.pdf)  
Mask Set Errata for Kinetis V Mask 0N51M at [http://cache.nxp.com/files/32bit/doc/errata/KINETIS\\_V\\_0N51M.pdf](http://cache.nxp.com/files/32bit/doc/errata/KINETIS_V_0N51M.pdf)  
Mask Set Errata for Kinetis V Mask 0N50M at [http://cache.nxp.com/files/32bit/doc/errata/KINETIS\\_V\\_0N50M.pdf](http://cache.nxp.com/files/32bit/doc/errata/KINETIS_V_0N50M.pdf)  
Mask Set Errata for Kinetis V Mask 0N74K at [http://cache.nxp.com/files/32bit/doc/errata/KINETIS\\_V\\_0N74K.pdf](http://cache.nxp.com/files/32bit/doc/errata/KINETIS_V_0N74K.pdf)

### Errata Application Summary for KV3x MCUs

Errata # added	KV30F128	KV31F128	KV31F256	KV31F512	Errata Title
e10121	Yes	Yes			FTFA: For MCUs prior to work week 14 of 2016, FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured.
e10120			Yes		FTFA: For MCUs prior to work week 14 of 2016, FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured.
e10028				Yes	FTFA: For MCUs prior to work week 14 of 2016, FSEC[MEEN] = 10 disables Mass Erase only when the MCU is secured.
e9646	Yes				WDOG: Unexpected watchdog behavior on LLS exit
e7857	Yes				UART: WT timer in T=0 mode and CWT timer in T=1 mode can expire between 0.2 ETU to 0.8 ETU earlier than programmed.
e10123	Yes	Yes			Kinetis Flashloader/ ROM Bootloader: For MCUs prior to work week 14 of 2016, the peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader
e10122			Yes		Kinetis Flashloader/ ROM Bootloader: For MCUs prior to work week 14 of 2016, the peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader
e10116				Yes	Kinetis Flashloader/ ROM Bootloader: For MCUs prior to work week 14 of 2016, the peripheral auto-detect code in bootloader can falsely detect presence of SPI host causing non-responsive bootloader
e8184	Yes	Yes	Yes	Yes	UART: During ISO-7816 T=0, TC bit set at 12 ETUs may cause loss of characters when UART is switched from transmit to receive mode
e9005	Yes	Yes	Yes	Yes	Core: Store immediate overlapping exception return operation might vector to incorrect interrupt
e8992	Yes	Yes	Yes	Yes	AWIC: Early NMI wakeup not detected upon entry to stop mode from VLPR mode
e8361	Yes	Yes	Yes	Yes	SMC: Compute Operation cannot be enabled in HSRUN mode
e7986				Yes	LPUART: The LPUART_TX pin is tri-stated when the transmitter is disabled
e8807		Yes	Yes	Yes	USB: In Host mode, transmission errors may occur when communicating with a Low Speed (LS) device through a USB hub
e8101			Yes	Yes	e8101: USBOTG: USB host signal crossover voltage higher than specification at low temperature
e8096		Yes	Yes	Yes	DAC12: DNL for DAC12 operating in Low-Power Mode larger than specification for some devices

•Note - 'Yes' in part number column means the errata is added. Blank indicate n/a

•Note - Workarounds available for all errata,

–e009457 is fixed errata removed e10123,e10122 and e10116 explain transition, Updated Flashloader included with this release.

–e010028,e10120 and e10121, added to explain Flash IP added features.

#### DATA SHEETS:

Kinetis KV31: 100MHz Cortex-M4F 128KB Flash (64/100pin) at [http://cache.nxp.com/files/microcontrollers/doc/data\\_sheet/KV31P100M100SF9.pdf](http://cache.nxp.com/files/microcontrollers/doc/data_sheet/KV31P100M100SF9.pdf)  
Kinetis KV31: 120MHz Cortex-M4F 512KB Flash (64/100pin) at [http://cache.nxp.com/files/microcontrollers/doc/data\\_sheet/KV31P100M120SF7.pdf](http://cache.nxp.com/files/microcontrollers/doc/data_sheet/KV31P100M120SF7.pdf)  
Kinetis KV31: 120MHz Cortex-M4F 256KB Flash (64/100pin) at [http://cache.nxp.com/files/microcontrollers/doc/data\\_sheet/KV31P100M120SF8.pdf](http://cache.nxp.com/files/microcontrollers/doc/data_sheet/KV31P100M120SF8.pdf)  
Kinetis KV30: 100MHz Cortex-M4F 64/128KB Flash 32-64pin at [http://cache.nxp.com/files/microcontrollers/doc/data\\_sheet/KV30P64M100SFA.pdf](http://cache.nxp.com/files/microcontrollers/doc/data_sheet/KV30P64M100SFA.pdf)

#### Updates Include:

Added Kinetis Motor Suite(KMS) Functionality described in KV3x Data Sheets and new orderable part numbers for KMS

Added "S" in format and part number table and updated part number example

Added Terminology and Guidelines section.

Features added to MCUS:

Mass erase from the MDM-AP control register is disable if MEEN bits are set to disable Mass erase. (FSEC[MEEN] = 10).

The FSEC[MEEN] bits are relevant at all times in all NVM modes.

The Erase all Blocks command blocked by FSEC[MEEN]=10.

EZPORT - Bulk Erase command is accepted only when mass erase is enabled.

Two new Flash commands are being added.

- 1) 0x4A Read 1s All Execute only Segments
- 2) 0x4B Erase All Execute-only Segments

### **REASON FOR CHANGE**

Kinetis Motor Suite(KMS) is being introduced for KV3x MCUs.

Kinetis Motor Suite (KMS) is a bundled hardware and software solution aimed at enabling rapid configuration

of motor drive systems and accelerating application development. KMS includes firmware targeting the Kinetis V (KV) series of microcontrollers (MCUs) and an intuitive PC-based graphical user interface. It supports field oriented velocity and position control of three phase permanent magnet and brushless DC motors.

Updates to the Reference Manual, Data Sheet and Errata reports were made to support the KMS introduction. Additional documentation errors were fixed and recently discovered errata have been added.

Additional flash features were added to MCU's with Flash Access Controls features in order to provide increased protection the flash contents from accidental erasure.

### **ANTICIPATED IMPACT OF PRODUCT CHANGE(FORM, FIT, FUNCTION, OR RELIABILITY)**

The flash operation is 100% backward compatible with existing use of the flash protection. The flash features added increases protection against accidental mass erasure of the flash contents. Errata number ERR010028 describe the basic features and implementation date. There are possible software implications to customers if the new features are to be used.

The errata describe existing conditions identified on current production devices.

Kinetis Motor Suite(KMS) features and enabled part numbers have been added to data sheet and reference manual documents.

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#### **NOTE:**

THE CHANGE(S) SPECIFIED IN THIS NOTIFICATION WILL BE IMPLEMENTED ON THE EFFECTIVE DATE LISTED ABOVE. To request further data or inquire about the notification, please enter a [Support Case](#). Be aware that after you select this link to enter your request, you must choose the

topic "Product Change Notification" once on the Salesforce page.

For sample inquiries - please go to [www.nxp.com](http://www.nxp.com)

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**QUAL DATA AVAILABILITY DATE:** 22-Feb-2016

**QUALIFICATION STATUS:** N/A

**QUALIFICATION PLAN:**

N/A

**RELIABILITY DATA SUMMARY:**

N/A

**ELECTRICAL CHARACTERISTIC SUMMARY:**

N/A

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**CHANGED PART IDENTIFICATION:**

N/A

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**ATTACHMENT(S):**

N/A

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