PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPD-PWR/12/7506
Dated 10 Oct 2012

IPAK and Short IPAK in ECOPACK 2, graded Moulding Compound Assembly capacity expansion - Nantong Fujitsu Microelectronics (China) Subcontractor

Table 1. Change Implementation Schedule

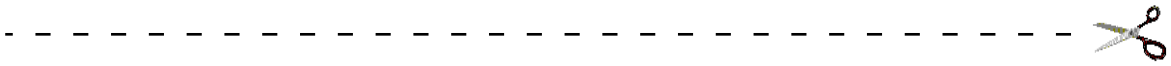
Forecasted implementation date for change	05-Oct-2012
Forecasted availability date of samples for customer	05-Oct-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	05-Oct-2012
Estimated date of changed product first shipment	09-Jan-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly location change, Testing location change
Reason for change	To increase capacity on IPAK and Short IPAK package
Description of the change	Continuing in the program to introduce ECOPACK 2, graded Moulding Compound products and in order to be ready to support the market demand of Power MOSFET Transistors, the products listed in this PCN will be manufactured also in Nantong Fujitsu Microelectronics (China) Subcontractor. Products are in agreement with ST standards and guarantee the same quality and the electrical characteristics as the current production. Devices used for qualification are available as samples.
Change Product Identification	1st two digits of the traceability code are "GF"
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPD-PWR/12/7506**
Please sign and return to STMicroelectronics Sales Office	**Dated 10 Oct 2012**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Please be informed that IPAK and Short IPAK Package, manufactured in ST sites, will be also produced in Nantong Fujitsu Microelectronics (China) Subcontractor, according to the program to introduce ECOPACK 2 grade products.

The involved product series and affected packages are listed in the table below:

Product Family	Package	Commercial Product / Series
Power MOSFET Transistors	Short IPAK	STUXXX-S
	IPAK	STUxxx/STDxxx-1

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 40-2012.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Part Number - Test Vehicle
Power MOSFET Transistors	STU7NM60N STD4NK60Z-1 STU60N3LH5

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors	From Week 01-2013

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipments may start earlier with customer written agreement.

Marking and traceability:

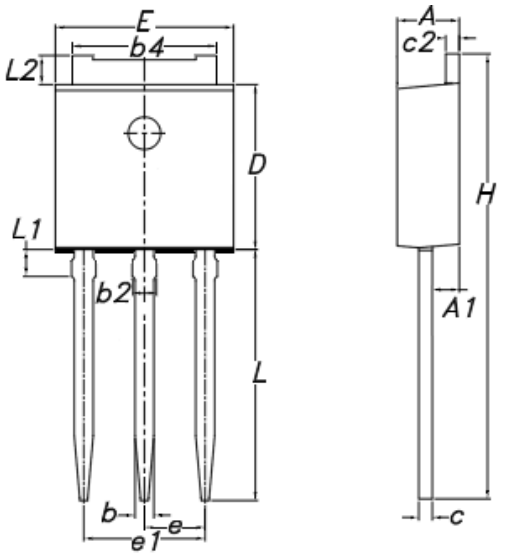
Unless otherwise stated by customer specific requirement, traceability of IPAK and Short IPAK ECOPACK 2 graded moulding compound products, manufactured in Nantong Fujitsu Microelectronics (China), will be ensured by the 1st two digits of the traceability code "GF".

Sincerely Yours.

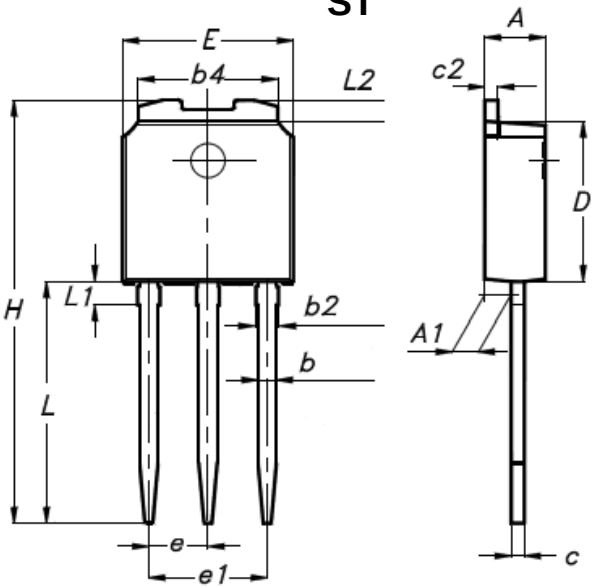
IPAK package comparison Fujitsu Vs ST

SYMBOL	FUJITSU			ST		
	IPAK			IPAK		
	MIN	NOM	MAX	MIN	NOM	MAX
A		2.3	2.35	2.2	-	2.35
A1	0.9	1	1.1	0.9	-	1.1
b	0.58	-	0.79	0.64	-	0.9
b2	-	-	0.9	-	-	0.95
b4	5.23	5.33	5.43	5.2	-	5.4
c	0.46	-	0.59	0.45	-	0.6
c2	0.46	-	0.59	0.48	-	0.6
D	6	6.1	6.2	6	-	6.15
E	6.5	6.6	6.7	6.4	-	6.55
e		2.25		-	2.28	-
e1	4.4	4.5	4.6	4.4	-	4.6
H		16.48		-	16.1	-
L	9	9.3	9.6	9	-	9.4
L1	0.8	1	1.2	0.8	-	1.2
L2		1.08	1.25	-	0.8	1

Fujitsu



ST



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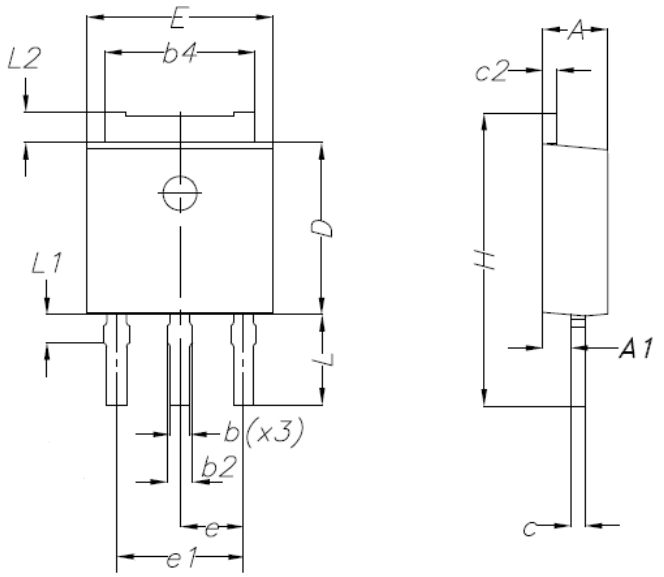
Short IPAK package comparison Fujitsu Vs ST

SYMBOL	FUJITSU			ST		
	Short IPAK			Short IPAK		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.2	2.3	2.35	2.2	-	2.35
A1	0.9	1	1.1	0.9	-	1.1
b	0.58	-	0.79	0.64	-	0.9
b2	-	-	0.9	-	-	0.95
b4	5.23	5.33	5.43	5.2	-	5.4
c	0.46	-	0.59	0.45	-	0.6
c2	0.46	-	0.59	0.48	-	0.6
D	6	6.1	6.2	6	-	6.15
E	6.5	6.6	6.7	6.4	-	6.55
e		2.25		-	2.25	-
e1	4.4	4.5	4.6	4.4	-	4.6
H	10.08	10.38	10.68	9.8	10.4	-
L	3	3.2	3.4	3	-	3.4
L1	0.8	1	1.2	0.8	-	1.2
L2		1.08	1.25	-	0.8	1

Fujitsu



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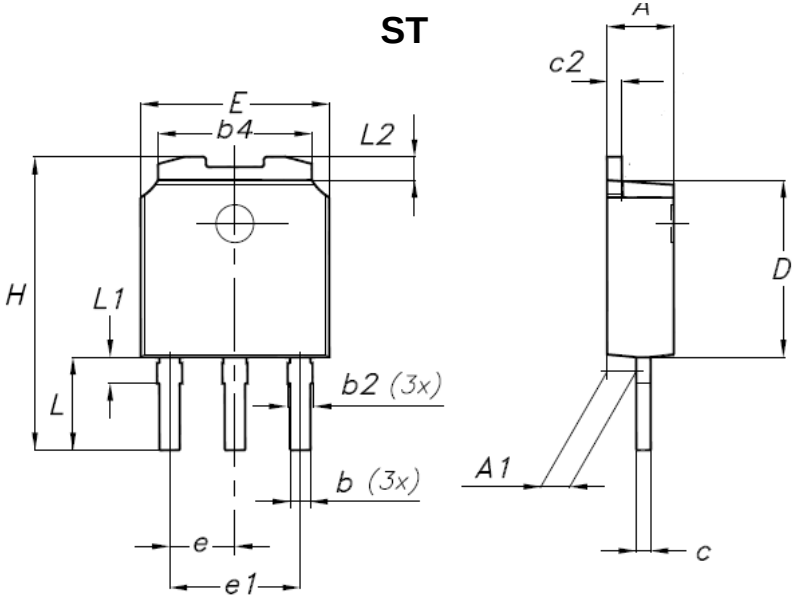

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Reliability Report

IPAK and Short IPAK in ECOPACK 2, Graded Molding Compound Assembly capacity expansion – Nantong Fujitsu Microelectronics (China) Subcontractor

General Information	
Product Lines:	M260 - EZ62 - 5H33
Product Families:	Power MOSFET
P/Ns:	STU7NM60N (M260) STD4NK60Z-1 (EZ62) STU60N3LH5 (5H33)
Product Group:	IMS - IPD
Product division:	Power Transistor Division
Package:	IPAK
Silicon Process techn.:	MDmesh™ II, SuperMESH™, STripFET™ V

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio (SINGAPORE) – M5 Catania (ITALY)*
EWS Plants:	*Ang Mo Kio (SINGAPORE) – M5 Catania (ITALY)*
Assembly plant:	*Nantong Fujitsu Microelectronics (China)*
Reliability Lab:	*IMS-IPD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	September 2012	9	C. Cappello	G.Falcone	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the IPAK and Short IPAK package graded Molding Compound manufactured in Nantong Fujitsu Microelectronics (China).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STU7NM60N LINE: M260 PACKAGE: IPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	MDmesh™ II
Die finishing back side	Ti/Ni/Au
Die size	2410 x 2400 µm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	NANTONG FUJITSU (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Ni on T-post
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 5 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	NANTONG FUJITSU (China)
Tester	JUNO

D.U.T.: STD4NK60Z-1 LINE: EZ62 PACKAGE: IPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*Ang Mo Kio (Singapore)*
Technology	SuperMESH™
Die finishing back side	Ti/Ni/Ag
Die size	3186 x 2654 μm^2
Metal	Al/Si
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*Ang Mo Kio (Singapore)*
Test program	WPIS

Assembly information	
Assembly site	NANTONG FUJITSU (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Ni on T-post
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 5 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	NANTONG FUJITSU (China)
Tester	JUNO

D.U.T.: STU60N3LH5 LINE: 5H33 PACKAGE: IPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	*M5 Catania (ITALY)*
Technology	STripFET™ V
Die finishing back side	Ti/Ni/Ag
Die size	2300 x 1750 µm^2
Metal	Al/Cu
Passivation type	None

Wafer Testing (EWS) information	
Electrical testing manufacturing location	*M5 Catania (ITALY)*
Test program	WPIS

Assembly information	
Assembly site	NANTONG FUJITSU (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper - Ni on T-post
Die attach process	Soft Solder
Die attach material	Pb/Ag/Sn
Wire bonding process	Ultrasonic
Wires bonding materials	Al 5 mils Gate Al 10 mils Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	NANTONG FUJITSU (China)
Tester	JUNO

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STU7NM60N	M260	Power MOSFET
2	STU7NM60N	M260	Power MOSFET
3	STU7NM60N	M260	Power MOSFET
4	STD4NK60Z-1	EZ62	Power MOSFET
5	STU60N3LH5	5H33	Power MOSFET

5.2 Reliability test plan summary

Lot. 1÷3 - D.U.T.: STU7NM60N LINE: M260 PACKAGE: IPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS		
						Lot 1	Lot 2	Lot 3
HTRB	N	JESD22 A-108	T.A.=150℃ Vdss=480V	77 x 3 lots	168 H	0/77	0/77	0/77
					500 H			
					1000 H			
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 30V	77 x 3 lots	168 H	0/77	0/77	0/77
					500 H			
					1000 H			
HTSL	N	JESD22 A-103	TA = 150℃	77 x 3 lots	168 H	0/77	0/77	0/77
					500 H			
					1000 H			
H3TRB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77 x 3 lots	168 H	0/77	0/77	0/77
					500 H			
					1000 H			
TC	N	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77 x 3 lots	100 cy	0/77	0/77	0/77
					200 cy			
					500 cy			
					1000 cy			
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105℃	20 x 3 lots	5K cy	0/20	0/20	0/20
					10K cy			
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77 x 3 lots	96 H	0/77	0/77	0/77

Lot. 4 - D.U.T.: STD4NK60Z-1 LINE: EZ62 PACKAGE: IPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 4
HTRB	N	JESD22 A-108	T.A.=150℃ Vdss=480V	77 x 1 lot	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 30V	77 x 1 lot	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 150℃	77 x 3 lots	168 H 500 H 1000 H	0/77
H3TRB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=100V	77 x 1 lot	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77 x 1 lot	100 cy 200 cy 500 cy 1000 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105℃	20 x 1 lot	5K cy 10K cy	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77 x 1 lot	96 H	0/77

Lot. 5 - D.U.T.: STU60N3LH5 LINE: 5H33 PACKAGE: IPAK

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS Lot 4
HTRB	N	JESD22 A-108	T.A.=175℃ Vdss=24V	77 x 1 lot	168 H 500 H 1000 H	0/77
HTGB	N	JESD22 A-108	TA = 150℃ Vgss= 20V	77 x 1 lot	168 H 500 H 1000 H	0/77
HTSL	N	JESD22 A-103	TA = 175℃	77 x 3 lots	168 H 500 H 1000 H	0/77
H3TRB	N	JESD22 A-101	Ta=85℃ Rh=85%, Vdd=30V	77 x 1 lot	168 H 500 H 1000 H	0/77
TC	N	JESD22 A-104	TA=-65℃ TO 150℃ (1 HOUR/CYCLE)	77 x 1 lot	100 cy 200 cy 500 cy 1000 cy	0/77
TF/IOL	N	Mil-STD 750D Method 1037	ΔTc=+105℃	20 x 1 lot	5K cy 10K cy	0/20
AC	N	JESD22 A-102	TA=121℃ – PA=2 ATM	77 x 1 lot	96 H	0/77

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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