



PQMD13

NPN/PNP resistor-equipped transistors;
R1 = 4.7 k Ω , R2 = 47 k Ω

4 November 2015

Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistors (RET) in a leadless ultra small DFN1010B-6 (SOT1216) Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PQMH13

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Low package height of 0.37 mm
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

4. Quick reference data

Table 1. Quick reference data

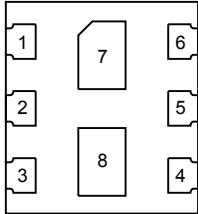
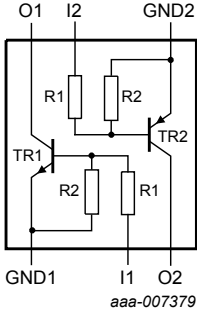
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor; for the PNP transistor with negative polarity							
V _{CEO}	collector-emitter voltage	open base	-	-	50	V	
I _O	output current		-	-	100	mA	
Per transistor; for the PNP transistor with negative polarity							
R1	bias resistor 1	T _{amb} = 25 °C	[1]	3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		[1]	8	10	12	

[1] See section "Test information" for resistor calculation and test conditions.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view DFN1010B-6 (SOT1216)</p>	 <p>GND1 I2 GND2 O1 I1 O2 TR1 TR2 R1 R2 aaa-007379</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PQMD13	DFN1010B-6	DFN1010B-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1216

7. Marking

Table 4. Marking codes

Type number	Marking code
PQMD13	B 011

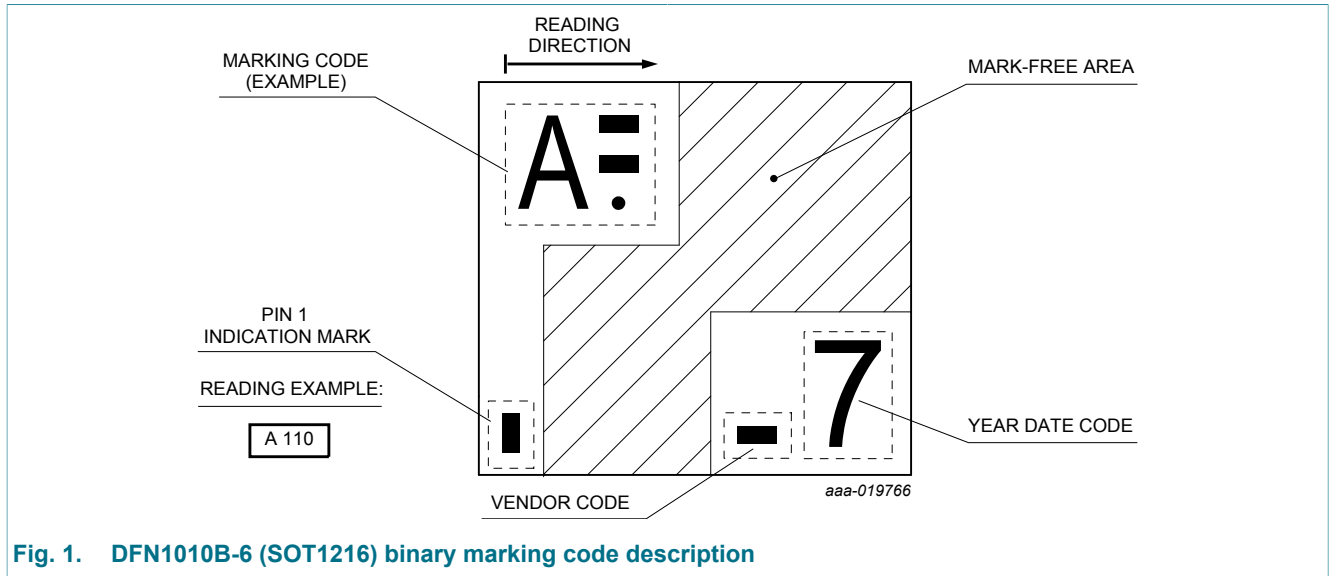


Fig. 1. DFN1010B-6 (SOT1216) binary marking code description

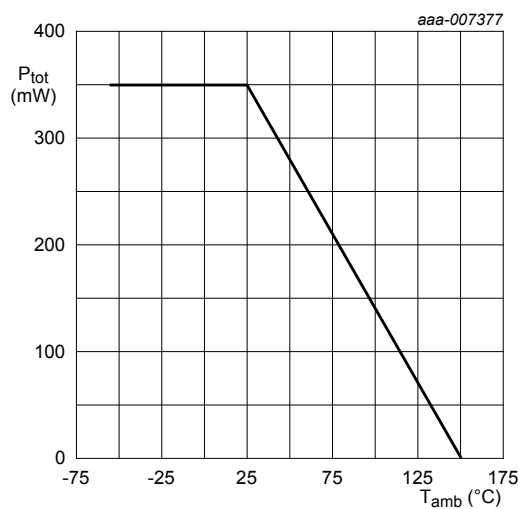
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
V _I	input voltage	TR1; positive		-	30	V
		TR1; negative		-	-5	V
		TR2; positive		-	5	V
		TR2; negative		-	-30	V
I _O	output current			-	100	mA
I _{CM}	peak collector current	t _p ≤ 1 ms; single pulse		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	230	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	350	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, standard footprint

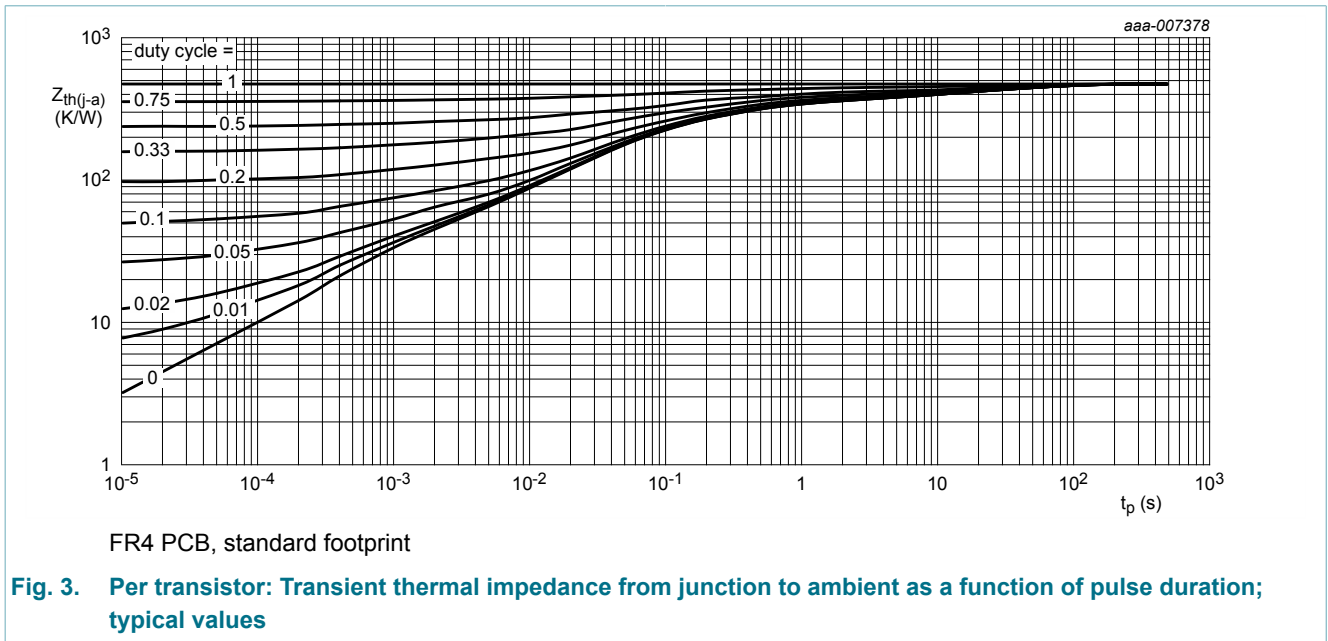
Fig. 2. Per device: Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	543	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	357	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
I_{CBO}	collector-base cut-off current (emitter open)	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$		-	-	100	nA
I_{CEO}	collector-emitter cut-off current (base open)	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$		-	-	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_{amb} = 150\text{ }^\circ\text{C}$		-	-	5	μA
I_{EBO}	emitter-base cut-off current (collector open)	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}; T_{amb} = 25\text{ }^\circ\text{C}$		-	-	170	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 5\text{ mA}; I_B = 0.25\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$		-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}; T_{amb} = 25\text{ }^\circ\text{C}$		-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 5\text{ mA}; T_{amb} = 25\text{ }^\circ\text{C}$		1.3	0.9	-	V
R1	bias resistor 1	$T_{amb} = 25\text{ }^\circ\text{C}$	[1]	3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		[1]	8	10	12	
C_C	collector capacitance	$V_{CB} = 10\text{ V}; I_E = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR1 (NPN)}$		-	-	2.5	pF
		$V_{CB} = -10\text{ V}; I_E = 0\text{ A}; f = 1\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR2 (PNP)}$		-	-	3	pF
f_T	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR1 (NPN)}$	[2]	-	230	-	MHz
		$V_{CE} = -5\text{ V}; I_C = -10\text{ mA}; f = 100\text{ MHz}; T_{amb} = 25\text{ }^\circ\text{C}; \text{TR2 (PNP)}$	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor

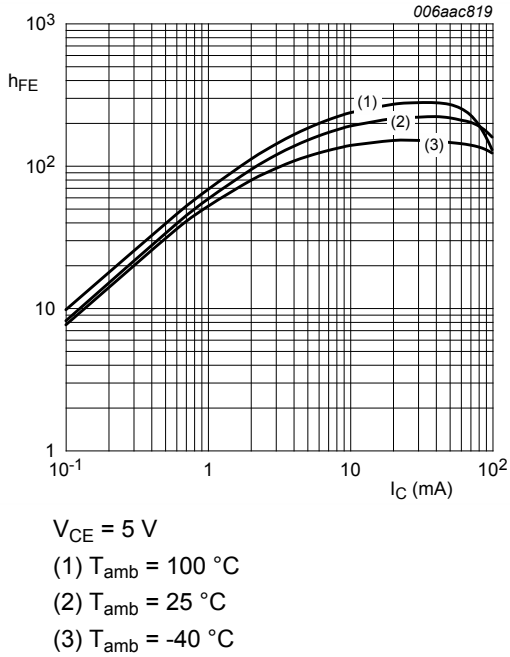


Fig. 4. NPN transistor: DC current gain as a function of collector current; typical values

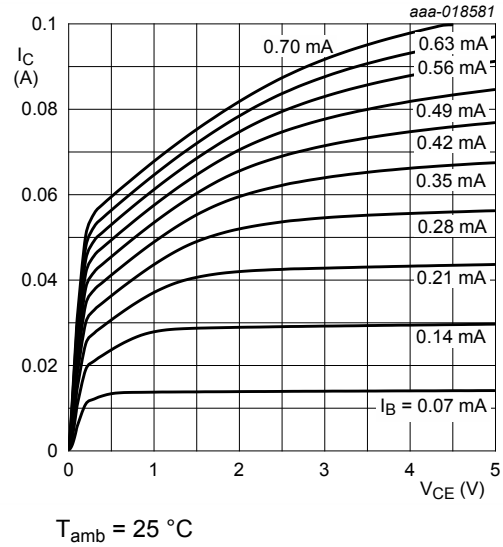


Fig. 5. NPN transistor: Collector current as a function of collector-emitter voltage; typical values

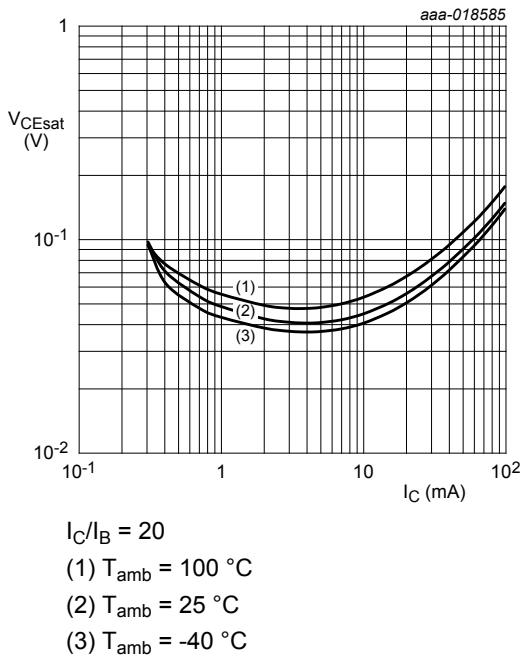


Fig. 6. NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values

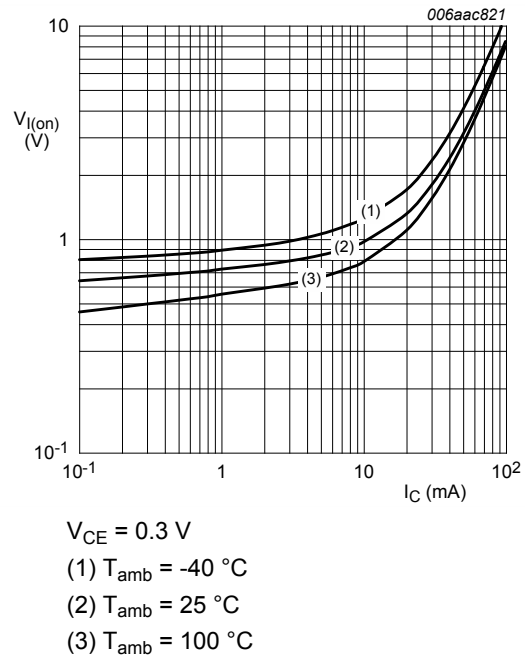
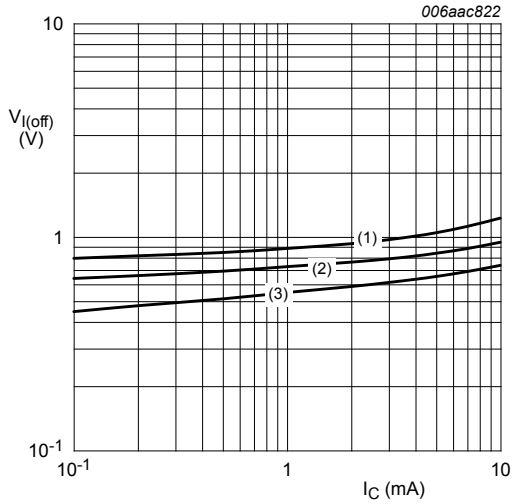
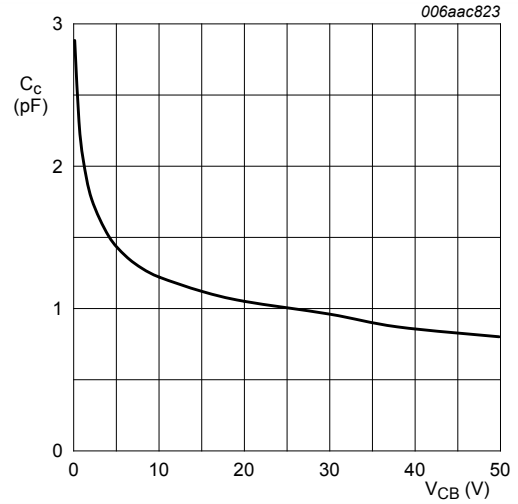


Fig. 7. NPN transistor: On-state input voltage as a function of collector current; typical values



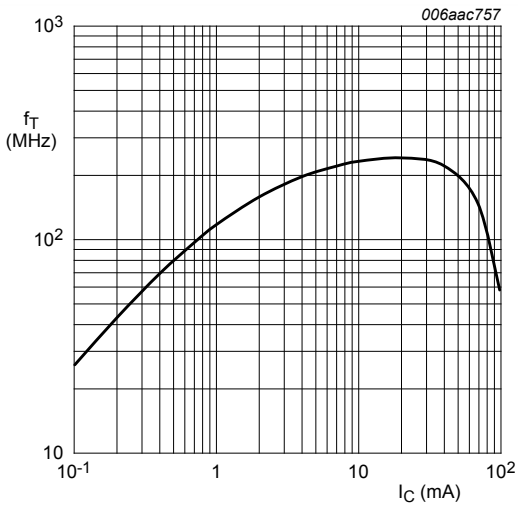
$V_{CE} = 5\text{ V}$
 (1) $T_{amb} = -40\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig. 8. NPN transistor: Off-state input voltage as a function of collector current; typical values



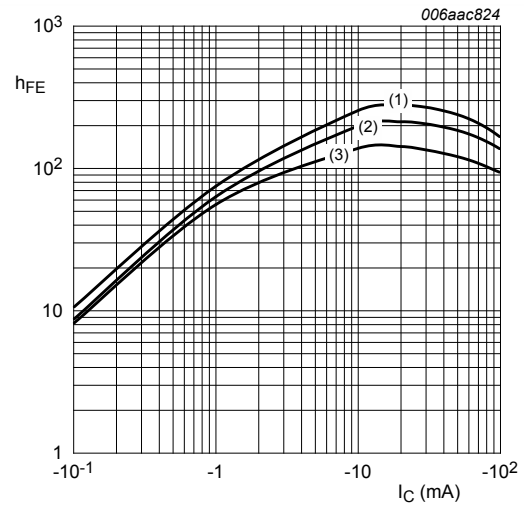
$f = 1\text{ MHz}; T_{amb} = 25\text{ °C}$

Fig. 9. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values



$V_{CE} = 5\text{ V}; T_{amb} = 25\text{ °C}$

Fig. 10. NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor



$V_{CE} = -5\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -40\text{ °C}$

Fig. 11. PNP transistor: DC current gain as a function of collector current; typical values

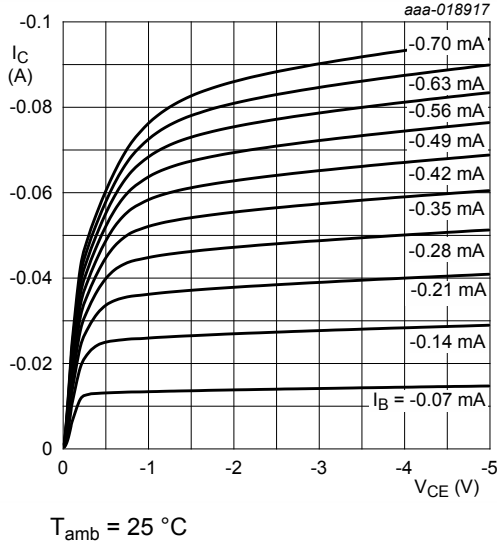


Fig. 12. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

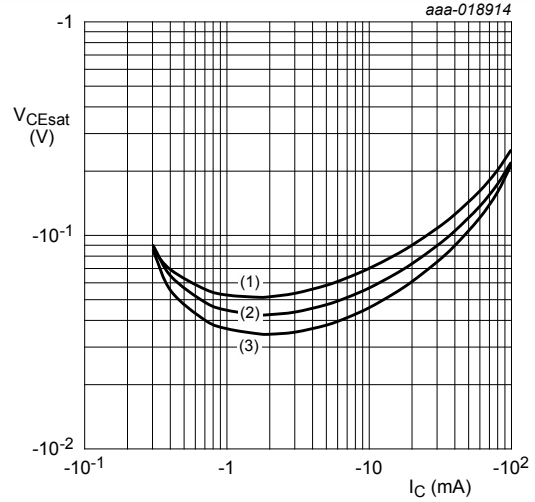


Fig. 13. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

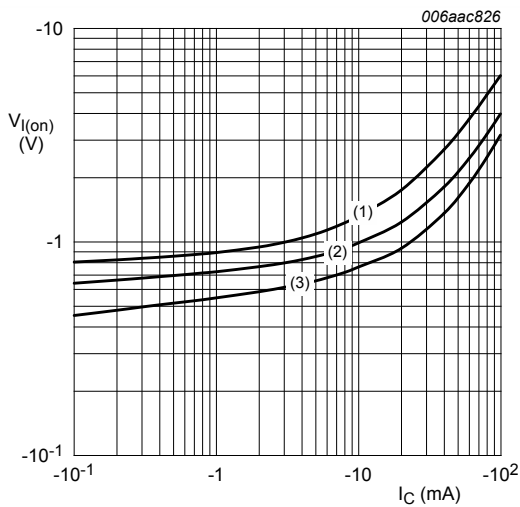


Fig. 14. PNP transistor: On-state input voltage as a function of collector current; typical values

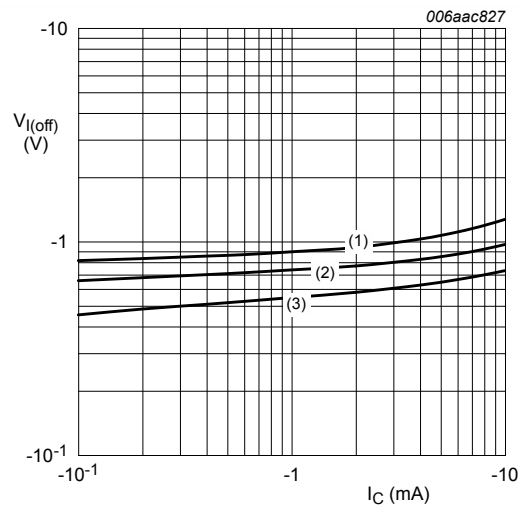
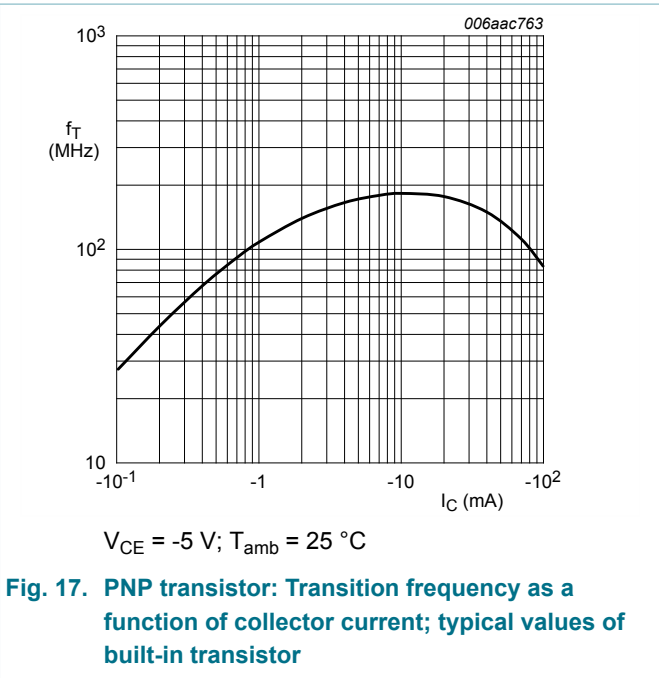
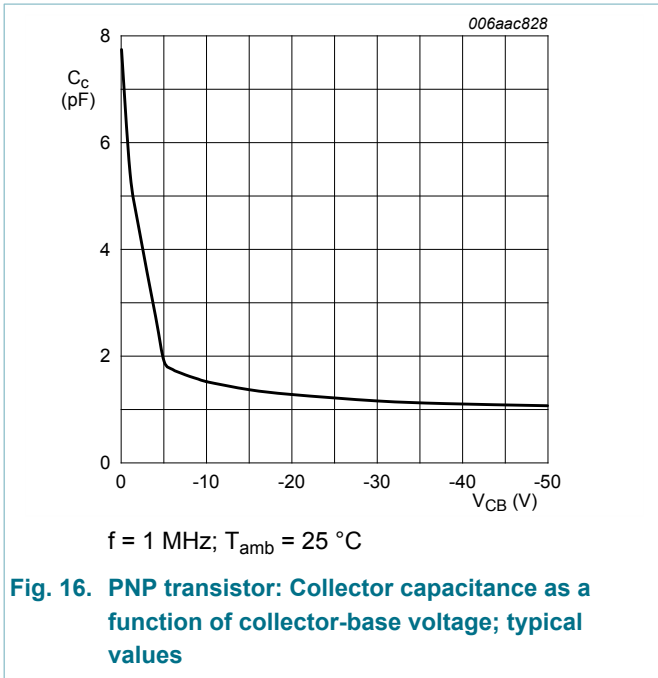


Fig. 15. PNP transistor: Off-state input voltage as a function of collector current; typical values



11. Test information

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

11.2 Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

NPN/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 47 kΩ

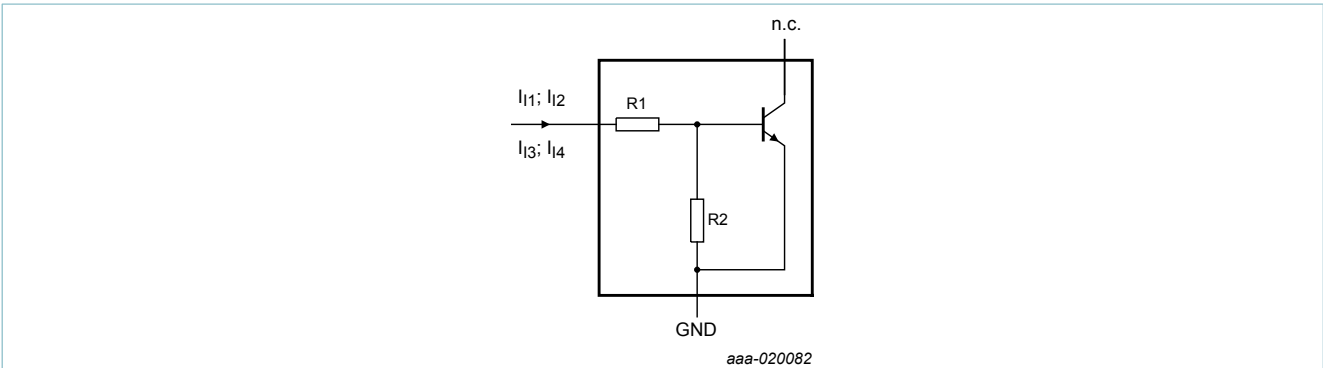


Fig. 18. NPN transistor: Resistor test circuit

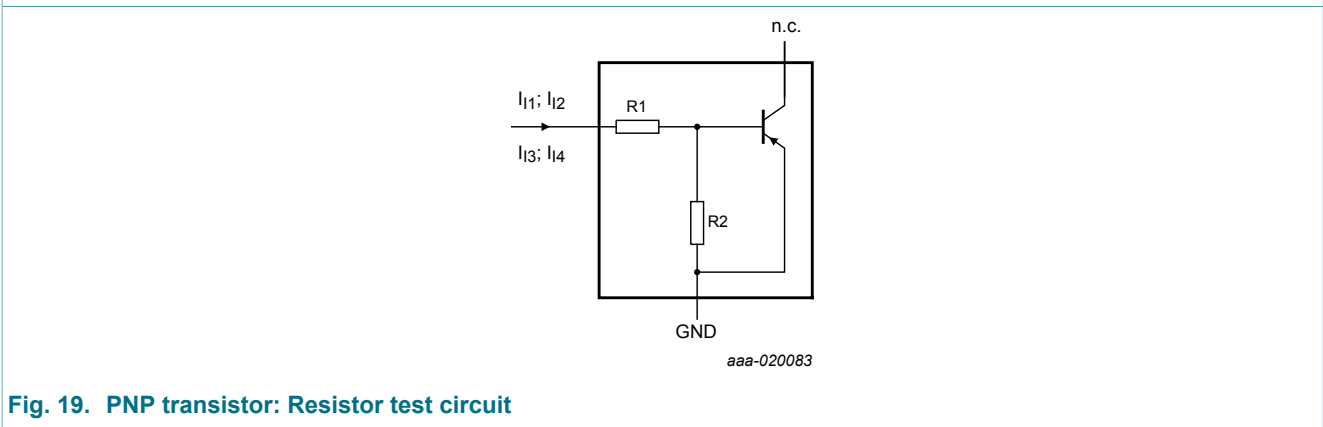


Fig. 19. PNP transistor: Resistor test circuit

11.3 Resistor test conditions

Table 8. Resistor test conditions

Per transistor; for the PNP transistor with negative polarity

R1 (kΩ)	R2 (kΩ)	Test conditions			
		I ₁₁	I ₁₂	I ₁₃	I ₁₄
4.7	47	90 μA	140 μA	-55 μA	-105 μA

12. Package outline

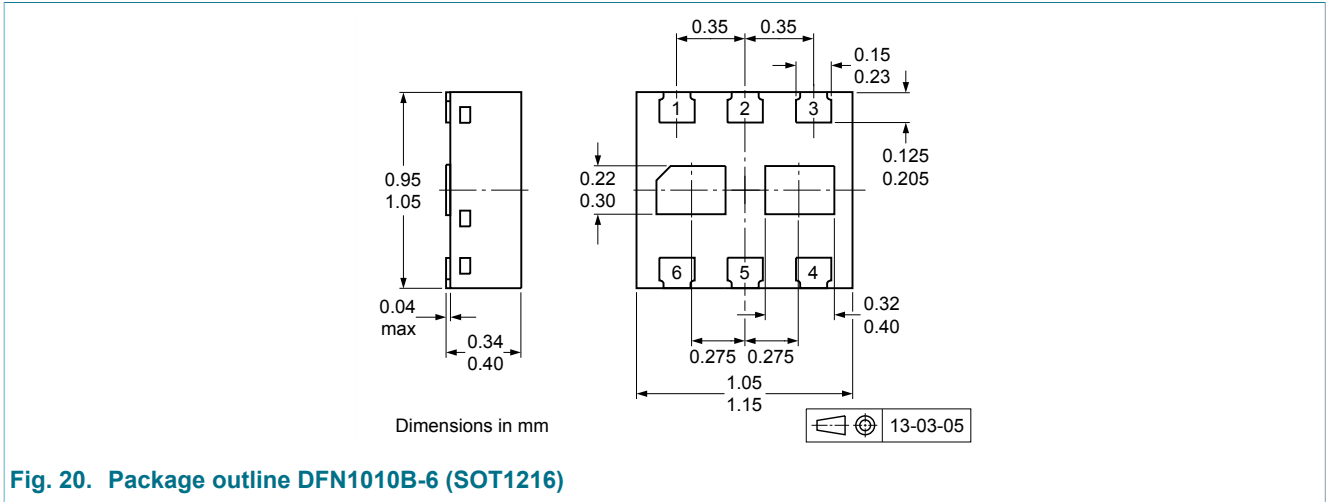


Fig. 20. Package outline DFN1010B-6 (SOT1216)

13. Soldering

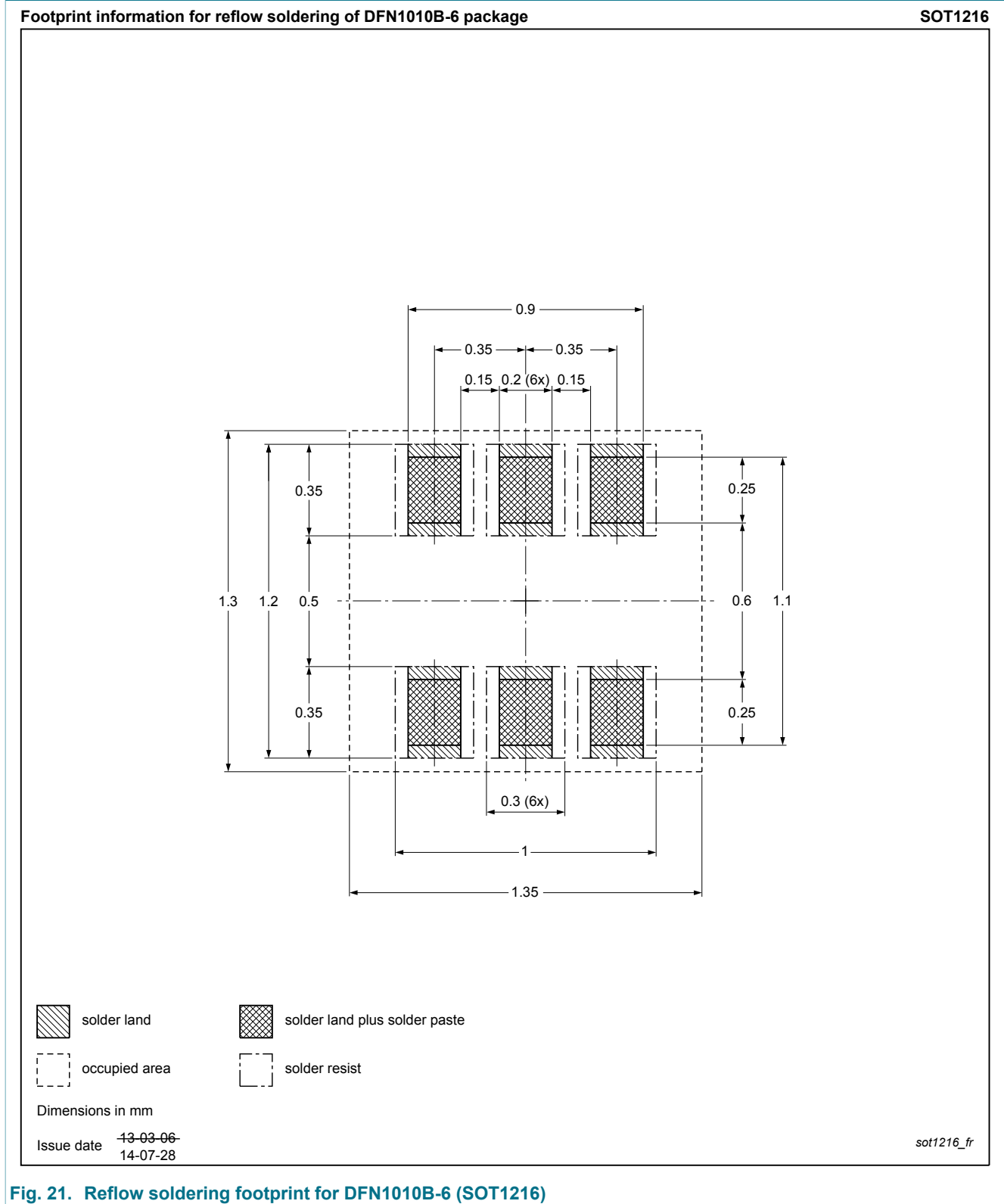


Fig. 21. Reflow soldering footprint for DFN1010B-6 (SOT1216)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PQMD13 v.1	20151104	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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16. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	3
8	Limiting values	4
9	Thermal characteristics	5
10	Characteristics	6
11	Test information	10
11.1	Quality information	10
11.2	Resistor calculation	10
11.3	Resistor test conditions	11
12	Package outline	12
13	Soldering	13
14	Revision history	14
15	Legal information	15
15.1	Data sheet status	15
15.2	Definitions	15
15.3	Disclaimers	15
15.4	Trademarks	16

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