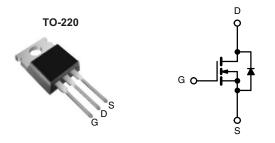


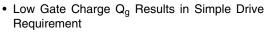
### **Power MOSFET**

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	50	500				
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.21				
Q <sub>g</sub> (Max.) (nC)	110	0				
Q <sub>gs</sub> (nC)	33	33				
Q <sub>gd</sub> (nC)	54	54				
Configuration	Sino	Single				



N-Channel MOSFET

#### **FEATURES**





 Improved Gate, Avalanche and Dynamic dV/dt Ruggedness

RoHS\*

- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low R<sub>DS(on)</sub>
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- · High Speed Power Switching
- · Hard Switched and High Frequency Circuits

ORDERING INFORMATION				
TO-220				
IRFB20N50KPbF				
SiHFB20N50K-E3				
IRFB20N50K				
SiHFB20N50K				

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_C = 25$ °C, unless otherw PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	500		
Gate-Source Voltage			V <sub>GS</sub>	± 30	V	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C		20	A	
		T <sub>C</sub> = 100 °C	I <sub>D</sub>	12		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	80		
Linear Derating Factor				2.2	W/°C	
Single Pulse Avalanche Energy <sup>b</sup>			E <sub>AS</sub>	330	mJ	
Repetitive Avalanche Current <sup>a</sup>			I <sub>AR</sub>	20	Α	
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>	28	mJ			
Maximum Power Dissipation $T_C = 25  ^{\circ}C$		P <sub>D</sub>	280	W		
Peak Diode Recovery dV/dt <sup>c</sup>			dV/dt	10	V/ns	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150		
Soldering Recommendations (Peak Temperature)	for	10 s		300 <sup>d</sup>	- °C	
Mounting Torque	6-32 or N	M3 screw		10	N	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Starting  $T_J = 25$  °C, L = 1.6 mH,  $R_g = 25 \Omega$ ,  $I_{AS} = 20$  A.
- c.  $I_{SD} \le 20$  A,  $dI/dt \le 350$  A/ $\mu$ s,  $V_{DD} \le V_{DS}$ ,  $T_J \le 150$  °C.
- d. 1.6 mm from case.

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply

# IRFB20N50K, SiHFB20N50K

## Vishay Siliconix



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	TYP.	MAX.	UNIT		
Maximum Junction-to-Ambient	R <sub>thJA</sub>	-	58			
Case-to-Sink, Flat, Greased Surface	R <sub>thCS</sub>	0.50	-	°C/W		
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	0.45			

PARAMETER	unless other	1	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
	STINIBUL	l les	T CONDITIONS	WIIN.	ITP.	WAX.	UNIT
Static	.,		0.1/ 1 050 4	500	l	l	· .,
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		500	-	-	V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	+	ce to 25 °C, I <sub>D</sub> = 1 mA	-	0.61	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	-	$= V_{GS}, I_D = 250 \mu A$	3.0	-	5.0	V
Gate-Source Leakage	I <sub>GSS</sub>	<b>.</b>	$V_{GS} = \pm 30 \text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>		V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V		-	50	μΑ
			$V, V_{GS} = 0 V, T_{J} = 125 °C$	-	-	250	'
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 12 A <sup>b</sup>	-	0.21	0.25	Ω
Forward Transconductance	9 <sub>fs</sub>	$V_{DS}$	= 50 V, I <sub>D</sub> = 12 A	11	-	-	S
Dynamic							
Input Capacitance	$C_{iss}$		$V_{GS} = 0 V$ ,	-	2870	-	
Output Capacitance	$C_{oss}$		$V_{DS} = 25 V$ ,	-	320	-	
Reverse Transfer Capacitance	$C_{rss}$	f = 1.0 MHz, see fig. 5		-	34	-	
Outrout Consolitance	C <sub>oss</sub>		V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	3480	-	pF
Output Capacitance		$V_{GS} = 0 V$	V <sub>DS</sub> = 400 V, f = 1.0 MHz	-	85	-	
Effective Output Capacitance	Coss eff.		V <sub>DS</sub> = 0 V to 400 V	-	160	-	
Total Gate Charge	Qg		V <sub>GS</sub> = 10 V	-	-	110	nC
Gate-Source Charge	$Q_{gs}$	V <sub>GS</sub> = 10 V		-	-	33	
Gate-Drain Charge	$Q_{gd}$	see fig. 6 and 13 <sup>b</sup>		-	-	54	
Turn-On Delay Time	t <sub>d(on)</sub>			-	22	-	
Rise Time	t <sub>r</sub>	$V_{DD}$	= 250 V, I <sub>D</sub> = 20 A	-	74	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$R_g = 7.5 \Omega$ , $V_{GS} = 10 V$ , see fig. $10^b$		-	45	-	ns -
Fall Time	t <sub>f</sub>			-	33	-	
Drain-Source Body Diode Characteristic	s						,
Continuous Source-Drain Diode Current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	Α
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			-	-	80	
Body Diode Voltage	$V_{SD}$	$T_J = 25  ^{\circ}\text{C},  I_S = 20  \text{A},  V_{GS} = 0  \text{V}^{\text{b}}$		-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 20 A, dI/dt = 100 A/μs <sup>b</sup>		-	520	780	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			-	5.3	8.0	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )					_D)

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. Pulse width  $\leq$  400  $\mu$ s; duty cycle  $\leq$  2 %.



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

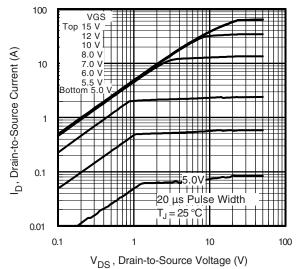


Fig. 1 - Typical Output Characteristics

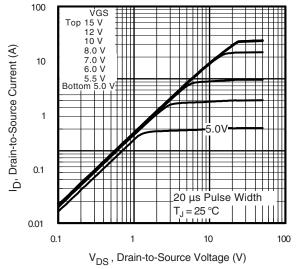


Fig. 2 - Typical Output Characteristics

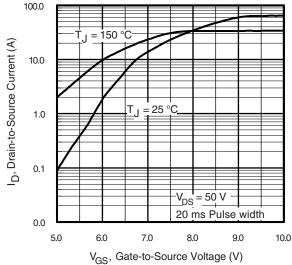


Fig. 3 - Typical Transfer Characteristics

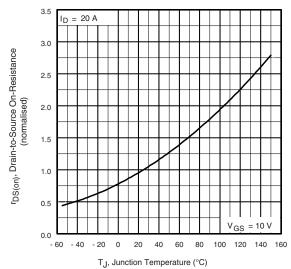


Fig. 4 - Normalized On-Resistance vs. Temperature

## IRFB20N50K, SiHFB20N50K

## Vishay Siliconix



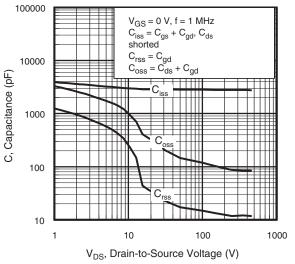


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

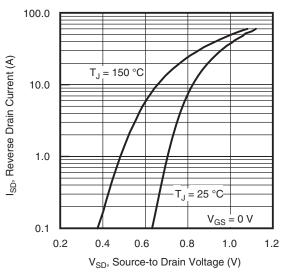


Fig. 7 - Typical Source-Drain Diode Forward Voltage

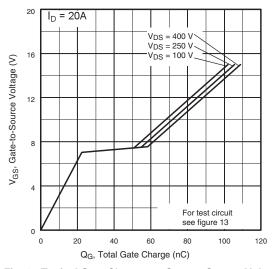


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

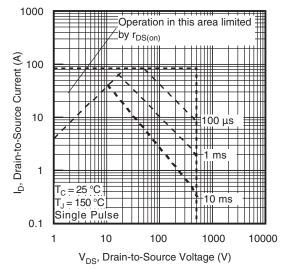


Fig. 8 - Maximum Safe Operating Area



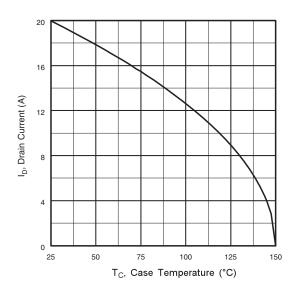


Fig. 9 - Maximum Drain Current vs. Case Temperature

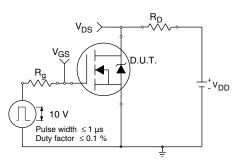


Fig. 10a - Switching Time Test Circuit

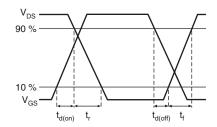


Fig. 10b - Switching Time Waveforms

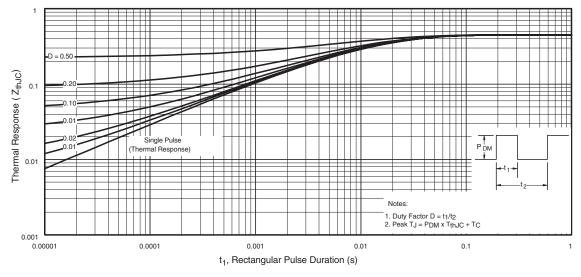


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

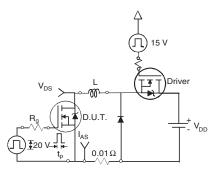


Fig. 12a - Unclamped Inductive Test Circuit

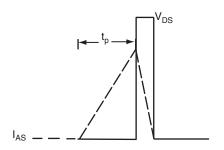


Fig. 12b - Unclamped Inductive Waveforms



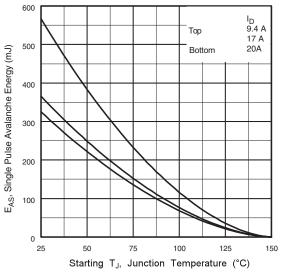


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

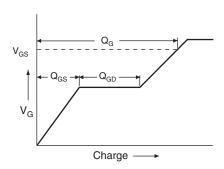


Fig. 13a - Basic Gate Charge Waveform

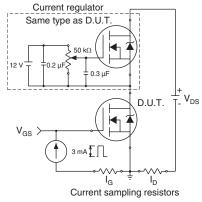
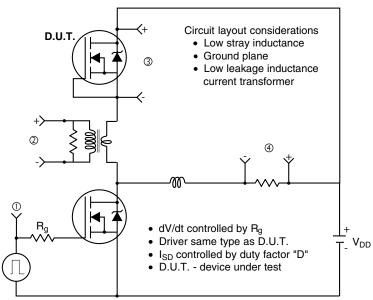
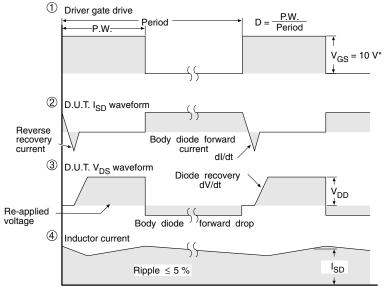


Fig. 13b - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit





\* V<sub>GS</sub> = 5 V for logic level devices

Fig. 14 - For N-Channel

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### TO-220-1



DIM	MILLIN	IETERS	INCHES			
DIM.	MIN.	MAX.	MIN.	MAX.		
Α	4.24	4.65	0.167	0.183		
b	0.69	1.02	0.027	0.040		
b(1)	1.14	1.78	0.045	0.070		
С	0.36	0.61	0.014	0.024		
D	14.33	15.85	0.564	0.624		
E	9.96	10.52	0.392	0.414		
е	2.41	2.67	0.095	0.105		
e(1)	4.88	5.28	0.192	0.208		
F	1.14	1.40	0.045	0.055		
H(1)	6.10	6.71	0.240	0.264		
J(1)	2.41	2.92	0.095	0.115		
L	13.36	14.40	0.526	0.567		
L(1)	3.33	4.04	0.131	0.159		
ØР	3.53	3.94	0.139	0.155		
Q	2.54	3.00	0.100	0.118		
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031						

#### Note

 $\bullet$   $M^{\star}=0.052$  inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



Revison: 14-Dec-15 1 Document Number: 66542



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Vishay

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

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Revision: 02-Oct-12 Document Number: 91000