EVALSPEAr600 - evaluation board for the SPEAr600

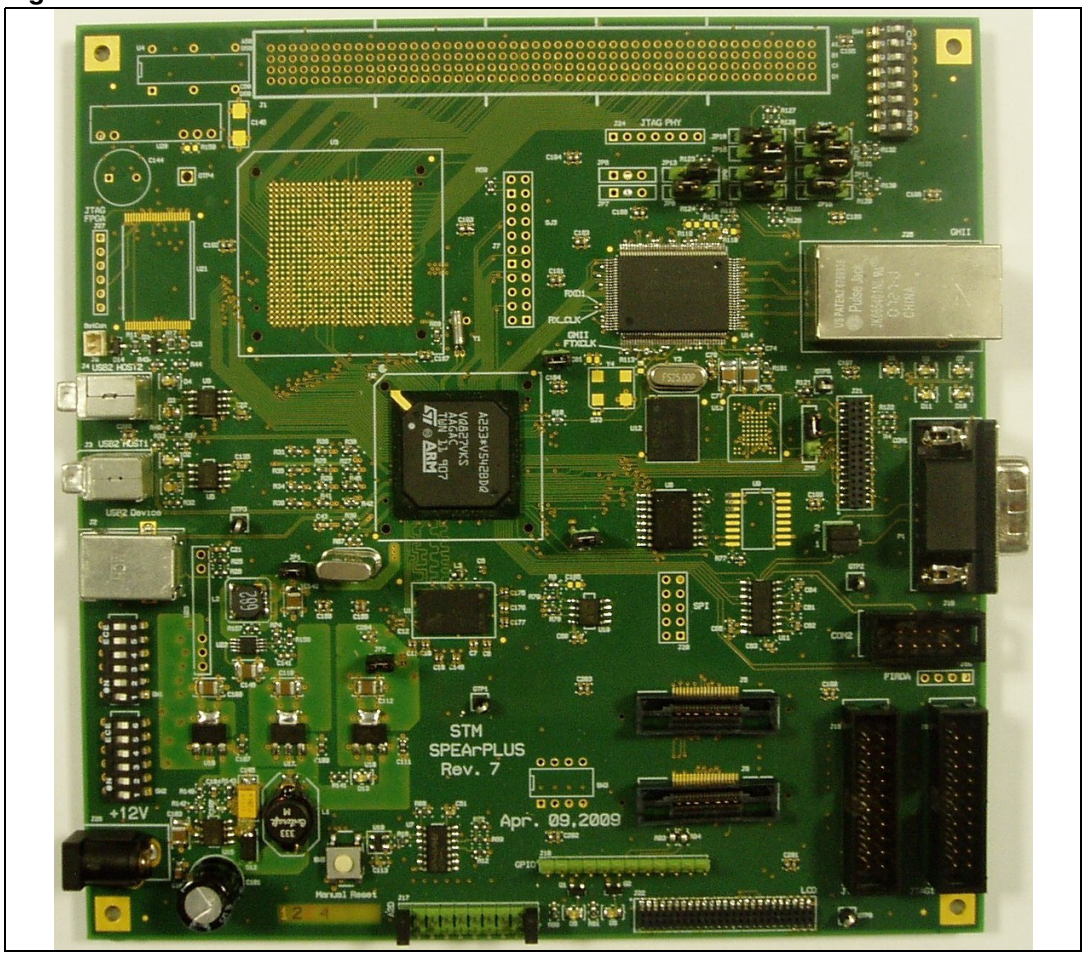
# 1 Description

The EVALSPEAr600 evaluation board for SPEAr600 is intended to be used for three main purposes:

- To allow you to quickly evaluate and debug software for the SPEAr600
- Act as a learning tool to rapidly get familiar with the SPEAr600 features
- Provide a reference design to be used as a starting point for the development of a final application board

It is equipped with all the interfaces offered by the SPEAr600. A special version of the board populated with an FPGA also exists for developing customer-specific IPs.

**Figure 1. EVALSPEAr600 evaluation board**



# List of tables

# Contents

# List of figures

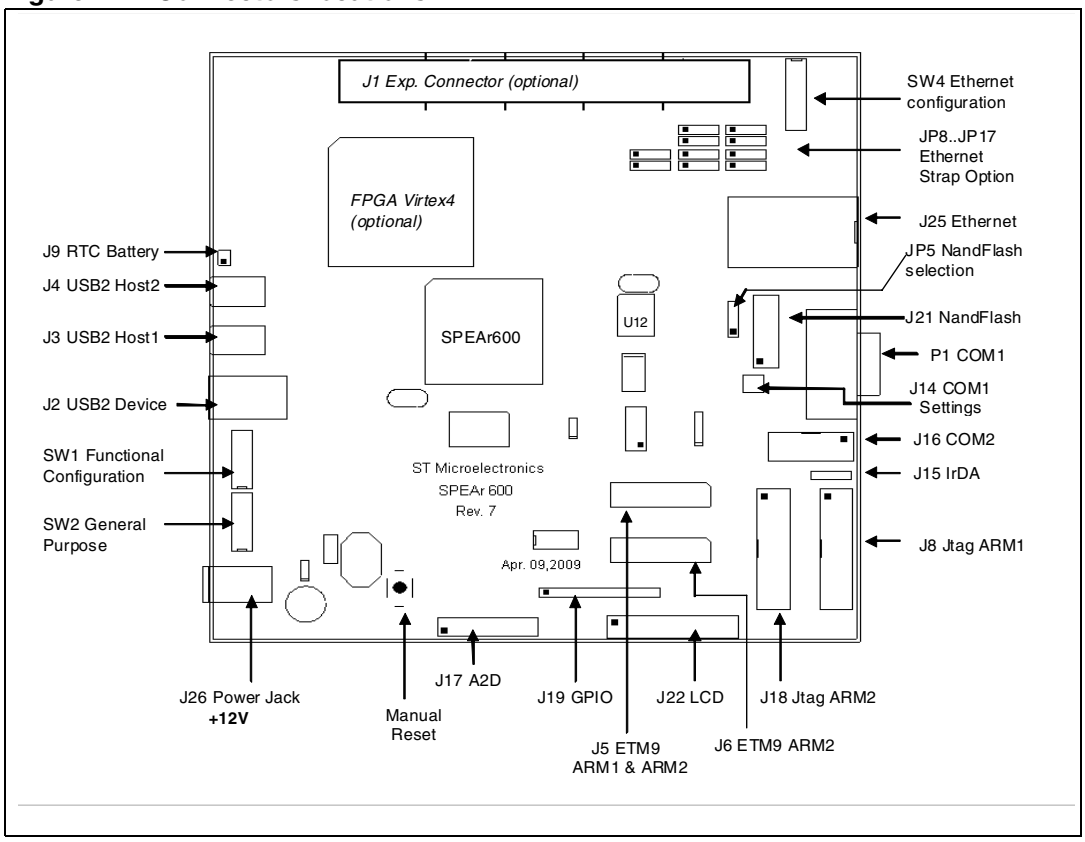
# 2 Contents of the kit

The EVALSPEAr600 evaluation board kit contains:

- SPEAr600 evaluation board
- AC/adapter (output voltage 12 V)
- 2 power cords (USA/Europe)
- User manual /Getting started documentation

# 3 Connectors locations

**Figure 2. Connectors locations**



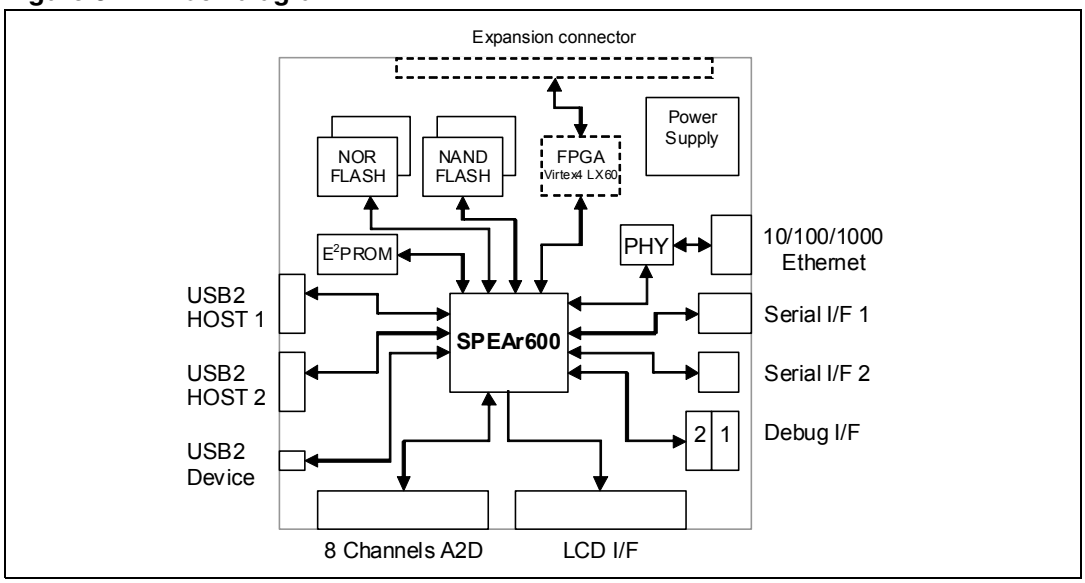
# 4 Features and block diagram

## 4.1 Features

- SPEAr600 embedded MPU
- Up to 2 Gb DDR2-333 MHz (std 128 MB)
- Up to 16 MB Serial Flash (std 8 MB)
- Up to 2 Gb NAND Flash (std 64 MB)
- 4 Kb Serial $I^2C$
- Two USB 2.0 full Host port channels
- One USB 2.0 HS Device
- 10/100/1000 Ethernet port
- Two Serial ports (up to 115 Kbaud)
- Debug ports (JTAG + ETM9)
- 8 ADC channels (10 bit, 1 Msamples)
- 10 GPIOs
- LCD I/F up to 24 *bits-per-pixel* (bpp)
- Additional 112 GPIOs when the external FPGA is used

## 4.2 Block diagram

**Figure 3. Block diagram**



# 5 Start up

## 5.1 Unpacking

**ELECTROSTATIC WARNING:**
**The EVALSPEAr600 Evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. General practices for working with static sensitive devices should be applied when working with this board.**

- **Wear an anti-static wristband** - Wearing a simple anti-static wristband can help to prevent ESD from damaging the SPEAr600 evaluation board.
- **Self-grounding** - Touch a grounded conducting material before handling and periodically while handling the SPEAr600 evaluation board.
- **Use an anti-static pad** - When configuring the SPEAr600 evaluation board, place it on an antic-static pad to reduce the possibility of ESD damage.
- **Only handle the board edges** - When handling the SPEAr600 evaluation board.

## 5.2 Connection

- Connect a serial cable (RS232 on P1) to a host PC (see *Figure 2*).
- On a host PC running Windows or Linux, start the Terminal program.
- Connect the AC Adapter to a power outlet.
- Power ON the board (plug the jack of the AC/Adapter on J26). A sequence of boot messages is displayed, followed by the Linux console prompt.

For more information, refer to the UM0844 available on www.st.com/spear.

## 5.3 Booting procedure

The SPEAr600 Board is able to boot a Linux kernel pre-installed in the serial NOR Flash.

At power on, the serial port outputs a brief header message with some uBoot information (uBoot version, SDK version, and some internal hardware information). At this point you can choose to:

1. **Stop the system directly in uBoot**: For this you have to press the spacebar on the host computer keyboard before the boot delay time expires (default is 3 seconds).
2. **Boot Linux**: The system logs you in automatically as super user and the Linux shell prompt is displayed on the screen.

# 6 Block descriptions

## 6.1 Dynamic memory subsystem

The Dynamic memory subsystem is composed of three major parts:

### 6.1.1 Memory chip

The memory used is a Micron DDR2 device and its part number is: MT47H64M16HR-3. Its size is 128 Mb x 8 (16 Mb x 8 x 8 banks).

### 6.1.2 Local power supply

It is based on a linear regulator with a low drop voltage (LD1117-1.8). It is generated locally in order to minimize the layout impact and also to avoid any noise injection between different subsystems.

### 6.1.3 Signal termination

A parallel termination is added on the clock lines to compensate, if needed, the layout dissymmetry. Two 100 Ohm resistors are used for each line in order to obtain an impedance of 50 ohms. All the other terminations are directly inside the pads (both on the SPEAr600 and the memory sides).

## 6.2 Static memory subsystem

### 6.2.1 Serial Flash memory

This block is based on an M25P64 ST Serial Flash memory device. The size of this chip is 8 MB and with both the two banks populated we have a total of 16 Mbytes.

A switch (SW2-2) is also provided to protect the Flash memory from any unwanted write access.

### 6.2.2 Serial $I^2C$ EEPROM

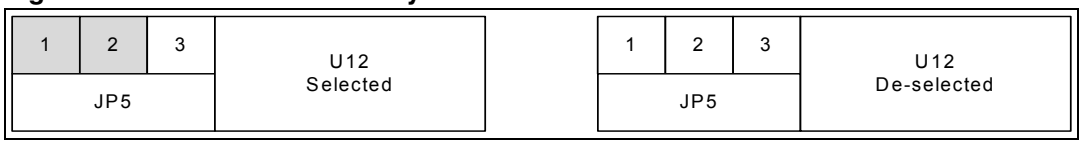
This block is based on the M24C04W ST Serial $I^2C$ EEPROM. The size of this chip is 4 Kb.

It also has a switch (SW2-3) to protect the EEPROM from unwanted write access.

### 6.2.3 NAND Flash memory

This block is based on ST NAND Flash NAND512W3A (U12) its size is 64 MB and its bus width x8. If required this chip can be replaced and another can be used. To do this, deselect the on-board Flash by removing jumper JP5 and connect an adapter board on J21.

**Figure 4. NAND Flash memory selection**



## 6.3 External FPGA subsystem (optional)

This block includes an FPGA (Xilinx Virtex4 LX60) plus its Flash memories and the JTAG interface for programming it. The FPGA is connected to the SPEAr600 through a proprietary bidirectional bus. This enables the development of IPs in the FPGA. In this way the FPGA can be used as an expansion of the system. When the FPGA is present, 112 additional I/O lines are provided on the expansion connector (J1). A dedicated clock input line for the FPGA is also connected to socket U4 where an external oscillator can be installed if a special clock frequency needs to be input to the FPGA. The oscillator output can be enabled or disabled using switch SW2-4.

The interface between the FPGA and the SPEAr600 can be synchronous or asynchronous. Its speed can also be set independently from the system speed. This means that, even with this interface is running at 60~80 MHz (which can be considered as a reasonable speed) all the other blocks of the SPEAr can still work at their maximum frequency.

## 6.4 Ethernet subsystem

This subsystem is based on the Ethernet GMII PHY DP83865 (U14) and a connector that also includes all the required magnetics. Several configuration jumpers are present and also several LEDs to display the line status/activity.

### 6.4.1 Configuration jumpers and switches

**Table 1. Switch 4 configuration**

| Bit | Description |
|---|---|
| 1 | PHY Address bit 1 (default value = 0) |
| 2 | PHY Address bit 2 (default value = 1) |
| 3 | PHY Address bit 3 (default value = 0) |
| 4 | PHY Address bit 4 (default value = 0) |
| 5 | **Multiple Node Enable**: This pin determines if the PHY advertises Master (multiple nodes) or Slave (single node) priority during 1000BASE-T Auto-Negotiation.<br>1: Selects multiple node priority (switch or hub).<br>0: Selects single node priority (NIC) (default value). |
| 6 | **Auto MDIX Enable**: This pin controls the automatic pair swap (Auto-MDIX) of the MDI/MDIX interface.<br>1: Enables pair swap mode.<br>0: Disables the Auto-MDIX and defaults the part into the mode preset by the MAN_MDIX_STRAP pin (default value) |
| 7 | **Clock To MAC Enable**:<br>1: CLK_TO_MAC clock output enabled (default value)<br>0: CLK_TO_MAC disabled |
| 8 | Not used. |

*Note: When DIP switch SW4-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.*

**Table 2. Default settings for other jumpers**

| Reference designator | | | | | | Description |
|---|---|---|---|---|---|---|
| On | | | Off | | | |
| JP8 | | | JP13 | | | PHY Address bit 0 |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP9 | | | JP14 | | | Auto-negotiation enable bit |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP10 | | | JP15 | | | Full Duplex select bit |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP11 | | | JP16 | | | Speed 1 select bit (See *Table 3* and *Table 4*) |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP12 | | | JP17 | | | Speed 0 select bit (See *Table 3* and *Table 4*) |
| 1 | 2 | 3 | 1 | 2 | 3 | |

## Speed select strap

These strap option pins have 2 different functions depending on whether Auto-Negotiation is enabled or not. Refer to *Table 2*.

**Table 3. Auto-negotiation disabled**

| Speed[1] | Speed[0] | Speed enabled |
|---|---|---|
| 1 | 1 | Reserved |
| 1 | 0 | 1000BASE-T |
| 0 | 1 | 100BASE-T |
| 0 | 0 | 10BASE-T |

**Table 4. Auto-negotiation enabled (advertised capability)**

| Speed[1] | Speed[0] | Speed enabled |
|---|---|---|
| 1 | 1 | 1000BASE-T, 10BASE-t |
| 1 | 0 | 1000BASE-T |
| 0 | 1 | 1000BASE-T, 100BASE-T |
| 0 | 0 | 1000BASE-T, 100BASE-T, 10BASE-T |

### 6.4.2 Ethernet LEDs

**Table 5. Ethernet LEDs**

| Reference | Description |
|---|---|
| D7 | **Duplex Status**: The LED is lit when the PHY is in Full Duplex operation after the link is established. |
| D8 | **1000M Speed and Good Link LED**: The LED output indicates that the PHY has established a good link at 1000 Mbps.<br>In 1000BASE-T mode, the link is established as a result of training, Auto-Negotiation completed, valid 1000BASE-T link established and reliable reception of signals transmitted from a remote PHY is received. |
| D9 | **100M Speed and Good Link LED**: The LED output indicates that the PHY has established a good link at 100 Mbps.<br>In 100BASE-T mode, the link is established as results of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LINK100_LED will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LINK100_LED will de-assert immediately following the de-assertion of the internal Signal Detect. |
| D10 | **10M Good Link LED**: In the standard 5-LED display mode, this LED output indicates that the PHY has established a good link at 10 Mbps. |
| D11 | **Activity LED**: The LED output indicates the occurrence of either idle error or packet transfer. |

## 6.5 USB 2.0 subsystem

### 6.5.1 Host ports

The board has two host ports that are fully compliant with the USB 2.0 specification (two controllers with one port each). This means that the two hosts can work in concurrent mode with the maximum possible bandwidth. Each host has also full control of the VBUS supplied by the TPS2030 power switch that also provides overcurrent protection in case of a short circuit in the USB cable. The ports are equipped with LEDs showing the power status of each port. (The green LED indicates the presence of VBUS and the red one the current limiter status).

### 6.5.2 Device port

A USB 2.0 device port is also provided.

## 6.6 Debug interface

Two debug interfaces are provided:

1. The JTAG interface can be used for "static" debug. This means that is possible to set a breakpoint and, when the system stops, to verify the contents of the memory and/or registers and modify them if needed.
2. The ETM9 interface can be used for "dynamic" debug. The ETM9 block embedded in the SPEAr600 chip, sends all the information about the AHB transactions during code

execution to the external trace box and the external box stores this information in a local buffer. This makes it possible, by stopping the CPU activity, to analyze the actual program flow. For example, if a particular data abort occurs, you can set a breakpoint on the data abort location and then, when the breakpoint is reached you can analyze the trace buffer. With this information, it becomes a simple task to identify the event that produced the problem.

The following configurations can be selected by setting SW1 bits [3:1].

**Table 6. Switch 1 configuration settings**

| Switch 1 | | | Description |
|---|---|---|---|
| 3 | 2 | 1 | |
| 0 | 0 | 0 | No debug features available. |
| 0 | 0 | 1 | The 1st ARM JTAG is connected to J8. |
| 0 | 1 | 0 | The 2nd ARM JTAG is connected to J8. |
| 0 | 1 | 1 | Both the ARM JTAGs are connected in a daisy chain on J8. |
| 1 | 0 | 0 | The 1st ARM JTAG is connected to J8 and the 2nd ARM JTAG is connected to J18. |
| 1 | 0 | 1 | ARM1 ETM bus available on J5 (4-bit demultiplexed mode). |
| 1 | 1 | 0 | ARM2 ETM bus available on J5 (4-bit demultiplexed mode). |
| 1 | 1 | 1 | ARM1 ETM bus available on J5 and ARM2 ETM bus available on J6 (Both in 4-bit demultiplexed mode). (1) |

1. To make the ARM2 ETM bus fully available on J6, the board has to be set up as follows:
   1. Populate resistors R48, R49, R50, R51 and R52 with 0 ohm resistors.
   2. Remove resistors R93 and R94.

Please refer to the documentation of the trace box manufacturers for more information on the ETM interface (www.lauterbach.com, www.agilent.com, www.yokogawa.com).

## 6.7 A/D interface

Eight analog input lines are provided on the J17 connector. The connector also allows you to determine the conversion range by setting the conversion limits on pins J17-19 (lower limit) and J17-1 (upper limit). The default setting is to have pins 1-2 and 19-20 shorted by jumpers.

In this way the conversion range is set to the maximum value (0 ~ 2.5V with a granularity of 2.44 mV) but by removing the two jumpers and providing different values on pin 1 and 19 it is possible to reduce the range and thus increase the granularity. For example if you input 1 V on J17-19 and 2 V on J17-1 the range will be 1 V ~ 2 V in steps of less than 1 mV.

In any case the following relationships between the pins should be ensured:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 V | ≤ | J17-19 | ≤ | J17 17 ~ 3 | ≤ | J17-1 | ≤ | 2.5 V |
| AGND | ≤ | Vref_n | ≤ | ADC_In channels | ≤ | Vref_p | ≤ | AVDD |

## 6.8 Real time clock (battery powered)

The real time clock (RTC) is powered with a 3V external battery (J9) in order to avoid losing its data even if the main power supply is switched off.

## 6.9 General power supply

From a 12 V ~ 25 V external AC/DC regulator power source, this block generates all the required voltages as follows:

- 1.0 V (Switching regulator) to supply the internal logic of the SPEAr600
- 1.2 V (Switching regulator) for the FPGA core
- 1.8 V (LDO regulator) for the DDR2 memory
- 2.5 V (LDO regulator) for the analog portion of SPEAr600 and for the Ethernet interface
- 3.3 V (LDO regulator) to supply the other interfaces
- 5 V (Switching regulator) to supply the USB Host VBUS

A power monitor is also present to provide the general reset of the board.

## 6.10 General-purpose I/Os

Ten general purpose I/Os are present on the board. Four of them are connected to a DIP switch to allow the user to select/deselect them. The other two, GPIO4 and GPIO5, drive two LEDs (one green and one yellow). All the GPIOs are also connected to the J19 connector which also has GND and 3.3V pins available.

*Note: For the connector pinout, refer to the schematic drawing available on www.st.com/spear.*

## 6.11 LEDs

Several LEDs are present on the board. They display the following status information:

- D13 (green) - Main power present
- D1 (green) - VBUS present on USB HOST port 1
- D3 (green) - VBUS present on USB HOST port 1
- D2 (red) - Abnormal current flowing on USB HOST 1 port
- D4 (red) - Abnormal current flowing on USB HOST 1 port
- D5 (yellow) - Switched on/off by GPIO4
- D6 (green) - Switched on/off by GPIO5
- D7-11 (yellow) - Ethernet line status LEDs. Refer to *Section 6.4: Ethernet subsystem*.

## 6.12 LCD Interface

The J22 connector (P/N SFM-125-02-S-D Samtec) is provided to allow the user to connect an LCD daughter board. It mates with TFM-125-02-S-D

The following signals are available on the J22 connector:

- All the LCD interface signals
- Two analog inputs (A/D)
- Three GPIO lines
- +12 V
- +5 V
- GND

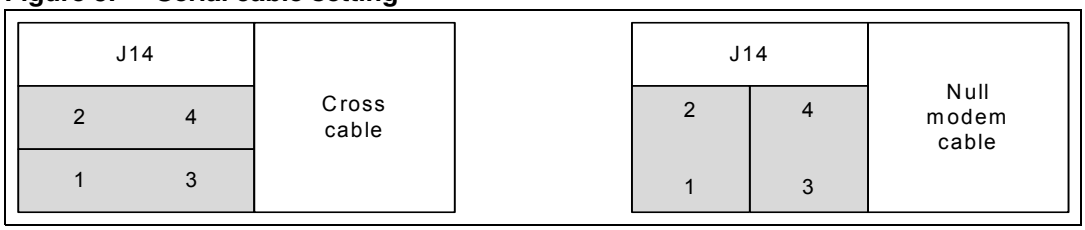
*Note: For the connector pinout, refer to the schematic drawing available on www.st.com/spear.*

# 7 Serial interface

Two serial interface ports are available. The 1st one, typically used as an OS monitor, is available on the P1 connector. It is possible to simulate a cross-cable by changing the position of the J14 jumpers as shown in *Figure 5*.

The 2nd serial interface port is available on J16. For the pinout of the connectors, refer to the schematic drawing available on www.st.com/spear.

**Figure 5. Serial cable setting**




# 8 Reset switch

A manual reset switch (SW5) is available on the top side of the board.

# 9 Switch settings

## 9.1 Switch 1 (SoC functional configuration)

**Table 7. Switch 1 (SoC functional configuration)**

| Bit | Description |
|---|---|
| 1 | Test0 – see Debug configuration below |
| 2 | Test1 – see Debug configuration below |
| 3 | Test2 – see Debug configuration below |
| 4 | Test3 – see Functional configuration below |
| 5 | Test4 – see Functional configuration below |
| 6 | Test5 – see Functional configuration below |

**Table 8. Switch 1 (debug configuration)**

| Test bit | | | Debug configuration |
|---|---|---|---|
| 3 | 2 | 1 | |
| 0 | 0 | 0 | Normal Mode (No debug enabled) |
| 0 | 0 | 1 | ARM1 JTAG connected to J8 |
| 0 | 1 | 0 | ARM2 JTAG connected to J8 |
| 0 | 1 | 1 | ARM1 and ARM2 JTAG connected in daisy chain to J8 |
| 1 | 0 | 0 | ARM1 JTAG connected to J8 and ARM2 JTAG connected to J18. |
| 1 | 0 | 1 | ARM1 ETM interface enabled. (J5) |
| 1 | 1 | 0 | ARM2 ETM interface enabled. (J5) |
| 1 | 1 | 1 | ARM1 and ARM2 ETM interface enabled. ARM1 on J5 and AMR2 on J6. |

**Table 9. Switch 1 (functional configuration)**

| Test bit | | | Functional configuration |
|---|---|---|---|
| 6 | 5 | 4 | |
| 0 | 0 | 0 | Default configuration |
| 0 | 0 | 1 | Nand Flash Interface disable (not usable on the board) |
| 0 | 1 | 0 | LCD interface disabled (not usable on the board) |
| 0 | 1 | 1 | GMAC interface disabled (not usable on the board) |
| 1 | 0 | 0 | FPGA interface enabled with clock and reset coming from FPGA to SPEAr |
| 1 | 0 | 1 | FPGA interface enabled with clock and reset coming from SPEAr to FPGA. |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

*Note: When DIP switch SW1-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.*

The default setting of SW1 is: Bit 1 = OFF all other bits (2:6) = ON

For more details on these settings, refer to the miscellaneous register description in the SPEAr600 user manual available at www.st.com/spear.

## 9.2 Switch 2 (general-purpose settings)

Default setting = all bits OFF.

**Table 10. Switch 2 (general-purpose settings)**

| Bit | Description |
|---|---|
| 1 | On - The FPGA done signal controls the main reset to avoid any unwanted activity during the FPGA bit stream download. |
| 2 | On - The Serial Flash memories are protected against unwanted write operations. |
| 3 | On - Inhibits write operations on the $I^2C$ EEPROM device. |
| 4 | This switch controls the external oscillator (U4) enable. |
| 5 | This switch enables the boot through USB interface. |
| 6 | This switch should be closed when the ETM interface is enabled and there is an LCD connected to prevent the LCD from disabling the LCD power by itself. |

*Note: When DIP switch SW2-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.*

# 10 Expansion connector (optional)

An expansion connector (J1) is provided to allow the user to add an additional board. (Part number TMMS-150-01-FM-Q-FS Samtec). It mates with SQT-150-01-FM-Q

The following signals are available on connector J1:

- FPGA_GPIO(0) ~ FPGA_GPIO(111)
- Three SoC GPIO lines
- Five Analog inputs (A/D)
- +12V (1A)
- +5V (1A)
- +3.3V (200 mA)
- +1.2V (200 mA)

*Note: For the connector pinout, refer to the schematic drawing available on www.st.com/spear.*

# 11 User manual and board schematic

The user manual and board schematic are available on www.st.com/spear.

# 12 Evaluation board bill of materials (BOM)

**Reference**: SPEAr600 BOM Board Rev7 (Sept. 11, 2009)

**Table 11. Capacitors**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 1 | 98 | C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C17, C18, C19, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C39, C40, C41, C42, C44, C45, C46, C47, C48, C49, C50, C52,C53, C54, C55, C56, C57,C66, C88, C89, C90, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C130,C131, C132, C133, C134, C136, C139, C143, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155,C156, C157, C158, C159, C160, C161, C162, C163, C164, C166, C167, C168, C175, C176, C177 | .1uF | KEMET Electronics | C0402C104K8PAC7867 |
| 2 | 13 | C16, C21, C71, C74, C78, C83, C84, C85, C86, C91, C92, C173, C174 | 10nF | KEMET Electronics | C0603C103K5RAC |
| 3 | 36 | C20, C22, C33, C34, C43, C51, C58, C60, C61, C62, C63, C64, C65, C67, C68, C72, C73, C75, C82, C87, C93, C94, C95, C96, C97, C98, C99, C100, C113, C135, C169, C170, C171, C172, C178, C179 | .1uF | VITRAMON | MR-VJ0603Y104KX |
| 4 | 4 | C37, C38, C79, C80 | 15pF | MURATA | GRM1885C1H150JZ01D |
| 5 | 2 | C35, C36, | 10pF | MURATA | GRM1885C1H100JA01D |

**Table 11. Capacitors (continued)**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 6 | 2 | C77, C76 | 22uF | KEMET Electronics | C1210C226Z8VAC |
| 7 | 1 | C101 | 220uF 50V +/- 20% YK | RUBYCON | |
| 8 | 1 | C102 | 1uF 25V | KEMET Electronics | C0805C105Z3VAC |
| 9 | 7 | C103, C108, C110, C112, C138, C140, C142 | 10uF | KEMET Electronics | C1210C106Z4VAC |
| 10 | 1 | C104 | 22nF | KEMET Electronics | C0603C223K5RAC |
| 11 | 2 | C145,C105 | 100uF 6.3V Tantalum | AVX | TPSC107K006R0150 |
| 12 | 1 | C106 | 220pF | KEMET Electronics | C0603C221J5GAC |
| 13 | 30 | C107, C109, C111, C137, C180, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205 | 1uF | KEMET Electronics | C0603C105K8PAC7867 |
| 14 | 1 | C141 | 1nF | KEMET Electronics | C0603C102K5RAC |
| 15 | 1 | C144 | 100uF 16V | | |

**Table 12. Diodes, connectors, inductors and transistors**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 16 | 4 | D1, D3, D6, D13 | LED Green | KINGBRIGHT | KP-2012SGC |
| 17 | 2 | D2, D4 | LED Red | KINGBRIGHT | KP-2012SRC-PRV |
| 18 | 6 | D5, D7, D8, D9, D10, D11 | LED Yellow | KINGBRIGHT | KP-2012SYC |
| 19 | 1 | D12 | STPS2L60 | STM | STPS2L60A |
| 20 | 1 | D14 | BAV70 | On Semiconductor | BAV70E6327 |
| 21 | 6 | GTP1, GTP2, GTP3, GTP4, GTP5, GTP6 | GTP | VERO Technologies | 20-2136 |
| 22 | 4 | JP1, JP2, JP3, JP4 | Jumper | TYCO Electronics AMP | 5-826629-0 |
| 23 | 13 | JP5, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13,J P14, JP15, JP16, JP17 | Jumper3 | TYCO Electronics AMP | 5-826629-0 |
| 24 | 1 | J1 | YTQ-150-01-F | SAMTEC | TMMS-150-01-FM-Q-FS |
| 25 | 1 | J2 | USB Device | SAMTEC | USB-B-S-F-B-TH |

**Table 12. Diodes, connectors, inductors and transistors**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 26 | 2 | J3, J4 | USB Host1-2 | MOLEX Electronics | 89485-8000 |
| 27 | 2 | J5, J6 | Mictor 5767061-1 | TYCO Electronics AMP | 5767061-1 |
| 28 | 1 | J7 | CON22A | TYCO Electronics AMP | 5-826925-0 |
| 29 | 2 | J18, J8 | CON20A | TYCO Electronics AMP | 2-1634688-0 |
| 30 | 1 | J9 | BatCon | MOLEX Electronics | 53047-0210 |
| 31 | 1 | J14 | Jumper2x2 | TYCO Electronics AMP | 5-826925-0 |
| 32 | 1 | J15 | CON4 | TYCO Electronics AMP | 5-826629-0 |
| 33 | 1 | J16 | CON10A | TYCO Electronics AMP | 1-1634688-0 |
| 34 | 1 | J17 | CON20A | TYCO Electronics AMP | 5-826925-0 |
| 35 | 1 | J19 | CON12 | TYCO Electronics AMP | 5-826629-0 |
| 36 | 1 | J20 | CON10A | TYCO Electronics AMP | 5-826925-0 |
| 37 | 1 | J21 | CON30A | SAMTEC | CLP-115-02-L-D |
| 38 | 1 | J22 | CON50A | SAMTEC | SFM-125-02-S-D |
| 39 | 1 | J25 | JK065401NL | PULSE | JK065401NL |
| 40 | 1 | J26 | TAP_2.5mm | CLIFF Electronics | FC681491 |
| 41 | 1 | J27 | CON6 | TYCO Electronics AMP | 5-826629-0 |
| 42 | 1 | L1 | 33uH | COILCRAFT | DO3316P-333MLB |
| 43 | 1 | L2 | 6.8uH | COILCRAFT | MSS6132-682MLC |
| 44 | 2 | L4, L3 | BLM18AG102 SN1D | MURATA | BLM18AG102SN1D |
| 45 | 1 | P1 | CON. DB9 Male | TYCO Electronics AMP | 5747840-2 |
| 46 | 2 | Q1, Q2 | BCR112 | INFINEON | BCR112E6327 |
| 47 | 1 | Q3 | BC848 | INFINEON | BC848CE6327 |

**Table 13. Resistors**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 48 | 6 | R37, R44, R71, R77, R78, R79 | 1K | TYCO Electronics UK | CRG0603F1K0 |
| 49 | 3 | R2, R3, R46 | 121K 1% | | |

Table 13. Resistors (continued)

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 50 | 19 | R4, R12, R16, R26, R68, R69, R112, R119, R120, R133, R134, R135, R136, R137, R138, R139, R143, R152, R155 | 4.7K | TYCO Electronics UK | CRG0603F4K7 |
| 51 | 8 | R5, R24, R105, R123, R125, R127, R129, R131 | 2.2K | TYCO Electronics UK | CRG0603F2K2 |
| 52 | 17 | R6, R7, R27, R28, R29, R30, R31, R34, R35, R36, R38, R39, R41, R42, R82, R101, R159 | 10 | TYCO Electronics UK | CRG0603F10R |
| 53 | 2 | R8, R15 | 470 | TYCO Electronics UK | CRG0603F470R |
| 54 | 9 | R9, R72, R93, R94, R95, R96, R97, R98, R99 | 0 | TYCO Electronics UK | CRG0603ZR |
| 55 | 2 | R104, R10 | 33 | TYCO Electronics UK | CRG0603F33R |
| 56 | 1 | R11 | 180K | TYCO Electronics UK | CRG0603F180K |
| 57 | 4 | R13, R14, R20, R21 | 100 | TYCO Electronics UK | MR-CRG0402F100R |
| 58 | 1 | R17 | 470K | TYCO Electronics UK | CRG0603F470K |
| 59 | 1 | R23 | 22 | TYCO Electronics UK | CRG0603F22R |
| 60 | 28 | R25, R53, R54, R55, R56, R57, R60, R61, R62, R63, R64, R65, R66, R70, R73, R74, R75, R83, R84, R85, R86, R87, R88, R89, R90, R91, R121, R122 | 10K | TYCO Electronics UK | CRG0603F10K |
| 61 | 3 | R32, R40, R141 | 270 | TYCO Electronics UK | CRG0603F270R |
| 62 | 4 | R33, R43, R80, R81 | 150 | TYCO Electronics UK | CRG0603F150R |
| 63 | 1 | R45, R156 | 1.5K 1% | TYCO Electronics UK | CRG0603F1K5 |
| 64 | 3 | R59, R151, R153 | 100 | TYCO Electronics UK | CRG0603F100R |
| 65 | 1 | R103 | 1M | TYCO Electronics UK | CRG0603F1M0 |
| 66 | 1 | R100 | 18 | TYCO Electronics UK | CRG0603F18R |
| 67 | 1 | R102 | 9.76K 1% | | |
| 68 | 8 | R106, R107, R108, R109, R111, R114, R115, R117 | 49,9 | | |
| 69 | 6 | R124, R126, R128, R130, R132, R154 | 330 | TYCO Electronics UK | CRG0603F330R |
| 70 | 1 | R140 | 3.9K | TYCO Electronics UK | CRG0603F3K9 |
| 71 | 1 | R142 | 1.2K | TYCO Electronics UK | CRG0603F1K2 |
| 72 | 1 | R150 | 22K | | |
| 73 | 1 | R157 | 100K | TYCO Electronics UK | CRG0603F100K |

**Table 14. Switches, semiconductors and crystals**

| Item | Qty | Reference | Part | Manufacturer | Manufacturer P/N |
|---|---|---|---|---|---|
| 74 | 2 | SW1, SW2 | SW DIP-6 | APEM Components | DS06 |
| 75 | 1 | SW3 | SW DIP-4 | APEM Components | DS04 |
| 76 | 1 | SW4 | SW DIP-8 | APEM Components | DS08 |
| 77 | 1 | SW5 | Push Button | OMRON Electronics | B3S-1000 |
| 78 | 1 | U1 | MT47H64M16HR-3 | MICRON | MT47H64M16HR-3E |
| 79 | 1 | U2 | SPEAr600 | STM | SPEAR-09-P022 |
| 80 | 1 | U3 | XXC4VLX60_11FFG668 | XILINX | XC4VLX60-11FFG668C |
| 81 | 1 | U4 | Socket Augat | WINSLOW Adaptics | W30514TT |
| 82 | 2 | U5, U6 | TPS2030 | TEXAS Instruments | TPS2030D |
| 83 | 1 | U7 | 74HC09 | STM | M74HC09RM13TR |
| 84 | 1 | U8 | M25P64 | STM | M25P64-VMF6P |
| 85 | 1 | U10 | M24C04 | STM | M24C04-WMN6P |
| 86 | 1 | U11 | ST3232CD | STM | ST3232CDR |
| 87 | 1 | U12 | NandFlashx8_FBGA63 | STM | Nand512W3A2CZA6 |
| 88 | 1 | U14 | GigPhy DP83865 | NATIONAL | DP83865DVH/NOPB |
| 89 | 1 | U15 | L5972D | STM | E-L5972D |
| 90 | 1 | U16 | LD1117S33TR | STM | LD1117S33TR |
| 91 | 1 | U17 | LD1117S25TR | STM | LD1117S25TR |
| 92 | 1 | U18 | LD1117S18TR | STM | LD1117S18TR |
| 93 | 1 | U19 | STM811 | STM | STM811SW16F |
| 94 | 1 | U20 | PL5S-12C | TDK-Lambda | PL5S-12-C |
| 95 | 1 | U21 | XCF32PVOG48C | XILINX | XCF32PVOG48C |
| 96 | 1 | U22 | L6926 | STM | L6926 |
| 97 | 1 | Y1 | 32kHz | FOX Electronics | NC26LF-327 |
| 98 | 1 | Y2 | 30MHz | C-MAC | XTAL003342 |
| 99 | 1 | Y3 | 25MHz | FOX Electronics | FOXS/250F-20 |
| 100 | 15 | | Jumper | WINSLOW Adaptics | W8010T50 |
| 101 | 4 | | Rubber feet | PDE | PD2115BL |

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# Revision history

**Table 15. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 25-Sep-2009 | 1 | Initial release. |
| 25-Feb-2010 | 2 | Corrected the reference on page 8 from figure 4 to figure2 .<br>Updated *Figure 5*.<br>Corrected the revision number of the SPEAr600 BOM board on page 18 from Rev1 to Rev7.<br>Changed the title of the document .<br>Minor text changes. |
| 28-May-2010 | 3 | *Table 2: Default settings for other jumpers*: added the last row.<br>*Table 7: Switch 1 (SoC functional configuration)*, *Table 8: Switch 1 (debug configuration)* and *Table 9: Switch 1 (functional configuration)* updated.<br>Corrected a mistake in the *Chapter 8: Reset switch*.<br>Updated *Figure 4* and *Figure 5* |

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