Precision 8-Ch / Dual 4-Ch Low Voltage Analog Multiplexers

DESCRIPTION

The DG408L, DG409L are low voltage pin-for-pin compatible companion devices to the industry standard DG408, DG409 with improved performance.

Using BiCMOS wafer fabrication technology allows the DG408L, DG409L to operate on single and dual supplies. Single supply voltage ranges from 3 V to 12 V while dual supply operation is recommended with ± 3 V to ± 6 V.

The DG408L is an 8 channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3 bit binary address (A_0, A_1, A_2). The DG409L is a dual 4 channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2 bit binary address (A_0, A_1). Break-before-make switching action to protect against momentary crosstalk between adjacent channels.

The DG408L, DG409L provides lower on-resistance, faster switching time, lower leakage, less power consumption, and higher off-isolation than the DG408, DG409.

FEATURES

- Pin-for-pin compatibility with DG408, DG409
- 2.7 V to 12 V single supply or ± 3 V to ± 6 V dual supply operation
- Lower on-resistance: $R_{DS(on)}$ - 17 Ω typ.
- Fast switching: t_{ON} - 38 ns, t_{OFF} - 18 ns
- Break-before-make guaranteed
- Low leakage: $I_{S(OFF)}$ - 0.2 nA max.
- Low charge injection: 1 pC
- TTL, CMOS, LV logic (3 V) compatible
- 82 dB off-isolation at 1 MHz
- 2000 V ESD protection (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available

RoHS* Available

HALOGEN FREE Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

BENEFITS

- High accuracy
- Single and dual power rail capacity
- Wide operating voltage range
- Simple logic interface

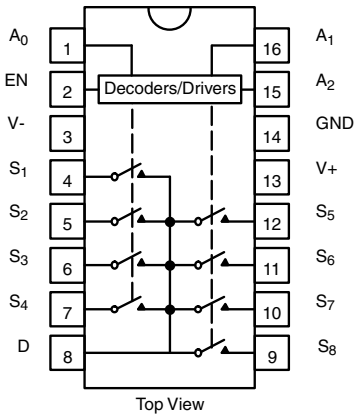
APPLICATIONS

- Data acquisition systems
- Battery operated equipment
- Portable test equipment
- Sample and hold circuits
- Communication systems
- SDSL, DSLAM
- Audio and video signal routing

FUNCTIONAL BLOCK DIAGRAMS AND PIN CONFIGURATIONS

DG408L

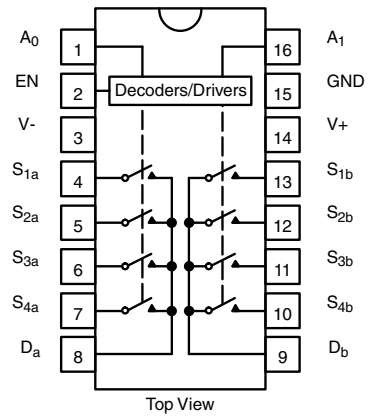
Dual-In- Line, SOIC, and TSSOP



Top View

DG409L

Dual-In- Line, SOIC, and TSSOP



Top View

TRUTH TABLE (DG408L)				
A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE (DG409L)			
A_1	A_0	EN	ON SWITCH
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic “0” = $V_{AL} \leq 0.8$ V
Logic “1” = $V_{AH} \geq 2.4$ V
X = do not care

Note

- For low and high voltage levels for V_{AX} and V_{EN} consult “Digital Control” parameters for specific V+ operation.

ORDERING INFORMATION (DG408L)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	16-pin SOIC	DG408LDY DG408LDY-E3 DG408LDY-T1 DG408LDY-T1-E3
	16-pin TSSOP	DG408LDQ DG408LDQ-E3 DG408LDQ-T1 DG408LDQ-T1-E3

ORDERING INFORMATION (DG409L)		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	16-pin SOIC	DG409LDY DG409LDY-E3 DG409LDY-T1 DG409LDY-T1-E3
	16-pin TSSOP	DG409LDQ DG409LDQ-E3 DG409LDQ-T1 DG409LDQ-T1-E3

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltage Referenced V+ to V- [e]		14	V
GND		7	
Digital Inputs [a], V_S, V_D		(V-) - 0.3 to (V) + 0.3	
Current (any terminal)		30	mA
Peak Current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(A suffix)	-65 to +150	°C
	(D suffix)	-65 to +125	
Power Dissipation (package) [b]	16-pin plastic TSSOP [c]	650	mW
	16-pin narrow SOIC [c]	600	
	16-pin CerDIP [d]	900	
	LCC-20 [e]	750	

Notes

a. Signals on S_X, D_X, A_X, or EN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 7.6 mW/°C above 75 °C.
d. Derate 12 mW/°C above 75 °C
e. Derate 10 mW/°C above 75 °C

SPECIFICATIONS (Single Supply 12 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 12 V, ± 10 %, V- = 0 V V_{EN} = 0.8 V or 2.4 V [f]	**TEMP.** [b]	**TYP.** [d]	**A SUFFIX** -55 °C to +125 °C		**D SUFFIX** -40 °C to +85 °C		**UNIT**
					MIN. [c]	**MAX.** [c]	**MIN.** [c]	**MAX.** [c]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	12	0	12	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = 10.8 V, V_D = 2 V or 9 V, I_S = 10 mA, sequence each switch on	Room	17	-	29	-	29	Ω
			Full	-	-	38	-	35	
$R_{DS(on)}$ Matching Between Channels [g]	ΔR_{DS}	V_D = 10.8 V, V_D = 2 V or 9 V, I_S = 10 mA,	Room	1	-	3	-	3	
On-Resistance Flatness [i]	$R_{FLAT(on)}$		Room	3	-	7		7	
Switch Off Leakage Current [a]	$I_{S(off)}$	V_{EN} = 0 V, V_D = 11 V or 1 V, V_S = 1 V or 11 V	Room	-	-1	1	-1	1	nA
			Full	-	-15	15	-10	10	
	$I_{D(off)}$		Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Channel On Leakage Current [a]	$I_{D(on)}$	V_S = V_D = 1 V or 11 V	Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Digital Control									
Logic High Input Voltage	V_{INH}		Full	-	2.4	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.8	-	0.8	
Input Current	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.8 V	Full	-	-1.5	1.5	-1	1	µA
Dynamic Characteristics									
Transition Time	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, (DG408L) V_{S1b} = 8 V, V_{S4b} = 0 V, (DG409L) see figure 2	Room	30	-	60	-	60	ns
			Full	-	-	68	-	65	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 5 V, see figure 4	Room	11	1	-	1	-	
			Full	-	-	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 5 V (DG408L) V_{AX} = 0 V, V_{S1b} = 5 V (DG409L) see figure 3	Room	38	-	55	-	55	
			Full	-	-	60	-	60	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	18	-	25	-	25	
			Full	-	-	30	-	30	
Charge Injection [e]	Q	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	1	-	5	-	5	pC
Off Isolation [e, h]	OIRR	f = 100 kHz, R_L = 1 kΩ	Room	-70	-	-	-	-	dB
Crosstalk [e]	X_{TALK}		Room	-82	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	7	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz, V_D = 2.4 V, V_{EN} = 0 V	Room	20	-	-	-	-	
Drain On Capacitance [e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V (DG409L only)	Room	31	-	-	-	-	
Power Supplies									
Power Supply Range	V+			-	3	12	3	12	V
Power Supply Current	I+	V_{EN} = V_A = 0 V or 5 V	Room	0.2	-	0.7	-	0.7	µA

Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)}$ = $R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on Channel 4 do to proximity to the drain pin.
i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

SPECIFICATIONS (Dual Supply V+ = 5 V, V - = -5 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, ± 10 %, V- = -5 V V_{EN} = 0.6 V or 2.4 V [f]	**TEMP.** [b]	**TYP.** [d]	**A SUFFIX** -55 °C to +125 °C		**D SUFFIX** -40 °C to +85 °C		**UNIT**
					MIN. [c]	**MAX.** [c]	**MIN.** [c]	**MAX.** [c]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	-5	5	-5	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 3.5 V, I_S = 10 mA, sequence each switch on	Room	20	-	40	-	40	Ω
			Full	-	-	50	-	50	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 5.5, V- = 5.5 V V_{EN} = 0 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room	-	-1	1	-1	1	nA
			Full	-	-15	15	-10	10	
	$I_{D(off)}$		Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V, V_{EN} = 2.4 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Digital Control									
Logic High Input Voltage	V_{INH}		Full	-	2.4	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.6	-	0.6	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.6 V	Full	-	-1.5	1.5	-1	1	µA
Dynamic Characteristics									
Transition Time [e]	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = 0 V, (DG408L) V_{S1b} = 3.5 V, V_{S4b} = 0 V, (DG409L) see figure 2	Room	30	-	60	-	60	ns
			Full	-	-	78	-	65	
Break-Before-Make Time [e]	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 3.5 V, see figure 4	Room	8	1	-	1	-	
			Full	-	-	-	-	-	
Enable Turn-On Time [e]	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG408L) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG409L) see figure 3	Room	25	-	55	-	55	
			Full	-	-	68	-	60	
Enable Turn-Off Time [e]	$t_{OFF(EN)}$		Room	20	-	40	-	40	
			Full	-	-	50	-	45	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	6	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	15	-	-	-	-	
Drain On Capacitance [e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V	Room	29	-	-	-	-	

Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.
i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

SPECIFICATIONS (Single Supply 5 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 5 V, ± 10 %, V- = 0 V V_{EN} = 0.6 V or 2.4 V [f]	**TEMP.** [b]	**TYP.** [d]	**A SUFFIX** -55 °C to +125 °C		**D SUFFIX** -40 °C to +85 °C		**UNIT**
					MIN. [c]	**MAX.** [c]	**MIN.** [c]	**MAX.** [c]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	5	0	5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 4.5 V, V_D or V_S = 1 V or 3.5 V, I_S = 5 mA	Room	35	-	49	-	40	Ω
			Full	-	-	62	-	62	
$R_{DS(on)}$ Matching Between Channels [g]	ΔR_{DS}	V+ = 4.5 V, V_D = 1 V or 3.5 V, I_S = 5 mA	Room	1.5	-	3	-	3	
On-Resistance Flatness [i]	$R_{FLAT(on)}$		Room	-	-	4	-	4	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 5.5 V, V_S = 1 V or 4 V, V_D = 4 V or 1 V	Room	-	-1	1	-1	1	nA
			Full	-	-15	15	-10	10	
	$I_{D(off)}$		Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 5.5 V, V_D = V_S = 1 V or 4 V, sequence each switch on	Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Digital Control									
Logic High Input Voltage	V_{INH}	V+ = 5 V	Full	-	2.4	-	2.4	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.6	-	0.6	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.6 V	Full	-	-1.5	1.5	-1	1	µA
Dynamic Characteristics									
Transition Time [e]	t_{TRANS}	V_{S1} = 3.5 V, V_{S8} = 0 V, (DG408L) V_{S1b} = 3.5 V, V_{S4b} = 0 V, (DG409L) see figure 2	Room	44	-	125	-	125	ns
			Full	-	-	138	-	135	
Break-Before-Make Time [e]	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 3.5 V, see figure 4	Room	17	1	-	1	-	
			Full	-	-	-	-	-	
Enable Turn-On Time [e]	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 3.5 V (DG408L) V_{AX} = 0 V, V_{S1b} = 3.5 V (DG409L) see figure 3	Room	43	-	60	-	60	
			Full	-	-	70	-	65	
Enable Turn-Off Time [e]	$t_{OFF(EN)}$		Room	26	-	45	-	45	
			Full	-	-	60	-	50	
Charge Injection [e]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Room	-1	-	-	-	-	pC
Off Isolation [e, h]	OIRR	f = 100 kHz, R_L = 1 kΩ	Room	-70	-	-	-	-	dB
Crosstalk [e]	X_{TALK}		Room	-80	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	8	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	21	-	-	-	-	
Drain On Capacitance [e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2.4 V	Room	32	-	-	-	-	

Notes

a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)}$ = $R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.
i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

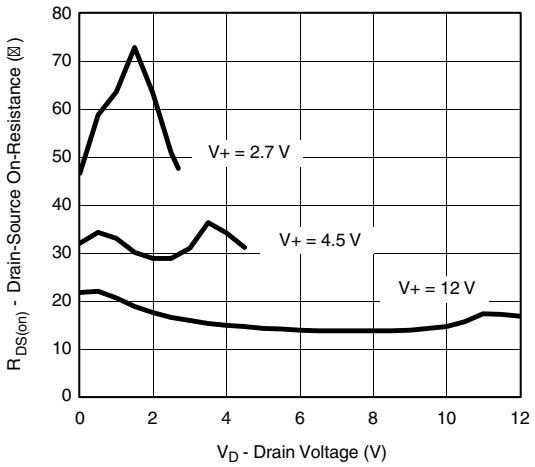
SPECIFICATIONS (Single Supply 3 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 3 V, ± 10 %, V- = 0 V V_{EN} = 0.4 V or 2 V [f]	**TEMP.** [b]	**TYP.** [d]	**A SUFFIX** -55 °C to +125 °C		**D SUFFIX** -40 °C to +85 °C		**UNIT**
					MIN. [c]	**MAX.** [c]	**MIN.** [c]	**MAX.** [c]	
Analog Switch									
Analog Signal Range [e]	V_{ANALOG}		Full	-	0	3	0	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V+ = 2.7 V, V_D = 0.5 or 2.2 V, I_S = 5 mA	Room	60	-	80	-	80	Ω
			Full	-	-	105	-	100	
Switch Off Leakage Current [a]	$I_{S(off)}$	V+ = 3.3 V, V_S = 2 or 1 V, V_D = 1 or 2 V	Room	-	-1	1	-1	1	nA
			Full	-	-15	15	-10	10	
	$I_{D(off)}$		Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Channel On Leakage Current [a]	$I_{D(on)}$	V+ = 3.3 V, V_D = V_S = 1 V or 2 V, sequence each switch on	Room	-	-1	1	-1	1	
			Full	-	-15	15	-10	10	
Digital Control									
Logic High Input Voltage	V_{INH}		Full	-	2	-	2	-	V
Logic Low Input Voltage	V_{INL}		Full	-	-	0.4	-	0.4	
Input Current [a]	I_{IN}	V_{AX} = V_{EN} = 2.4 V or 0.4 V	Full	-	-1.5	1.5	-1	1	µA
Dynamic Characteristics									
Transition Time	t_{TRANS}	V_{S1} = 1.5 V, V_{S8} = 0 V, (DG408L) V_{S1b} = 1.5 V, V_{S4b} = 0 V, (DG409L) see figure 2	Room	75	-	150	-	150	ns
			Full	-	-	175	-	175	
Break-Before-Make Time	t_{OPEN}	$V_{S(all)}$ = V_{DA} = 1.5 V, see figure 4	Room	32	1	-	1	-	
			Full	-	-	-	-	-	
Enable Turn-On Time	$t_{ON(EN)}$	V_{AX} = 0 V, V_{S1} = 1.5 V (DG408L) V_{AX} = 0 V, V_{S1b} = 1.5 V (DG409L) see figure 3	Room	70	-	95	-	95	
			Full	-	-	115	-	105	
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	55	-	100	-	100	
			Full	-	-	115	-	105	
Charge Injection [e]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 1.5 V	Room	0.4	-	-	-	-	pC
Off Isolation [e, h]	OIRR	f = 100 kHz, R_L = 50 Ω	Room	-70	-	-	-	-	dB
Crosstalk [e]	X_{TALK}		Room	-79	-	-	-	-	
Source Off Capacitance [e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, V_{EN} = 0 V	Room	8	-	-	-	-	pF
Drain Off Capacitance [e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 0 V	Room	19	-	-	-	-	
Drain On Capacitance [e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, V_{EN} = 2 V (DG409L only)	Room	33	-	-	-	-	

Notes

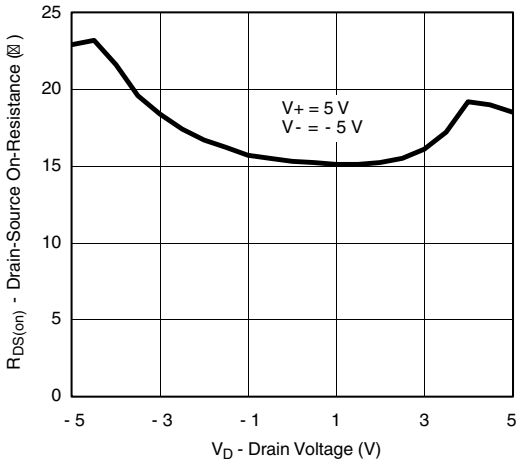
a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25 °C, full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta R_{DS(on)}$ = $R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on channel 4 do to proximity to the drain pin.
i. $R_{DS(on)}$ flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

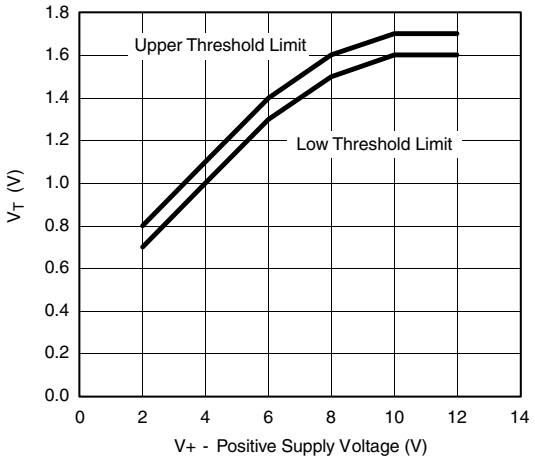
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



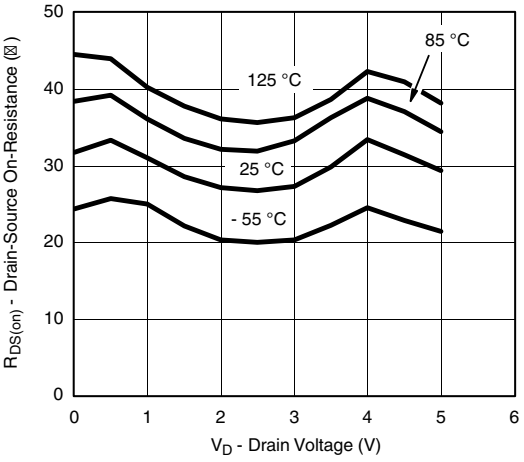
$R_{DS(on)}$ vs. V_D and Power Supply



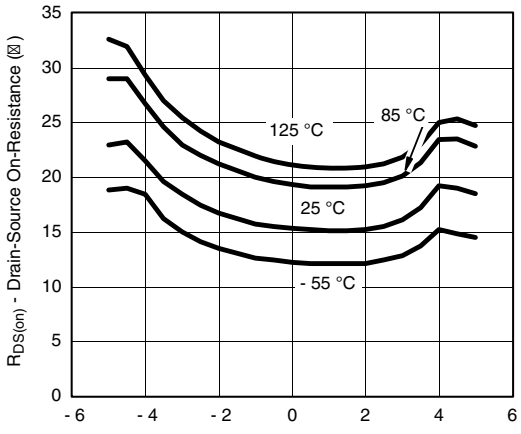
$R_{DS(on)}$ vs. V_D and Power Supply



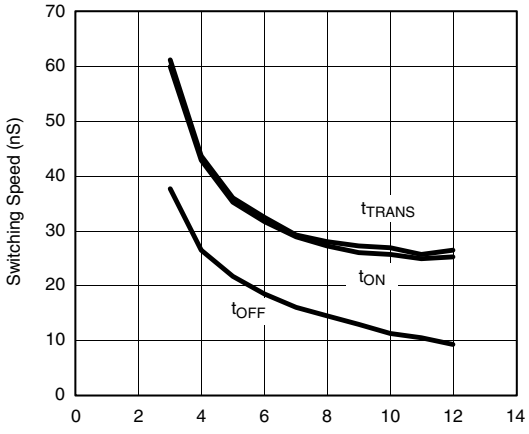
Input Threshold vs. V+ Supply Voltage



$R_{DS(on)}$ vs. V_D and Temperature

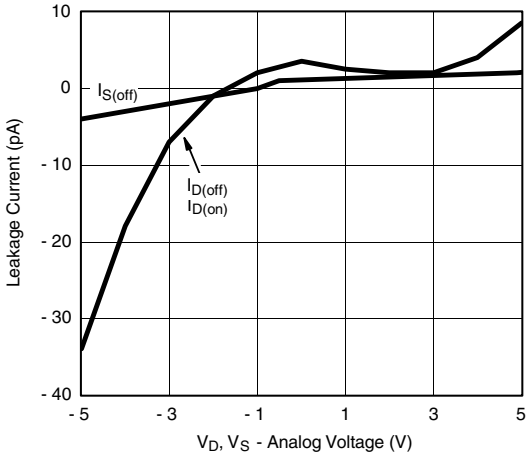


$R_{DS(on)}$ vs. V_D and Temperature

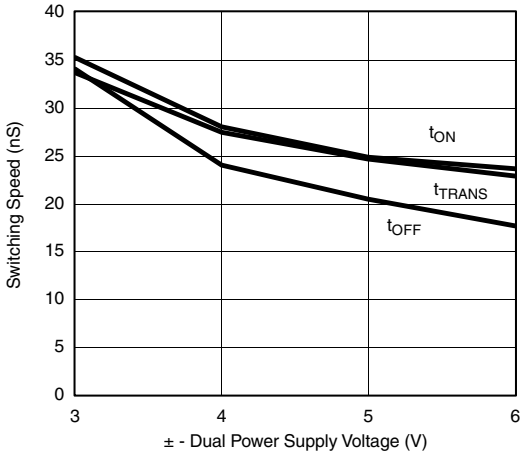


Switching Time vs. Positive Supply Voltage

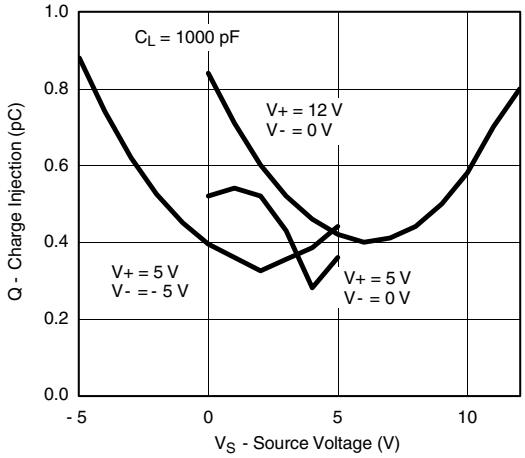
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



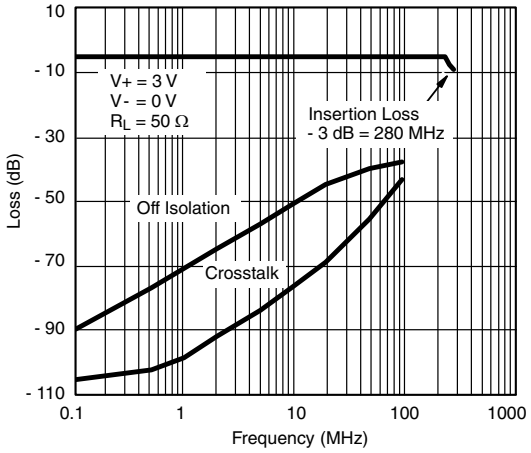
Leakage Current vs. Analog Voltage



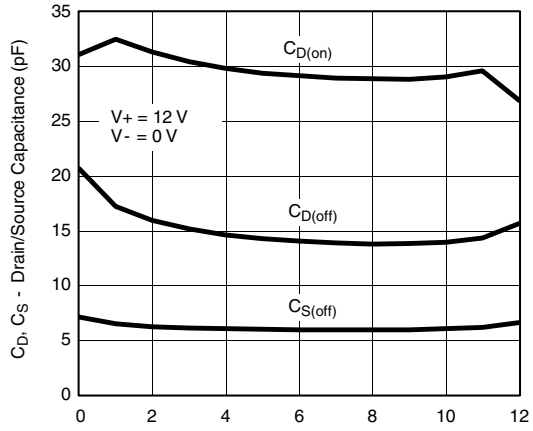
Switching Time vs. Dual Power Supply Voltage



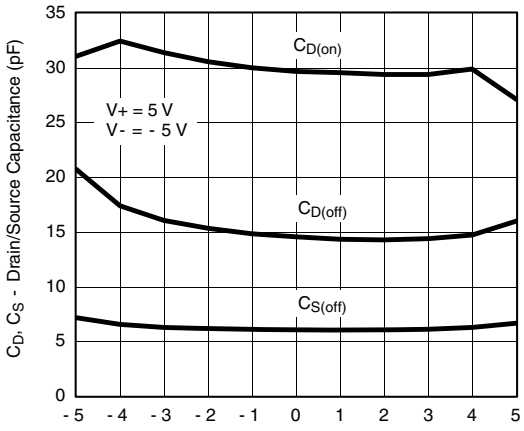
Charge Injection vs. Analog Voltage



Insertion Loss, Off Isolation, and Crosstalk vs. Frequency (Single Supply)



Drain/Source Capacitance vs. Analog Voltage



Charge Injection vs. Analog Voltage

SCHEMATIC DIAGRAM (Typical Channel)

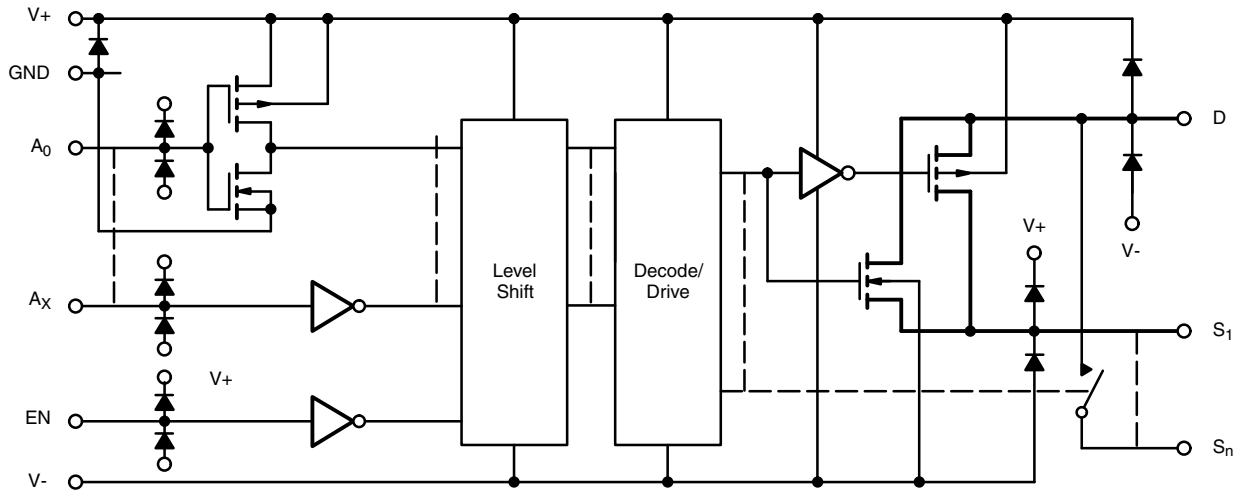
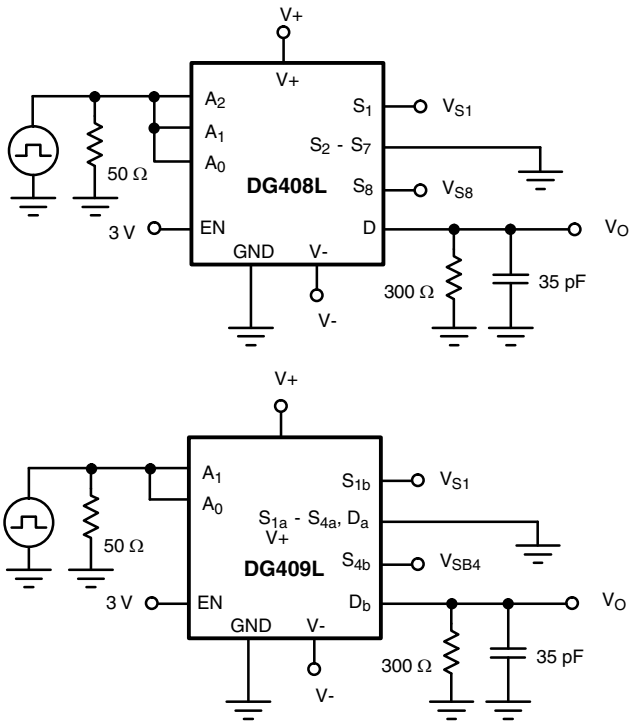


Fig. 1

TEST CIRCUITS



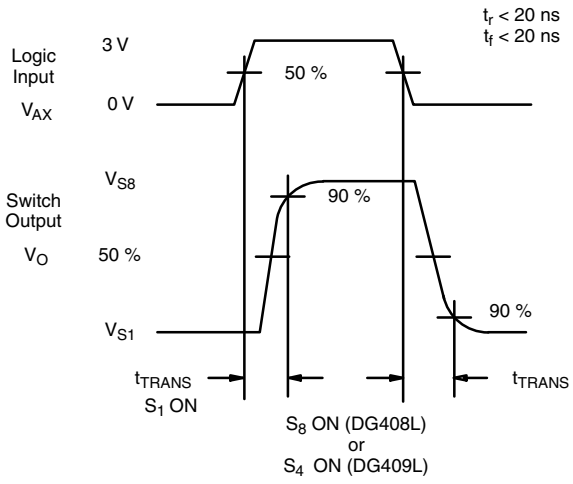


Fig. 2 - Transition Time

TEST CIRCUITS

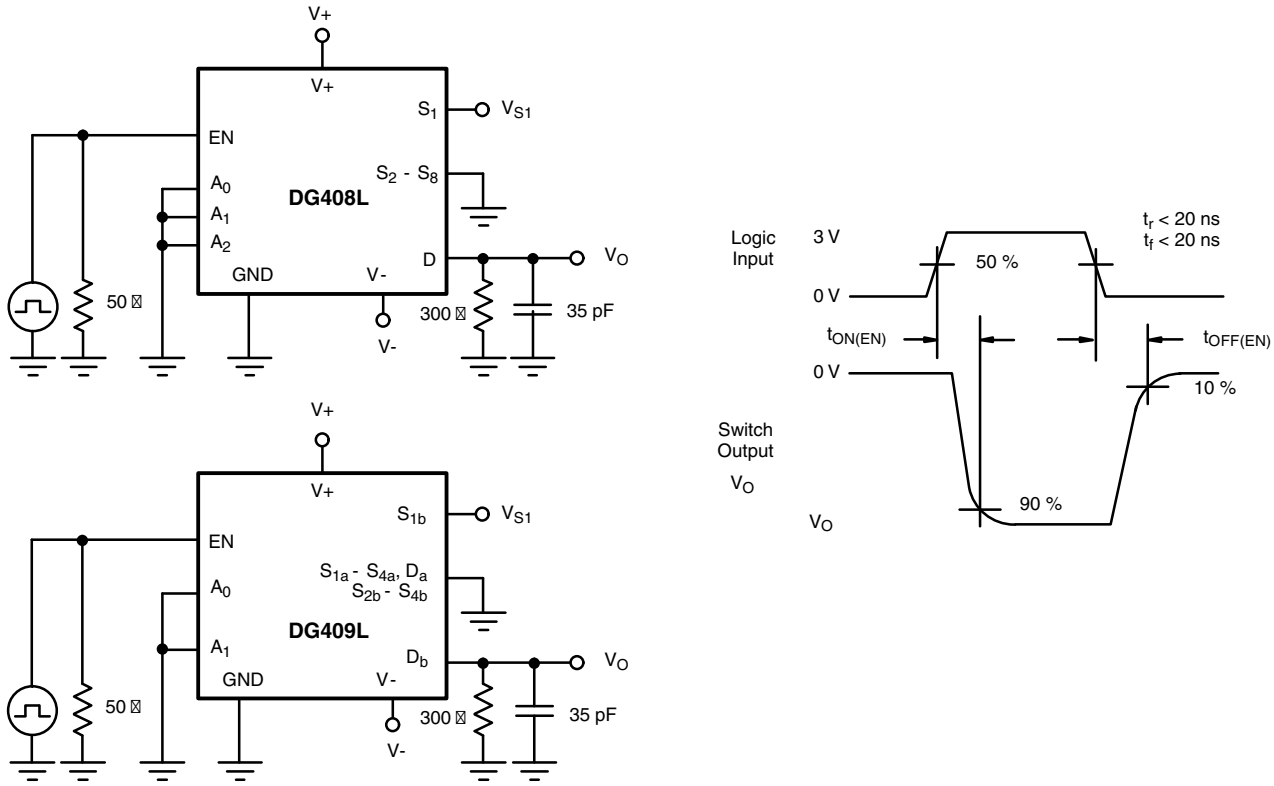


Fig. 3 - Enable Switching Time

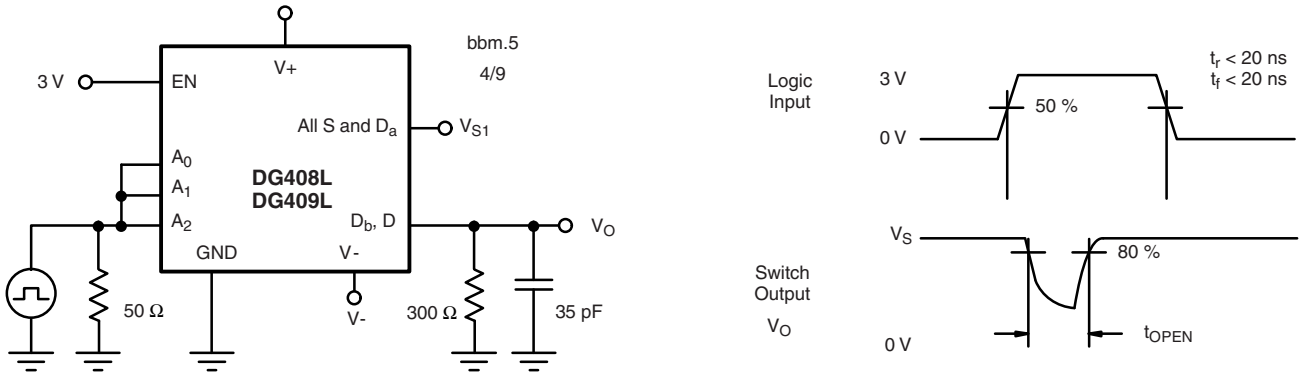


Fig. 4 - Break-Before-Make Interval

TEST CIRCUITS

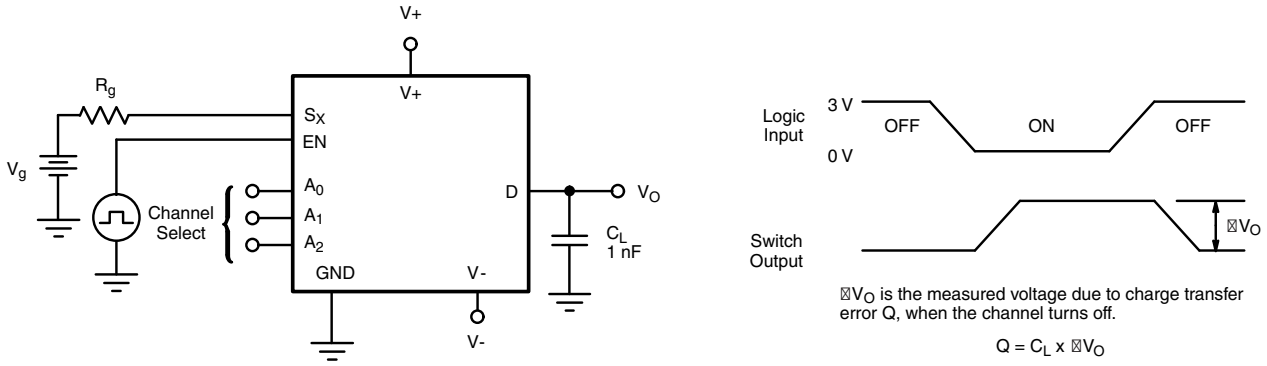


Fig. 5 - Charge Injection

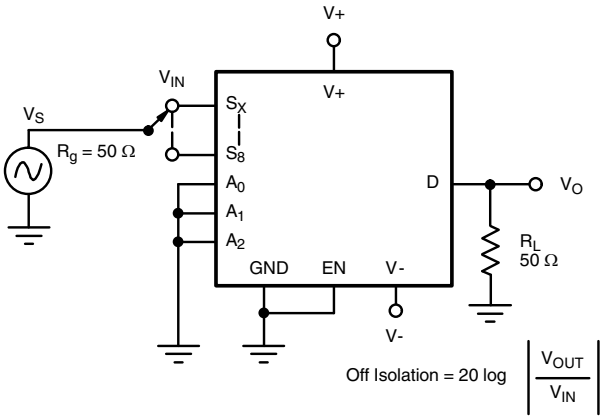


Fig. 6 - Off Isolation

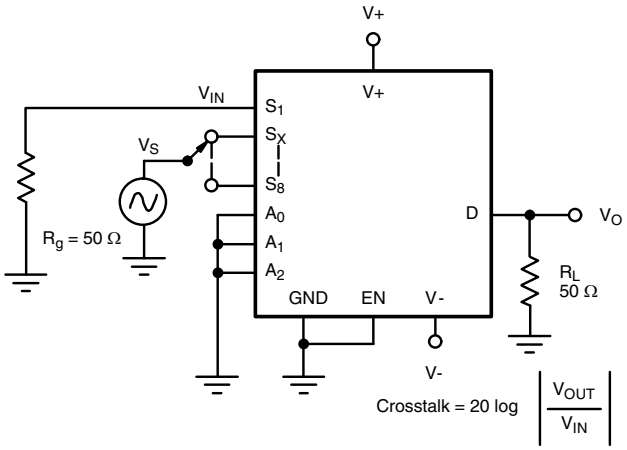


Fig. 7 - Crosstalk

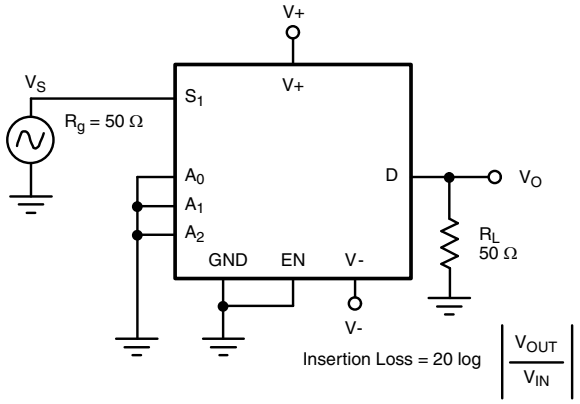


Fig. 8 - Insertion Loss

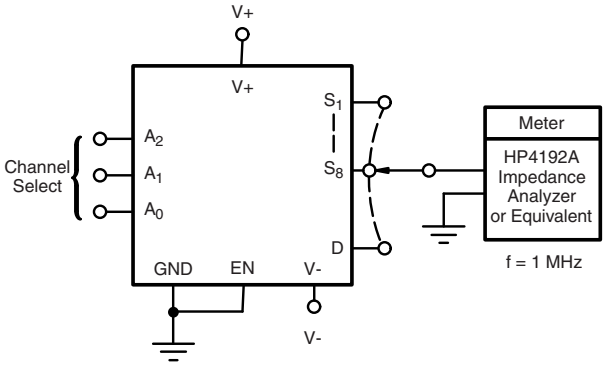


Fig. 9 - Source Drain Capacitance

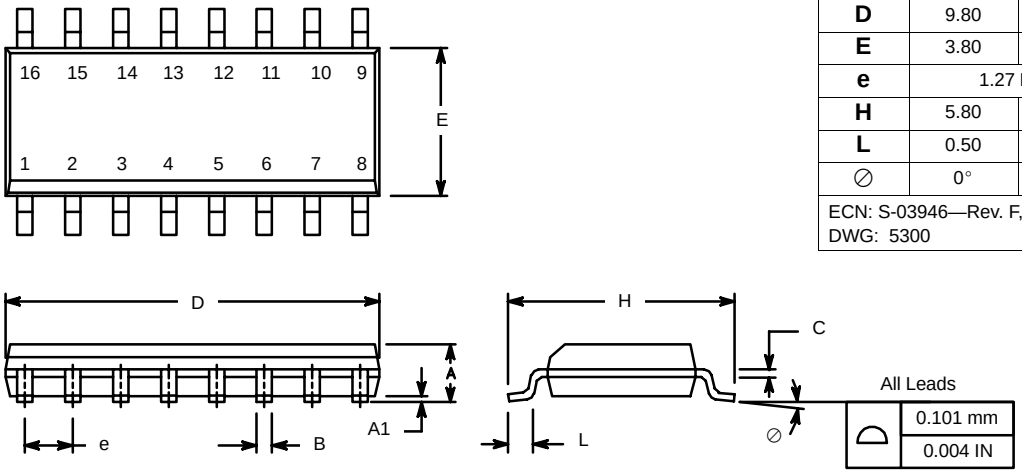
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71342.

SOIC (NARROW): 16-LEAD

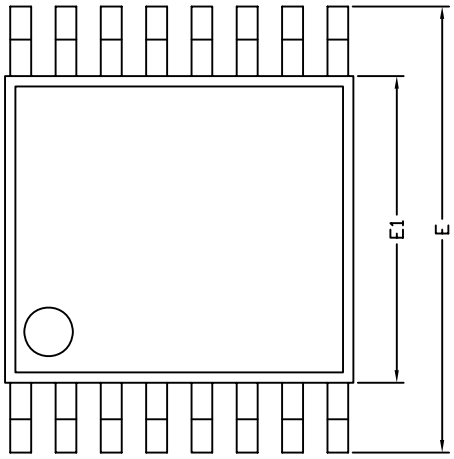
JEDEC Part Number: MS-012

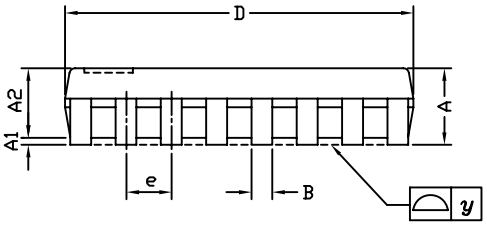
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

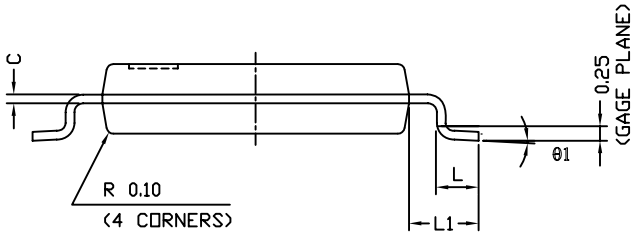
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



TSSOP: 16-LEAD

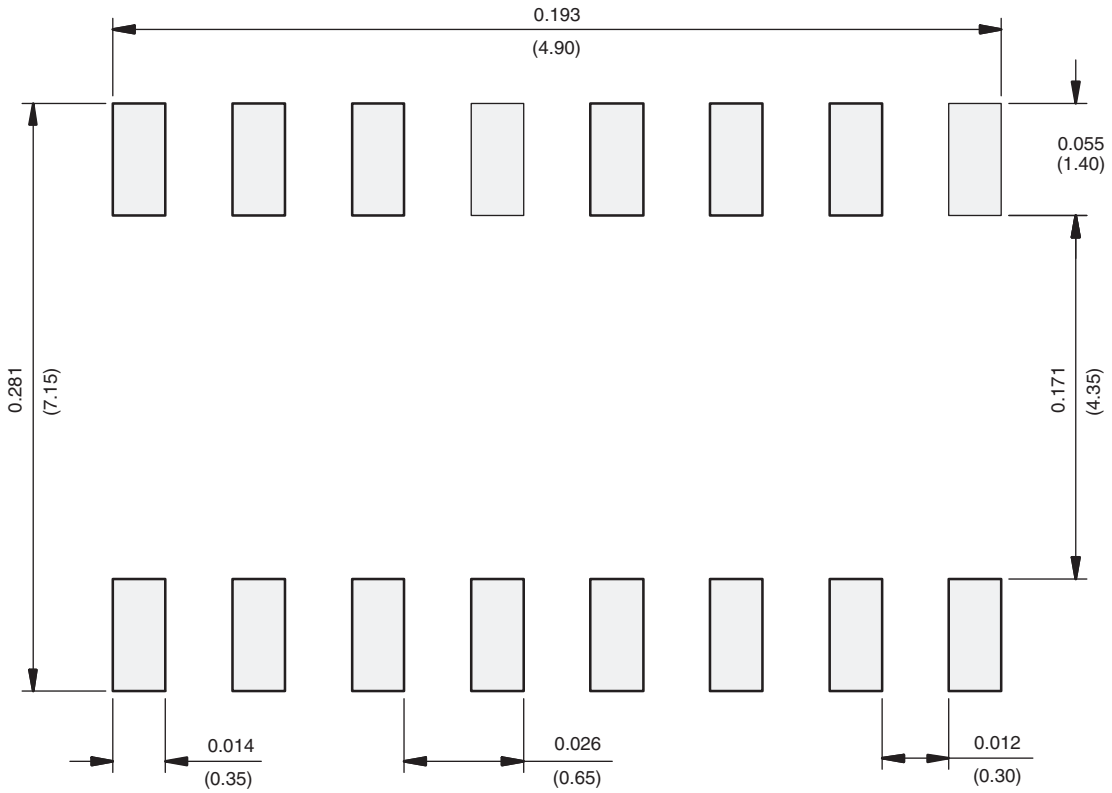






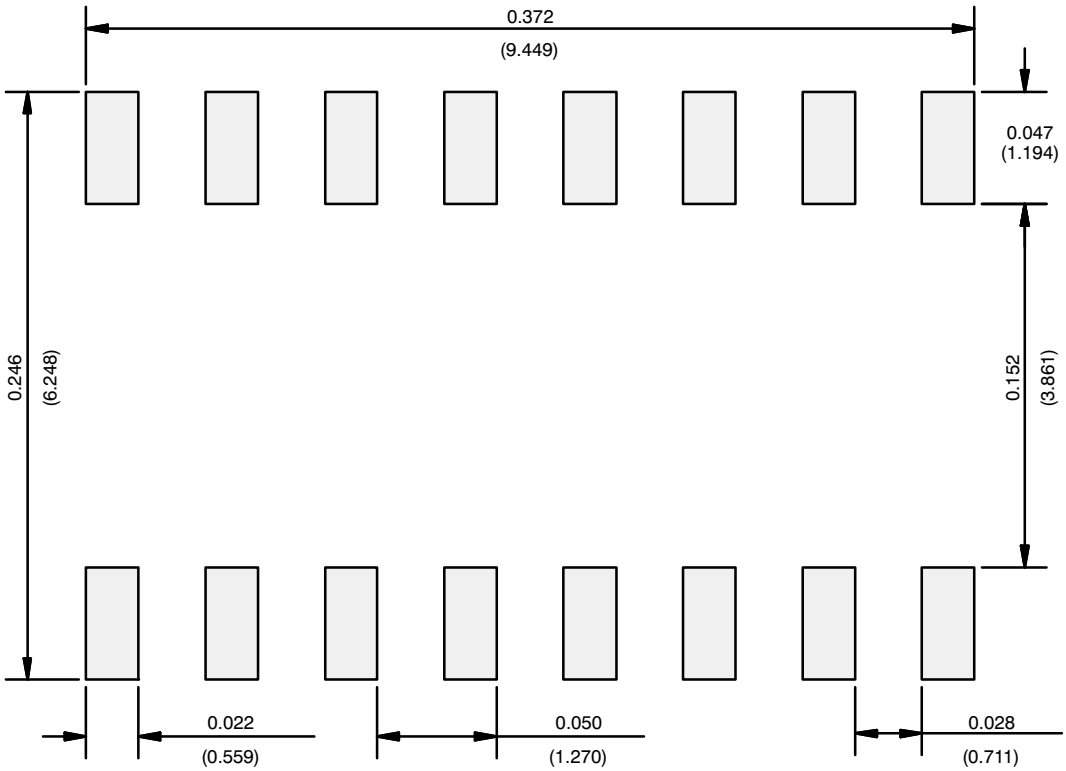
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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