Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the PGA400-Q1EVM. An EVM overview, graphical user-interface (GUI) description, interface requirements, and complete schematic are included in this document.

How to Use This Manual

This document contains the following chapters:

1. *Chapter 1: Power Supply Requirements and Connections*
2. *Chapter 2: Jumper Settings*
3. *Chapter 3: Sensor Inputs and Simulators*
4. *Chapter 4: PGA400-Q1 VOUT1 and VOUT2 Output Circuitry*
5. *Chapter 5: PGA400-Q1 Communication interfaces*
6. *Chapter 6: Controlling the PGA400-Q1 Memory Spaces with the GUI*
7. *Chapter 7: Controlling the PGA400-Q1 Functions with the GUI*
8. *Chapter 8: PGA400-Q1 EVM Schematics and Layout Drawings*

EVM Overview

Features

The EVM includes the following features:

- Single 12-VDC power-supply input for basic operation
- Resistive and capacitive sensor simulators
- PC Control with a GUI and USB communications board
- One-wire-interface (OWI) activation and communication circuitry
- RS-232 transceiver for UART testing and debug

Introduction

The PGA400-Q1 device is a generic-sensor interface integrated circuit (IC) for resistive and capacitive sensors. The device features a configurable analog front-end (AFE) with diagnostics, sigma-delta ADC, 8051 microcontroller, DACs, SPI, I^2C, and a one-wire interface (OWI).

Power Supply Requirements and Connections

The PGA400-Q1EVM has only one main 9-VDC to 12-VDC power connector that supplies power to the entire board. The user is required to connect a power supply to the banana jacks, P1 *VPWR* and P3 *GND* or use the screw terminal P2. Figure 1-1 shows an example using the banana jack connections.

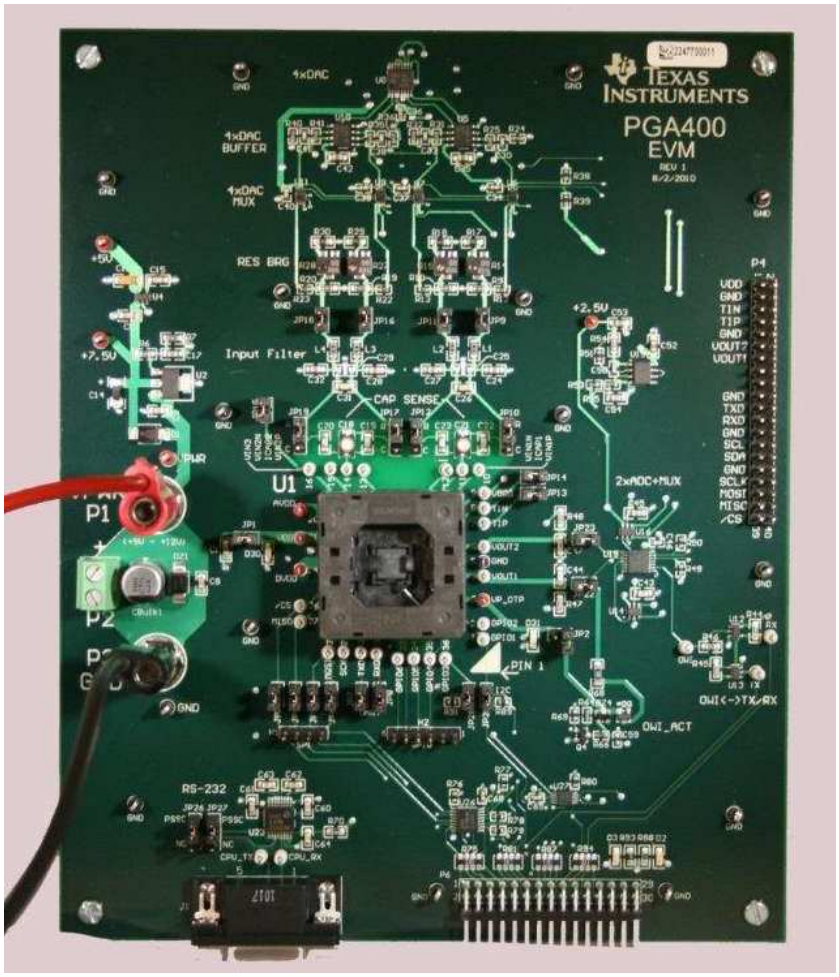


Figure 1-1. Minimum Power Connections to the PGA400-Q1 EVM

Configure the power supply based on the following table:

CONNECTION	VOLTAGE	CURRENT LIMIT
VPWR	9 – 12 VDC	100 mA

When powered, the D30 LED should light up and the EVM should draw between 30 and 55 mA depending on what state of operation the device is in.

1.1 Controlling and Powering the R2D2 EVM through TI-GER USB Board

The PGA400-Q1 EVM is shipped with a TI-GER USB communication board that provides a link from the PC controlled GUI (see Chapter 6) to the EVM. The user must connect the TI-GER board to the PGA400-Q1 by connecting the 15 × 2 100-mil female header on the TI-GER board to P6, the male 15 × 2 header on the PGA400-Q1 EVM. The TI logo on the TI-GER board should face up when it is plugged in. Figure 1-2 shows the TI-GER board connected to the PGA400-Q1 EVM.

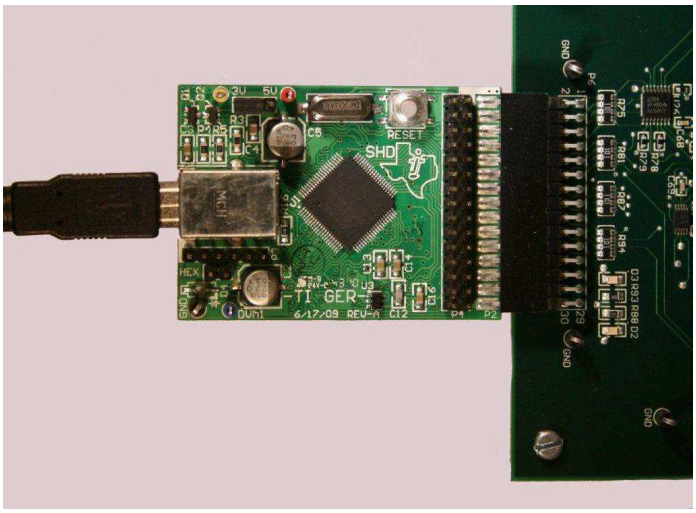


Figure 1-2. Connecting the TI-GER USB Communication Board to the PGA400-Q1 EVM

1.2 Power Supply LEDs

LEDs are installed in several places on the EVM to provide the user an indication that power-supplies are connected correctly. The V_{DD} and VP_OTP connections on the PGA400-Q1 device have LEDs to indicate that power is applied. Also, two LEDS indicate that the USB power supplies on the TI-GER boards are present.

Table 1-1. Power Supply LED Connections

LED	SUPPLY
D2	TI-GER 3.3 V
D3	TI-GER 5 V
D30	PGA400-Q1 V_{DD}
D31	PGA400-Q1 VP_OTP

Jumper Settings

Several jumpers are located on the board used to configure the connections to the PGA400-Q1 device and the remaining part of the EVM. Although the jumpers are installed to default settings in the factory, TI recommends that the user verify that the shunts are installed to the default settings before powering on the EVM. Section 2.1 lists the default settings and effects.

2.1 Default Jumper Settings

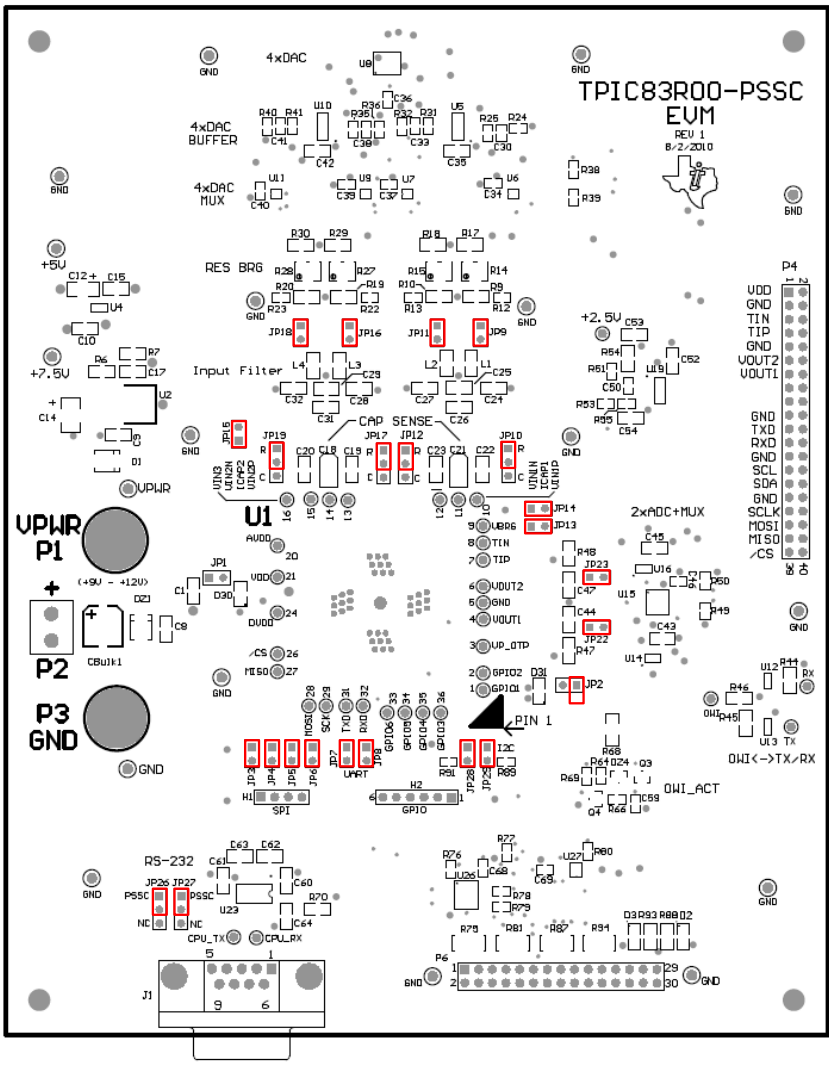


Figure 2-1. Default Jumper Settings

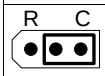
Table 2-1. Default Jumper Settings

REFERENCE	JUMPER POSITION	FUNCTION
JP1	Closed	The V_{DD} power-supply input on the PGA400-Q1 device is supplied from the 5-V regulator on the EVM.
JP2	Open	The VP_OTP power-supply input on the PGA400-Q1 device is not connected to the 7.5-V regulator on the EVM.
JP3	Closed	The $\overline{CS}$ signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
JP4	Closed	The MISO signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
JP5	Closed	The MOSI signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
JP6	Closed	The SCLK signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
JP7	Closed	The TXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver.
JP8	Closed	The RXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver.
JP9	Closed	The VIN1P input filter is connected to the DAC MUX and variable resistive bridge.
JP10	Closed	The VIN1P signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
JP11	Closed	The VIN1N input filter is connected to the DAC MUX and variable resistive bridge.
JP12	1-2	The VIN1N signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
JP13	Closed	The TIP signal on the PGA400-Q1 device is connected to the DAC MUX.
JP14	Closed	The TIN signal on the PGA400-Q1 device is connected to the DAC MUX.
JP15	Closed	The VIN3 signal on the PGA400-Q1 device is connected to the DAC MUX.
JP16	Closed	The VIN2P input filter is connected to the DAC MUX and variable resistive bridge.
JP17	Closed	The VIN2P signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
JP18	Closed	The VIN2N input filter is connected to the DAC MUX and variable resistive bridge.
JP19	Closed	The VIN2N signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
JP22	Closed	The VOUT1 signal on the PGA400-Q1 device is connected to the DAC Output MUX and to the P4 header.
JP23	Closed	The VOUT2 signal on the PGA400-Q1 device is connected to the DAC Output MUX and to the P4 header.
JP26	1-2	The U23 RS-232 Transceiver TX signal is connected to the PGA400-Q1 device.
JP27	1-2	The U23 RS-232 Transceiver RX signal is connected to the PGA400-Q1 device.
JP28	Closed	The SCL signal from the TI-GER is connected to the GPIO_3 signal on the PGA400-Q1 device.
JP29	Closed	The SDA signal from the TI-GER is connected to the GPIO_1 signal on the PGA400-Q1 device.

2.1.1 Jumper Setting Options

Table 2-2 lists the function of each specific jumper setting on the EVM.

Table 2-2. Jumper Setting Options

REFERENCE	JUMPER SETTING[1]	FUNCTION
JP1		The V_{DD} power-supply input on the PGA400-Q1 device is supplied from the 5-V regulator on the EVM.
		The V_{DD} power-supply input on the PGA400-Q1 device is not supplied from the 5-V regulator on the EVM and can be connected to an external 5-V power supply.
JP2		The VP_OTP power-supply input on the PGA400-Q1 device is connected to the 7.5-V regulator on the EVM.
		The VP_OTP power-supply input on the PGA400-Q1 device is not connected to the 7.5-V regulator on the EVM.
JP3		The $\overline{CS}$ signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
		The $\overline{CS}$ signal from the TI-GER board is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header.
JP4		The MISO signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header. The MISO signal from the TI-GER board is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header.
		
JP5		The MOSI signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
		The MOSI signal from the TI-GER board is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header.
JP6		The SCLK signal from the TI-GER board is connected to the PGA400-Q1 device in the U1 socket and to the P4 header.
		The SCLK signal from the TI-GER board is not connected to the PGA400-Q1 device in the U1 socket and is only connected to the P4 header.
JP7		The TXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver.
		The TXD signal from the PGA400-Q1 device is not connected to the U23 RS-232 transceiver.
JP8		The RXD signal from the PGA400-Q1 device is connected to the U23 RS-232 transceiver.
		The RXD signal from the PGA400-Q1 device is not connected to the U23 RS-232 transceiver.
JP9		The VIN1P input filter is connected to the DAC MUX and variable resistive bridge.
		The VIN1P input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that passes through the input filter to the PGA400-Q1 device.
JP10		The VIN1P signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
		The VIN1P signal on the PGA400-Q1 device is connected to the capacitive sensor simulator on the EVM.
		The VIN1P signal on the PGA400-Q1 device is not connected to anything on the EVM.
JP11		The VIN1N input filter is connected to the DAC MUX and variable resistive bridge.
		The VIN1N input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that passes through the input filter to the PGA400-Q1 device.

(1)  Indicates the corresponding pins that are shorted or closed.

Table 2-2. Jumper Setting Options (continued)

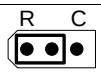
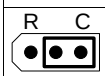
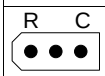
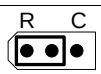
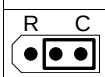
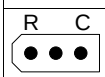
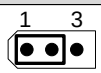
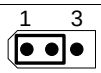
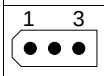
REFERENCE	JUMPER SETTING[1]	FUNCTION
JP12		The VIN1N signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
		The VIN1N signal on the PGA400-Q1 device is connected to the capacitive sensor simulator on the EVM.
		The VIN1P signal on the PGA400-Q1 device is not connected to anything on the EVM.
JP13		The TIP signal on the PGA400-Q1 device is connected to the DAC MUX and the P4 header.
		The TIP signal on the PGA400-Q1 device is not connected to anything on the EVM. The TIP signal on the P4 header is still connected to the DAC MUX.
JP14		The TIN signal on the PGA400-Q1 device is connected to the DAC MUX.
		The TIN signal on the PGA400-Q1 device is not connected to anything on the EVM. The TIN signal on the P4 header is still connected to the DAC MUX.
JP15		The VIN3 signal on the PGA400-Q1 device is connected to the DAC MUX.
		The VIN3 signal on the PGA400-Q1 device is not connected to anything on the EVM.
JP16		The VIN2P input filter is connected to the DAC MUX and variable resistive bridge.
		The VIN2P input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that passes through the input filter to the PGA400-Q1 device.
JP17		The VIN2P signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
		The VIN2P signal on the PGA400-Q1 device is connected to the capacitive sensor simulator on the EVM.
		The VIN2P signal on the PGA400-Q1 device is not connected to anything on the EVM.
JP18		The VIN2N input filter is connected to the DAC MUX and variable resistive bridge.
		The VIN2N input filter is not connected to the DAC MUX and variable resistive bridge. An external stimulus voltage can be applied that passes through the input filter to the PGA400-Q1 device.
JP19		The VIN2N signal on the PGA400-Q1 device is connected to the resistive bridge sensor simulators and input filters on the EVM.
		The VIN2N signal on the PGA400-Q1 device is connected to the capacitive sensor simulator on the EVM.
		The VIN2N signal on the PGA400-Q1 device is not connected to anything on the EVM.
JP22		The VOUT1 signal on the PGA400-Q1 device is connected to the DAC Output MUX , the OWI activation circuit, and the P4 header.
		The VOUT1 signal on the PGA400-Q1 device is not connected to the DAC Output MUX and the OWI activation circuit. The VOUT1 signal on the P4 header is still connected to the DAC Output MUX.
JP23		The VOUT2 signal on the PGA400-Q1 device is connected to the DAC Output MUX , and the P4 header.
		The VOUT2 signal on the PGA400-Q1 device is not connected to the DAC Output MUX. The VOUT2 signal on the P4 header is still connected to the DAC Output MUX.

Table 2-2. Jumper Setting Options (continued)

REFERENCE	JUMPER SETTING[1]	FUNCTION
JP26		The TXD signal on the PGA400-Q1 device is connected to the RS-232 transceiver.
		The TXD input of the RS-232 transceiver is not connected to the PGA400-Q1 device and is open so an external signal can be connected.
JP27		The RXD signal on the PGA400-Q1 device is connected to the RS-232 transceiver.
		The RXD input of the RS-232 transceiver is not connected to the PGA400-Q1 device and is open so an external signal can be connected.
JP28		The GPIO_3 signal on the PGA400-Q1 device is connected to the SCL signal on the TI-GER board and also to the P4 header.
		The GPIO_3 signal on the PGA400-Q1 device is not connected to the SCL signal on the TI-GER board. The SCL signal from the TI-GER board is still connected to the P4 header.
JP29		The GPIO_1 signal on the PGA400-Q1 device is connected to the SDA signal on the TI-GER board and also to the P4 header.
		The GPIO_1 signal on the PGA400-Q1 device is not connected to the SDA signal on the TI-GER board. The SDA signal from the TI-GER board is still connected to the P4 header.

Sensor Inputs and Simulators

The PGA400-Q1 device has two main-sensor AFEs in the sensor-signal conditions. One sensor is targeted towards resistive or voltage based sensors and the other sensor is targeted for capacitive sensors. The PGA400-Q1 EVM is equipped with simple circuits to simulate the basic functionality of these different sensors. Figure 3-1 shows a simplified block diagram of the sensor simulators on the PGA400-Q1 EVM.

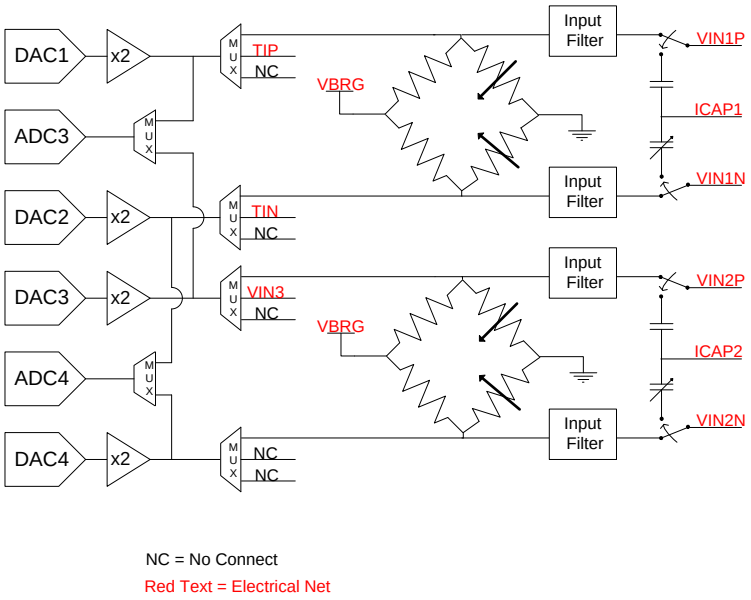


Figure 3-1. Simplified Block Diagram of PGA400-Q1 Input Circuitry

3.1 Resistive Bridge Sensors

A resistive bridge sensor on the PGA400-Q1 EVM can be simulated in two main ways. The first way is a simple resistive bridge with two variable legs that can be used to adjust the voltage to the VIN1P and VIN1N and the VIN2P and VIN2N inputs. The second uses 16-bit DACs and ADCs to set and measure the voltage at the inputs. Either of these simulators can be fed through an input filter and then into the PGA400-Q1 inputs.

3.1.1 Variable Resistive Bridge

The EVM is equipped with a variable resistive bridge that can be used to adjust the voltage at the inputs of the PGA400-Q1 device. The bridge is biased with the VBRG regulator from the PGA400-Q1 device. The resistance of each leg of the bridge varies from 17.5 kΩ to 22 kΩ. Figure 3-2 shows the channel-1 resistive bridge that is used to vary the voltage to the VIN1P and VIN1N inputs. The channel 2 resistive bridge is identical.

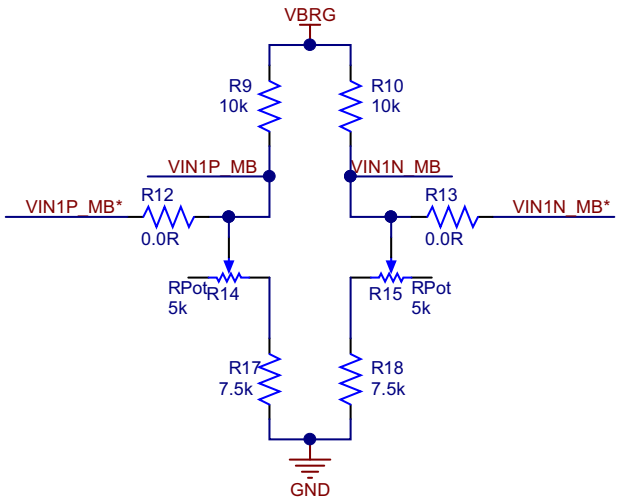


Figure 3-2. Channel-1 Resistive Bridge Sensor Simulator

3.1.2 Buffered DAC Outputs

The second way to excite the voltage inputs to the PGA400-Q1 device is to use the buffered DAC outputs on the EVM. The DAC8574, a four-channel 16-bit DAC, is used to generate voltage signals that can be used to excite the VIN1P, VIN1N, VIN2P, and VIN2N inputs. When the DAC MUX is set to the VIN1P, VIN1N, VIN2P, and VIN2N sensor inputs, the DAC buffers over-drive the voltage that the resistive bridge was previously producing. The buffered DAC voltage is measured with the ADS1100, 16-bit ADCs, and then adjusted to serve out errors. The DACs are controlled with the GUI (see Chapter 6). Figure 3-3 shows the DACs and the DAC buffers.

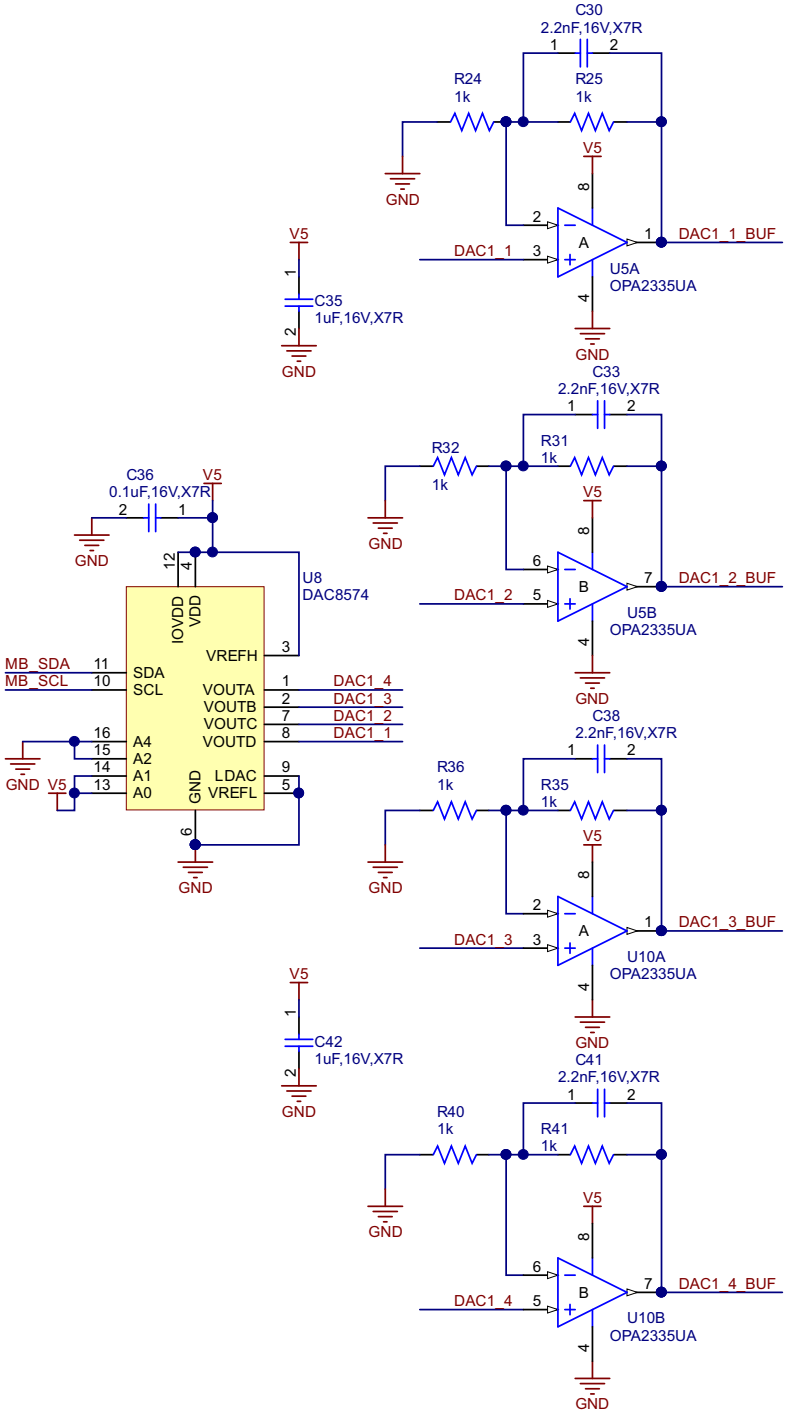


Figure 3-3. 4-Channel DAC8574 and OPA2335 Buffers

3.1.3 Input Filters

Both the buffered DAC outputs and the resistive bridge outputs feed through the input filter on the EVM before they connect to the inputs to the PGA400-Q1 device. The input filter is comprised of a common-mode and differential filter made from ferrite beads and capacitors. When the EVM is delivered to the customer, the ferrite beads L1 through L4 are populated with 49-Ω resistors so that the filters work as simple RC low-pass filters. If desired, the resistors can be replaced with ferrite beads that meet the requirements of the final customer system. Similarly, the EVM has an unpopulated footprint for an X2Y capacitor to replace the two common-mode and single differential capacitor. To use the X2Y capacitor, uninstall the three populated filter capacitors on the desired channels and install a single X2Y capacitor. Figure 3-4 shows the input filters on the EVM.

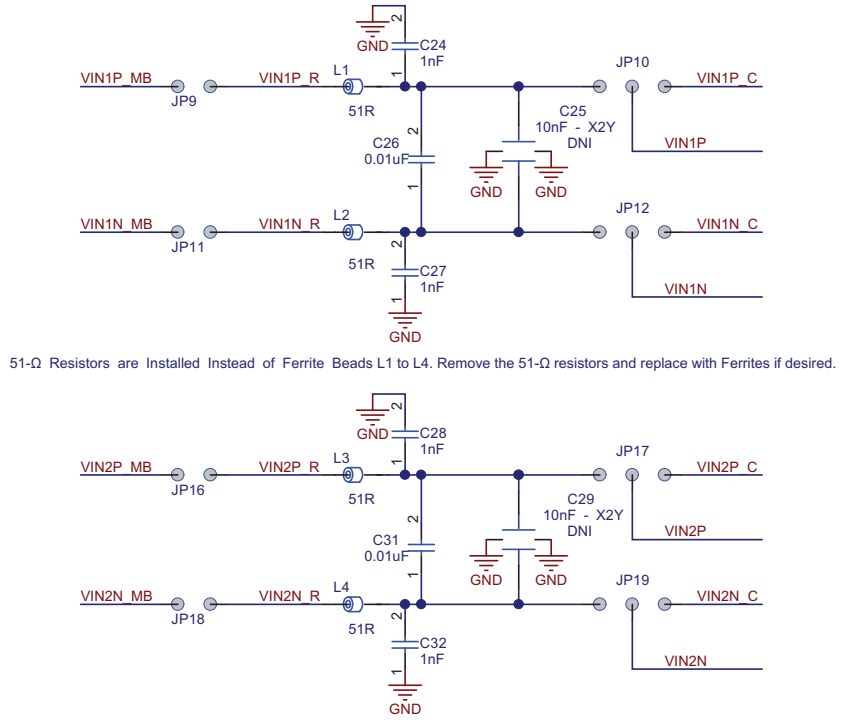


Figure 3-4. Input Filtering and Selection on the PGA400-Q1 EVM

3.2 Capacitive Sensors

The capacitive sensors on the PGA400-Q1 EVM can only be simulated in one way. This method uses a fixed reference capacitor on one leg, and then a fixed capacitor in parallel with a variable trim capacitor on the other leg. The reference leg capacitance is set to 56 pF, and the variable leg is adjustable from 35 to 80 pF. Figure 3-5 shows the circuit for the capacitive sensor simulator.

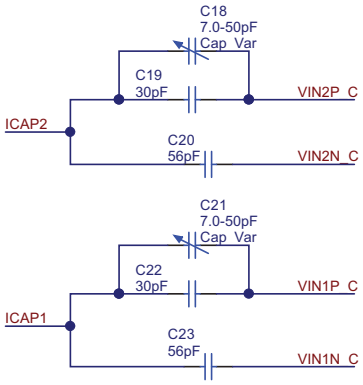


Figure 3-5. Capacitive Sensor Simulator

PGA400-Q1 VOUT1 and VOUT2 Output Circuitry

The PGA400-Q1 device has two DAC outputs, VOUT1 and VOUT2, which serve as the main output for the PGA400-Q1 device. Simple circuitry including output filtering and ADC monitoring of the DAC outputs are present on the EVM. The VOUT1 output also has circuitry that is used for the OWI activation as well as the OWI communication.

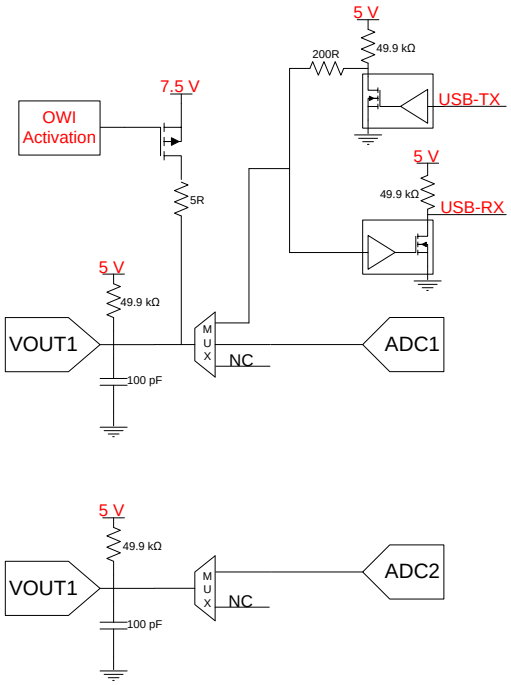


Figure 4-1. Simplified Block Diagram of PGA400-Q1 Output Circuitry

4.1 Output Filtering for VOUT1 and VOUT2

Both the VOUT1 and VOUT2 outputs on the PGA400-Q1 device have simple output filtering comprised of a resistive pull-up and a capacitor to GND. The capacitor is used to form a low-pass filter with the output impedance of the VOUT1 and VOUT2 DACs. The resistive pull-up is primarily used to fill the requirements for an external pull-up in OWI mode. Figure 4-2 shows the output filters on the VOUT1 and VOUT2 pins.

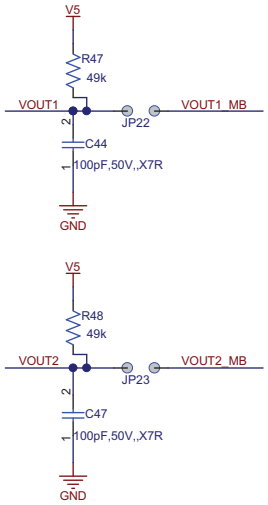


Figure 4-2. VOUT1 and VOUT2 (PSSC DAC) Output Filtering

4.2 ADC Measurement of VOUT1 and VOUT2 DAC Outputs

The EVM has two ADCs that are used to monitor and report the voltage at the VOUT1 and VOUT2 outputs back to the GUI. The EVM uses two ADS1100, 16-bit ADCs, to monitor the two outputs. The ADCs are enabled by configuring the PGA400-Q1 DAC output MUX to route the VOUT1 and VOUT2 outputs into the ADCs. The PGA400-Q1 DAC output MUX and the ADCs are all configurable with the GUI.

4.3 OWI Activation Circuitry — VOUT1

The VOUT1 pin on the PGA400-Q1 device is shared between the DAC output and the OWI transceiver. When the PGA400-Q1 device is running in MCU mode, the only way to signal to the IC that the device must enter OWI mode is to use a pull-up to bring the VOUT1 pin of the device to 7.5 V for at least 10 ms before the VOUT1 pin is released back to the previous value. The OWI activation circuitry is comprised of a simple PMOS pull-up to 7.5 V that is activated with a GPIO from the TI-GER USB communication board. The GUI ensures that the PGA400-Q1 DAC output MUX is open while the OWI activation pulse occurs so that the 5-V tolerant circuitry for the ADCs and the OWI transceiver are not damaged with the 7.5-V pulse. Figure 4-3 shows the OWI activation circuit.

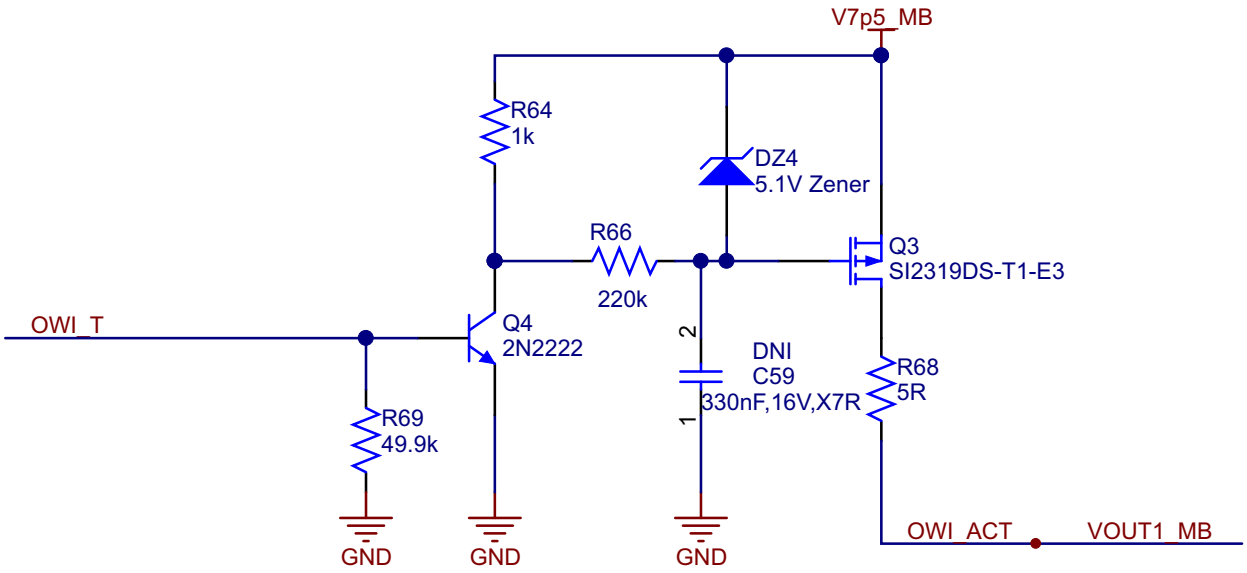


Figure 4-3. OWI Activation Circuit

4.4 OWI Transceiver — VOUT1

When the OWI transceiver in the PGA400-Q1 device has been activated either by the OWI activation pulse, or by a direct SPI write, the TI-GER board must communicate with the PGA400-Q1 device with the proper OWI signals. A simple circuit is used to convert the two-signal TI-GER USART (TX/RX) into the single wire OWI signal. The circuit operates in a way that the receiver is constantly monitoring even while transmitting so a loop-bak feature is always by the GUI uses to ensure the correct information was transmitted out of the TI-GER board. When a read is requested from the PGA400-Q1 device, an OWI message is transmitted from the VOUT1 pin, which is then received by the TI-GER. No issues of possible bus contention occur and the OWI transceiver circuit ensures that only the RX line is affected by the data transmitted out of the PGA400-Q1 device. Figure 4-4 shows OWI transceiver circuit.

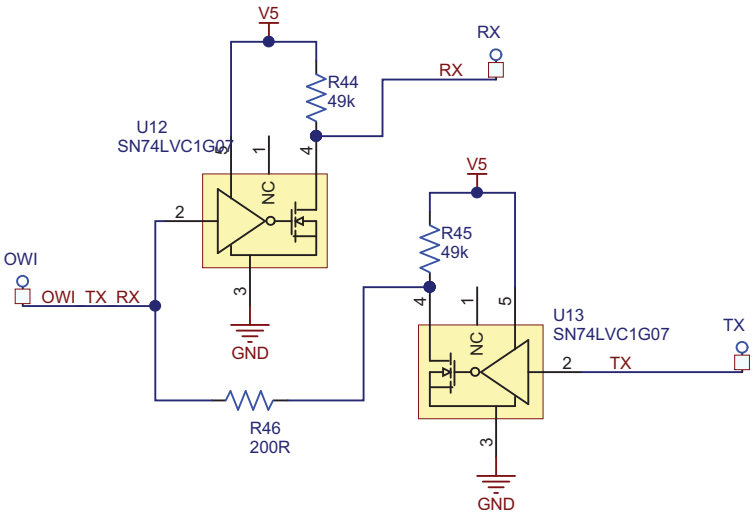


Figure 4-4. OWI Transceiver

PGA400-Q1 Communication Interfaces

The PGA400-Q1 device has several communication options including: SPI, I²C, OWI, and UART. All of these communication interfaces and related circuitry are present on the PGA400-Q1 EVM.

5.1 SPI

SPI is the main communication method on the PGA400-Q1 device and must be used to initially select one of the other communication methods (with the exception of the OWI activation pulse). Because the SPI and I²C pins are shared on the TI-GER communication board, a communication MUX is used to differentiate between the SPI and I²C functions on the EVM. By default the EVM powers up with the SPI communication interface selected. The user must change the setting on the communication MUX to change to I²C. The SPI signals can be monitored on the H1 header on the EVM. Figure 5-1 the SPI and I²C communication MUX.

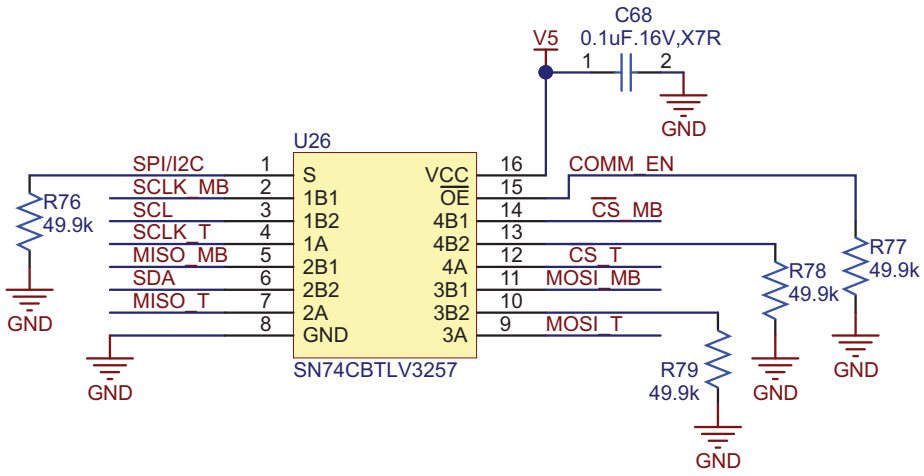


Figure 5-1. SPI and I²C Communication MUX

5.2 I²C

The I²C is the second most common protocol for communicating with the PGA400-Q1 device. The I²C communication method must be selected in the PGA400-Q1 device by sending the appropriate SPI commands before the communication will work. If the GUI is used to change from SPI to I²C mode, the GUI will configure the SPI and I²C MUX to send the I²C signals to the PGA400-Q1 device. The I²C is also used as the main communication method for the DAC and ADC peripherals on the EVM. To avoid any conflicts between I²C signals meant for the PGA400-Q1 device and I²C signals meant for the EVM peripherals. A second MUX is installed that splits the I²C signals between the PGA400-Q1 device and the rest of the EVM. Figure 5-2 shows the circuit of this MUX.

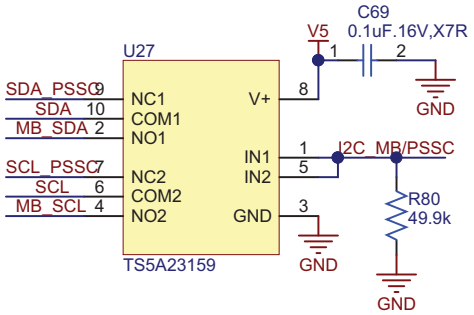


Figure 5-2. PGA400-Q1 EVM I²C MUX

5.3 OWI

During final system calibration, the OWI communication method is preferred because it allows for a three-pin sensor module (Power, GND, VOUT/OWI). The OWI communication method can be selected in the PGA400-Q1 device by either sending the appropriate SPI commands to place the device in OWI mode, or by issuing the OWI activation pulse and writing software in the 8051 MCU to switch to OWI mode when the OWI activation pulse is detected. The GUI can be used to create the OWI activation signal as well as performing the direct SPI writes to place the EVM into OWI mode. If the GUI is used to send the signals to enter OWI mode, then the EVM is automatically configured to route the TX and RX lines from the TI-GER board through the OWI transceiver to the VOUT1 pin.

5.4 UART

An RS-232 transceiver (MAX3221) is present on the EVM that can be used as a debugging interface from the 8051 MCU to a host PC. The circuit connects the TXD and RXD pins on the PGA400-Q1 to the MAX3221. The ±15-V RS-232 signals are routed to a standard DB-9 connector on the EVM. Figure 5-3 shows the RS-232 circuit.

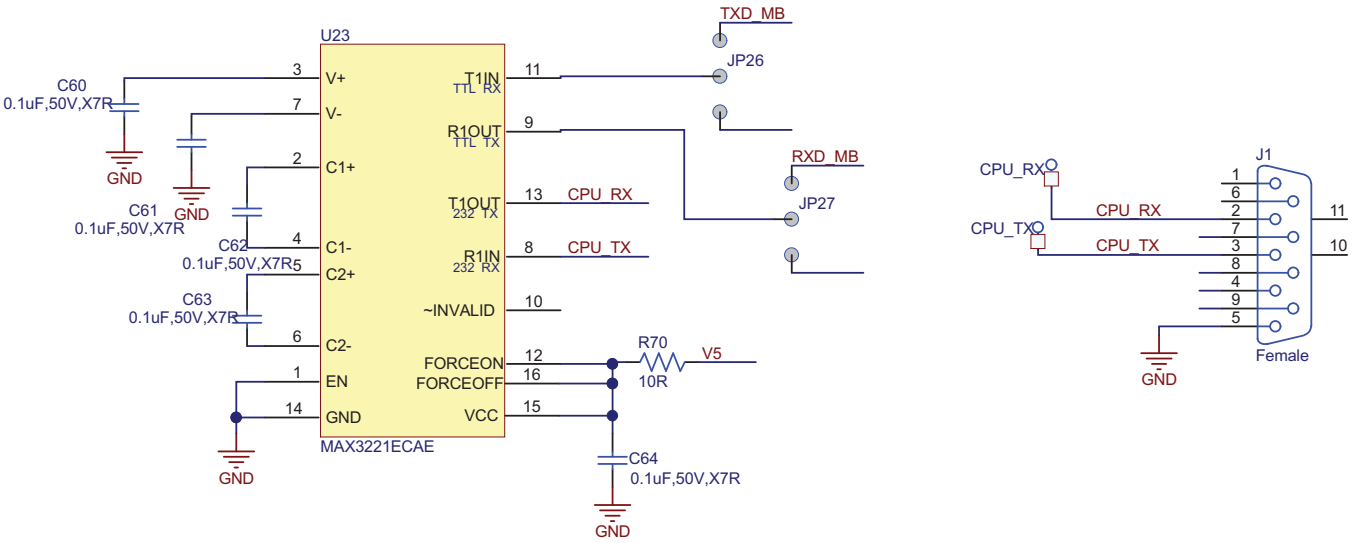


Figure 5-3. RS-232 Transceiver

Controlling the PGA400-Q1 Memory Spaces with the GUI

The PGA400-Q1 EVM is controlled by the user through a PC with the TI-GER USB communication board and associated GUI. The PGA400-Q1 EVM GUI provides ways to manipulate all of the register spaces present inside the PGA400-Q1 device (TEST, ESFR, EEPROM, IRAM, OTP). The following sections describe how to manipulate the register spaces.

6.1 Using the Register Grids to Manipulate the Register Spaces

Most of the register spaces have register grids associated with them that provide a simple way to read, write, or read and write the registers in the grid. Eight buttons are associated with the grid operations: *ZERO GRID*, *DESELECT GRID*, *SAVE GRID*, *RECALL GRID*, *READ SELECTED*, *WRITE SELECTED*, *READ ALL*, and *WRITE ALL*. These buttons perform operations on whichever register grid is currently displayed. For example, when the GUI first loads, the *TEST* register tab is displayed. If any of the previously listed buttons are pressed the buttons perform operations on the TEST register space. The following sections describe each of the grid functions.

6.1.1 ZERO GRID

The *ZERO GRID* button replaces the contents of the entire grid with 0.

6.1.2 DESELECT GRID

The *DESELECT GRID* button removes any selections that have been made in the grid without performing any operations on the registers that were selected.

6.1.3 SAVE GRID

The *SAVE GRID* button takes the contents of the register grid and save them to a .TXT file. The data is saved in comma-separated-values format.

6.1.4 RECALL GRID

The *RECALL GRID* button opens a prompt that allows the user to select a .TXT file that was produced during the *SAVE GRID* operation and then loads the grid with the contents from the .TXT file.

6.1.5 READ SELECTED

The *READ SELECTED* button performs a read operation on any registers in the grid that have been selected by clicking the desired register number. Any selected registers are displayed in blue.

6.1.6 WRITE SELECTED

The *WRITE SELECTED* button performs a write operation on any registers in the grid that have been selected by clicking the register number or modifying the register contents. Any selected registers are displayed in blue and any modified registers are displayed in yellow. Any blue or yellow registers are written to when the *WRITE SELECTED* button is pressed.

6.1.7 READ ALL

The *READ ALL* button performs a read operation on every register in the grid.

6.1.8 WRITE ALL

The *WRITE ALL* button performs a write operation on every register in the grid.

6.2 Test Registers

By default, the GUI opens with the TEST register-grid displayed. Aside from the functions associated directly with the grid, the *TEST* tab includes two buttons related to the TEST registers.

6.2.1 IFSEL/uC_RST

The *IFSEL/uC_RST* button toggles bit 0 and bit 1 of register 0x0E. Press this button to select SPI and shutdown the 8051 MCU before most other commands on the GUI will take affect is required.

6.2.2 Restricted Access

As described in the PGA400-Q1 data sheet (SLDS186), in order to access some of the features in the TEST register map, a special unlock sequence must be sent to register 0xFF. The *Restricted Access* button sends this sequence to the PGA400-Q1 device.

6.3 ESFR Registers

The *ESFR* register tab only contains a grid that can be used with the functions described before to directly manipulate the ESFR register space. Most of the buttons on the right half of the GUI control bits in the ESFR register tab. These buttons are described in Chapter 7.

6.4 EEPROM Registers

The EEPROM in the PGA400-Q1 device is comprised of six banks of EEPROM (BANK_0 to BANK_5) and a shared cache. In the PGA400-Q1 GUI, each EEPROM BANK is given a grid even though all operations are performed on the shared cache. As before, whichever *BANK* tab is displayed is the EEPROM bank that is operated on which is achieved by updating the EEPROM bank select bits in the TEST register space when the user selects a different EEPROM tab. By default, BANK_0 is selected. The four buttons on the *EEPROM* tab are described in the following sections.

6.4.1 Auto Program EEPROM

The *Auto Program EEPROM* button uses the internal EEPROM charge pump and timer to enable and then disable the EEPROM charge pump after the programming time has been met. This button should be used if the user desires to burn the current EEPROM cache contents to the EEPROM bank.

6.4.2 PROG_ON

The *PROG_ON* button is used for a manual method of programming/testing the EEPROM. The *PROG_ON* button turns on the EEPROM charge pump. Because no timer exists to automatically turn the EEPROM charge pump back off, the user must press the *PROG_OFF* button to disable the charge-pump

6.4.3 PROG_OFF

The *PROG_OFF* button is used to complete a manual EEPROM programming by disabling the EEPROM charge pump.

6.4.4 Reload CACHE

The *Reload CACHE* button uses the TEST register 0x0D to reload the CACHE with the contents of the selected EEPROM bank and then performs a read-all to update the grid with the refreshed contents of the EEPROM bank.

6.5 IRAM

The *IRAM* tab is setup only for individual register read and writes without the use of the grid. When this tab is displayed, the READ SELECTED / READ ALL and WRITE SELECTED / WRITE ALL buttons perform the same operations respectively.

6.6 OTP

The OTP tab is setup only for individual register read/writes without the use of the grid. When this tab is displayed, the *READ SELECTED*, *READ ALL*, *WRITE SELECTED*, and *WRITE ALL* buttons perform the same operations respectively. The OTP tab also contains buttons used to load a .HEX 8051 program file into the 8051 MCU in the PGA400-Q1 device.

6.6.1 Load .HEX File into GUI

The *Load .HEX File into GUI* button is used to load the contents of a .HEX file into the GUI RAM for use with other operations. When the button is pressed, a second window opens that allows the user to locate and open the desired .HEX file on the PC. Figure 6-1 shows an example of this operation.

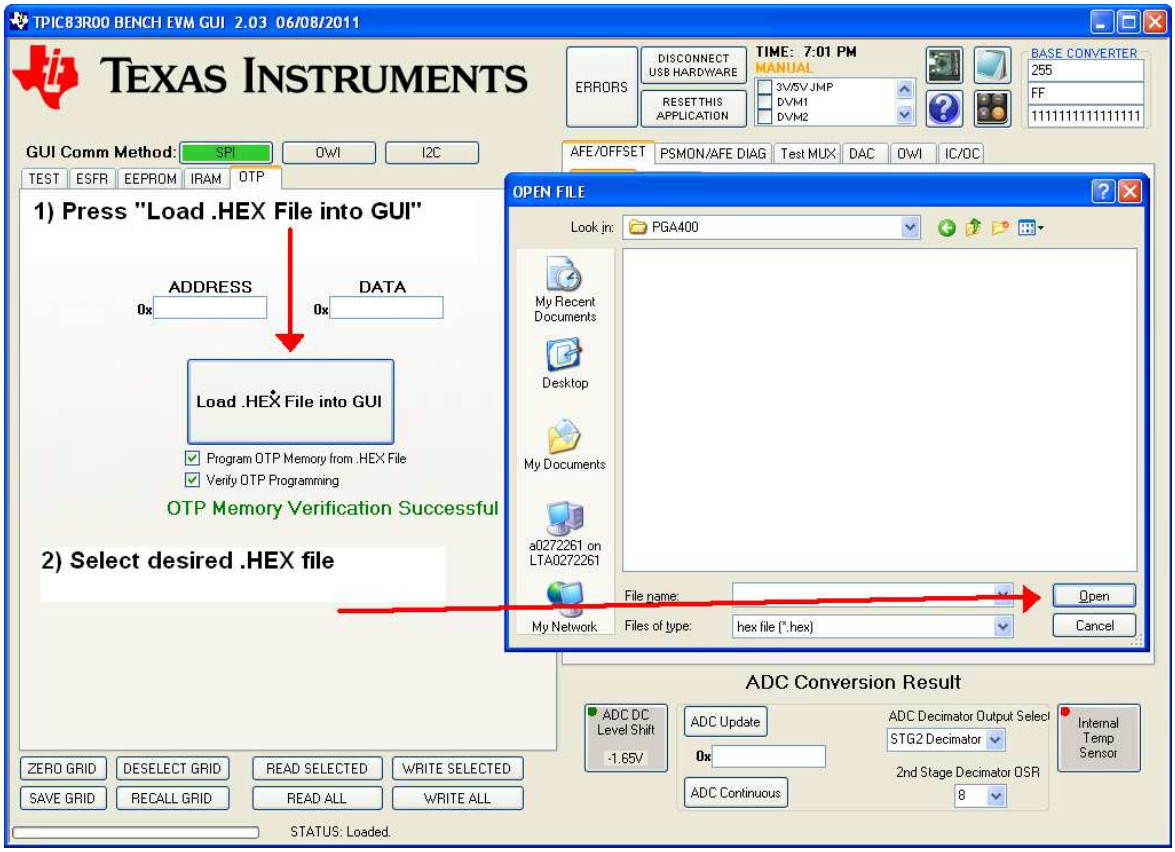


Figure 6-1. Loading a .HEX File into the GUI

6.6.2 Program OTP Memory from .HEX File

If the *Program OTP Memory from .HEX File* check box was checked (default) when the .HEX file was loaded into the GUI, the OTP memory is programmed with the contents of the .HEX file.

6.6.3 Verify OTP Programming

If the *Verify OTP Programming* button was also checked (default) then after the OTP memory is finished programming, the GUI resets the MCU and then verifies that the contents of the OTP memory match the .HEX file. If the OTP memory matches the contents of the .HEX file, the GUI displays the message *OTP Memory Verification Successful* as shown in green text in Figure 6-2.

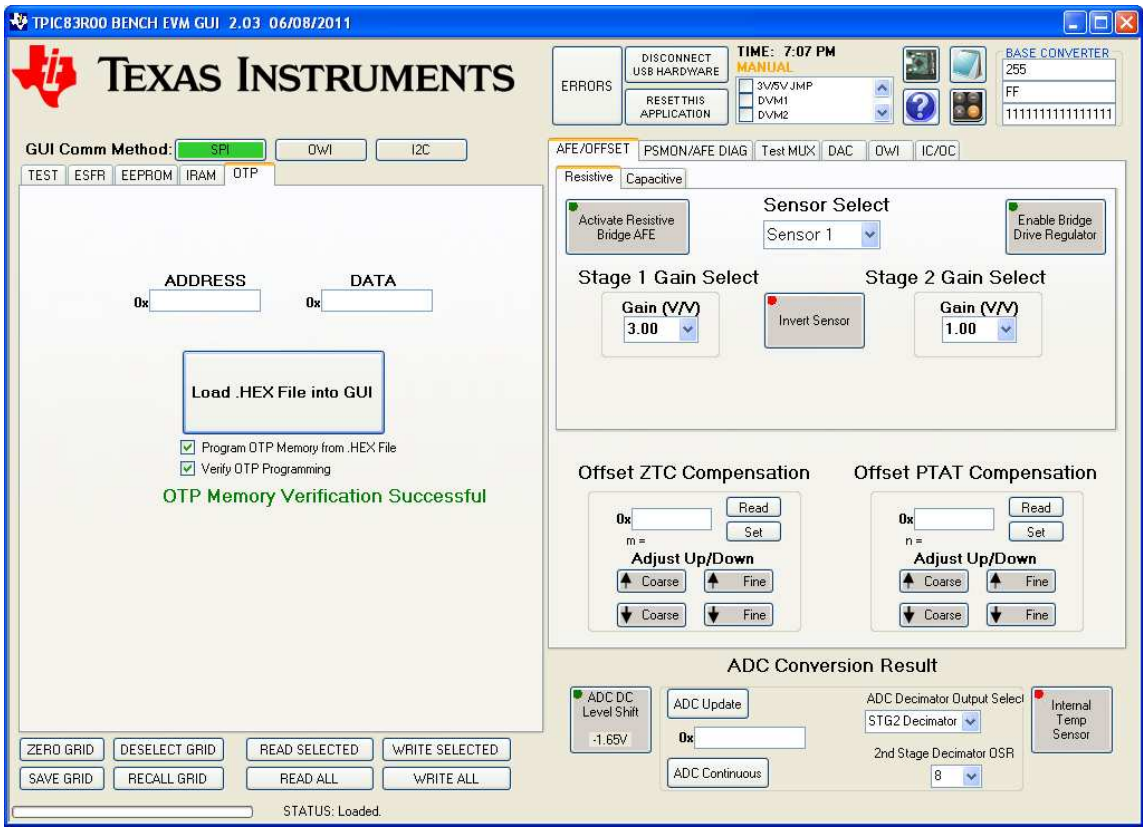


Figure 6-2. OTP Memory Successful Programming Verification

Controlling the PGA400-Q1 Functions with the GUI

The previous section focused on the left side of the GUI which is primarily used for direct register manipulation. The right side of the GUI is focused on providing a graphical method for controlling the PGA400-Q1 device.

7.1 ADC Conversion Result Section of the GUI

The bottom-right corner of the GUI is dedicated for functions that support or directly read from the internal ADC inside the PGA400-Q1 device. These buttons were not put inside a tab like the rest of the buttons because reading the ADC registers that modify the AFE settings without switching tabs is useful. Figure 7-1 shows the ADC Conversion Result section of the GUI. The following sections include figures and descriptions of the buttons found on this section.

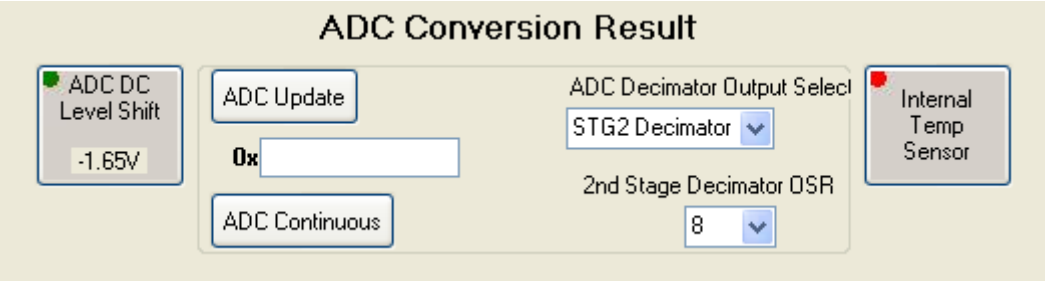


Figure 7-1. ADC Conversion Result Section of GUI

7.1.1 ADC Update

The *ADC Update* button is used to load the contents of the ADC into the shadow register and then read the contents into the GUI. The *ADC Update* button loads the output from the decimator that is selected with the *ADC Decimator Output Select* combo-box. Results are displayed in both twos complement and signed decimal.

7.1.2 ADC Decimator Output Select

The *ADC Decimator Output Select* combo-box is used to control with ADC decimator output is loaded when the *ADC Update* button is pressed. The combo-box controls bits 2 to 0 in ESFR 0xB3.

7.1.3 ADC DC Level Shift

The *ADC DC Level Shift* button controls bit 5 in ESFR 0xA9.

7.1.4 Internal Temp Sensor

The *Internal Temp Sensor* button controls bit 4 in ESFR 0xA9.

7.2 AFE/Offset Tab

By default, the *AFE/Offset* tab is displayed in the right side of the GUI. This tab is divided into two parts. The first part enables and controls either the resistive or capacitive AFEs. The second part manipulates the shared offset DACs in the PGA400-Q1 device. The following sections describe the buttons on these tabs.

7.2.1 Resistive AFE Tab

The *Resistive* tab under the *AFE/OFFSET* tab is selected by default when the GUI loads. This tabe corresponds to the default setting to have the resistive AFE selected on power-up. Figure 7-2 shows the resistive AFE tab. The following sections describe the buttons on this tab.

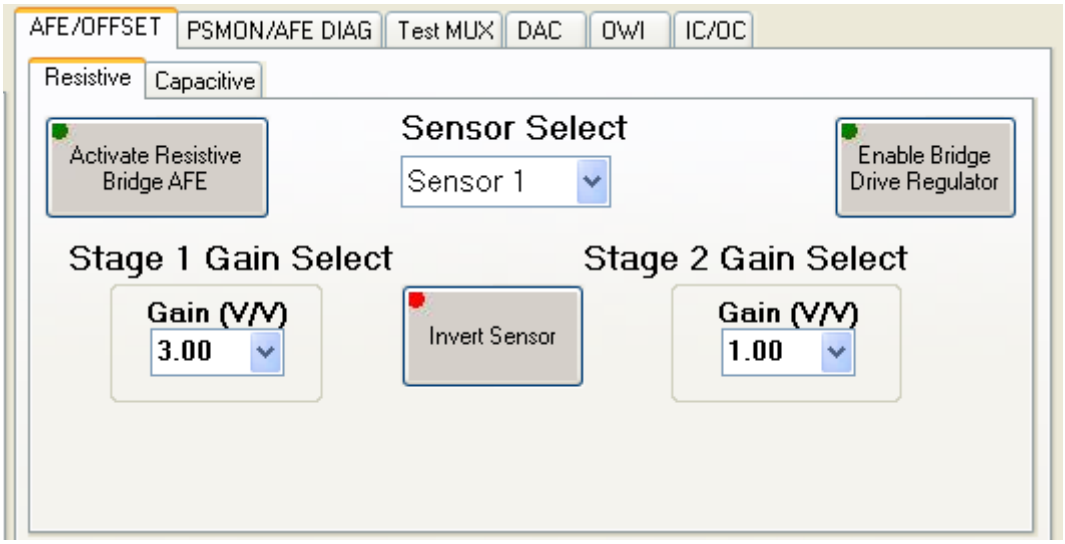


Figure 7-2. Resistive AFE Tab

7.2.1.1 Activate Resistive Bridge AFE

The *Activate Resistive Bride AFE* button configures the PGA400-Q1 device for the resistive AFE by controlling bit 7 in ESFR 0xA7.

7.2.1.2 Enable Bridge Drive Regulator

The *Enable Bridge Drive Regulator* button enables and disables the VBRG regulator by controlling bit 2 in ESFR 0xA9.

7.2.1.3 Sensor Select

The *Sensor Select* combo-box controls which input signals are routed through the AFE by controlling bit 7 of ESFR 0xA9. The combo-box also controls which set of registers the rest of the resistive AFE GUI controls. By default, Sensor 1 and all of the sensor specific buttons on the resistive tab are selected to control the Sensor 1registers. The Offset section is also set to control the Sensor 1 registers. If the combo-box is changed, the buttons will control the registers associated with the Sensor 2 inputs.

7.2.1.4 Invert Sensor

The *Invert Sensor* button controls the sign-bit MUX in the PGA400-Q1 device by controlling either bit 5 or bit 6 in register 0xA9 depending on the state of the *Sensor Select* combo-box.

7.2.1.5 Stage 1 Gain Select

The *Stage 1 Gain Select* combo-box controls bits 5-7 of either register 0xA1 or 0xA2 depending on the state of the *Sensor Select* combo-box

7.2.1.6 Stage 2 Gain Select

The *Stage 2 Gain Select* combo-box controls bits 0-4 of either register 0xA1 or 0xA2 depending on the state of the *Sensor Select* combo-box

7.2.2 Capacitive AFE Tab

The capacitive AFE tab is not activated by default when the GUI loads. The user can select the capacitive tab and then enable the capacitive AFE to begin evaluating the capacitive signal chain on the PGA400-Q1 device. Figure 7-3 shows the capacitive AFE tab. The following sections describe the buttons found on this tab.

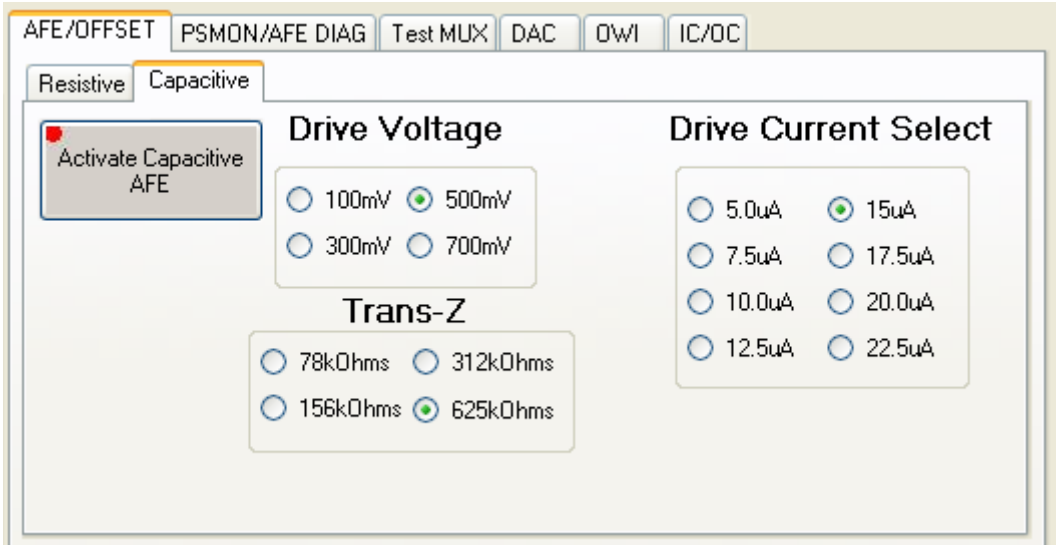


Figure 7-3. Capacitive AFE Tab

7.2.2.1 Activate Capacitive AFE

The *Activate Capacitive AFE* button configures the PGA400-Q1 device for the resistive AFE by controlling bit 7 in ESFR 0xA7.

7.2.2.2 Drive Voltage

The *Drive Voltage* selection boxes control the voltage on the clock generator comparator in the PGA400-Q1 device by controlling bits 2 and 3 in ESFR 0xA7.

7.2.2.3 Drive Current Select

The *Drive Current Select* selection boxes control the current that is switched in and out of the ICAP pins by controlling bits 4-6 in ESFR 0xA7.

7.2.2.4 Trans-Z

The *Trans-Z* selection boxes control the transimpedance resistance by controlling bits 0 and 1 in ESFR 0xA7.

7.2.3 ZTC and PTAT Offset Control

The ZTC and PTAT offset circuits are shared whether the user is using the PGA400-Q1 device in resistive or capacitive mode, therefore theses circuits are displayed when either AFE tab is selected. Figure 7-4 shows offset control region of the GUI. The following sections describe the buttons on the offset control region of the GUI.

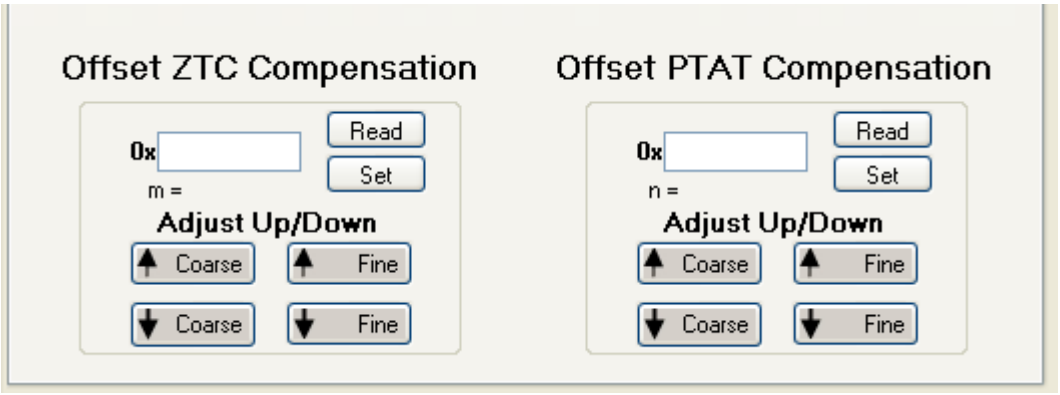


Figure 7-4. ZTC and PTAT Offset Control

7.2.3.1 Offset ZTC Compenstation Read/Set

The *Read* and *Set* buttons in the *Offset ZTC Compensation* region can be used to directly enter in the desired offset values. The buttons either read to or write from the ZTC offset bits in ESFRs 0xA3 and 0xA4 or 0xA5 and 0xA6 depending on the state of the *Sensor Select* combo-box.

7.2.3.2 Offset ZTC Compenstation Adjust Up/Down

The ↑ *Coarse*, ↓ *Coarse*, ↑ *Fine*, and↓ *Fine* buttons are used to adjust the value of the ZTC offset register up or down in set increments. The buttons write to the ZTC offset bits in ESFRs 0xA3 and 0xA4 or 0xA5 and 0xA6 depending on the state of the *Sensor Select* combo-box. The fine adjustments move the ZTC offset value by one, while the coarse adjustments move the ZTC offset value by 50.

7.2.3.3 Offset PTAT Compenstation Read/Set

The *Read* and *Set* buttons in the *Offset PTAT Compensation* region can be used to directly enter in the desired offset values. The buttons either read to or write from the PTAT offset bits in ESFRs 0xA4 or 0xA6 depending on the state of the *Sensor Select* combo-box.

7.2.3.4 Offset PTAT Compenstation Adjust Up/Down

The ↑ *Coarse*, ↓ *Coarse*, ↑ *Fine*, and↓ *Fine* buttons are used to adjust the value of the PTAT offset register up or down in set increments. The buttons write to the PTAT offset bits in ESFRs 0xA4 or 0xA6 depending on the state of the *Sensor Select* combo-box. The fine adjustments move the PTAT offset value by one, while the coarse adjustments move the PTAT offset value by 50.

7.3 PSMON/AFE Diagnostics Tab

The *PSMON/AFE Diagnostics* tab is the second tab in the right half tab control. The tab is setup so that when activated, any flags that are currently set are displayed in red, while all of the bits that do not have flags set are displayed in green. Figure 7-5 shows the *PSMON/AFE Diagnostics* tab the *ADC_INPUT_OV* flag is set showing that the input to the ADC is out of range (over voltage). All of the power supplies are in the correct range so none of the flags are set. The following sections describe the buttons on this tab.

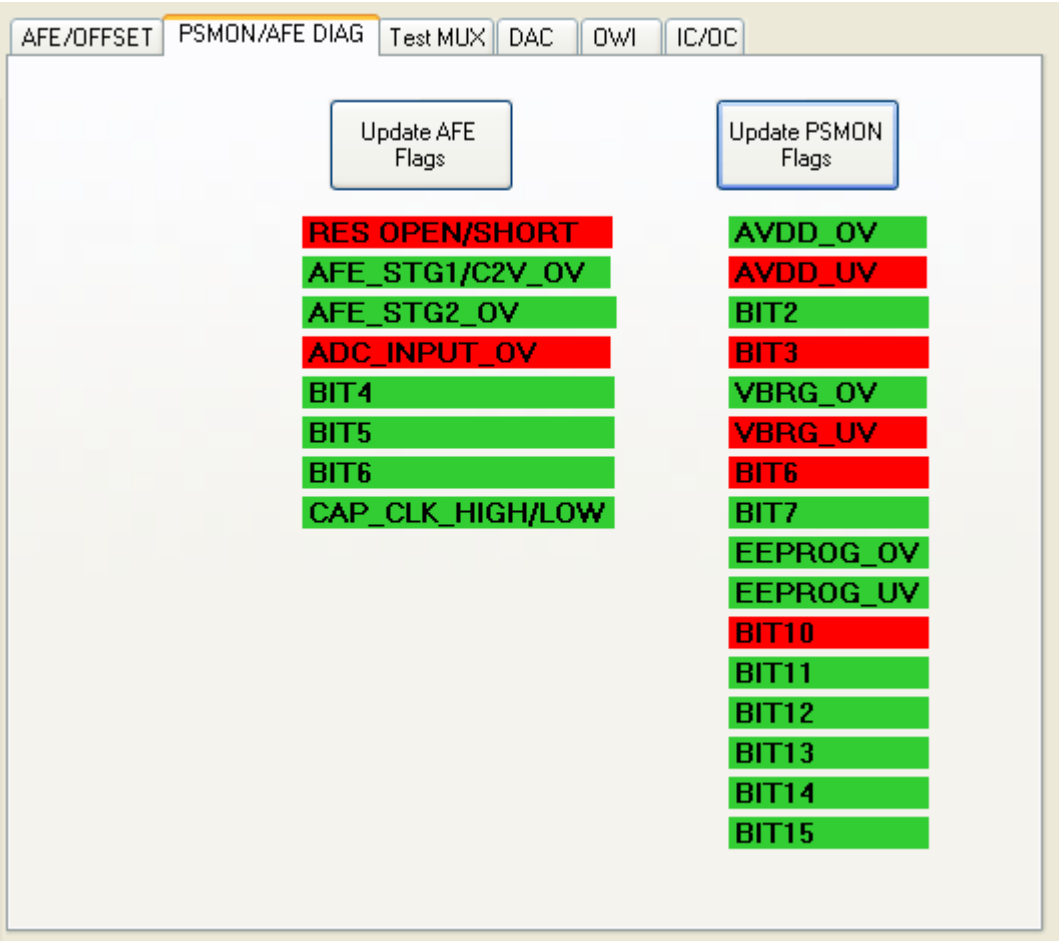


Figure 7-5. PSMON/ AFE Diagnostics Tab

7.3.1 Update AFE Flags

The *Update AFE Flags* button reads from ESFR 0x93 and then updates the color of the flags in the GUI accordingly.

7.3.2 Update PSMON Flags

The *Update PSMON Flags* button reads from ESFRs 0x91 and 0x92 and then updates the color of the flags in the GUI accordingly.

7.4 Test MUX

The *Test MUX* tab can be used to activate and control the settings on the analog and digital test in and out MUXs that are present inside the PGA400-Q1 device. The tab is divided into two tabs, one tabe for the analog test MUXs and the other tab for the digital test MUXs.

7.4.1 Analog Test MUX Tab

The *Analog Test MUX* tab is used to control the settings for the analog test MUXs inside the PGA400-Q1 device. Before any changes on the *Analog Test MUX* tab go into effect, the user must activate *Restricted Access* mode from the *TEST* tab. Figure 7-6 shows this tab. The following sections describe the controls on this tab.

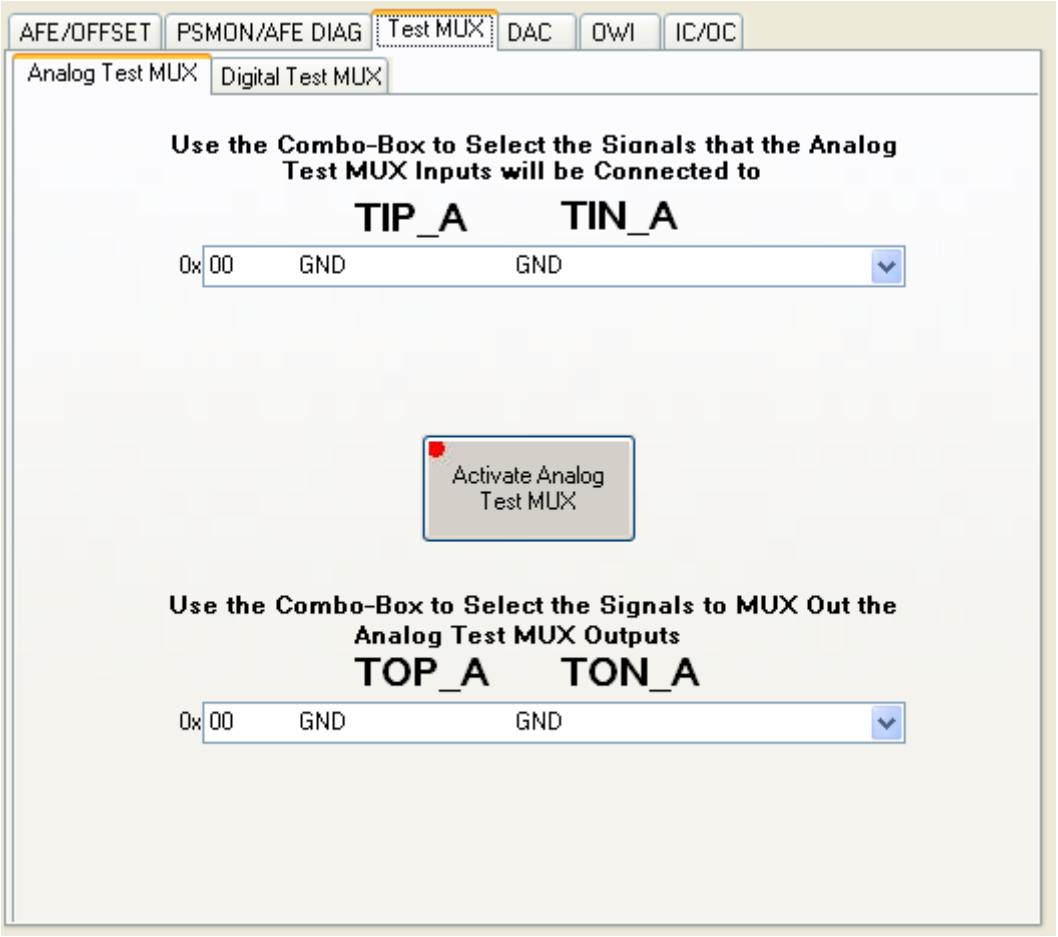


Figure 7-6. Analog Test MUX Tab

7.4.1.1 Activate Analog Test MUX

The *Activate Analog Test MUX* button disables the VOUT1 and VOUT2 DACs and activates the analog test MUXs by controlling bits 3 and 4 of TEST register 0x10.

7.4.1.2 TIP_A and TIN_A Combo-Box

The *TIP_A* and *TIN_A* combo-box is used to select where the TIN and TIP signals get routed inside the PGA400-Q1 device by controlling TEST register 0x08.

7.4.1.3 TOP_A and TON_A Combo-Box

The *TOP_A* and *TON_A* combo-box is used to select where the VOUT1 and VOUT2 signals get routed inside the PGA400-Q1 device by controlling TEST register 0x06.

7.4.2 Digital Test MUX Tab

The *Digital Test MUX* tab is used to control the settings for the digital test MUXs inside the PGA400-Q1 device. Before any changes on the *Digital Test MUX* tab goes into effect, the user must activate *Restricted Access* mode from the *TEST* tab. Figure 7-7 shows the *Digital Test MUX* tab. The following sections describe the controls on this tab.

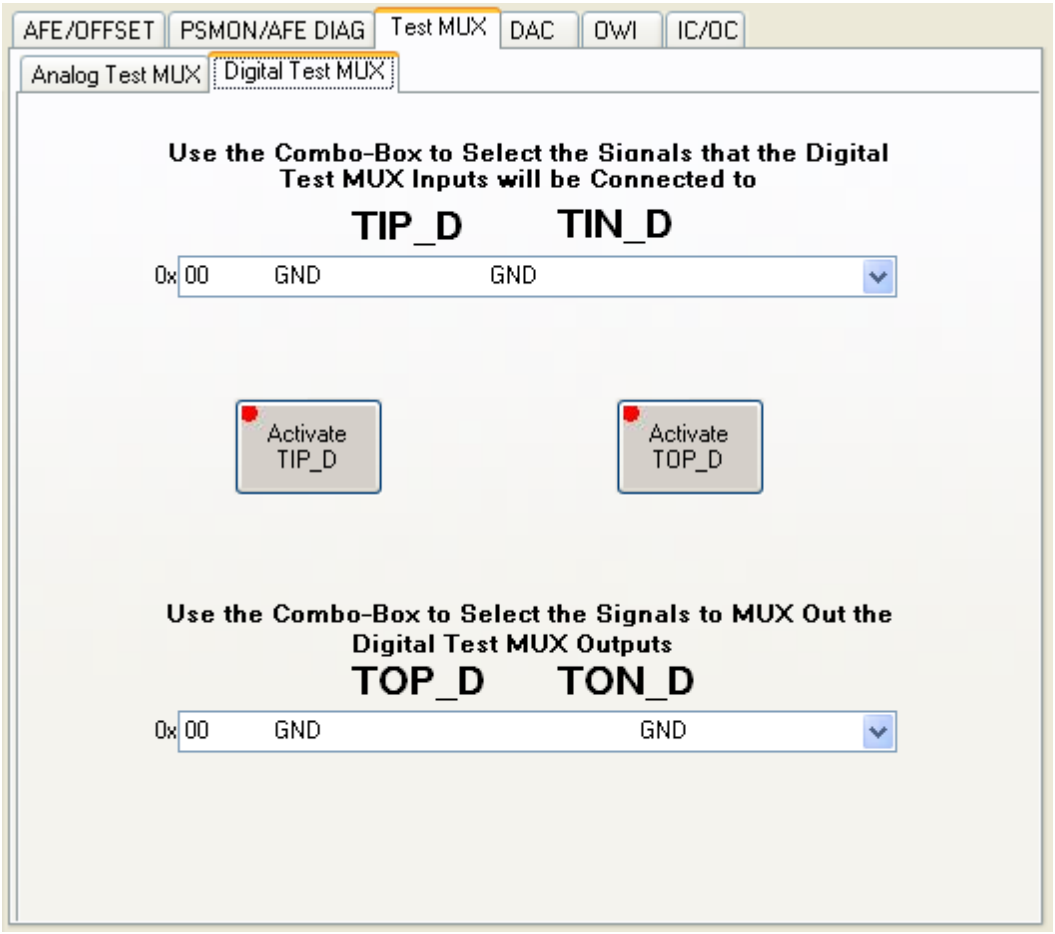


Figure 7-7. Analog Test MUX Tab

7.4.2.1 Activate TIP_D

The *Activate TIP_D* button disables the digital test input signal by controlling bit 1 of TEST register 0x03.

7.4.2.2 Activate TOP_D

The *Activate TOP_D* button disables the activates the digital test output signal by controlling bits 2 and 3 of TEST register 0x03.

7.4.2.3 TIP_D and TIN_D Combo-Box

The *TIP_D* and *TIN_D* combo-box is used to select where the digital test input signals get routed inside the PGA400-Q1 device by controlling TEST register 0x07.

7.4.2.4 TOP_D and TON_D Combo-Box

The *TOP_A* and *TON_A* combo-box is used to select where the VOUT1 and VOUT2 signals get routed inside the PGA400-Q1 device by controlling TEST register 0x06.

7.5 DAC Output Tab

The *DAC Output* tab can be used to directly control the output of the VOUT1 and VOUT2 DACs on the PGA400-Q1. Figure 7-8 shows the *DAC Output* tab. The following sections describe the buttons on this tab.

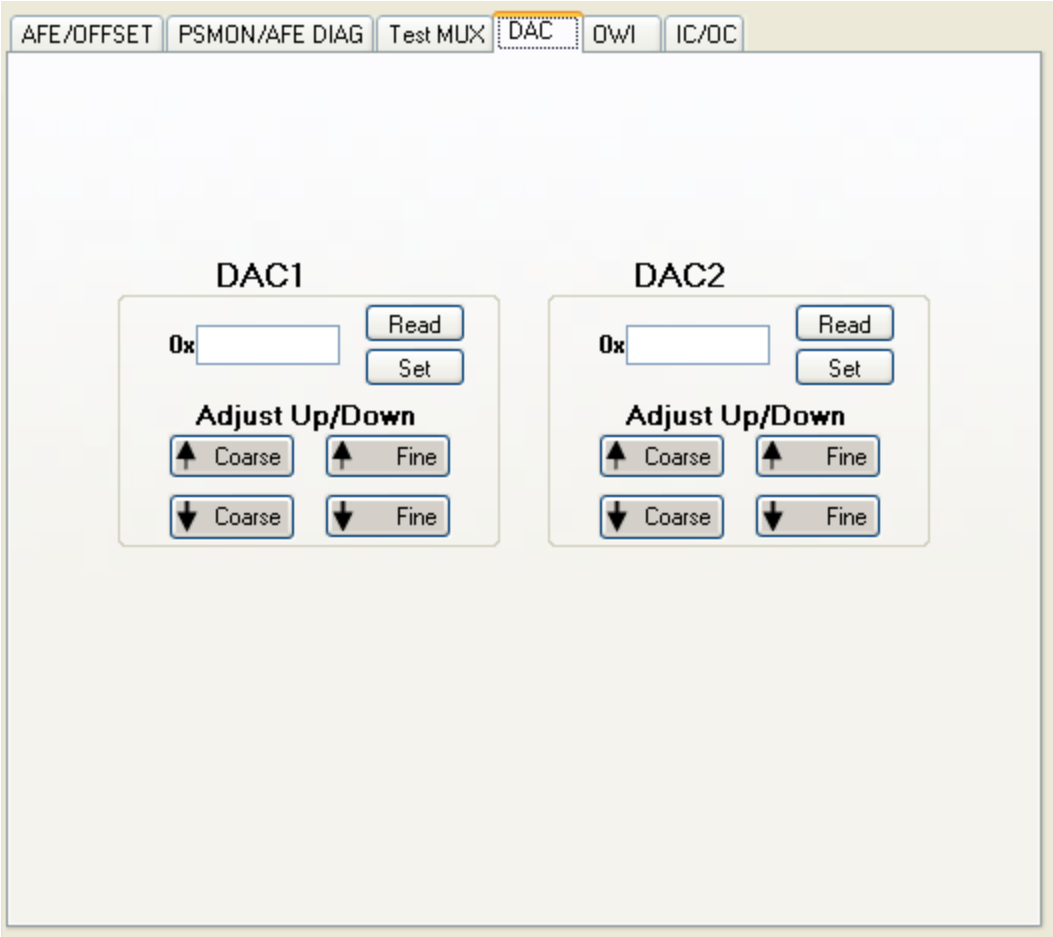


Figure 7-8. DAC Output Tab

7.5.1 DAC1 Output Read/Set

The *Read* and *Set* buttons in the DAC1 region can be used to directly enter in the desired DAC1 values. The buttons either read to or write from the DAC1 ESFRs 0xB7/0xB9.

7.5.2 DAC1 Output Adjust Up/Down

The ↑ *Coarse*, ↓ *Coarse*, ↑ *Fine*, and↓ *Fine* buttons are used to adjust the value of the DAC1 output register up or down in set increments. The buttons write to the DAC1 output bits in ESFRs 0xB7/0xB9. The fine adjustments move the DAC1 output value by one, while the coarse adjustments move the DAC1 output value by 50.

7.5.3 DAC2 Output Read/Set

The *Read* and *Set* buttons in the DAC2 region can be used to directly enter in the desired DAC2 values. The buttons either read to or write from the DAC2 ESFRs 0xBA/0xBB.

7.5.4 DAC2 Output Adjust Up/Down

The ↑ *Coarse*, ↓ *Coarse*, ↑ *Fine*, and↓ *Fine* buttons are used to adjust the value of the DAC2 output register up or down in set increments. The buttons write to the DAC2 output bits in ESFRs 0xBA/0xBB. The fine adjustments move the DAC2 output value by one, while the coarse adjustments move the DAC2 output value by 50.

7.6 OWI Tab

The *OWI* tab in the GUI is used to initialize the OWI communication interface in the PGA400-Q1 device along with perform direct OWI writes or reads. Figure 7-9 shows the *OWI* tab. The following sections describe the buttons on this tab.

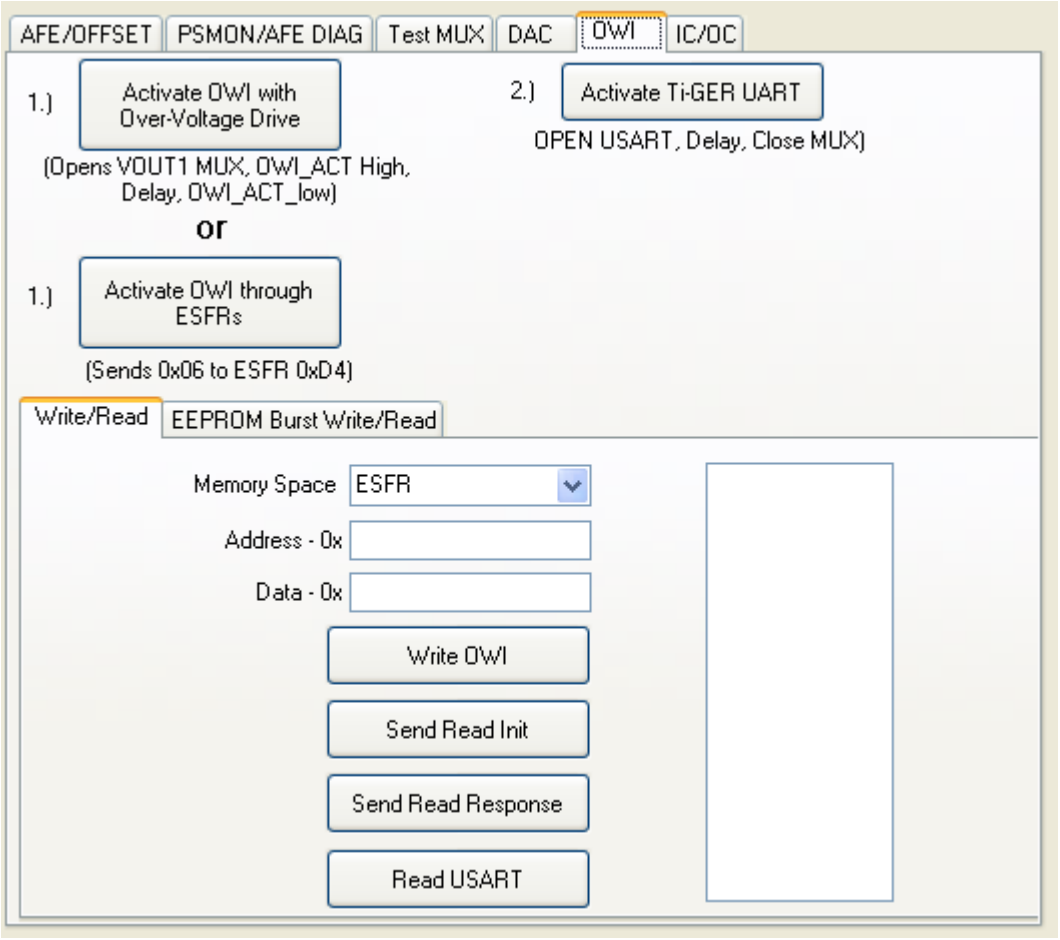


Figure 7-9. OWI GUI Tab

7.6.1 Activate OWI with Over-Voltage Drive

The *Activate OWI with Over-Voltage Drive* button on the GUI initializes the OWI activation circuit by controlling the signal that drives the Q4 BJT. Pressing the button disables the PGA400-Q1 output MUX and activates the 7.5-V pullup. The device waits about 200 ms and then releases the OWI pull-up. The 8051 MCU must be running and have code loaded into it that sends the signals to activate the OWI transceiver.

7.6.2 Activate OWI with ESFRs

The *Activate OWI with ESFRs* button activates the OWI transceiver by directly writing to ESFR 0xD4. After this button is pressed, the PGA400-Q1 device is in OWI mode and SPI commands will no longer work.

7.6.3 Activate TI-GER UART

The *Activate TI-GER UART* button initializes the UART hardware module in the TI-GER board in preparation for OWI communication.

7.6.4 Send Sync

The *Send Sync* button sends the required preliminary sync pulse to flush the contents of the OWI transceiver shift buffer.

7.6.5 Write/Read Tab

The bottom portion of the main OWI tab is divided between performing simple OWI writes and reads and performing OWI burst writes and reads. Figure 7-9 shows the *Write/Read* tab. The following sections describe the buttons on this tab.

7.6.5.1 Memory Space Selection Box

The currently selected memory space in the *Memory Space* selection box is used to form the correct packet when an OWI write or read is performed using the Write/Read buttons on the *Write/Read* tab.

7.6.5.2 Address Text Box

The *Address* text box is used to enter the address that the user desires to write or read from when using the write and read buttons.

7.6.5.3 Data Text Box

The *Data* text box is used to enter the data that the user desires to write or read from when using the write and read buttons.

7.6.5.4 Write OWI

The *Write OWI* button collects information from the *Memory Space* selection box, the *Address* text box, and the *Data* text box and then form the appropriate packet to write the data into the selected address in the correct memory space.

7.6.5.5 Send Read Init

The *Send Read Init* button collects information from the *Memory Space* selection box and the *Address* and then form the appropriate packet to send in the *Read Init* command when reading from a selected address in the correct memory space.

7.6.5.6 Send Read Response

The *Send Read Response* button sends the *Read Response* command to the PGA400-Q1 device that is be followed by the data that was requested in the *Read Init* command.

7.6.5.7 Read USART

The *Read USART* button reads out the contents of the TI-GER USART buffer. Data is shifted out of the FIFO buffer when the button is pressed and then displayed in the text box on the right side of the *Write/Read* tab. Because the OWI always works in loop-back mode, the results of any OWI writes can be seen by reading the USART after a write is performed.

7.6.6 EEPROM Burst Write/Read Tab

The second tab on the bottom portion of the OWI tab is the *EEPROM Burst Write/Read* tab. This tab is used to perform the EEPROM burst write and read commands that the PGA400-Q1 device supports. Figure 7-10 shows the *EEPROM Burst Write/Read* tab. The following sections describe the buttons on this tab.

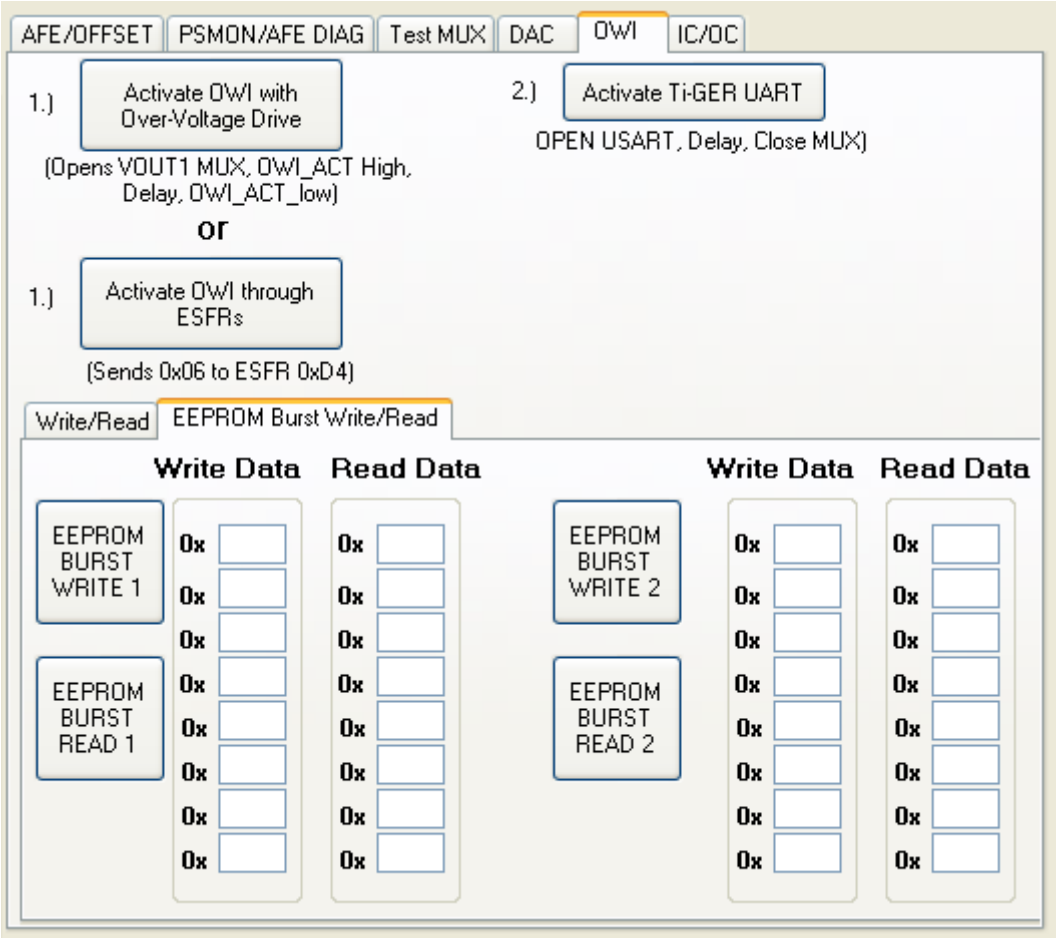


Figure 7-10. EEPROM Burst Write/Read Tab

7.6.6.1 EEPROM Burst Write 1

The *EEPROM BURST WRITE 1* button performs a burst write with the data that has been entered into the text boxes under the *Write Data* label on the left side of the tab.

7.6.6.2 EEPROM Burst Read 1

The *EEPROM BURST READ 1* button performs a burst read and then populate the data into the text boxes under the *Read Data* with the data that has been entered into the text boxes under the *Read Data* label on the left side of the tab.

7.6.6.3 EEPROM Burst Write 2

The *EEPROM BURST WRITE 2* button performs a burst write with the data that has been entered into the text boxes under the *Write Data* label on the right side of the tab.

7.6.6.4 EEPROM Burst Read 2

The *EEPROM BURST READ 2* button performs a burst read and then populate the data into the text boxes under the *Read Data* with the data that has been entered into the text boxes under the *Read Data* label on the right side of the tab.

7.7 IC/OC Tab

The *IC/OC* (input compare and output compare) tab on the GUI is used to read from and configure the input and output compare registers on the PGA400-Q1 device. The tab is broken into five main regions: Input Compare 1 (IC1), Input Compare 2 (IC2), Output Compare 1 (OC1), Output Compare 2 (OC2), and Free Running Timer. Figure 7-11 shows the *IC/OC* tab. The following sections describe the buttons on this tab.

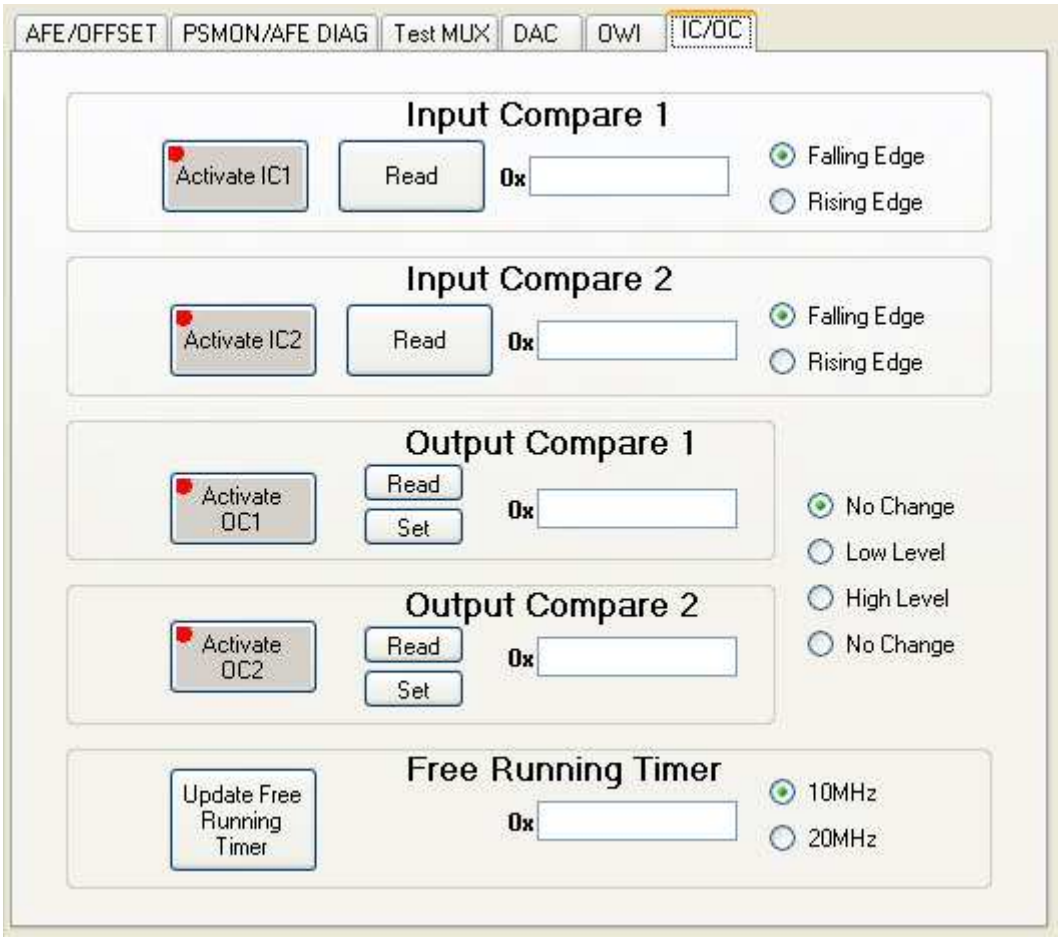


Figure 7-11. IC/OC GUI Tab

7.7.1 Input Compare 1 Region

The *Input Compare 1* region is used to activate and read from the Input Compare 1 peripheral in the PGA400-Q1 device.

7.7.1.1 Activate IC1

The *Activate IC1* button activates the Input Compare 1 function in the PGA400-Q1 device by controlling bit 0 of ESFR 0xC7.

7.7.1.2 Read IC1

The *Read* button in the IC1 region is used to update the text box with the contents of the input compare registers by reading ESFRs 0xC1 and 0xC2.

7.7.1.3 Falling/Rising Edge Selection Box

The *Falling/Rising Edge* selection box is used to change the polarity that the input compare peripheral uses by controlling bit 1 of ESFR 0xC0.

7.7.2 Input Compare 2 Region

The *Input Compare 2* region is used to activate and read from the Input Compare 2 peripheral in the PGA400-Q1.

7.7.2.1 Activate IC2

The *Activate IC2* button activates the Input Compare 2 function in the PGA400-Q1 device by controlling bit 1 of ESFR 0xC7.

7.7.2.2 Read IC2

The *Read* button in the IC2 region is used to update the text box with the contents of the input compare registers by reading ESFRs 0xC3 and 0xC4.

7.7.2.3 Falling/Rising Edge Selection Box

The *Falling/Rising Edge* selection box is used to change the polarity that the input compare peripheral uses by controlling bit 2 of ESFR 0xC0.

7.7.3 Output Compare 1 Region

The *Output Compare 1* region is used to activate and set/read the Output Compare 1 peripheral in the PGA400-Q1.

7.7.3.1 Activate OC1

The *Activate OC1* button activates the Output Compare 1 function in the PGA400-Q1 device by controlling bit 2 of ESFR 0xC7.

7.7.3.2 Read OC1

The *Read* button in the OC1 region is used to update the text box with the contents of the output compare registers by reading ESFRs 0xC5 and 0xC6.

7.7.3.3 Set OC1

The *Set* button in the OC1 region is used to set the value in the Output Compare 1 register by writing to ESFR 0xC5 and 0xC6.

7.7.4 Output Compare 2 Region

The *Output Compare 2* region is used to activate and set and read the Output Compare 2 peripheral in the PGA400-Q1.

7.7.4.1 Activate OC2

The *Activate OC2* button activates the Output Compare 2 function in the PGA400-Q1 device by controlling bit 3 of ESFR 0xC7.

7.7.4.2 Read OC2

The *Read* button in the OC2 region is used to update the text box with the contents of the output compare registers by reading ESFRs 0xC9 and 0xCA.

7.7.4.3 Set OC2

The *Set* button in the OC2 region is used to set the value in the Output Compare 2 register by writing to ESFR 0xC9 and 0xCA.

7.7.5 No Change / Low Level / High Level Selection Box

The *No Change / Low Level / High Level* selection box is used to control the level that both the OC1 and OC2 peripherals use for the output compare functions. This control is achieved by controlling bits 3 and 4 of ESFR 0xC0.

7.7.6 Free Running Timer Region

The *Free Running Timer* region of the *IC/OC* tab is used to monitor the Free Running Timer in the PGA400-Q1.

7.7.6.1 Update Free Running Timer

The *Update Free Running Timer* button is used to populate the text box in the *Free Running Timer* region with the contents of the PGA400-Q1 Free Running Timer.

7.7.6.2 10MHz / 20MHz Selection Box

The *10MHz / 20MHz* selection box is used to select between a 10-MHz and 20-MHz Free Running Timer inside the PGA400-Q1 device by controlling bit 0 of ESFR 0xC0.

PGA400-Q1 EVM Schematics and Layout Drawings

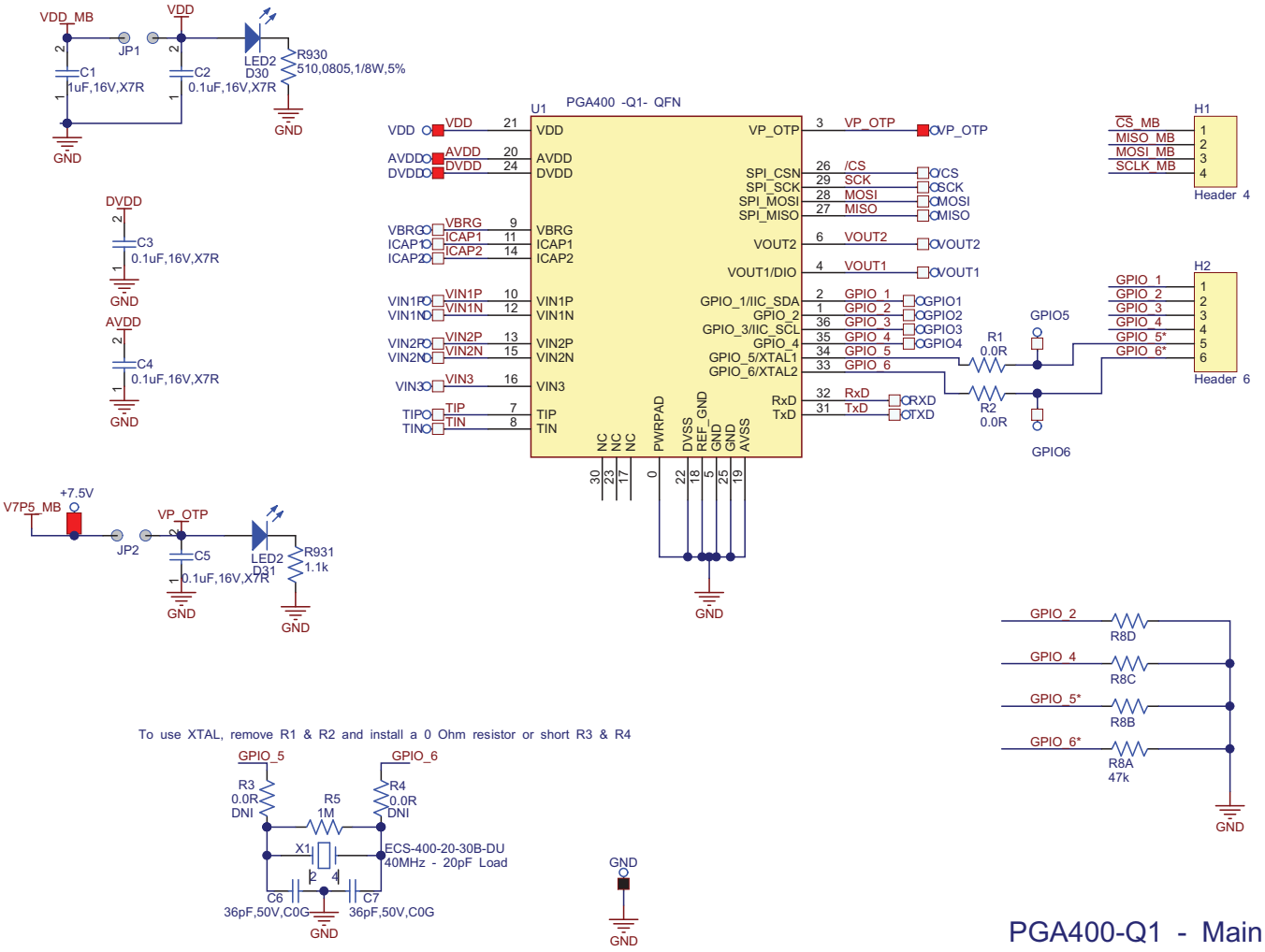


Figure 8-1.

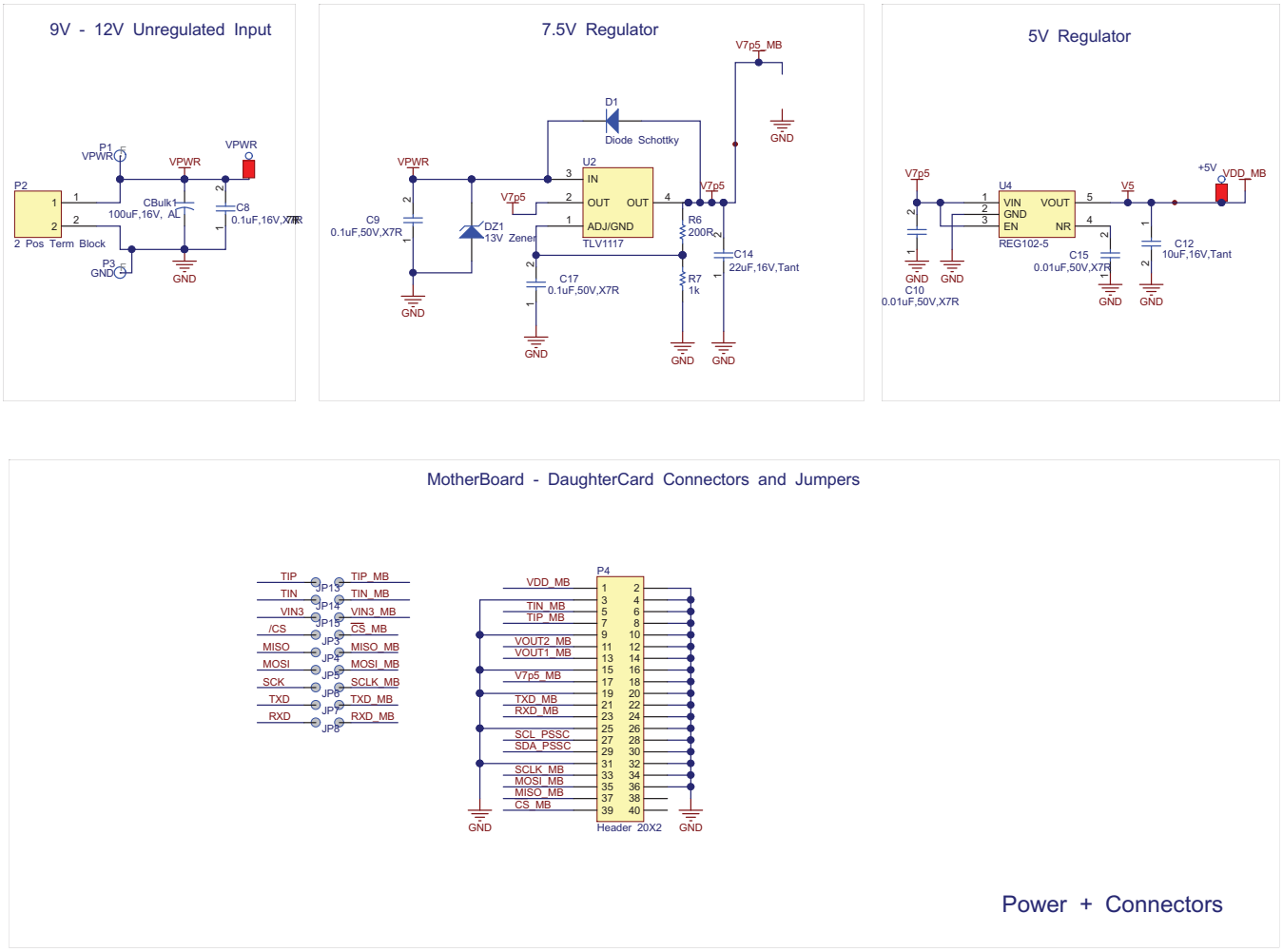


Figure 8-2.

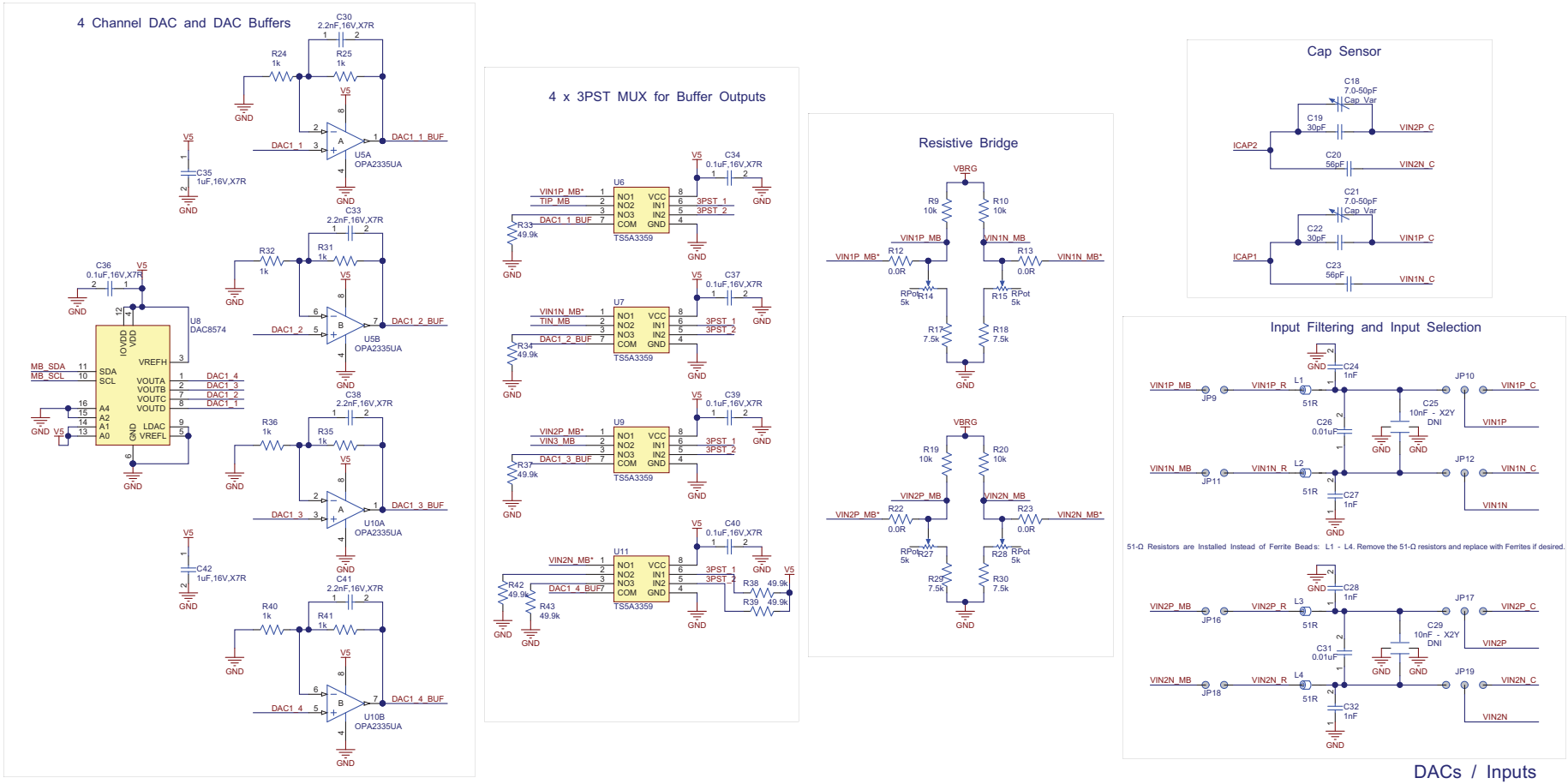


Figure 8-3.

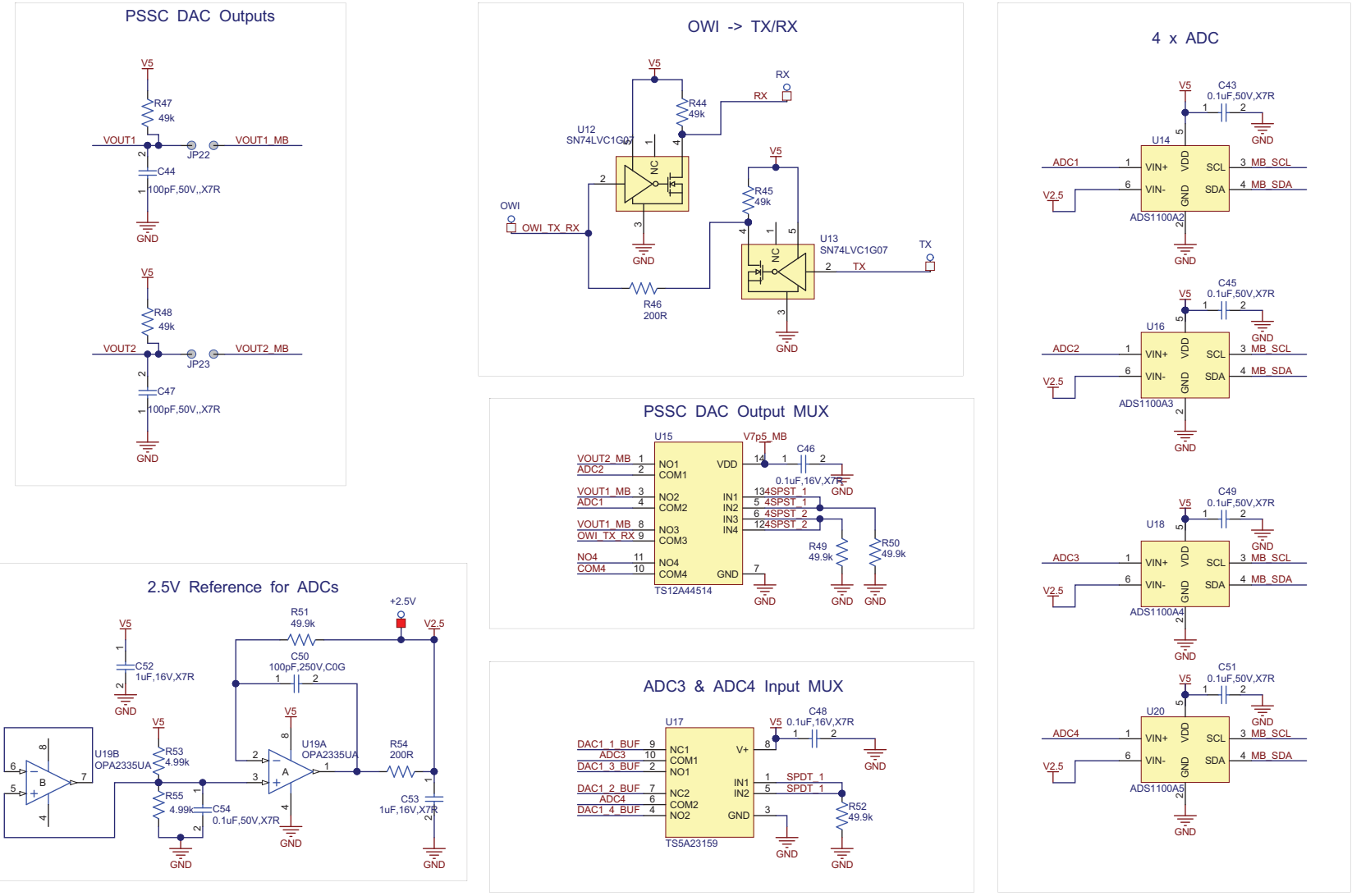


Figure 8-4.

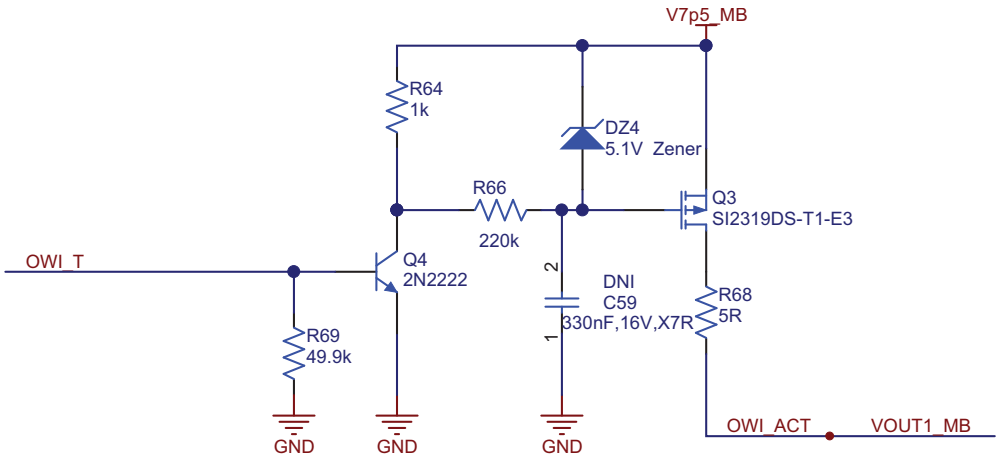


Figure 8-5.

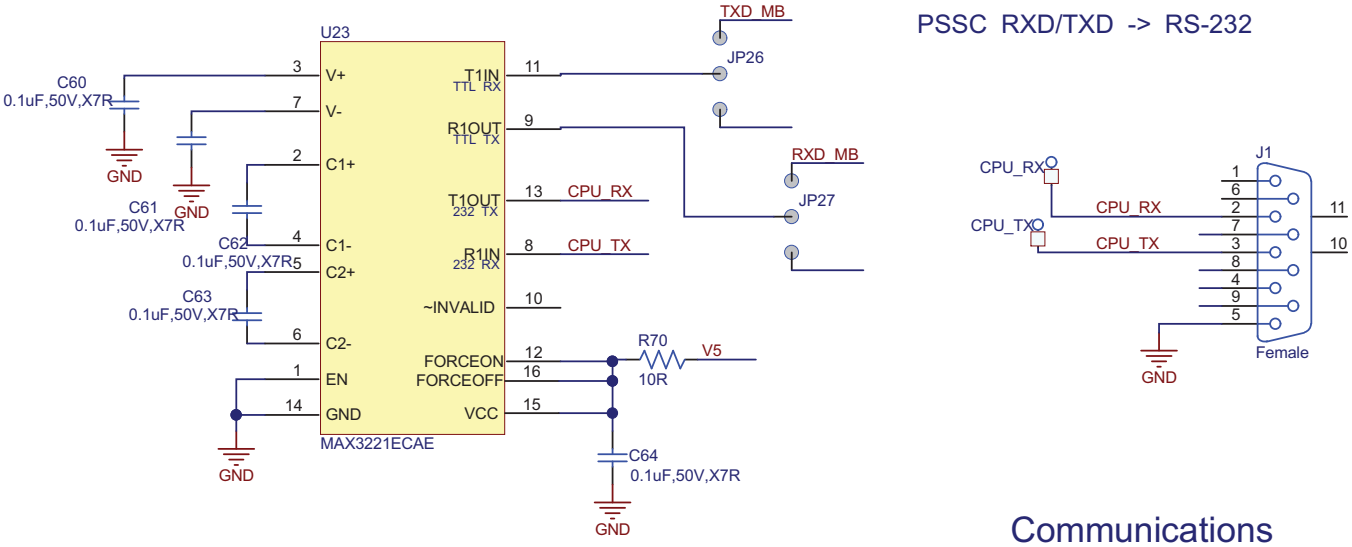


Figure 8-6.

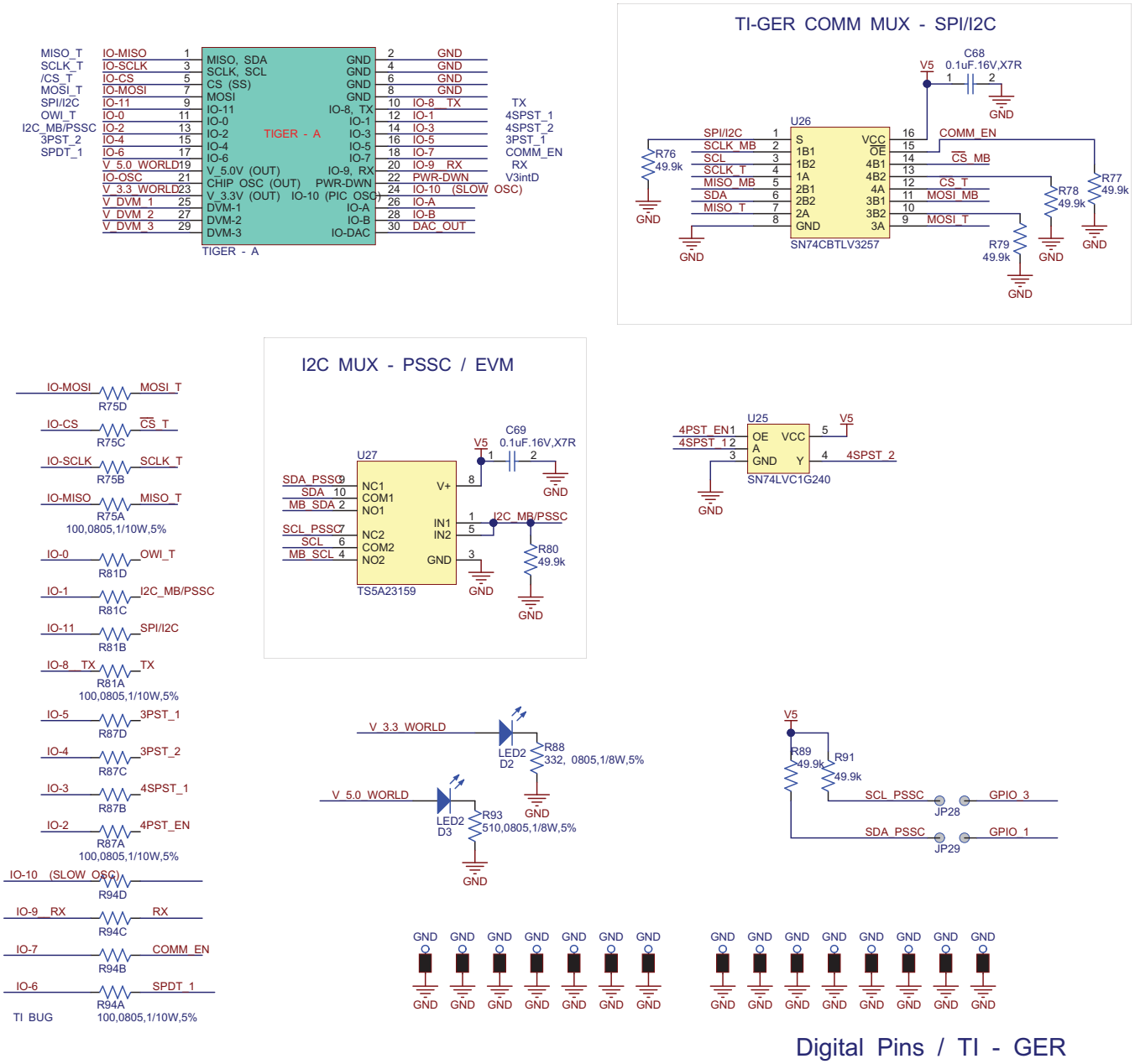


Figure 8-7.

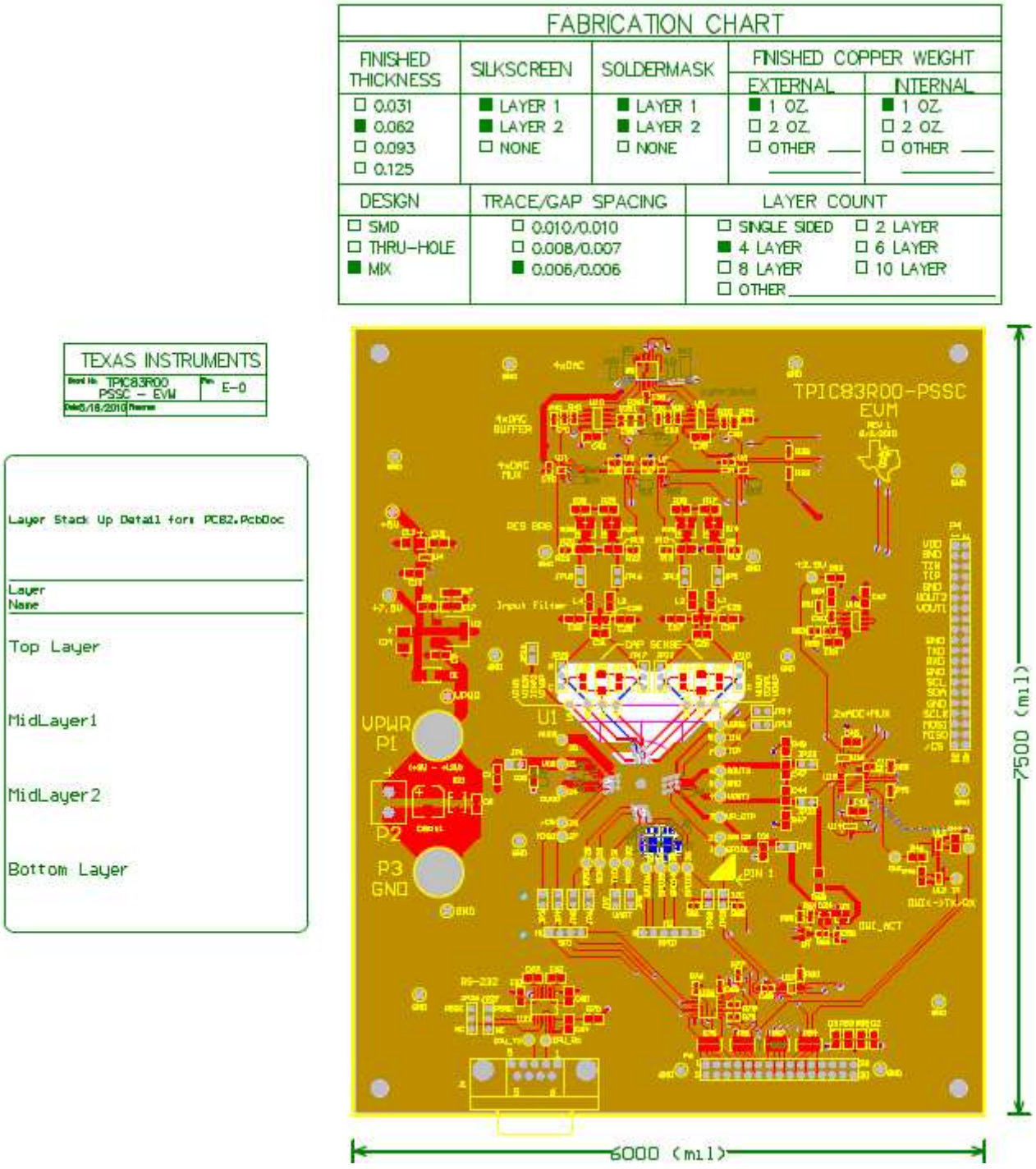


Figure 8-8.

Revision History

Changes from Original (March 2012) to A Revision	Page
• Deleted Reference to the *Chapter 8: Controlling the EVM peripherals with the GUI* section	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

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2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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