MAX40100

Precision, Low-Power and Low-Noise Op Amp with RRIO

General Description

The MAX40100 is a low-power, zero-drift operational amplifier available in a space-saving, 6-bump, wafer-level package (WLP).

Designed for use in portable consumer, medical, and industrial applications, the MAX40100 features rail-to-rail CMOS inputs and outputs, a 1.5MHz GBW at just 66µA supply current, and 10µV (max) “zero-drift” input voltage offset over time and temperature.

The zero-drift feature of the MAX40100 reduces the high 1/f noise typically found in CMOS input operational amplifiers, making it useful for a wide variety of low-frequency measurement applications.

The MAX40100 is available in a space-saving, 1.1 x 0.76mm, 6-bump WLP, with 0.35mm bump pitch.

The MAX40100 is specified over the -40°C to +125°C extended automotive operating temperature range.

Applications

- Cell Phones
- Sensor Interfaces
- Loop-Powered Systems
- Portable Medical Devices
- Battery-Powered Devices

Benefits and Features

- Low 66µA Quiescent Current
- Low Input Noise:
  - 42nV/√Hz @ 1kHz
  - 0.42µV$_{PP}$ from 0.1Hz to 10Hz
- Rail-to-Rail Inputs and Outputs (RRIO)
- 1.5MHz GBW
- Ultra-Low 10pA Input Bias Current
- Single 1.6V to 5.5V Supply Voltage Range
- Unity Gain Stable
- Power-Saving Shutdown Mode
- Tiny 1.1mm x 0.76mm 6-bump WLP

Ordering Information ***appears at end of data sheet.***

19-8539; Rev 0; 5/16

maxim integrated™

Absolute Maximum Ratings

Supply Voltage, $\overline{SHDN}$ (V_{DD} to GND) .....-0.3V to +6V
IN+, IN-, OUT .....(GND - 0.3V) to (V_{DD} + 0.3V)
Short-Circuit Duration to Either Supply Rail,
OUT, OUTA, OUTB 10s
Continuous Input Current (Any Pins) .....±20mA
Continuous Power Dissipation (T_A = +70°C)
6-bump WLP (Derate 10.19mW/°C above +70°C) 816mW

Package Thermal Characteristics (multilayer board)
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....98.06°C/W
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range.....-65ºC to +150°C
Lead Temperature (soldering 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{DD}	Guaranteed by PSRR, 0°C ≤ T_A ≤ +70°C		1.6		5.5	V
		Guaranteed by PSRR, -40°C ≤ T_A ≤ +125°C		1.8		5.5	
Quiescent Supply Current	I_{DD}	T_A =+25°C			66	92	µA
		-40°C ≤ T_A ≤ +125°C				124	
Power-Supply Rejection Ratio	PSRR	V_{DD} = 1.8V to 5.5V	T_A =+25°C	116	135		dB
			-40°C ≤ T_A ≤ +125°C	107			
		0°C ≤ T_A ≤ +70°C, V_{DD} = 1.6V to 5.5V		107			
Power-Up Time	t_{ON}	V_{DD} = 0 to 3V step, A_V = 1V/V			20		µs
Shutdown Supply Current	$I_{\overline{SHDN}}$					300	nA
Turn-On Time from Shutdown	t_{OSD}	V_{DD} = 3.3V, $V_{\overline{SHDN}}$ = 0 to 3.3V step in < 1µs			50		µs
DC SPECIFICATIONS							
Input Offset Voltage	V_{OS}	T_A = +25°C			0.8	10	µV
		-40°C ≤ T_A ≤ +125°C				25	
Input Offset Voltage Drift	ΔV_{OS}				5		nV/°C
Input Bias Current (Note 3)	I_B	T_A = +25°C			±0.031	±0.160	mA
		-40°C ≤ T_A ≤ +85°C				±4.6	
		-40°C ≤ T_A ≤ +125°C				±28	
Input Offset Current	I_{OS}				±0.005		
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	T_A = +25°C	-0.1		V_{DD} + 0.1	V
			-40°C ≤ T_A ≤ +125°C	-0.1		V_{DD} + 0.05	

Electrical Characteristics (continued)

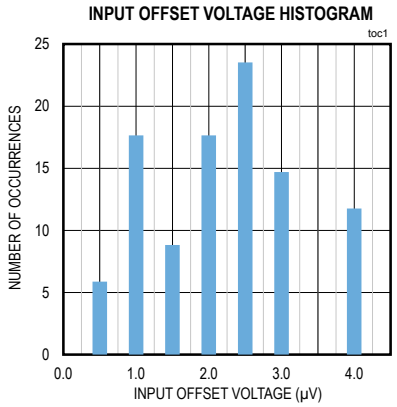
(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C) (Note 2)

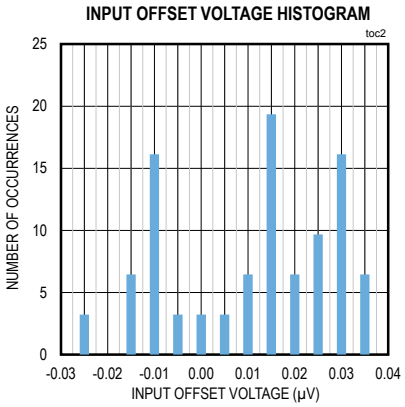
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	-0.1 ≤ V_{CM} ≤ V_{DD} + 0.1, T_A = +25°C		122	135		dB
		-0.1 ≤ V_{CM} ≤ V_{DD} + 0.05, -40°C ≤ T_A ≤ +125°C		116			
Open-Loop Gain	AV_{OL}	20mV ≤ V_{OUT} ≤ V_{DD} - 20mV, R_L = 100kΩ to V_{DD}/2		120	138		dB
		150mV ≤ V_{OUT} ≤ V_{DD} - 150mV, R_L = 5kΩ to V_{DD}/2		123	160		
Input Resistance	R_{IN}	Differential			50		MΩ
		Common-mode			200		
Output Voltage Swing	V_{OH}	V_{DD} - V_{OUT}	R_L = 100kΩ to V_{DD}/2			12	mV
			R_L = 50kΩ to V_{DD}/2			22	
			R_L = 600Ω to V_{DD}/2		50		
	V_{OL}	V_{OUT}	R_L =100kΩ to V_{DD}/2			11	
			R_L =50kΩ to V_{DD}/2			18	
			R_L =600Ω to V_{DD}/2		50		
Short-Circuit Current	I_{SC}				50		mA
AC SPECIFICATIONS							
Gain-Bandwidth Product	GBWP				1.5		MHz
Slew Rate	SR	0 ≤ V_{OUT} ≤ 2V			0.7		V/µs
Input Voltage Noise Density	En	f_{SW} = 1kHz			42		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f_{SW} ≤ 10Hz			0.42		$µV_{PP}$
Input Current Noise Density		f_{SW} = 1kHz			100		f_A/√Hz
Phase Margin		C_L = 20pF			60		°C
Capacitive Loading	C_L	No sustained oscillation, A_V = 1V/V			400		pF
LOGIC INPUT							
Shutdown Input Low	V_{IL}					0.5	V
Shutdown Input High	V_{IH}			1.3			V
Shutdown Input Leakage Current	I_{IL}/I_{IH}					100	nA

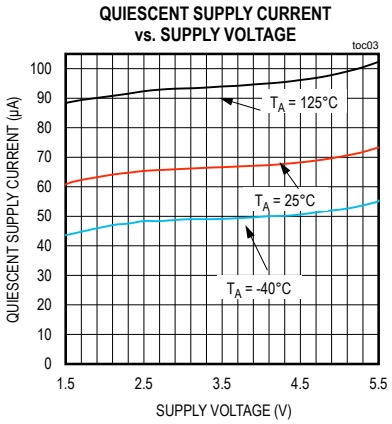
Note 2: Specifications are 100% tested at T_A = +25°C (exceptions noted). All temperature limits are guaranteed by design.
Note 3: Guaranteed by design.

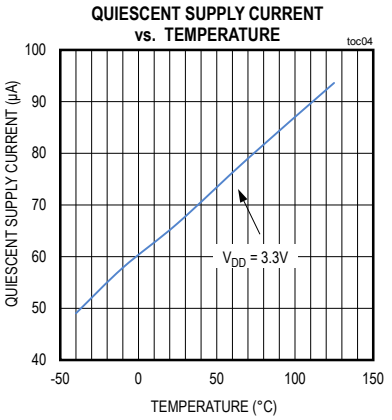
Typical Operating Characteristics

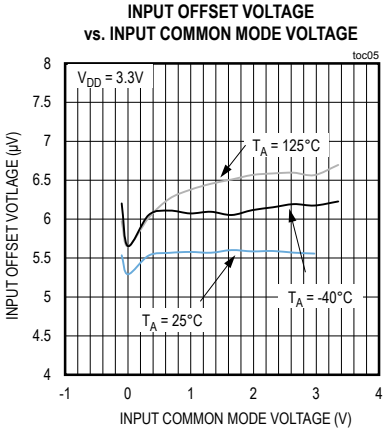
(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C)

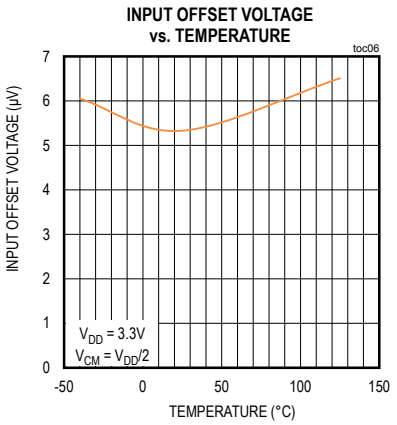






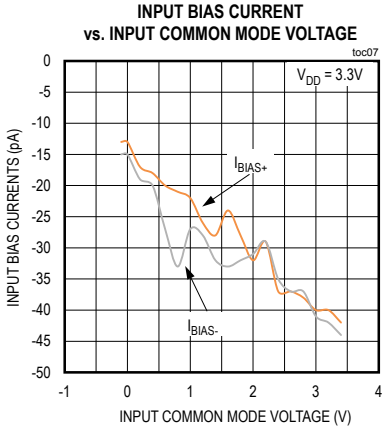


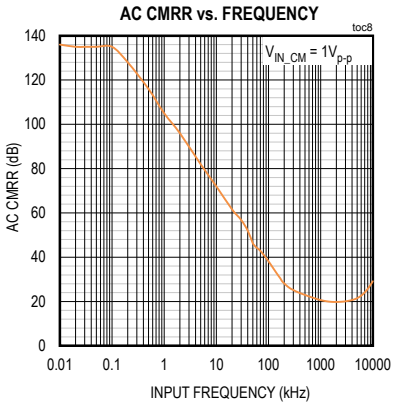


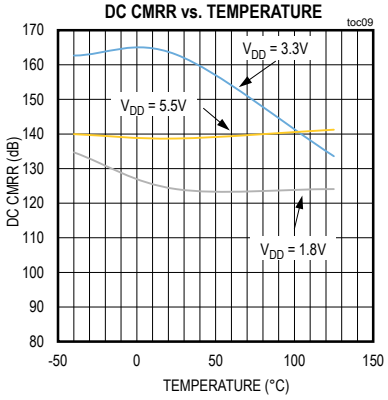


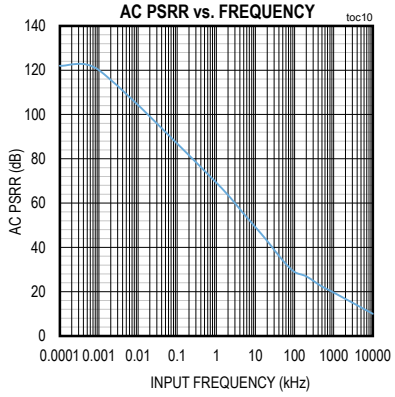
Typical Operating Characteristics (continued)

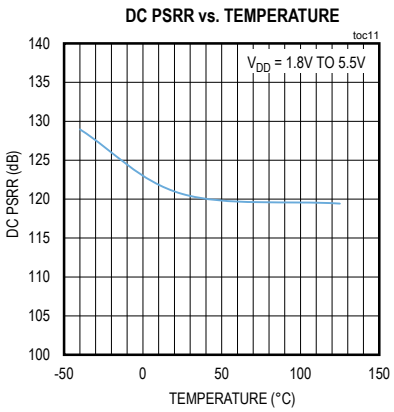
(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C)

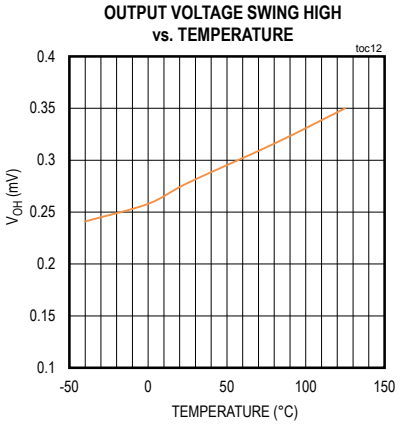








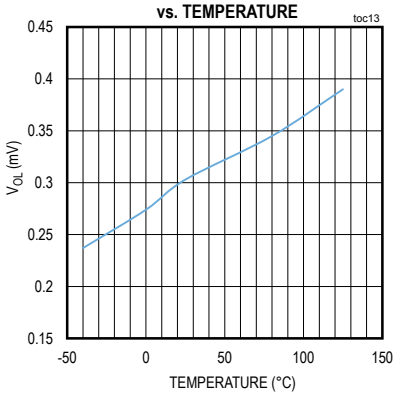




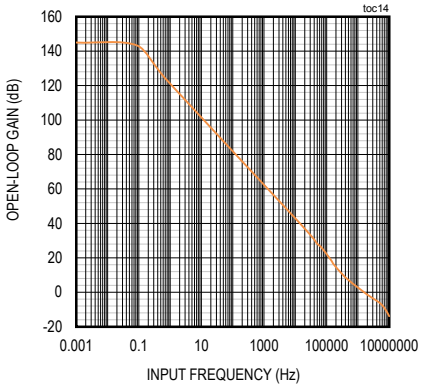
Typical Operating Characteristics

(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C)

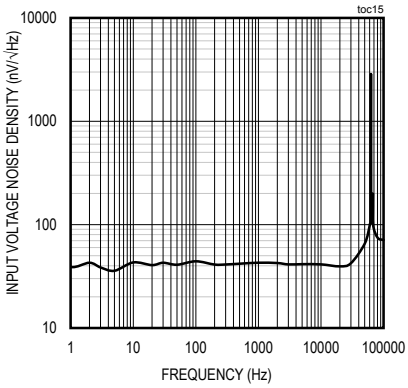
OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



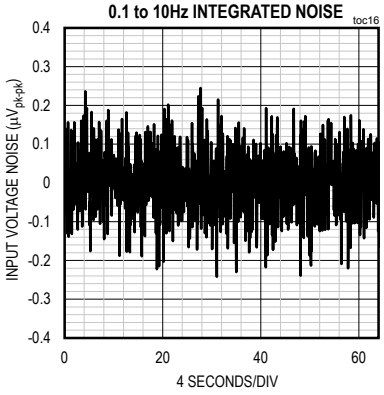
OPEN-LOOP GAIN vs. FREQUENCY



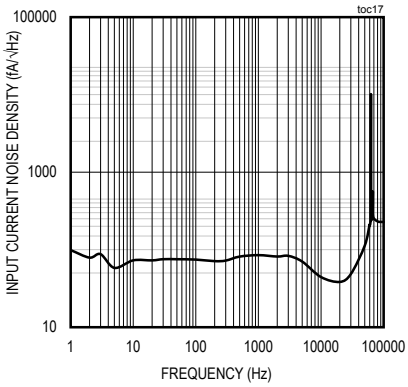
INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



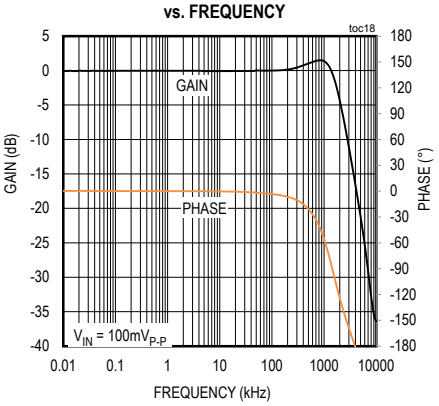
0.1 to 10Hz INTEGRATED NOISE



INPUT CURRENT NOISE DENSITY vs. FREQUENCY



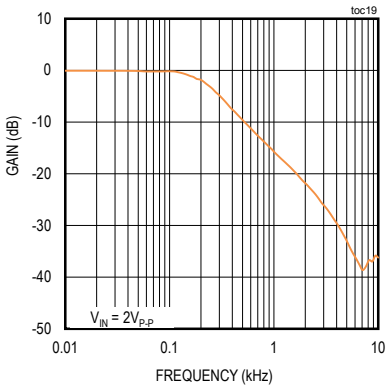
SMALL SIGNAL GAIN & PHASE vs. FREQUENCY



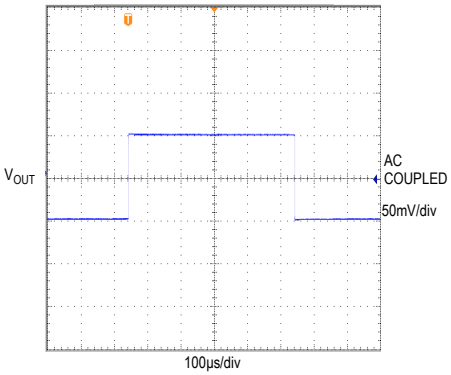
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, GND = 0, A_V = 1V/V, V_{OUT} = V_{DD}/2, C_L = 20pF, R_L = 100kΩ to V_{DD}/2, $V_{\overline{SHDN}}$ = V_{DD}, T_A = -40°C to +125°C unless otherwise noted. Typical values are at +25°C)

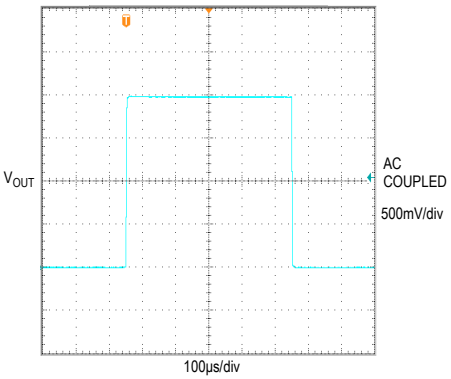
LARGE SIGNAL GAIN vs. FREQUENCY



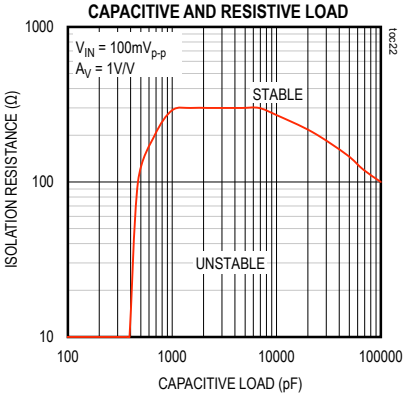
SMALL SIGNAL STEP RESPONSE vs. TIME



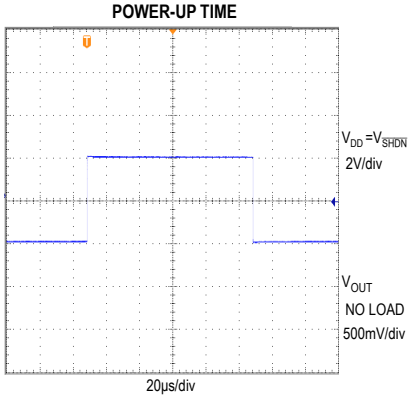
LARGE SIGNAL STEP RESPONSE vs. TIME



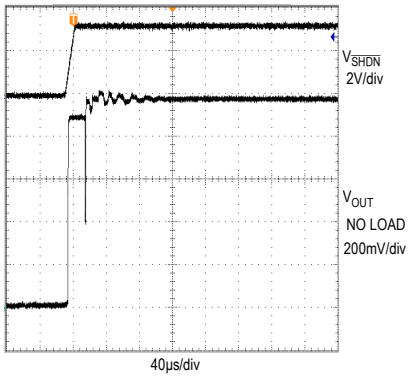
STABILITY vs.
CAPACITIVE AND RESISTIVE LOAD



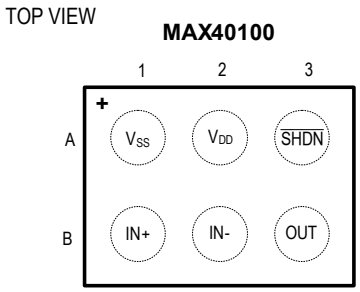
POWER-UP TIME



SHUTDOWN ENABLE RESPONSE



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	V_{SS}	Negative Supply Voltage
A2	V_{DD}	Positive Supply Voltage. Bypass to GND with a 0.1µF capacitor.
A3	$\overline{SHDN}$	Shutdown. Pull shutdown to V_{SS} to activate shutdown mode.
B1	IN+	Positive Input
B2	IN-	Negative Input
B3	OUT	Output

Detailed Description

The MAX40100 is a precision, low-power op-amps ideal for signal processing applications. This device use an innovative auto-zero technique that allows precision and low-noise with a minimum amount of power. The low input offset voltage, CMOS inputs, and the absence of 1/f noise allows for optimization of active-filter designs.

The MAX40100 achieves rail-to-rail performance at the input through the use of a low-noise charge pump. This ensures a glitch-free common-mode input voltage range extending from the negative supply rail up to the positive supply rail, eliminating cross over distortion common to traditional N-channel/P-channel CMOS pair inputs, reducing harmonic distortion at the output.

The device features a shutdown mode that greatly reduces quiescent current while the device is not operational.

Auto-Zero

The MAX40100 features an auto-zero circuit that allows the device to achieve less than 10µV of input offset voltage and eliminates the 1/f noise.

Internal Charge Pump

An internal charge pump provides an internal supply typically 1V beyond the upper rail. This internal rail allows the MAX40100 to achieve true rail-to-rail inputs and outputs, while providing excellent common-mode rejection, power-supply rejection ratios, and gain linearity.

The charge pump requires no external components, and in most applications is entirely transparent to the user. The operating frequency is well beyond the unity-gain frequency of the amplifier, avoiding aliasing or other signal integrity issues in sensitive applications.

Shutdown Operation

The device features an active-low shutdown mode that lowers the quiescent current to less than 1µA. In shutdown mode the inputs and output are high impedance. This allows multiple devices to be multiplexed onto a single line without the use of external buffers. Pull $\overline{SHDN}$ high for normal operation.

The shutdown high (V_{IH}) and low (V_{IL}) threshold voltages are designed for ease of integration with digital controls like microcontroller outputs. These thresholds are independent of supply, eliminating the need for external pulldown circuitry.

Applications Information

The MAX40100 low-power, low-noise and precision operational amplifiers designed for applications in the portable medical, such as ECG and Pulse Oximetry, portable consumer and industrial markets.

The MAX40100 is also ideal for loop-powered systems that interface with pressure sensors or strain-gauges.

Capacitive Load Stability

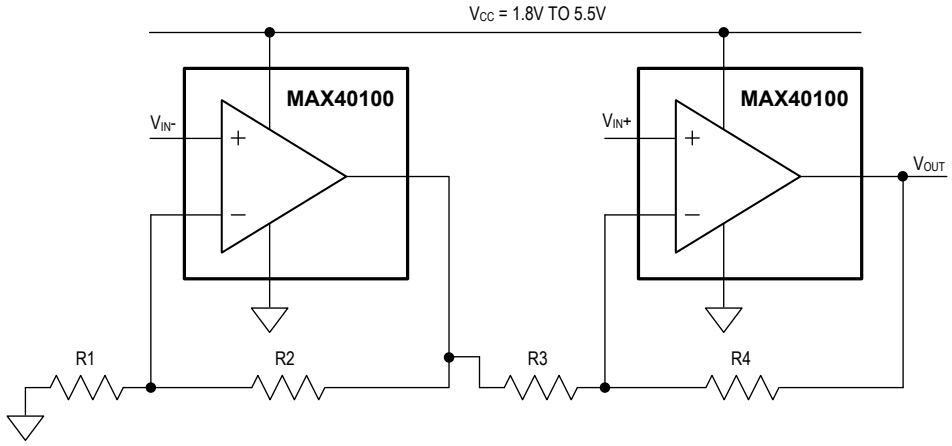
Driving large capacitive loads can cause instability in many op-amps. MAX40100 is stable with capacitive loads up to 400pF. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. The graph in the *Typical Operating Characteristics* gives the stable operation region for capacitive load versus isolation resistors.

Power Supplies and Layout

The MAX40100 operate either with a single supply from +1.6V to +5.5V with respect to ground or with dual supplies from ±0.8V to ±2.75V. When used with dual supplies, bypass both supplies with their own 0.1µF capacitor to ground. When used with a single supply, bypass V_{DD} with a 0.1µF capacitor to ground.

Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

Typical Application Circuit



HIGH INPUT IMPEDANCE 2-OP AMP INSTRUMENTATION AMPLIFIER
IF R1 = R4, R2 = R3, $V_{OUT} = (V_{IN+} - V_{IN-}) X (1 + R4/R3)$
R1, R2, R3, R4 ARE LOWER TOLERANCE (0.01%) FOR BETTER CMRR PERFORMANCE

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX40100ANT+	-40°C to +125°C	6-bump WLP

+Denotes lead(Pb)-free/RoHS compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6-bump WLP	N60D1+1	**21-100086**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/16	Initial release	—