

FEATURES**Fixed gain of 20 dB****Operation from 20 MHz to 1.0 GHz****Input and output internally matched to 50 Ω** **Integrated bias control circuit****OIP3****45.0 dBm at 190 MHz****49.0 dBm at 380 MHz****Noise figure****2.6 dB at 190 MHz****2.7 dB at 380 MHz****P1dB of 19.6 dBm at 190 MHz****Single 5 V power supply****Low quiescent current of 105 mA****MSL-1 rated SOT-89 package****ESD rating of ± 2 kV (Class 2)****Pin-compatible with the 16 dB gain [ADL5535](#)****GENERAL DESCRIPTION**

The [ADL5536](#) is a 20 dB linear amplifier that operates at frequencies up to 1 GHz. The device can be used in a wide variety of cellular, CATV, military, and instrumentation equipment.

The [ADL5536](#) provides the highest dynamic range available from an internally matched IF gain block. This is accomplished by providing extremely low noise figures and very high OIP3 specifications simultaneously across the entire 1 GHz frequency range. The [ADL5536](#) also provides extremely flat gain and P1dB over frequency, which are stable over temperature, power supply, and from device to device.

The device is internally matched to 50 Ω at the input and output, making the [ADL5536](#) very easy to implement in a wide variety of applications. Only input/output ac coupling capacitors, power supply decoupling capacitors, and an external inductor are required for operation.

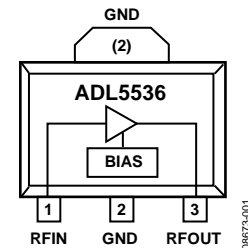
FUNCTIONAL BLOCK DIAGRAM

Figure 1.

The [ADL5536](#) is fabricated on a GaAs HBT process and has an ESD rating of ± 2 kV (Class 2). The device is assembled in an MSL-1 rated SOT-89 package that uses an exposed paddle for excellent thermal impedance.

The [ADL5536](#) consumes only 105 mA on a single 5 V supply and is fully specified for operation from -40°C to $+85^{\circ}\text{C}$.

The [ADL5536](#) is also pin-compatible with the 16 dB gain [ADL5535](#). Fully populated evaluation boards are available for each amplifier.

Rev. A**Document Feedback**

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- ADL5536 Evaluation Board

[Documentation](#)

Application Notes

- AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers
- Broadband Biasing of Amplifiers General Application Note
- MMIC Amplifier Biasing Procedure Application Note
- Thermal Management for Surface Mount Components General Application Note

Data Sheet

- ADL5536: 20 MHz to 1.0 GHz IF Gain Block Data Sheet

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- ADI RF Amplifier Library for Agilent ADS
- ADIsimPLL™
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TABLE OF CONTENTS

Features	1	Basic Connections	11
Functional Block Diagram	1	Soldering Information and Recommended PCB Land Pattern	11
General Description	1	ACPR Performance	12
Revision History	2	Error Vector Magnitude (EVM) Performance	12
Specifications.....	3	Evaluation Board	13
Typical Scattering Parameters (S-Parameters)	5	Outline Dimensions	14
Absolute Maximum Ratings.....	6	Ordering Guide	14
ESD Caution.....	6		
Pin Configuration and Function Descriptions.....	7		
Typical Performance Characteristics	8		

REVISION HISTORY

11/13—Rev. 0 to Rev. A

Added Figure 15, Renumbered Sequentially	10
Changes to Figure 17.....	11
Updated Outline Dimensions	14

4/10—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		20		1000	MHz
FREQUENCY = 20 MHz					
Gain			20.2		dB
Output 1 dB Compression Point (P1dB)			18.0		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1\text{ MHz}$, output power (P_{OUT}) = 3 dBm per tone		39.5		dBm
Second Harmonic	$P_{OUT} = 0\text{ dBm}$		-59.2		dBc
Third Harmonic	$P_{OUT} = 0\text{ dBm}$		-89.1		dBc
Noise Figure			2.5		dB
FREQUENCY = 70 MHz					
Gain			20.1		dB
vs. Frequency	$\pm 50\text{ MHz}$		± 0.10		dB
vs. Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.20		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.07		dB
Output 1 dB Compression Point (P1dB)			19.6		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1\text{ MHz}$, output power (P_{OUT}) = 3 dBm per tone		41.0		dBm
Second Harmonic	$P_{OUT} = 0\text{ dBm}$		-63		dBc
Third Harmonic	$P_{OUT} = 0\text{ dBm}$		-88		dBc
Noise Figure			2.4		dB
FREQUENCY = 190 MHz					
Gain		18.8	19.8	20.8	dB
vs. Frequency	$\pm 50\text{ MHz}$		± 0.06		dB
vs. Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.19		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.07		dB
Output 1 dB Compression Point (P1dB)		18.6	19.6		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1\text{ MHz}$, output power (P_{OUT}) = 3 dBm per tone		45.0		dBm
Second Harmonic	$P_{OUT} = 0\text{ dBm}$		-59.6		dBc
Third Harmonic	$P_{OUT} = 0\text{ dBm}$		-90.4		dBc
Noise Figure			2.6		dB
FREQUENCY = 380 MHz					
Gain		18.4	19.4	20.4	dB
vs. Frequency	$\pm 50\text{ MHz}$		± 0.10		dB
vs. Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.20		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.08		dB
Output 1 dB Compression Point (P1dB)		18.7	19.7		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1\text{ MHz}$, output power (P_{OUT}) = 3 dBm per tone		49.0		dBm
Second Harmonic	$P_{OUT} = 0\text{ dBm}$		-61.4		dBc
Third Harmonic	$P_{OUT} = 0\text{ dBm}$		-77.2		dBc
Noise Figure			2.7		dB
FREQUENCY = 748 MHz					
Gain			18.5		dB
vs. Frequency	$\pm 50\text{ MHz}$		± 0.14		dB
vs. Temperature	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		± 0.23		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.09		dB
Output 1 dB Compression Point (P1dB)			19.7		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1\text{ MHz}$, output power (P_{OUT}) = 3 dBm per tone		42.5		dBm
Second Harmonic	$P_{OUT} = 0\text{ dBm}$		-53.2		dBc
Third Harmonic	$P_{OUT} = 0\text{ dBm}$		-70.7		dBc
Noise Figure			2.7		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY = 900 MHz					
Gain			18.5		dB
vs. Frequency	± 50 MHz		± 0.14		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.23		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.10		dB
Output 1 dB Compression Point (P1dB)			19.9		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1$ MHz, output power (P_{OUT}) = 3 dBm per tone		41.5		dBm
Second Harmonic	$P_{\text{OUT}} = 0$ dBm		-64.9		dBc
Third Harmonic	$P_{\text{OUT}} = 0$ dBm		-68		dBc
Noise Figure			2.7		dB
FREQUENCY = 1000 MHz					
Gain			18.1		dB
vs. Frequency	± 50 MHz		± 0.14		dB
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 0.23		dB
vs. Supply Voltage	4.75 V to 5.25 V		± 0.10		dB
Output 1 dB Compression Point (P1dB)			19.7		dBm
Output Third-Order Intercept (OIP3)	$\Delta f = 1$ MHz, output power (P_{OUT}) = 3 dBm per tone		40.5		dBm
Second Harmonic	$P_{\text{OUT}} = 0$ dBm		-54.8		dBc
Third Harmonic	$P_{\text{OUT}} = 0$ dBm		-66.6		dBc
Noise Figure			2.8		dB
POWER INTERFACE					
Supply Voltage (V_{CC})		4.5	5.0	5.5	V
Supply Current			105	122	mA
vs. Temperature	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$		± 2.0		mA
Power Dissipation	$V_{\text{CC}} = 5$ V		0.53		W

TYPICAL SCATTERING PARAMETERS (S-PARAMETERS)

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, and the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

Frequency (MHz)	S11		S21		S12		S22	
	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
20	-14.53	-120.58	20.45	171.91	-22.63	+7.79	-16.26	-139.94
70	-19.07	-156.59	20.01	172.48	-22.66	+0.45	-16.29	-164.26
120	-19.61	-160.48	19.91	169.98	-22.65	-1.59	-16.26	-166.95
190	-19.62	-159.92	19.84	165.55	-22.64	-3.78	-16.06	-165.90
240	-19.43	-157.66	19.77	162.37	-22.63	-5.22	-15.84	-164.33
290	-19.04	-155.64	19.74	159.05	-22.62	-6.64	-15.58	-162.72
340	-18.78	-153.97	19.65	155.59	-22.62	-7.93	-15.28	-161.62
390	-18.37	-150.66	19.54	152.48	-22.59	-9.34	-14.97	-159.87
440	-17.83	-149.87	19.50	149.29	-22.57	-10.74	-14.53	-158.25
490	-17.32	-149.82	19.41	146.05	-22.61	-12.05	-14.14	-158.63
540	-16.88	-149.59	19.34	142.73	-22.61	-13.36	-13.80	-158.50
590	-16.51	-148.73	19.22	139.62	-22.59	-14.66	-13.47	-158.24
640	-16.06	-148.92	19.14	136.53	-22.59	-16.00	-13.12	-158.50
690	-15.72	-149.26	19.04	133.27	-22.59	-17.30	-12.80	-158.89
740	-15.37	-149.29	18.92	130.33	-22.58	-18.61	-12.51	-159.33
790	-15.04	-149.83	18.82	127.22	-22.57	-19.92	-12.23	-159.94
840	-14.73	-150.32	18.70	124.22	-22.57	-21.26	-11.96	-160.63
900	-14.35	-150.94	18.57	120.78	-22.56	-22.85	-11.65	-161.64
950	-14.10	-151.64	18.44	117.74	-22.56	-24.21	-11.42	-162.56
1000	-13.83	-152.27	18.32	115.01	-22.56	-25.53	-11.19	-163.52
1050	-13.59	-153.23	18.21	112.08	-22.55	-26.89	-10.99	-164.55
1100	-13.38	-153.86	18.06	109.34	-22.56	-28.24	-10.80	-165.66
1150	-13.16	-154.76	17.96	106.63	-22.55	-29.58	-10.63	-166.70
1200	-12.99	-155.57	17.82	103.80	-22.55	-30.95	-10.47	-167.80
1250	-12.77	-156.33	17.69	101.33	-22.54	-32.33	-10.30	-168.91
1300	-12.61	-157.32	17.57	98.53	-22.55	-33.74	-10.16	-170.07
1350	-12.44	-158.19	17.44	95.98	-22.56	-35.12	-10.03	-171.34
1400	-12.30	-159.08	17.32	93.44	-22.57	-36.43	-9.92	-172.44
1450	-12.17	-159.85	17.19	90.86	-22.56	-37.74	-9.81	-173.47
1500	-12.01	-160.65	17.06	88.41	-22.56	-39.12	-9.70	-174.66
1550	-11.89	-161.57	16.95	85.90	-22.56	-40.49	-9.59	-175.76

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{CC}	6.5 V
Input Power (Referred to 50 Ω)	20 dBm
Internal Power Dissipation (Paddle Soldered)	650 mW
θ_{JA} (Junction to Air)	30.7°C/W
θ_{JC} (Junction to Paddle)	5.0°C/W
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	240°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

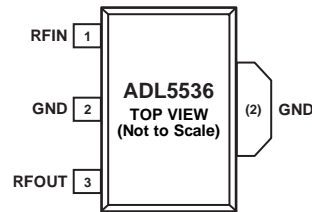
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXPOSED PADDLE IS INTERNALLY CONNECTED TO GND AND MUST BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.

08673-002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	RF Input. This pin requires a dc blocking capacitor.
2	GND	Ground. Connect this pin to a low impedance ground plane.
3	RFOUT	RF Output and Supply Voltage. A dc bias is provided to this pin through an inductor that is connected to the external power supply. The RF path requires a dc blocking capacitor.
(2)	Exposed Paddle	Exposed Paddle. The exposed paddle is internally connected to GND and must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

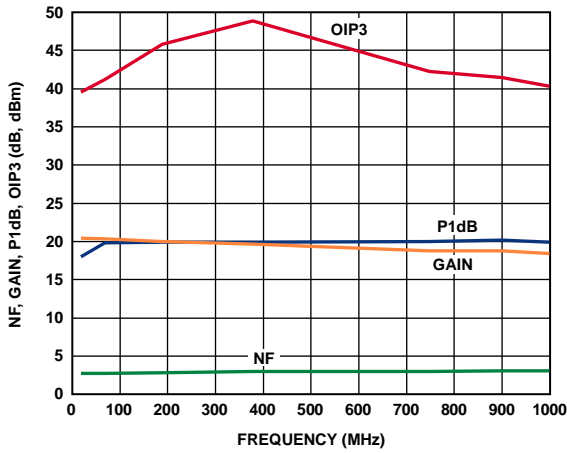


Figure 3. Noise Figure, Gain, P1dB, and OIP3 vs. Frequency

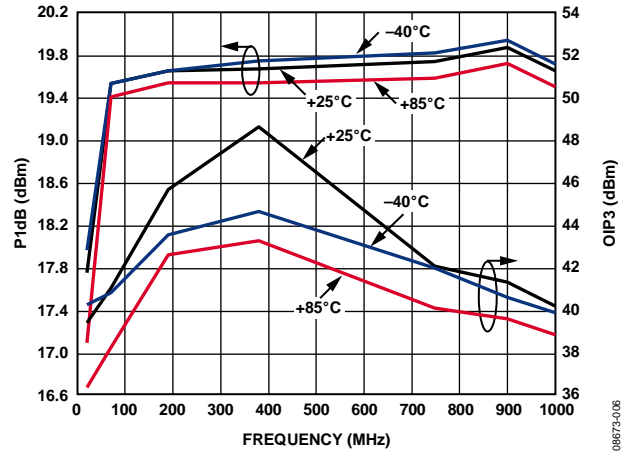


Figure 6. P1dB and OIP3 vs. Frequency and Temperature

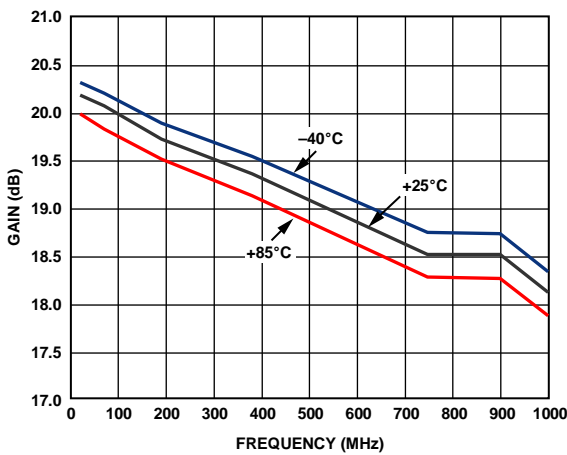


Figure 4. Gain vs. Frequency and Temperature

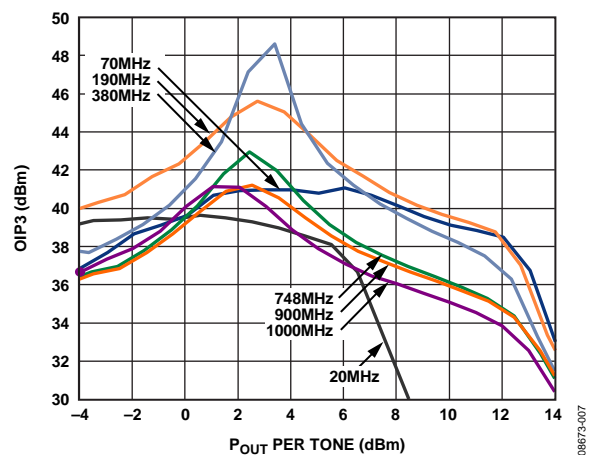


Figure 7. OIP3 vs. Output Power (P_{out}) and Frequency

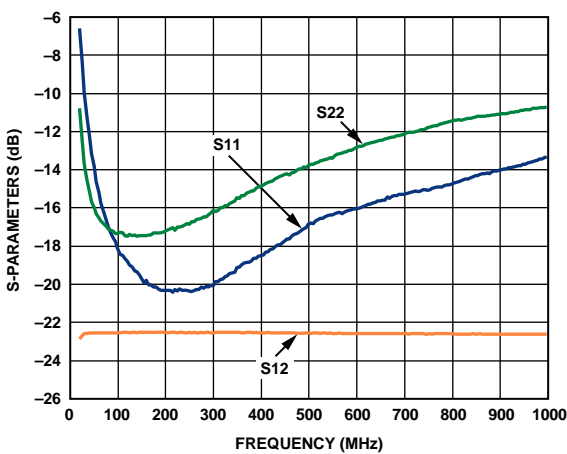


Figure 5. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

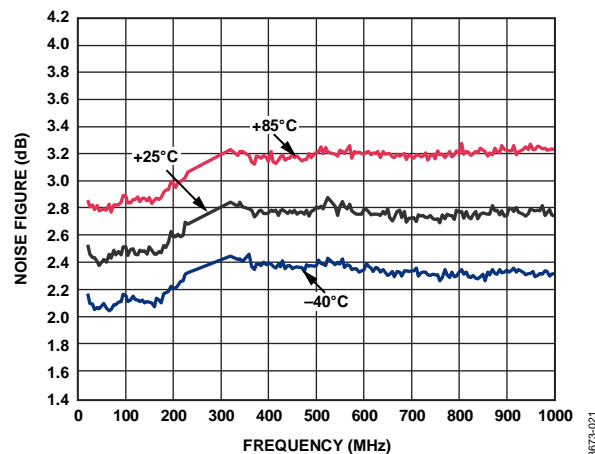


Figure 8. Noise Figure vs. Frequency and Temperature

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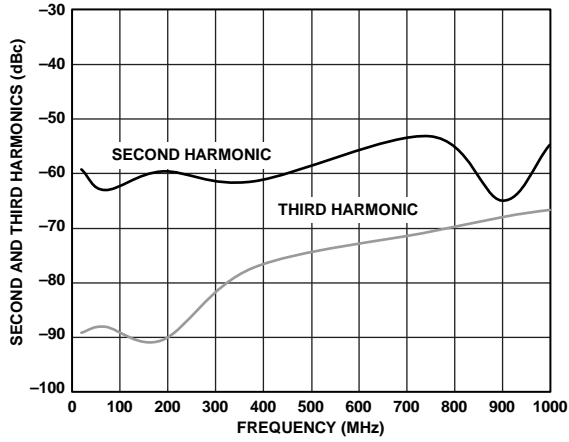


Figure 9. Single-Tone Harmonics vs. Frequency, $P_{OUT} = 0 \text{ dBm}$

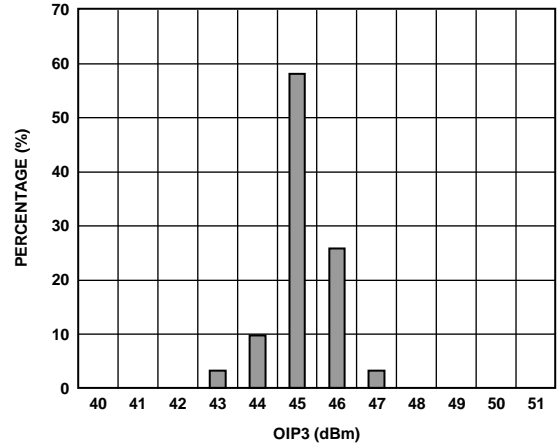


Figure 12. OIP3 Distribution at 190 MHz, $P_{OUT} = 3 \text{ dBm}$

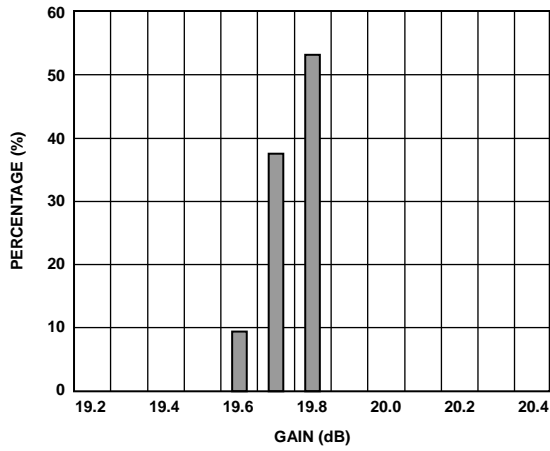


Figure 10. Gain Distribution at 190 MHz

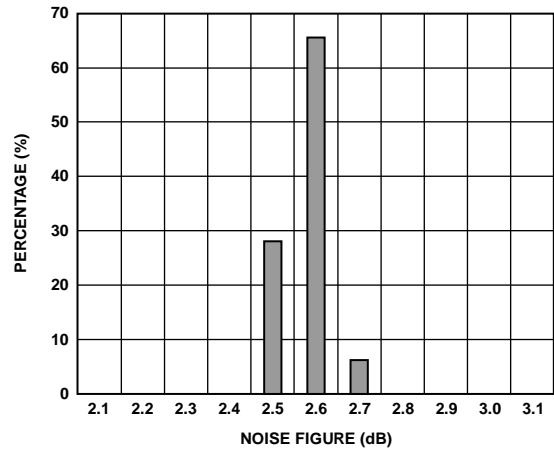


Figure 13. Noise Figure Distribution at 190 MHz

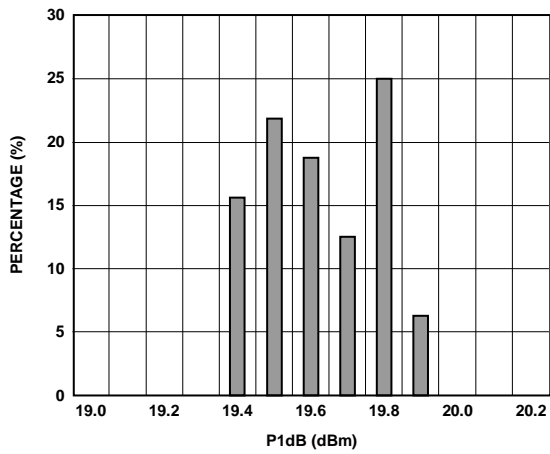


Figure 11. P1dB Distribution at 190 MHz

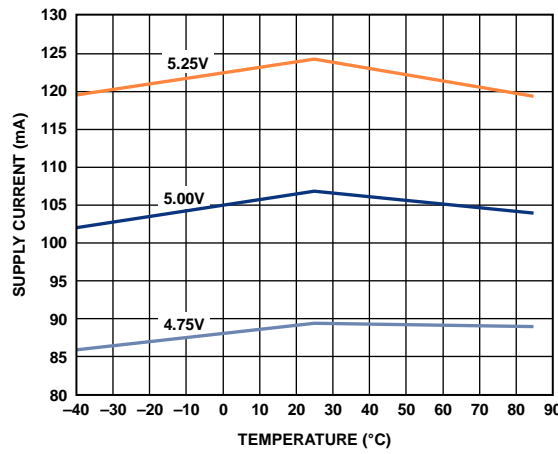


Figure 14. Supply Current vs. Temperature

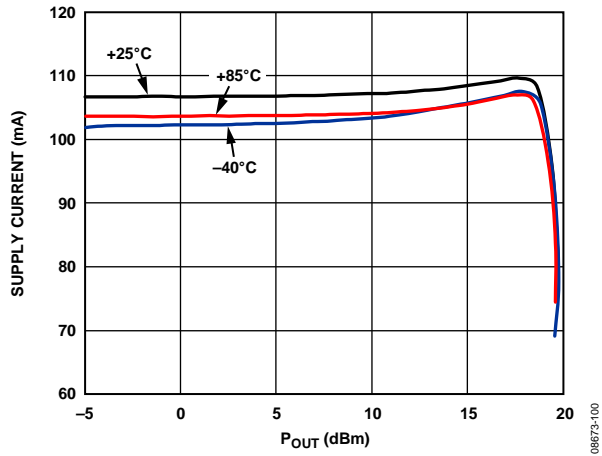


Figure 15. Supply Current vs. P_{OUT} and Temperature

BASIC CONNECTIONS

The basic connections for operating the ADL5536 are shown in Figure 16. Recommended components are listed in Table 5. The input and output should be ac-coupled with appropriately sized capacitors (device characterization was performed with 0.1 μF capacitors). A 5 V dc bias is supplied to the amplifier through the bias inductor connected to RFOUT (Pin 3). The bias voltage should be decoupled using a 1 μF capacitor, a 1.2 nF capacitor, and a 68 pF capacitor.

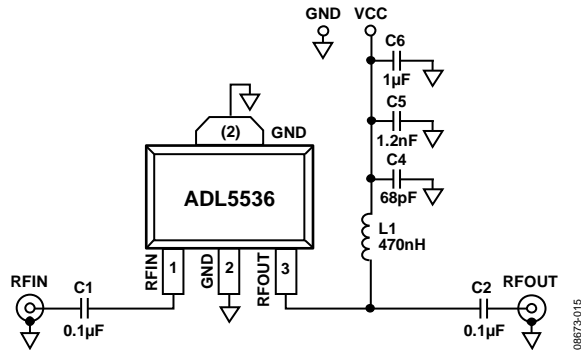


Figure 16. Basic Connections

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 17 shows the recommended land pattern for the ADL5536. To minimize thermal impedance, the exposed paddle on the package underside, along with Pin 2, should be soldered to a ground plane. If multiple ground layers exist, they should be stitched together using vias. For more information about land pattern design and layout, refer to the AN-772 Application Note, A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).

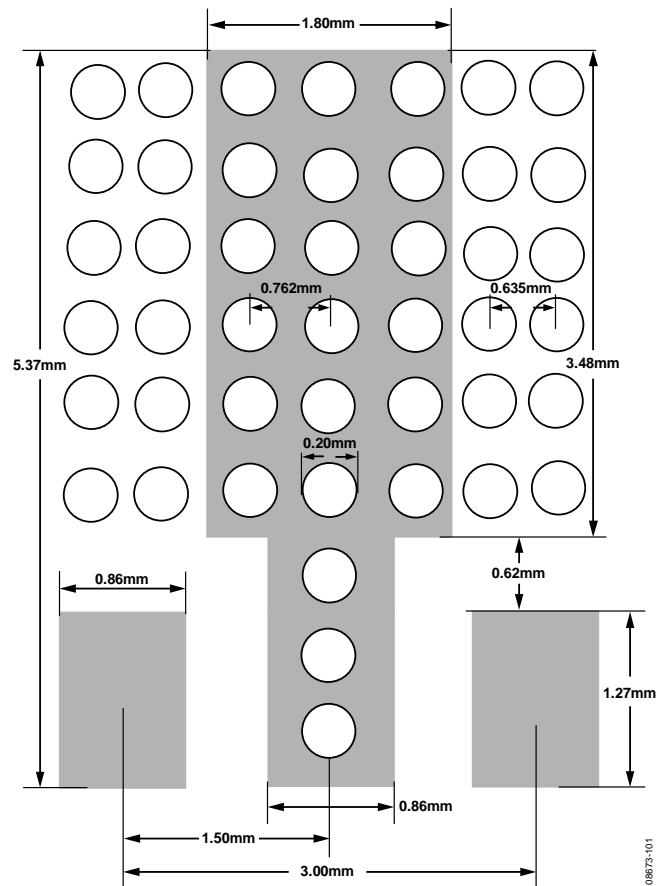


Figure 17. Recommended Land Pattern

Table 5. Recommended Components for Basic Connections

Frequency	C1	C2	L1	C4	C5	C6
20 MHz to 1000 MHz	0.1 μF	0.1 μF	470 nH (Coilcraft 0603LS-NX or equivalent)	68 pF	1.2 nF	1 μF

ACPR PERFORMANCE

Figure 18 shows a plot of the adjacent channel power ratio (ACPR) vs. P_{OUT} for the ADL5536. The signal type used is a single wideband code division multiple access (W-CDMA) carrier (Test Model 1-64). This signal is generated by a very low ACPR source. ACPR is measured at the output by a high dynamic range spectrum analyzer that incorporates an instrument noise-correction function. At an output power level of +8 dBm, ACPR is still very low at -65 dBc, making the device suitable for use in driver applications.

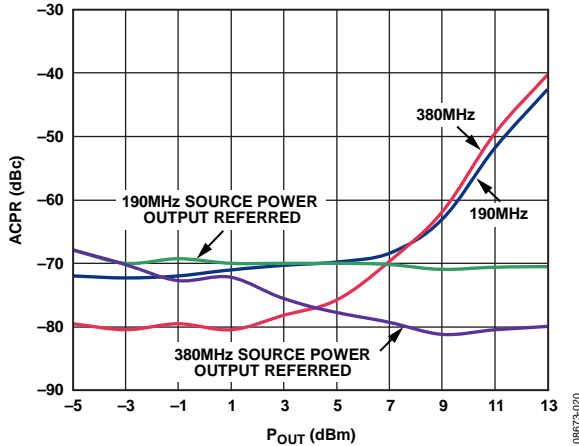


Figure 18. ACPR vs. P_{OUT} , Single W-CDMA Carrier (Test Model 1-64) at 190 MHz and 380 MHz

ERROR VECTOR MAGNITUDE (EVM) PERFORMANCE

Error vector magnitude (EVM) is a measure used to quantify the performance of a digital radio transmitter or receiver. A signal received by a receiver has all constellation points at their ideal locations; however, various imperfections in the implementation (such as magnitude imbalance, noise floor, and phase imbalance) cause the actual constellation points to deviate from their ideal locations. The ADL5536 shows excellent performance when used with higher-order modulation schemes, such as a 16 QAM. Figure 19 illustrates the EVM performance of the ADL5536 when driven with a 16 QAM 10 Msym/s signal. Degradation of the EVM performance starts to occur at an output power of +12 dBm.

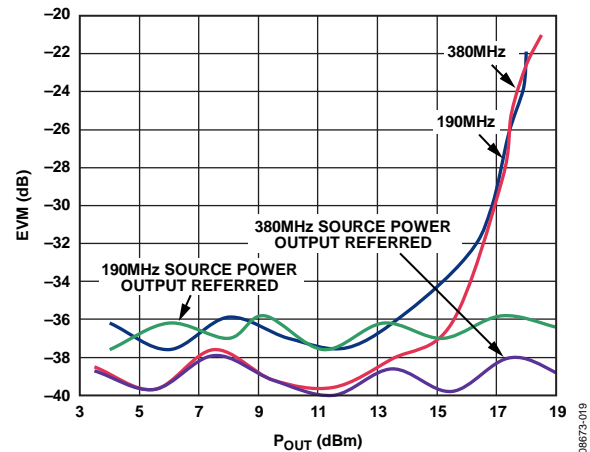


Figure 19. EVM Performance vs. P_{OUT} with a 16 QAM, 10 Msym/s Signal

EVALUATION BOARD

Figure 20 shows the evaluation board layout, and Figure 21 shows the schematic for the ADL5536 evaluation board. The board is powered by a single 5 V supply.

The components used on the board are listed in Table 6. Power can be applied to the board through clip-on leads (VCC and GND).

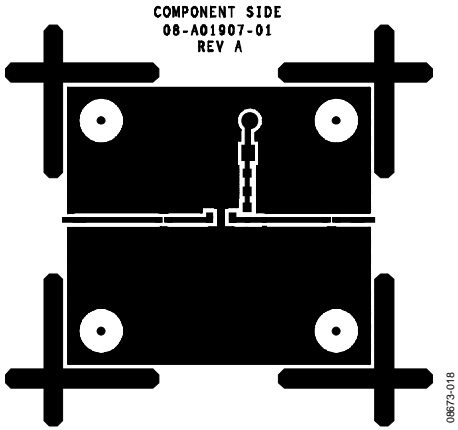


Figure 20. Evaluation Board Layout (Top)

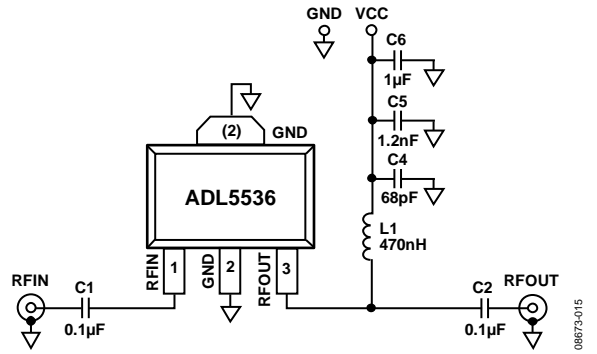
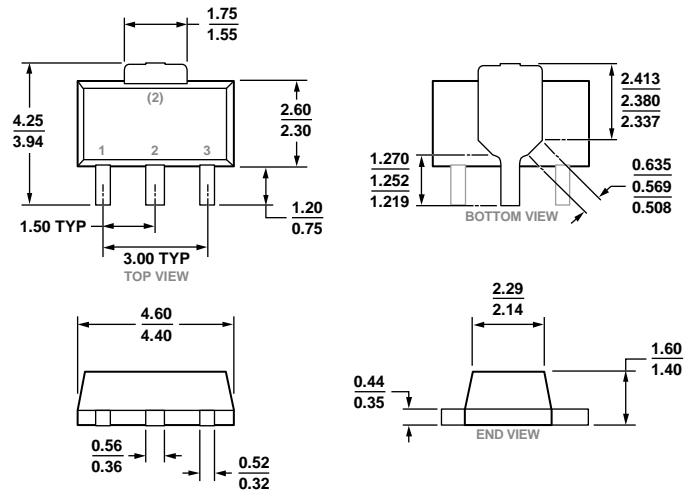


Figure 21. Evaluation Board Schematic

Table 6. Evaluation Board Components

Component	Description	Default Value
C1, C2	AC coupling capacitors	0.1 μF, 0402
L1	DC bias inductor	470 nH, 0603 (Coilcraft 0603LS-NX or equivalent)
VCC, GND	Clip-on terminals for power supply	
C4	Power supply decoupling capacitor	68 pF, 0603
C5	Power supply decoupling capacitor	1.2 nF, 0603
C6	Power supply decoupling capacitor	1 μF, 1206

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS TO-243

Figure 22. 3-Lead Small Outline Transistor Package [SOT-89] (RK-3)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADL5536ARKZ-R7	-40°C to +85°C	3-Lead SOT-89, 7" Tape and Reel	RK-3
ADL5536-EVALZ		Evaluation Board	

¹ Z = RoHS Compliant Part.

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