System PMIC for Battery Powered Systems

BD71815AGW

General Description

BD71815AGW is a single-chip power management IC for battery-powered portable devices. The IC integrates 5 buck converters, 8 LDOs, a boost driver for LED, and a 500mA single-cell linear charger. Also included is a Coulomb counter, a real-time clock (RTC), a 32 kHz crystal oscillator and a general-purpose output (GPO).

The IC's buck converters supply power to the application processor as well as system peripherals such as DDR memory, wireless modules, and touch controllers. These regulators maintain high efficiency over a wide range of current loads by supporting both PFM and PWM modes. They also operate at a high switching frequency of 6MHz, which allows the use of smaller and cheaper inductors and capacitors. The regulator supplying the processor core also supports Dynamic Voltage Scaling (DVS).

Features

- 5 buck converters:
  - 3 1000mA buck converters
  - 1 800mA buck converter
  - 1 500mA buck converter
- 3 general-purpose LDOs
  - 2 100mA LDOs
  - 1 50mA LDO
- LDO for DDR Reference Voltage (DVREF)
- LDO for Secure Non-Volatile Storage (SNVS)
- LDO for Low-Power State Retention (LPSR)
- LDO for SD Card with dedicated enable terminal
- LDO for SD Card Interface with dedicated terminal to dynamically change output voltage
- White LED Boost Converter
  -25mA LED Boost Converter
- Single-cell Linear LIB Charger with 30V OVP
  -Selectable charging voltage: 3.72 to 4.34 V
  -Programmable charge current: 100 to 500mA
  -Support for up to 2000mA charge current using external MOSFET
  -DCIN over voltage protection
  -Battery over voltage protection
  -Battery Supplement Mode support
  -Battery Short Circuit Detection
- Voltage Measurement for Thermistor
  -Bias voltage output for External Thermistor
- Embedded Coulomb Counter for Battery Fuel Gauging
  -15-bit ΔΣ-ADC with External Current Sense Resistor (10 mΩ, ±1% or 30mΩ, ±1%)
  -1-sec cycle, 28-bit accumulation
  -Coulomb count while charging/discharging
- Battery Monitoring and Alarm Output
  -Under Voltage Alarm while discharging
  -Over Current Alarm
  -Over/Under Temperature Alarm
  -Programmable thresholds and time durations
- Real Time Clock with 32.768kHz crystal oscillator
  -32.768kHz clock output (Open Drain or CMOS Output Selectable)
- 1 GPO (Open Drain or CMOS Output Selectable)
- Power Control I/O
  -Power On/Off control input
  -Standby Input for switching RUN/SUSPEND State
  -Reset Input to reset hung PMIC
  -Power On Reset output
- 1 LED Indicator
  -Indicate charger status
- I2C interface

Applications

- E-Book reader
- Media players with smart devices, wearables
- Portable Navigation Devices with Home POS, Human Machine Interfaces

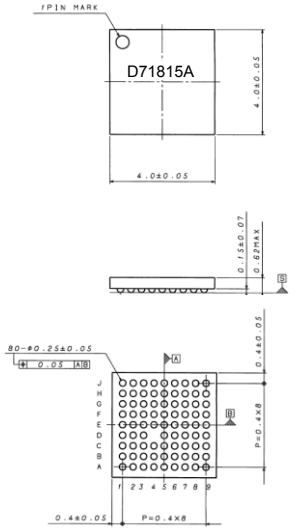
Key Specifications

- Input Voltage Range (DCIN): 3.5V to 28V
- Input Voltage Range (VIN, VSYS): 2.9V to 5.5V
- Input Voltage Range (DVDD): 1.5V to 3.4V
- Off Current: 20 µA (Typ)
  [RTC+ Coulomb counter+ LDO_SNVS only]
- Operating temperature range: -40°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)

UCSP55M4C 4.0mm x 4.0mm x 0.62mm



(Unit :mm)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Typical Application Circuit

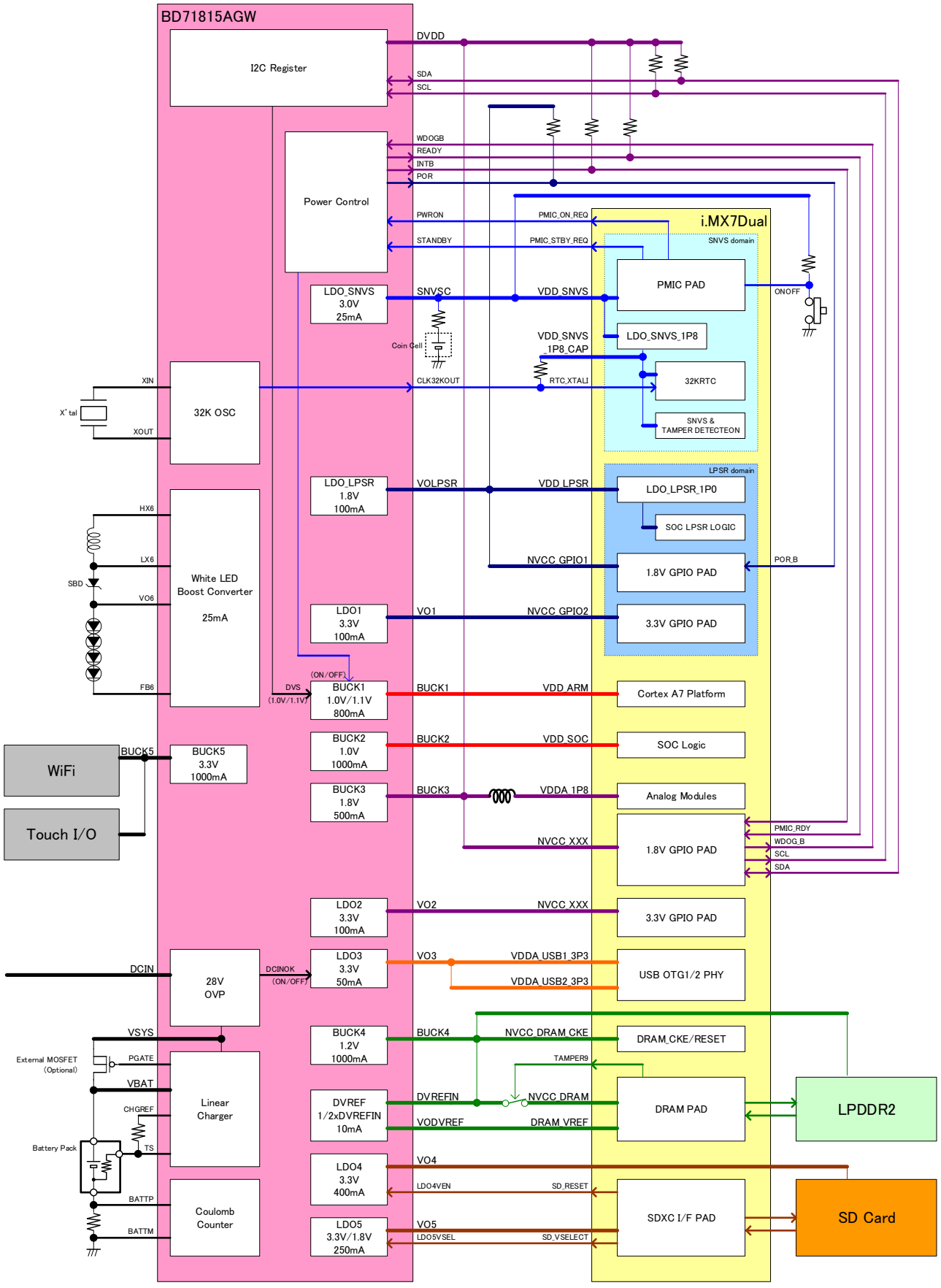


Figure 1. Typical Application (E-Book Reader with i.Mx7D)

Block Diagram

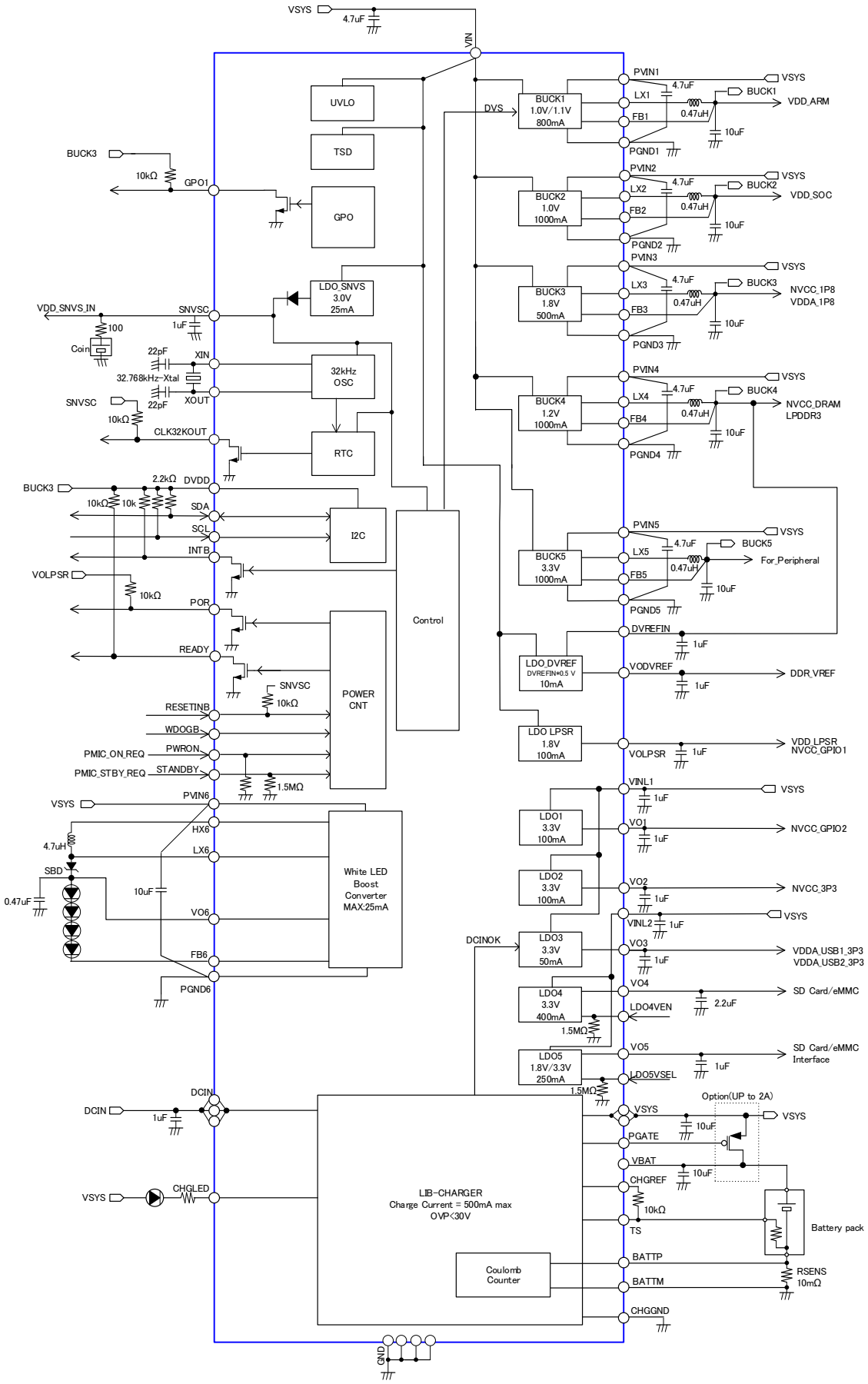


Figure 2. IC Block Diagram

Pin Configuration

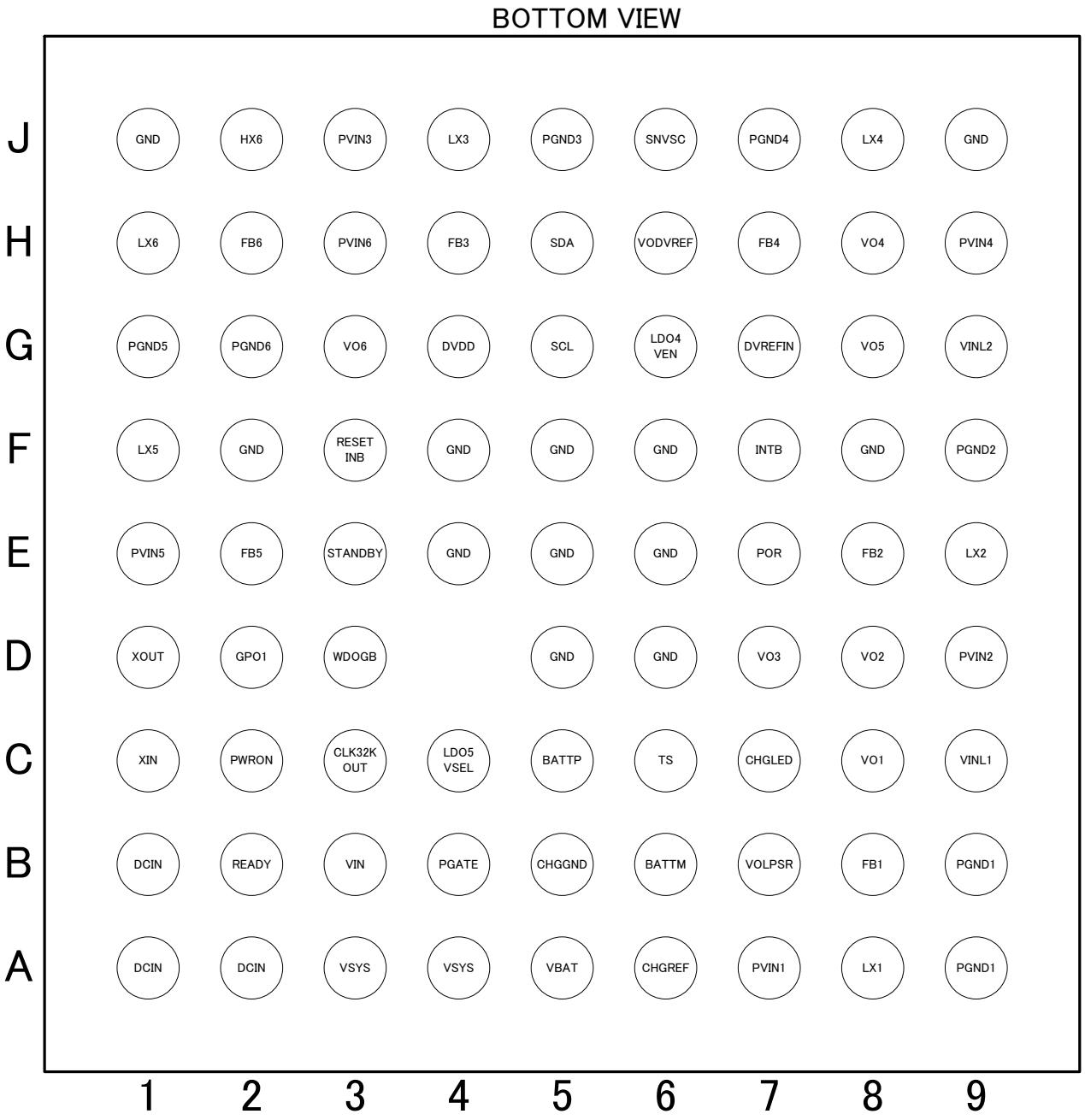


Figure 3. Pin Configuration (Bottom View)

Pin Descriptions

Table 1. BD71815AGW Pin Descriptions

Ball No.	Block Name	Terminal Name	I/O	Explanation	Internal Pull up/down
A7	BUCK1	PVIN1	I	Input power supply for BUCK1	
A8		LX1	O	Switch node connection for BUCK1	
B8		FB1	I	Output voltage feedback for BUCK1	
E3		STANDBY	I	Standby input signal	Pull down 1.5MΩ to GND
A9		PGND1	-	Power ground for BUCK1	
B9		PGND1	-	Power ground for BUCK1	
D9	BUCK2	PVIN2	I	Input power supply for BUCK2	
E9		LX2	O	Switch node connection for BUCK2	
E8		FB2	I	Output voltage feedback for BUCK2	
F9		PGND2	-	Power ground for BUCK2	
J3	BUCK3	PVIN3	I	Input power supply for BUCK3	
J4		LX3	O	Switch node connection for BUCK3	
H4		FB3	I	Output voltage feedback for BUCK3	
J5		PGND3	-	Power ground for BUCK3	
H9	BUCK4	PVIN4	I	Input power supply for BUCK4	
J8		LX4	O	Switch node connection for BUCK4	
H7		FB4	I	Output voltage feedback for BUCK4	
J7		PGND4	-	Power ground for BUCK4	
E1	BUCK5	PVIN5	I	Input power supply for BUCK5	
F1		LX5	O	Switch node connection for BUCK5	
E2		FB5	I	Output voltage feedback for BUCK5	
G1		PGND5	-	Power ground for BUCK5	
H3	LED Driver	PVIN6	I	Input power supply for BOOST	
J2		HX6	O	Switch node connection for BOOST	
H1		LX6	O	Switch node connection for BOOST	
G3		VO6	O	BOOST output	
H2		FB6	I	Output voltage feedback for BOOST	
G2		PGND6	-	Power ground for BOOST	
B7	LDOLPSR	VOLPSR	O	LDO output for LPSR	
C9	LDO	VINL1	I	LDO input for LDO1, LDO2 and LDO3	
C8		VO1	O	LDO output for LDO1	
D8		VO2	O	LDO output for LDO2	
D7		VO3	O	LDO output for LDO3	
G9		VINL2	I	LDO input for LDO4 and LDO5	
H8		VO4	O	LDO output for LDO4	
G8		VO5	O	LDO output for LDO5	
G6		LDO4VEN	I	LDO4 Enable	Pull down 1.5MΩ to GND
C4		LDO5VSEL	I	LDO5 Output Voltage select	Pull down 1.5MΩ to GND
G7	DVREF	DVREFIN	I	LDO input for DVREF/CLK32KOUT H-level(note3)	
H6		VODVREF	O	LDO output for DVREF	
J6	SNVS	SNVSC	O	LDO output for SNVS (requires capasitor)	

Table 2. BD71815AGW Pin Descriptions (continued)

Ball No.	Block Name	Terminal Name	I/O	Explanation	Pull up/down
G4	I2C	DVDD	I	Power Supply for I2C interface	
H5		SDA	I/O	I2C data line (Open drain)	note1
G5		SCL	I	I2C clock	note1
C1	RTC	XIN	I	32.768kHz-Xtal input	
D1		XOUT	O	32.768kHz-Xtal output	
C3		CLK32KOUT	O	32.768kHz clock output (Open drain/CMOS)	
C2	POWRCNT	PWRON	I	Power on/off control input	Pull down 1.5MΩ to GND
F3		RESETINB	I	Reset input to shutdown this device	Pull up 10kΩ to SNVSC
E7		POR	O	Power on reset output (Open drain)	note2
F7		INTB	O	Interrupt signal to processor (Open drain)	note2
D3		WDOGB	I	Watchdog input from processor	Pull up 1.5MΩ to VIN
B2		READY	O	PMIC ready output	note2
A1	OVP	DCIN	I	DCIN input	
A2		DCIN	I	DCIN input	
B1		DCIN	I	DCIN input	
A3		VSYS	O	System supply output	
A4		VSYS	O	System supply output	
A5	CHARGER	VBAT	I/O	Charger output / Battery input	
B4		PGATE	O	External power MOS gate control output	
C6		TS	I	Battery pack thermistor voltate sense	
A6		CHGREF	O	Internal reference for the Lib charger	
C5		BATTP	I	Current sense input (battery pack side)	
B6		BATTM	I	Current sense input (ground side)	
B5		CHGGND	-	Ground for Charger	
C7		CHGLED	O	Charging status indication output (Open drain)	
D2	GPO	GPO1	O	Output for general purpose	
B3	Power/GND	VIN	I	Input power supply	
J1		GND	-	Signal ground	
J9		GND	-	Signal ground	
F2		GND	-	Signal ground	
F8		GND	-	Signal ground	
D5		GND	-	Signal ground	
D6		GND	-	Signal ground	
E4		GND	-	Signal ground (for reduce Thermal resistance)	
E5		GND	-	Signal ground (for reduce Thermal resistance)	
E6		GND	-	Signal ground (for reduce Thermal resistance)	
F4		GND	-	Signal ground (for reduce Thermal resistance)	
F5		GND	-	Signal ground (for reduce Thermal resistance)	
F6		GND	-	Signal ground (for reduce Thermal resistance)	

note1 : SDA and SCL need pull up resistance to DVDD.

note2 : POR, INTB and READY need pull up resistance.

note3 : When CLK32KOUT is selected to CMOS output mode.

PCB Layout Recommendations

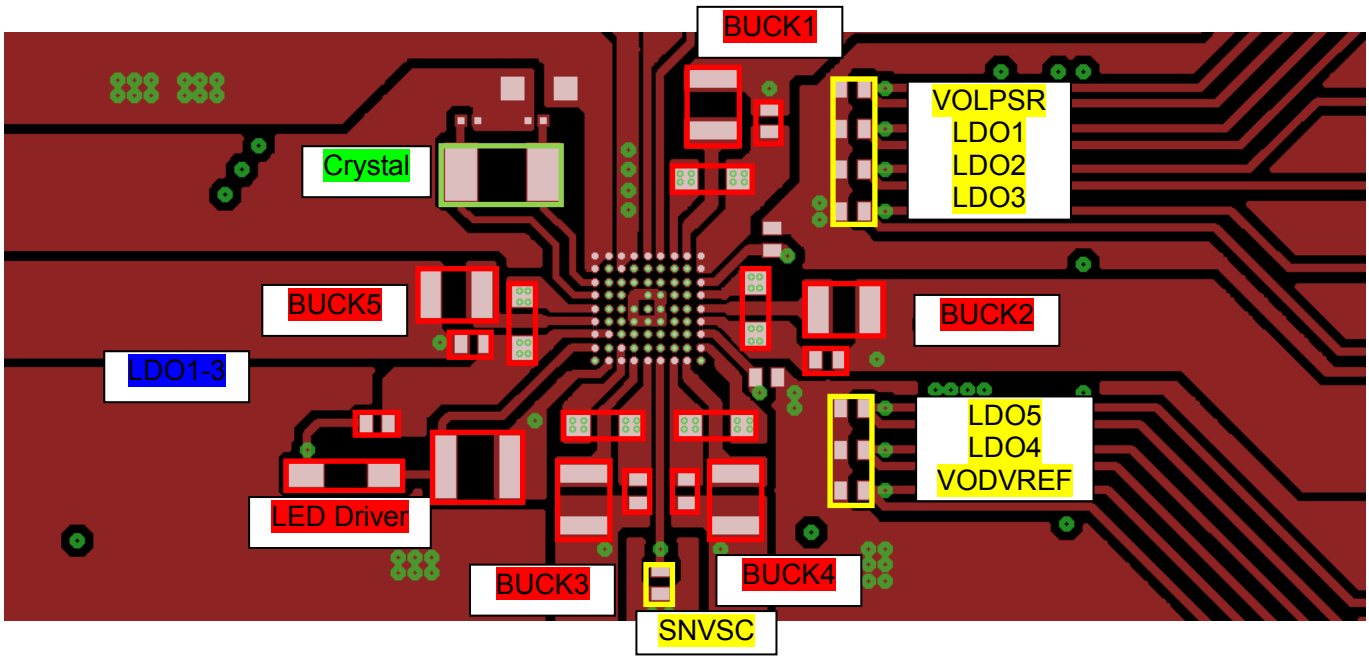


Figure 4. PCB Layout Recommendations (Top View)

Description of Blocks

1. High Efficiency Buck Converters (BUCK1 – 5) and LDOs

BD71815AGW step down converters operate at a fixed frequency of 6MHz. These converters employ Pulse Width Modulation (PWM) under moderate to heavy load and enter Power Save Mode when used under light load. In Power Save Mode, the step down converters operate using Pulse Frequency Modulation (PFM).

Table 3. BD71815AGW Output Power Rails

BD71815AGW Function	i.MX7 Dual Usage example	Power Supply	Initial Output Voltage	Load max	Adjustable range
BUCK1	VDD_ARM	PVIN1	1.1V	800mA	0.8 to 2.000V (25mV step) [DVS]
BUCK2	VDD_SOC	PVIN2	1.0V	1000mA	0.8 to 2.000V (25mV step) [DVS]
BUCK3	NVCC_1P8 / VDDA_1P8	PVIN3	1.8V	500mA	1.2V to 2.7V (50mV step)
BUCK4	NVCC_DRAM / LPDDR3	PVIN4	1.2V	1000mA	1.1 to 1.85V (25mV step)
BUCK5	Peripheral	PVIN5	3.3V	1000mA	1.8 to 3.3V (50mV step)
LDO1	NVCC_GPIO2	VINL1	3.3V	100mA	0.8 to 3.3V (50mV step)
LDO2	NVCC_3P3	VINL1	3.3V	100mA	0.8 to 3.3V (50mV step)
LDO3	VDDA_USB1_3P3 / VDDA_USB2_3P3	VINL1	3.3V	50mA	0.8 to 3.3V (50mV step)
LDO4	SD Card / eMMC	VINL2	3.3V	400mA	0.8V to 3.3V(50mV step)
LDO5	SD Card / eMMC	VINL2	1.8V / 3.3V	250mA	0.8V to 3.3V(50mV step)
VODVREF	LPDDR3	VIN	0.5*DVREFIN	10mA	0.55 to 0.925V (DVREFIN= BUCK4)
SNVSC	VDD_SNVS	VIN	3.0V	25mA	Fixed
LDO LPSR	VDD_LPSR / NVCC_GPIO1	VIN	1.8V	100mA	Fixed
White LED Driver	-	VIN	up to 18V	25mA	10uA to 25mA
I2C	-	DVDD	-	-	-
RTC	-	SNVS	-	-	-
Charger	-	VSYS	-	-	-
Coulomb Counter	-	SNVS	-	-	-
SNVS/VSYS Voltage monitor	-	VIN	-	-	-

Table 4. Voltage Identification Code for BD71815AGW Output Power Rails

#	I2C Register	BUCK1	BUCK2	BUCK3	BUCK4	BUCK5	LDO1	LDO2	LDO3	LDO4	LDO5
0	00 0000	0.800	0.800	1.200	1.100	1.800	0.80	0.80	0.80	0.80	0.80
1	00 0001	0.825	0.825	1.250	1.125	1.850	0.85	0.85	0.85	0.85	0.85
2	00 0010	0.850	0.850	1.300	1.150	1.900	0.90	0.90	0.90	0.90	0.90
3	00 0011	0.875	0.875	1.350	1.175	1.950	0.95	0.95	0.95	0.95	0.95
4	00 0100	0.900	0.900	1.400	1.200(note1)	2.000	1.00	1.00	1.00	1.00	1.00
5	00 0101	0.925	0.925	1.450	1.225	2.050	1.05	1.05	1.05	1.05	1.05
6	00 0110	0.950	0.950	1.500	1.250	2.100	1.10	1.10	1.10	1.10	1.10
7	00 0111	0.975	0.975	1.550	1.275	2.150	1.15	1.15	1.15	1.15	1.15
8	00 1000	1.000	1.000(note1)	1.600	1.300	2.200	1.20	1.20	1.20	1.20	1.20
9	00 1001	1.025	1.025	1.650	1.325	2.250	1.25	1.25	1.25	1.25	1.25
10	00 1010	1.050	1.050	1.700	1.350	2.300	1.30	1.30	1.30	1.30	1.30
11	00 1011	1.075	1.075	1.750	1.375	2.350	1.35	1.35	1.35	1.35	1.35
12	00 1100	1.100(note1)	1.100	1.800(note1)	1.400	2.400	1.40	1.40	1.40	1.40	1.40
13	00 1101	1.125	1.125	1.850	1.425	2.450	1.45	1.45	1.45	1.45	1.45
14	00 1110	1.150	1.150	1.900	1.450	2.500	1.50	1.50	1.50	1.50	1.50
15	00 1111	1.175	1.175	1.950	1.475	2.550	1.55	1.55	1.55	1.55	1.55
16	01 0000	1.200	1.200	2.000	1.500	2.600	1.60	1.60	1.60	1.60	1.60
17	01 0001	1.225	1.225	2.050	1.525	2.650	1.65	1.65	1.65	1.65	1.65
18	01 0010	1.250	1.250	2.100	1.550	2.700	1.70	1.70	1.70	1.70	1.70
19	01 0011	1.275	1.275	2.150	1.575	2.750	1.75	1.75	1.75	1.75	1.75
20	01 0100	1.300	1.300	2.200	1.600	2.800	1.80	1.80	1.80	1.80	1.80(note1)
21	01 0101	1.325	1.325	2.250	1.625	2.850	1.85	1.85	1.85	1.85	1.85
22	01 0110	1.350	1.350	2.300	1.650	2.900	1.90	1.90	1.90	1.90	1.90
23	01 0111	1.375	1.375	2.350	1.675	2.950	1.95	1.95	1.95	1.95	1.95
24	01 1000	1.400	1.400	2.400	1.700	3.000	2.00	2.00	2.00	2.00	2.00
25	01 1001	1.425	1.425	2.450	1.725	3.050	2.05	2.05	2.05	2.05	2.05
26	01 1010	1.450	1.450	2.500	1.750	3.100	2.10	2.10	2.10	2.10	2.10
27	01 1011	1.475	1.475	2.550	1.775	3.150	2.15	2.15	2.15	2.15	2.15
28	01 1100	1.500	1.500	2.600	1.800	3.200	2.20	2.20	2.20	2.20	2.20
29	01 1101	1.525	1.525	2.650	1.825	3.250	2.25	2.25	2.25	2.25	2.25
30	01 1110	1.550	1.550	2.700	1.850	3.300(note1)	2.30	2.30	2.30	2.30	2.30
31	01 1111	1.575	1.575				2.35	2.35	2.35	2.35	2.35
32	10 0000	1.600	1.600				2.40	2.40	2.40	2.40	2.40
33	10 0001	1.625	1.625				2.45	2.45	2.45	2.45	2.45
34	10 0010	1.650	1.650				2.50	2.50	2.50	2.50	2.50
35	10 0011	1.675	1.675				2.55	2.55	2.55	2.55	2.55
36	10 0100	1.700	1.700				2.60	2.60	2.60	2.60	2.60
37	10 0101	1.725	1.725				2.65	2.65	2.65	2.65	2.65
38	10 0110	1.750	1.750				2.70	2.70	2.70	2.70	2.70
39	10 0111	1.775	1.775				2.75	2.75	2.75	2.75	2.75
40	10 1000	1.800	1.800				2.80	2.80	2.80	2.80	2.80
41	10 1001	1.825	1.825				2.85	2.85	2.85	2.85	2.85
42	10 1010	1.850	1.850				2.90	2.90	2.90	2.90	2.90
43	10 1011	1.875	1.875				2.95	2.95	2.95	2.95	2.95
44	10 1100	1.900	1.900				3.00	3.00	3.00	3.00	3.00
45	10 1101	1.925	1.925				3.05	3.05	3.05	3.05	3.05
46	10 1110	1.950	1.950				3.10	3.10	3.10	3.10	3.10
47	10 1111	1.975	1.975				3.15	3.15	3.15	3.15	3.15
48	11 0000	2.000	2.000				3.20	3.20	3.20	3.20	3.20
49	11 0001						3.25	3.25	3.25	3.25	3.25
50	11 0010						3.30(note1)	3.30(note1)	3.30(note1)	3.30(note1)	3.30(note1)
51	11 0011										
52	11 0100										
53	11 0101										
54	11 0110										
55	11 0111										
56	11 1000										
57	11 1001										
58	11 1010										
59	11 1011										
60	11 1100										
61	11 1101										
62	11 1110										
63	11 1111										
Voltage step		25mV	25mV	50mV	25mV	50mV	50mV	50mV	50mV	50mV	50mV

(note1) Default output voltage setting

2. Power ON/OFF Sequence

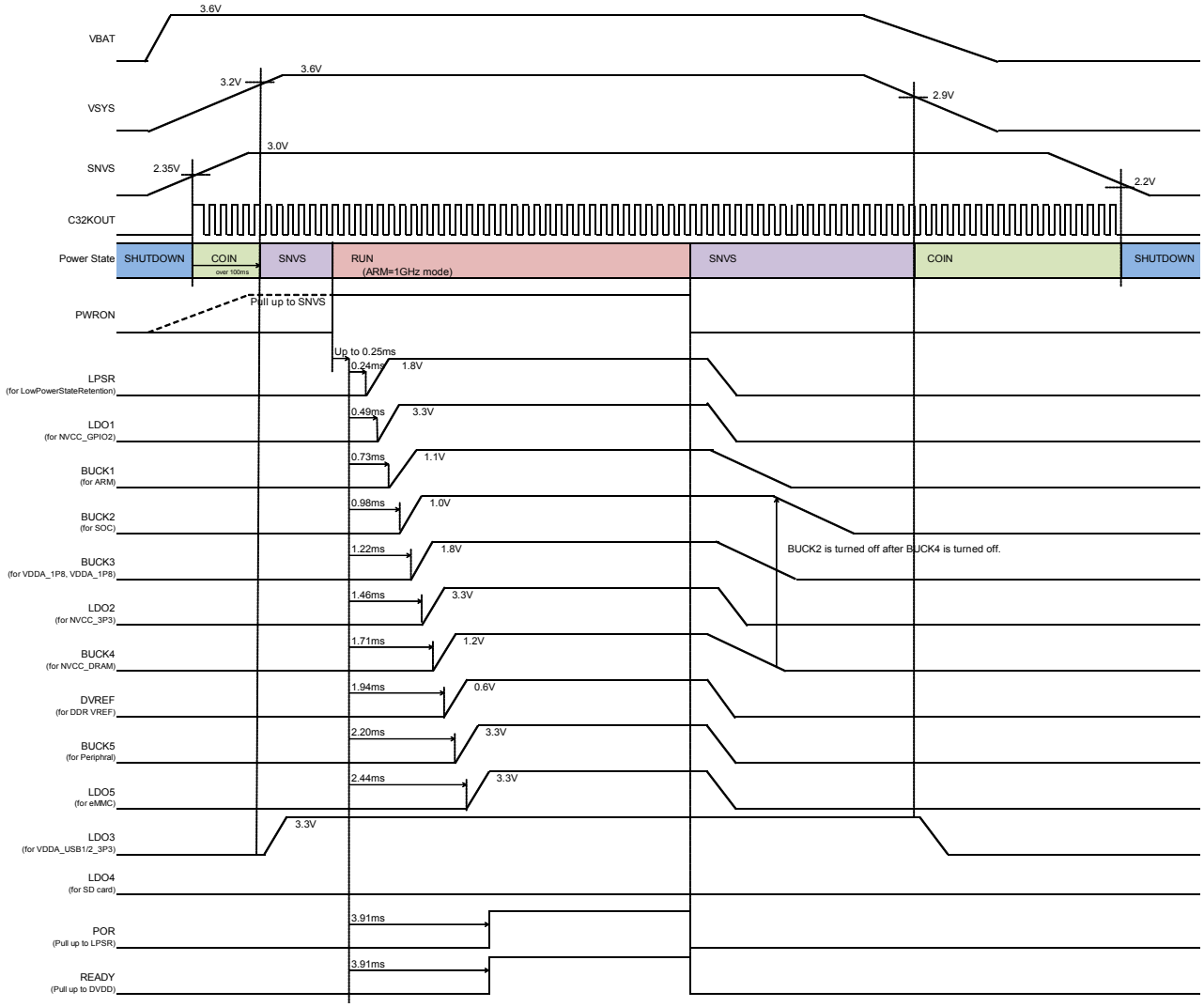


Figure 5. Power ON/OFF Sequence

3. States of Operation

BD71815AGW has six power states: RUN, SUSPEND, LPSR, SNVS, Coin, and Shutdown. Figure 6 shows the state transition diagram along with the conditions to enter and exit each state.

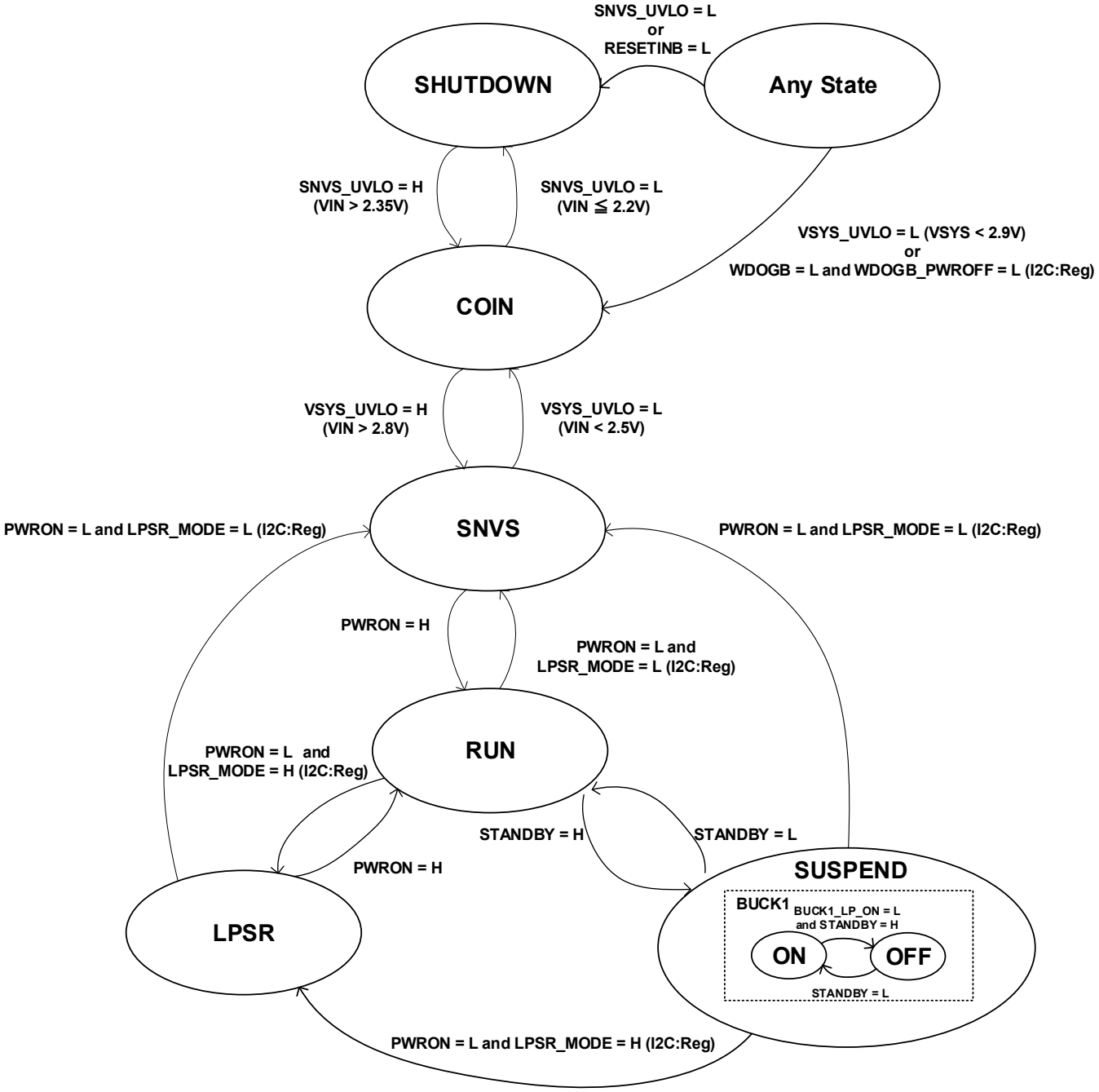


Figure 6. Power States Transitions

Description of states is provided in the following section. I2C Control is not possible in Shutdown state. However, the interrupt signal INTB is active during RUN and SUSPEND states.

Table 5. Voltage Rails ON/OFF for Respective Power States

BD71815AGW Function	Power Mode						Output Control	
	Shutdown	Coin	SNVS	LPSR	RUN	SUSPEND	ON/OFF	Sequence order
BUCK1	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	2
BUCK2	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	3
BUCK3	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	4
BUCK4	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	6
BUCK5	OFF	OFF	OFF	OFF	Auto	Auto	State or I2C register	8
LDO1	OFF	OFF	OFF	ON	ON	ON	State or I2C register	1
LDO2	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	5
LDO3	OFF	OFF	ON	ON	ON	ON	State or I2C register	9
LDO4	OFF	OFF	OFF	OFF	OFF	OFF	LDO4VEN	9
LDO5	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	9
VODVREF	OFF	OFF	OFF	OFF	ON	ON	State or I2C register	0
SNVSC	OFF	ON	ON	ON	ON	ON	State or I2C register	-
LDO LPSR	OFF	OFF	OFF	ON	ON	ON	State or I2C register	7
White LED Driver	OFF	OFF	OFF	OFF	OFF	OFF	State or I2C register	-
I2C	Reset	Disable	Disable	Disable	Enable	Enable	State	-
RTC	OFF	ON	ON	ON	ON	ON	State	-
Charger	OFF	OFF	ON/OFF	ON/OFF	ON/OFF	ON/OFF	DCIN	-
Coulomb Counter	OFF	OFF	ON	ON	ON	ON	State	-
SNVS/VSYS Voltage monitor	ON	ON	ON	ON	ON	ON	-	-

(Note) Auto : PWM/PFM mode change automatically depending on the load current

(1) Power Control States

(a) Shutdown State

BD71815AGW enters Shutdown State when SNVS falls below 2.2V or when BD71815AGW encounters a thermal shutdown event. In case of system hang-up, setting RESETINB to LOW will cause the IC to shut down. Only the SNVS and VSYS voltage measurement block (UVLO) is powered during Shutdown state. Data in all registers are reset to their initial settings. To exit Shutdown state, SNVS must exceed 2.35V.

(b) Coin State

BD71815AGW enters Coin State when SNVS exceeds 2.35V or VSYS falls below 2.9V. BD71815AGW also enters Coin State when only the coin battery is connected to SNVSC, or when WDOGB is asserted low. BD71815AGW starts the Off Sequence in this case.

UVLO, RTC, Battery measurement (Coulomb Counter), and SNVS blocks are powered in Coin State. All BUCK blocks and other LDOs are powered off. Registers cannot be accessed when BD71815AGW enters this state, but register data is retained.

(c) SNVS State

BD71815AGW enters SNVS State if PWRON is asserted low while LPSR_MODE registers are set low. SNVS State can also be accessed from Coin State when VSYS exceeds 3.2V.

In SNVS State, BUCKs and LDOs which have the SNVS_ON register set High are turned ON. Charger is also started when DCIN input is supplied with the appropriate voltage. These blocks are turned on in addition to blocks powered in Coin State.

(d) LPSR State

BD71815AGW enters LPSR state if PWRON is asserted Low while LPSR_MODE registers are set high.

In LPSR State, BUCKs and LDOs which have the LPSR_ON register set high are turned ON.

(d) RUN State

BD71815AGW enters RUN state when PWRON is asserted High. POR is negated in this state.

In RUN State, BUCKs and LDOs which have the RUN_ON register set High are turned ON. I2C registers can be accessed in this state.

(e) SUSPEND State

BD71815AGW enters SUSPEND State from RUN State when STANDBY is asserted high.

In SUSPEND State, BUCKs and LDOs which have the LP_ON register set low are turned OFF. I2C registers can be accessed in this state.

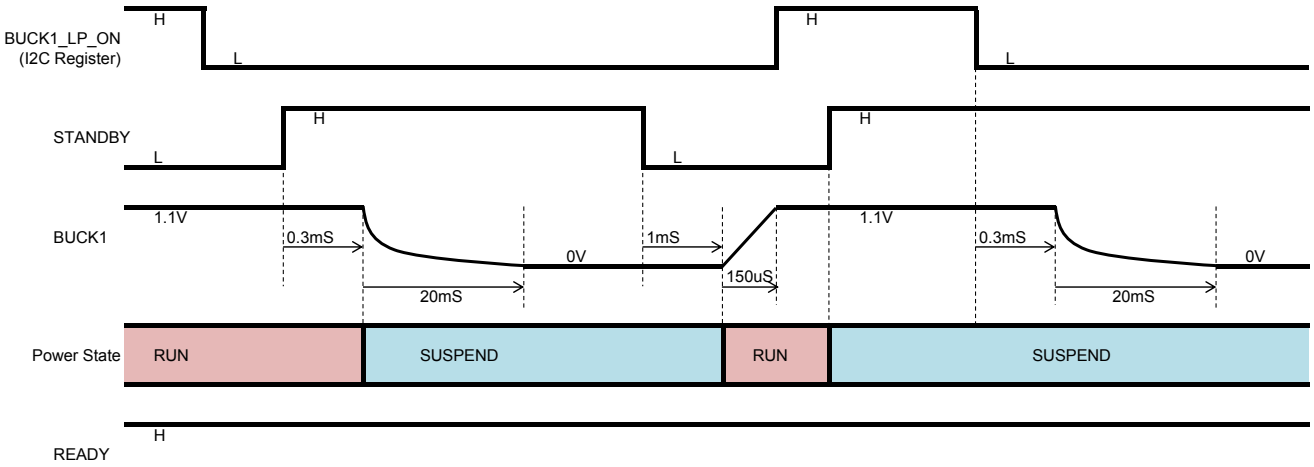


Figure 7 – SUSPEND State Control Timing Diagram

4. Dynamic Voltage Scaling (DVS) Control

BUCK1 and BUCK2 support Dynamic Voltage Scaling (DVS). BUCK1_DVSSEL and BUCK2_DVSSEL registers control the output voltage of BUCK1 and BUCK2, respectively. BUCK#_H controls the output voltage for when BUCK#_DVSSEL is set high, and BUCK#_L for when BUCK#_DVSSEL is set low. Slew rate is also set via the BUCK#_RAMPRATE register.

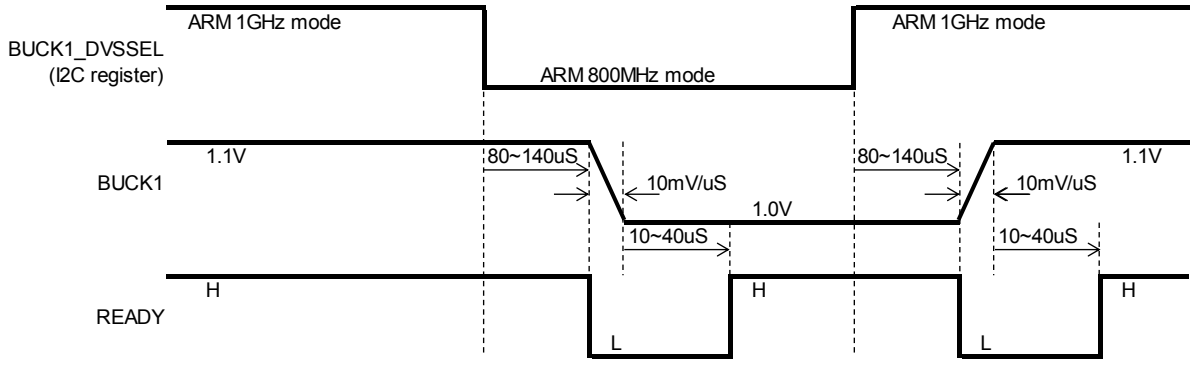


Figure 8 - DVS Control Timing Diagram

5. LDO4 and LDO5 Control (for SD Card)

LDO4 and LDO5 support High Speed SD Card and SD Card Interface power rails, respectively.

LDO4 is turned on and off by LDO4VEN. This function is for High Speed SD Card Reset operation.

LDO5 supports Dynamic Voltage Scaling (DVS). LDO5_H register controls the output voltage for when LDO5VSEL pin is set high, and LDO5_L register for when LDO5VSEL pin is set low. This function supplies dynamically changing output voltages for Normal to High Speed operation.

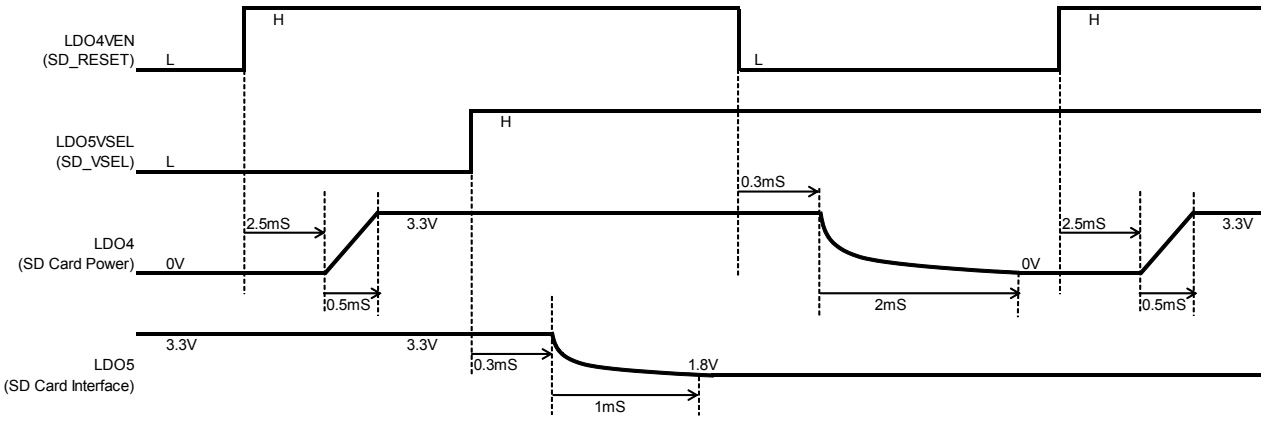


Figure 9 – SD Card Interface Control Timing Diagram

6. Real Time Clock (RTC) Block

Features

- RTC is driven by a 32.768 kHz oscillator and provides alarm and timekeeping functions to the nearest second.
- Time information is provided in seconds, minutes, and hours.
- Calendar information is provided in day, month, year, and day of the week.
- Alarm interrupt is sent at the time and day programmed into registers.
- Leap year compensation up to 2099
- Selectable 12-hour and 24-hour modes
- RTC calibration support
- Oscillator failure detection

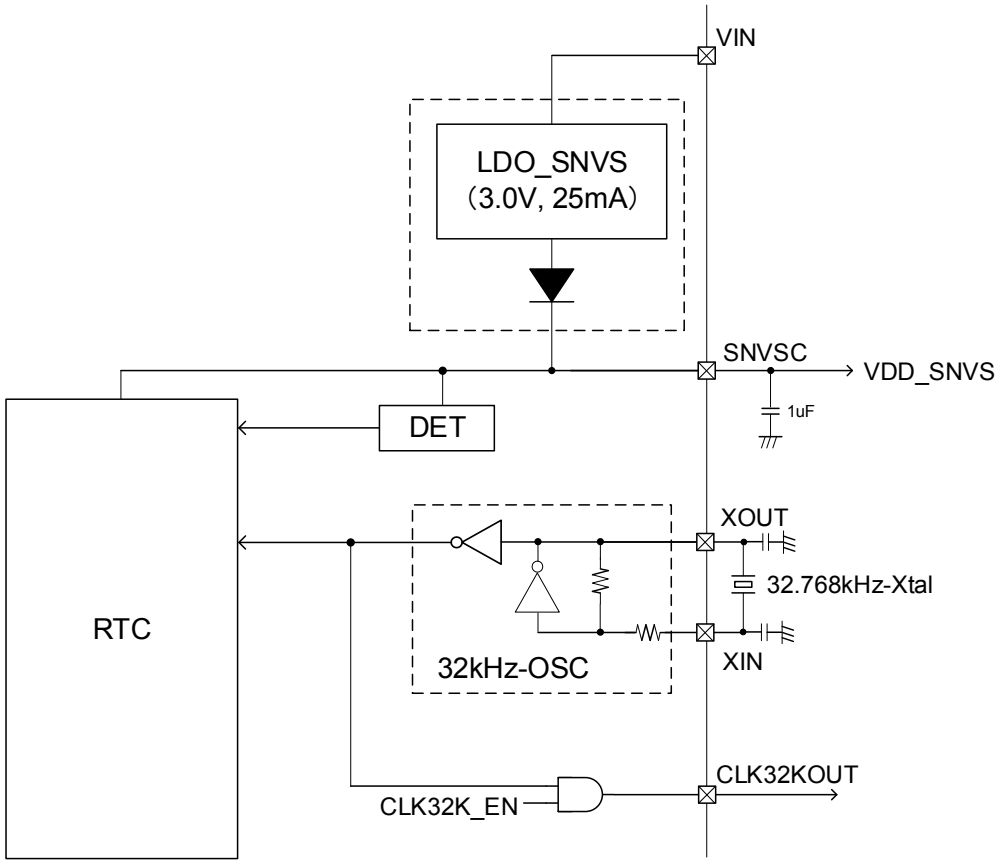


Figure 10. RTC Block Diagram

(1) Oscillation Adjustment

The oscillation adjustment circuit can be used to correct a time count gain or loss with high precision.
This is done by varying the number of 1-second clock pulses once every 20 or 60 seconds.
When DEV bit in the TRIM Register is set to "0", the Oscillation Adjustment Circuit varies the number of 1-second clock pulses once every 20 seconds. When the DEV bit in the TRIM Register is set to "1", the Oscillation Adjustment Circuit varies the number of 1-second clock pulses once every 60 seconds.
The Oscillation Adjustment Circuit can be disabled by writing the settings "*,0,0,0,0,0,*" ("*" represents "0" or "1") to the TRIM[6:0] bits of the TRIM Register. Conversely, when such oscillation adjustment is to be made, an appropriate oscillation adjustment value can be calculated using the equation below.

(a) When oscillation frequency is higher than target frequency

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10 + 1$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency} + 0.0333)}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30 + 1$$

Oscillation frequency: Frequency of clock pulse output from CLK32KOUT pin
Target frequency: Desired frequency to be set
Generally, a 32.768kHz quartz crystal unit has temperature characteristics that support the highest oscillation frequency at normal temperature. Consequently, the quartz crystal unit is recommended to have target frequency settings ranging from 32.768 to 32.76810 kHz (+3.05ppm relative to 32.768kHz).
Oscillation adjustment value: Value that is to be written to the TRIM[6:0] bits of the TRIM register
This value is represented in 7-bit coded decimal notation.

(b) When oscillation frequency is equal to target frequency

Oscillation adjustment value = 0, +1, -64, or -63.

(c) When oscillation frequency is lower than target frequency

When setting DEV bit to 0:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 10$$

When setting DEV bit to 1:

$$\text{Oscillation adjustment value} = \frac{(\text{Oscillation frequency - Target Frequency})}{\text{Oscillation frequency} \times 1.017 \times 10^{-6}}$$
$$\approx (\text{Oscillation frequency - Target Frequency}) \times 30$$

Sample oscillation adjustment value calculations follow.

(ex.A) For an oscillation frequency = 32768.85Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32768.85 - 32768.05 + 0.1}{32768.85 \times 3.051 \times 10^{-6}} \\ &\approx (32768.85 - 32768.05) \times 10 + 1 \\ &= 9\end{aligned}$$

In this instance, write the settings "00001001" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

When setting DEV bit to 1:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32768.85 - 32768.05 + 0.0333}{32768.85 \times 1.017 \times 10^{-6}} \\ &\approx (32768.85 - 32768.05) \times 30 + 1 \\ &= 25\end{aligned}$$

In this instance, write the settings "10011001" in the TRIM register.

(ex.B) For an oscillation frequency = 32762.22Hz and a target frequency = 32768.05Hz

When setting DEV bit to 0:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32762.22 - 32768.05}{32762.22 \times 3.051 \times 10^{-6}} \\ &\approx (32762.22 - 32768.05) \times 10 \\ &= -58\end{aligned}$$

To represent an oscillation adjustment value of -58 in 7bit coded decimal notation, subtract 58 (3Ah) from 128 (80h) to obtain 46h. In this instance, write the settings of "01000110" in the TRIM register. Thus, an appropriate oscillation adjustment value in the presence of any time count loss represents a distance from 80h.

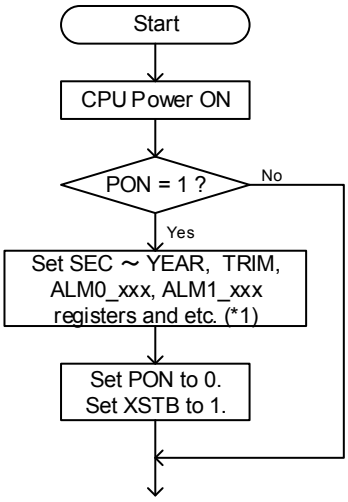
When setting DEV bit to 1:

$$\begin{aligned}\text{Oscillation adjustment value} &= \frac{32762.22 - 32768.05}{32762.22 \times 1.017 \times 10^{-6}} \\ &\approx (32762.22 - 32768.05) \times 30 \\ &= -175\end{aligned}$$

Oscillation adjustment value can be set from -62 to 63. Then, in this case, Oscillation adjustment value is out of range.

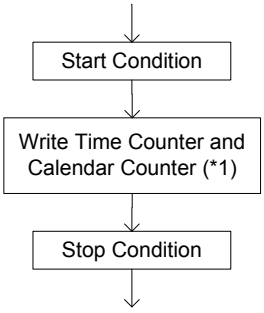
(3) Typical software-based operation

Initialization at Power-on



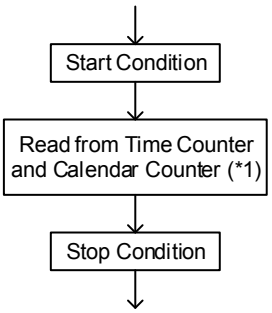
*1) This step involves ordinary initialization including, but not limited to, the Oscillation Adjustment Register and interrupt cycle settings.

Writing Time and Calendar Data



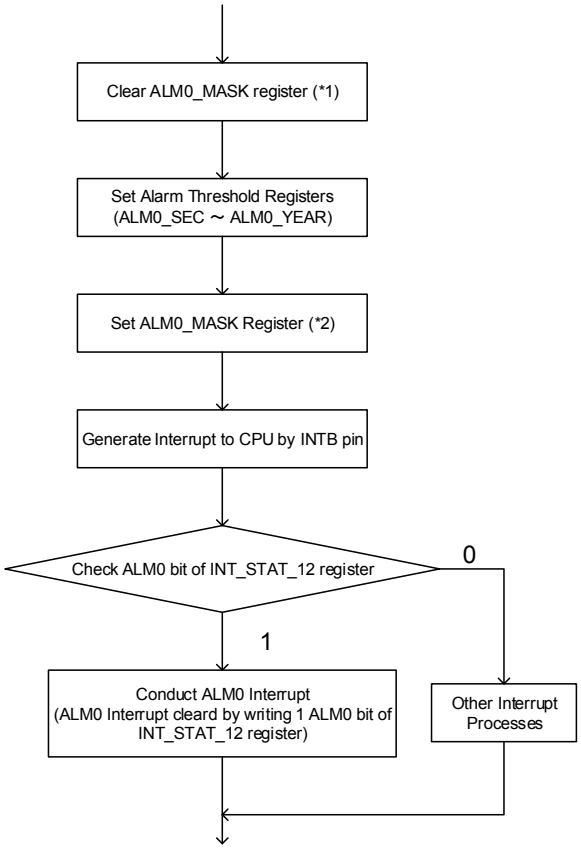
*1) It is recommended to also modify the sec register when one writes to the min~year registers.
When the seconds digit goes up while accessing I2C, the clock could assume an unpredictable value.
Writing to the sec register prevents the above behavior because less than 1Hz counter is cleared.

Reading Time and Calendar Data



*1) When reading clock and calendar counters, do not insert Stop Condition.

ALARM0 Interrupt Process



*1) This step is intended to disable the alarm interrupt circuit once by clearing ALM0_MASK register, in anticipation of a coincidental match between current time and preset alarm time as the alarm interrupt function is set.

*2) This step is intended to enable the alarm interrupt function after completion of all alarm interrupt settings.

7. Over Voltage Protection (OVP) Block

Features

- Single-input for the battery charger source: DCIN
- 30V over voltage protection for DCIN input.

8. Battery Charger Block

Features

- Supports battery insertion and removal detection
- JEITA-compliant Battery Charging Profile with thermal control of charging current and voltage settings. This is achieved by measuring the temperature of an external thermistor (The Initial setting of BD71815AGW is adjusted to TDK NTCG163JF103FT1S).
- Supports battery supplement mode
- Automatic or manual (software) control of Watch Dog Timer while Pre–charging and Fast-charging
- Charger statuses or Error conditions are indicated on CHGLED output (for LED lighting)

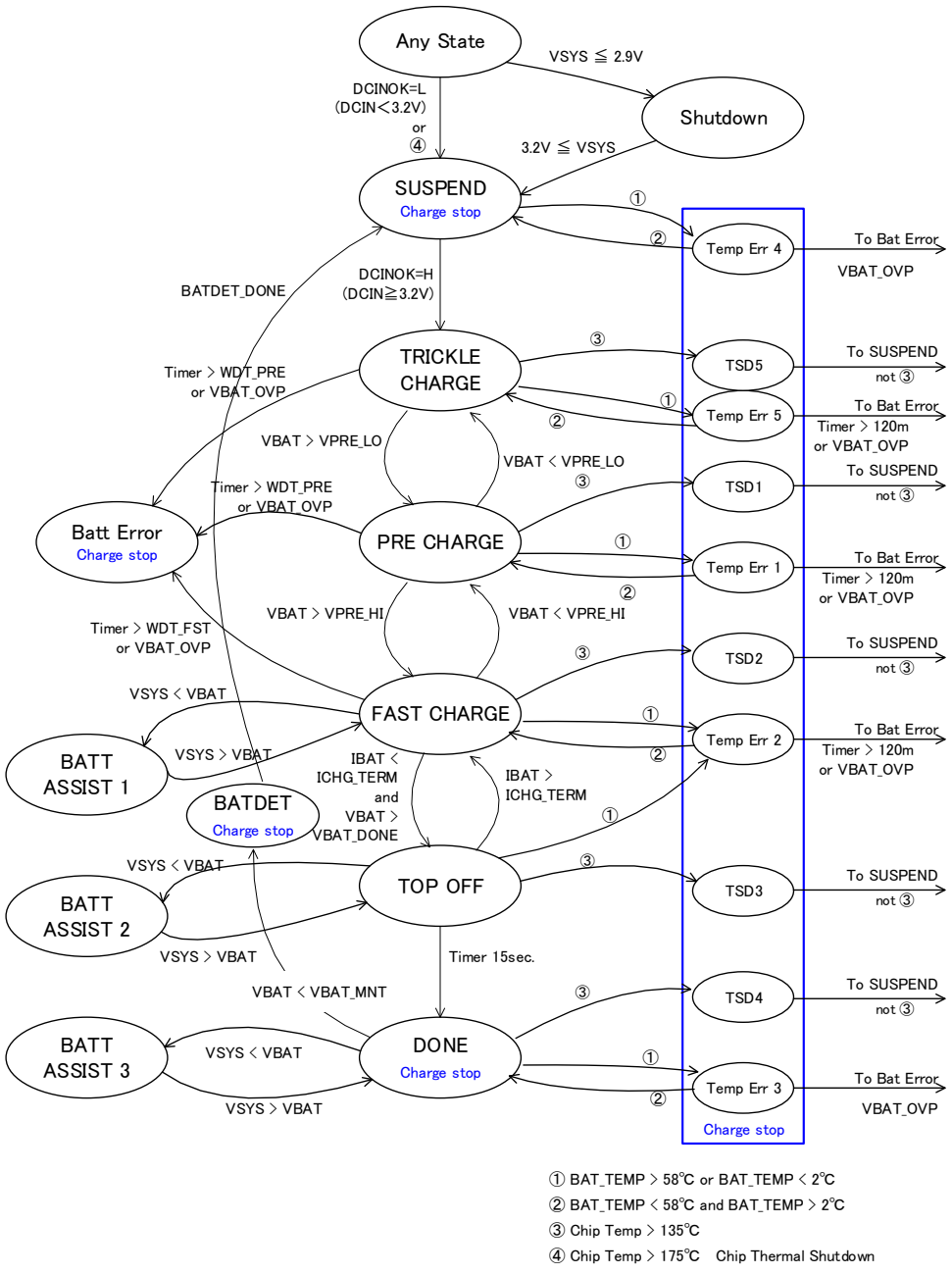


Figure 11. State Diagram of Battery Charger

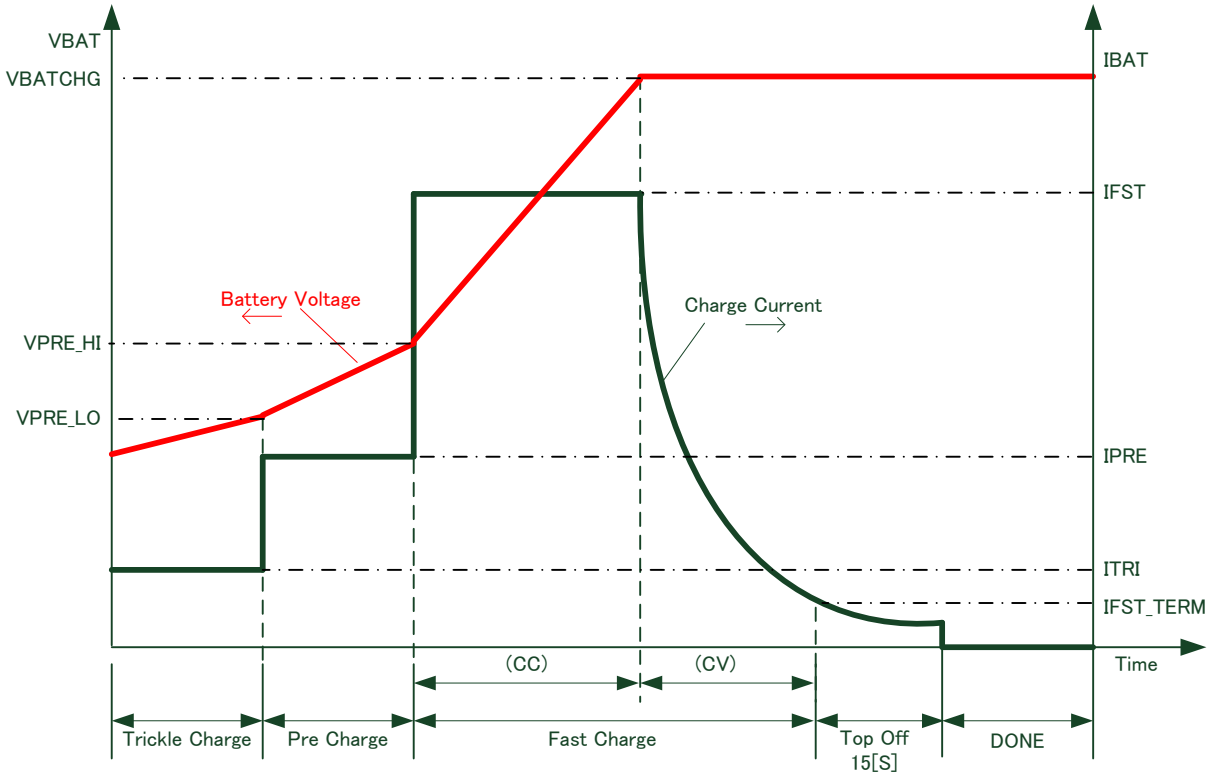


Figure 12. Battery Charger Output Control

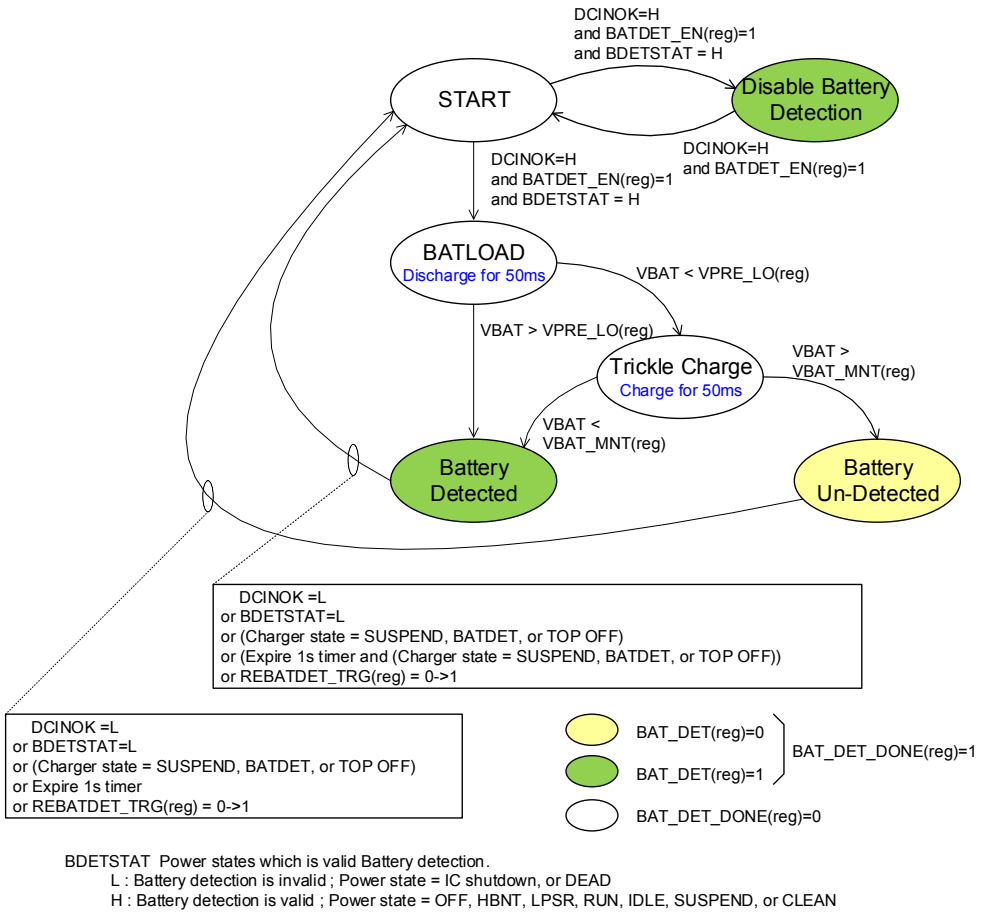


Figure 13. State Diagram of Battery Detection

BD71815AGW has four Watch Dog Timers.

(a) High Temperature Protection Timer
The High Temperature Protection Timer is a timer to count the duration that battery temperature is higher than T4 (default 58°C) (BAT_TEMP[2:0]=3h) at Temp_err1, Temp_err2 or Temp_err5 state. This timer counts down 1 in every 64 seconds and shifts to Batt Error state after 121 counts.

(b) Low Temperature Protection Timer
The Low Temperature Protection Timer is a timer to count the duration that battery temperature is less than T2 (default 2°C) (BAT_TEMP[2:0]=5h) at Temp_err1, Temp_err2 or Temp_err5 state. This timer counts down 1 in every 64 seconds and shifts to Batt Error state after 121 counts.

(c) Watch Dog Timer for TRICKLE CHARGE and PRE CHARGE states
During Trickle-charge or Pre-charge, this timer counts down once every 64 seconds and shifts to Batt Error state after 121 counts by default. The number of counts can be changed by register settings (WDT_AUTO and WDT_PRE).

Table 6. Watch Dog Timer for Pre-charging and Trickle-charging

39h: CHG_STATE	40h: BAT_TEMP[2:0]	47h: CHG_SET1		Initial set value	countdown value	threshold to Batt Error
		[7] WDT_DIS	[6] WDT_AUTO			
TRICKLE CHARGE(01h) or PRE CHARGE(02h)	ROOM(0h) or HOT1(1h) or HOT2(2h) or Temp. Disable(6h)	0	0	49h: WDT_PRE	-1	1
		0	1	122	-1	1

(d) Watch Dog Timer for FAST CHAREGE and TOP OFF states
During Fast-charge or TOPOFF, this timer counts down in every 512 seconds or 64 seconds, and shifts to Batt Error state after 601 counts. The counter speed depends on the battery temperature. The number of the counts can be changed by register settings (WDT_AUTO, WDT_FST, and COLD_ERR_EN).

Table 7. Fast-charging and TOPOFF Watch Dog Timer

39h:CHG_STATE	40h:BAT_TEMP[2:0]	47h: CHG_SET1			Initial set value	countdown value	threshold to Batt Error
		WDT_DIS	WDT_AUTO	COLD_ERR_EN			
TRICKLE CHARGE(01h) or TOP OFF(0Eh)	COLD1(4h)	0	0	1	1442	-1	3
		0	1	1	1442	-1	3
		0	0	0	WDT_FST * 8	-2	3
		0	1	0	1442	-2	3
	ROOM(0h) or HOT1(1h) or HOT2(2h) or Temp. Disable(6h)	0	0	1	WDT_FST * 8	-2	240
		0	1	1	1442	-2	240
		0	0	0	WDT_FST * 8	-2	240
		0	1	0	1442	-2	240

(1) Thermal Control for Charging

Charging current is controlled by the battery temperature, measured using an external thermistor.
In low-temperature condition, charging current is reduced to half of the set value ICHG.

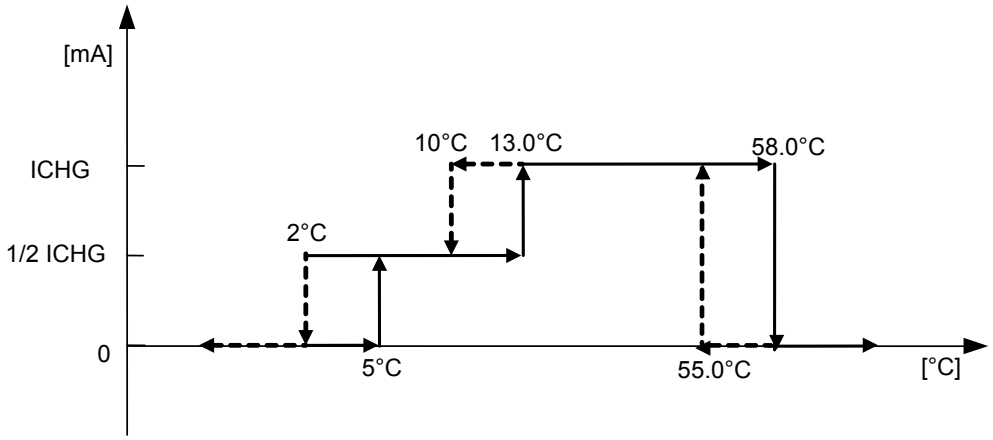


Figure 14. Charging Current vs. Battery Temperature

Charging voltage is also reduced by temperature and set by control registers.

Table 8. Charging Voltage vs. Battery Temperature

JEITA Temperature Range		Voltage Setting Register
T2 – T3	2°C to 45°C, (typ)	VBAT_CHG1
T3 – T5	45°C to 50°C, (typ)	VBAT_CHG2
T5 – T4	50°C to 58°C, (typ)	VBAT_CHG3

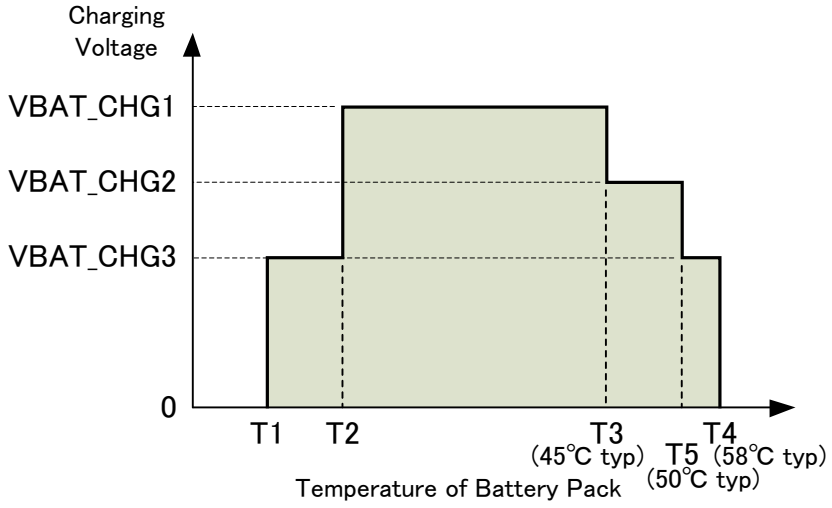


Figure 15. Charging Voltage vs. Battery Temperature

9. Coulomb Counter Block

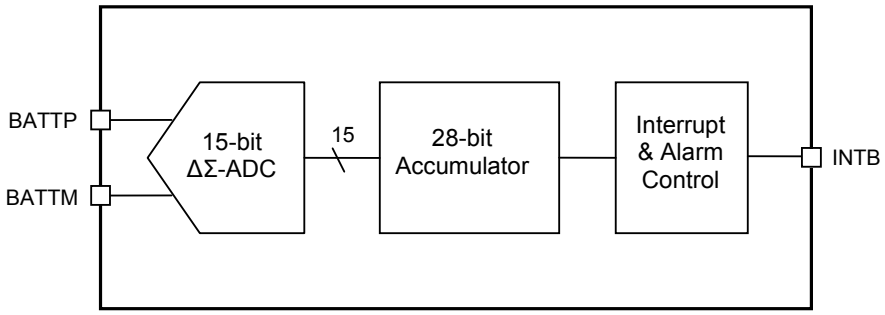


Figure 16. Coulomb Counter Block Diagram

Features

- 28-bit Coulomb Counter for battery fuel gauging
- 15-bit ΔΣ-ADC measures the battery's charge and discharge current by means of an external current sense resistor (10mΩ, ±1% or 30mΩ, ±1%).
- Charging/Discharging amount integration period : 1sec
- There are three programmable battery capacity thresholds for interrupt.

(1) Functions and Programmabilites

(a) 28-bit accumulator features

28-bit accumulator accumulates 15-bit ΔΣ-ADC results by each 1sec. The accumulated value is shown in CCNTD register. CCNTD value is accumulated when CCNTENB is set to 1. CCNTD value is held when CCNTENB is set to 0. When CCNTRST is set to 1, CCNTD value is cleared to 0.

(b) Three programmable Event Alarm outputs from INTB pin

BD71815AGW has alarm events using Coulomb Counter. The elements are shown in Table 9.

Table 9. Alarm events using Coulomb Counter

Status register name	Interrupt register name	Event	Condition
CC_MON1	CC_MON1_DET	Coulomb counter near full capacity alarm (AMBLED is turned off and GRNLED is turned on when CHGDONE_LED_EN(reg)=1)	0 : CCNTD ≤ CC_BATCAP1_TH(reg) 1 : CCNTD > CC_BATCAP1_TH(reg)
CC_MON2	CC_MON2_DET	Coulomb counter general alarm 2	0 : CCNTD ≥ CC_BATCAP2_TH(reg) 1 : CCNTD < CC_BATCAP2_TH(reg)
CC_MON3	CC_MON3_DET	Coulomb counter general alarm 3	0 : CCNTD ≥ CC_BATCAP3_TH(reg) 1 : CCNTD < CC_BATCAP3_TH(reg)
OCUR1	OCUR1_DET OCUR1_RES	Battery over current alarm 1	0 : CURCD < OCURTHR1_TH(reg) 1 : CURCD ≥ OCURTHR1_TH(reg) more than OCURDUR1(reg) time
OCUR2	OCUR2_DET OCUR2_RES	Battery over current alarm 2	0 : CURCD < OCURTHR2_TH(reg) 1 : CURCD ≥ OCURTHR2_TH(reg) more than OCURDUR2(reg) time
OCUR3	OCUR3_DET OCUR3_RES	Battery over current alarm 3	0 : CURCD < OCURTHR3_TH(reg) 1 : CURCD ≥ OCURTHR3_TH(reg) more than OCURDUR3(reg) time

10. 12-bit ADC (SAR) Block

Features

- 12-bit Successive Approximation Register A/D Converter
- Conversion period: 40µs
- Input Voltage range: 0.4V to 5.6V (VBAT for Battery voltage monitor)
- Input Voltage range: 0.5V to 7.0V (VSYS for System input voltage monitor)
- Input Voltage range: 0.1V to 1.4V (Vf for BD71815AGW die temperature monitor)
- Input Voltage range: 0.1V to 1.4V (TS for Battery temperature monitor)
- Input Voltage range: -30mV to 30mV (BATTP for Battery current monitor)
- Input Voltage range : 1.2V to 16.8V (DCIN for DCIN voltage monitor)

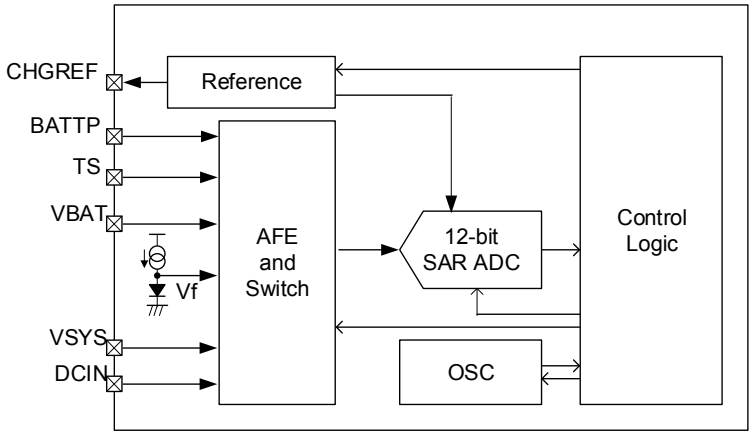


Figure 17. 12-bit ADC Block Diagram

11. Battery Monitor Block

BD71815AGW has alarm events using 12-bit SAR ADC. The elements are shown in Table 10.

Table 10. Alarm events using 12-bit SAR ADC

Status register name	Interrupt register name	Monitor terminal	Event	Condition
VBAT_OV	VBAT_OV_DET VBAT_OV_RES	VBAT	Battery voltage exceeds over voltage	0 : VBAT ≤ VBAT_OVP(reg) - 150mV 1 : VBAT ≥ VBAT_OVP(reg)
LOW_BAT	VBAT_LO_DET VBAT_LO_RES	VBAT	Battery voltage fall below low voltage	0 : VBAT > VBAT_LO(reg) 1 : VBAT ≤ VBAT_LO(reg)
VBAT_SHORT	VBAT_SHT_DET VBAT_SHT_RES	VBAT	Battery shorted to GND	0 : VBAT ≥ 1.6V 1 : VBAT ≤ 1.5V
DBAT_DET	DBAT_DET	VBAT	Dead battery detection	0 : Not detected 1: Detected = VBAT ≤ VBAT_LO(reg) more than TIM_DBP(reg) time
VRECHG_DET	BAT_MNT_IN BAT_MNT_OUT	VBAT	Battery voltage fall below to re-charge voltage	0 : VBAT > VBAT_MNT(reg) 1 : VBAT ≤ VBAT_MNT(reg)
N/A	VBAT_MON_DET VBAT_MON_RES	VBAT	Battery voltage general alarm	Detect :VBAT ≥ VBAT_TH(reg) -> VBAT ≤ VBAT_TH(reg) Resume : VBAT ≤ VBAT_TH(reg) -> VBAT ≥ VBAT_TH(reg)
VSYS_LO	VSYS_LO_DET VSYS_LO_RES	VSYS	VSYS voltage fall below low voltage	0 : VSYS ≤ VSYS_MIN(reg) 1 : VSYS ≥ VSYS_MAX(reg)
N/A	VSYS_MON_DET VSYS_MON_RES	VSYS	VSYS voltage general alarm	Detect : VSYS ≥ VSYS_TH(reg) -> VSYS ≤ VSYS_TH(reg) Resume : VSYS ≤ VSYS_TH(reg) -> VSYS ≥ VSYS_TH(reg)
DCIN_CLPS_DET	DCIN_CLPS_IN DCIN_CLPS_OUT	DCIN	DCIN anti-collapse detection	0 : DCIN ≥ DCIN_CLPS(reg) 1 : VSYS < DCIN_CLPS(reg)
N/A	DCIN_MON_DET DCIN_MON_RES	DCIN	DCIN voltage general alarm	Detect : DCIN ≥ DCIN_TH(reg) -> DCIN ≤ DCIN_TH(reg) Resume : DCIN ≤ DCIN_TH(reg) -> DCIN ≥ DCIN_TH(reg)
OVBTMP	OVTMP_DET OVTMP_RES	TS	Battery over temperature detection	0 : Not detected 1 : Detected : BTMP < OVBTMPTHR(reg) more than OVBTMPDUR(reg) time
LOBTMP	LOTMP_DET LOTMP_RES	TS	Battery low temperature detection	0 : Not detected 1 : Detected : BTMP > LOBTMPTHR(reg) more than LOBTMPDUR(reg) time
N/A	VF_DET VR_RES	Vf	Die temperature general alarm	Detect : VF ≤ VF_TH(reg) -> VF > VF_TH(reg) Resume : VF > VF_TH(reg) -> VF ≤ VF_TH(reg)
N/A	VF125_DET VR125_RES	Vf	Die temperature over 125°C detection	Detect : VF ≤ 125°C -> VF > 125°C Resume : VF > 125°C -> VF ≤ 125°C

12. White LED Boost Converter

Features

- Support series 6 LED lights for front light
- LED is ON/OFF by I2C register
- LED Current range : 10,20,30,50,70,100,200,300,500,700 uA,1~25mA(1mA Step)
- Protection Function : Over Current Protection, Over Voltage Protection, Short Circuit Protection

13. I2C Bus Interface Block

The I2C-compatible synchronous serial interface provides access to programmable functions and registers on the device.

This protocol uses a two-wire interface for bi-directional communication between LSI's connected to the bus.

The two interface lines are Serial Data Line (SDA), and Serial Clock Line (SCL). These lines should be connected to the power supply DVDD by a pull-up resistor and remain high even when the bus is idle.

(1) Start and Stop Conditions

When SCL is high, pulling SDA low produces a start condition, while pulling SDA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition happens.

During read, a stop condition causes reading to terminate, after which the chip enters the standby state. During write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. When writing is completed, the chip enters the standby state.

Two or more start conditions cannot be entered consecutively.

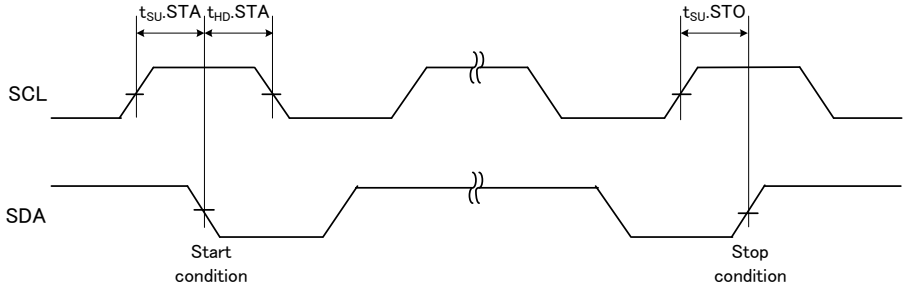


Figure 18. Start and Stop Conditions

(2) Modifying Data

Data on the SDA input can be modified while SCL is low. When SCL is high, modifying the SDA input means a start or stop condition.

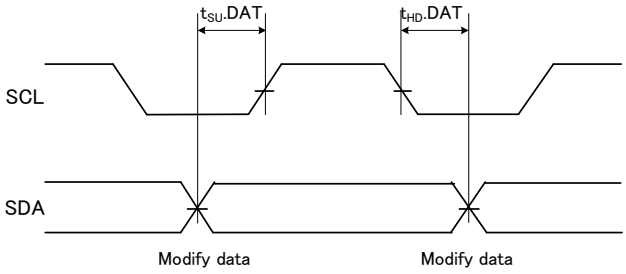


Figure 19. Modifying Data

(3) Acknowledge

Data is transmitted and received in 8-bit units. The receiver sends an acknowledge signal by outputting low on SDA in the 9th clock cycle, indicating that it has received data normally. The transmitter releases the bus in the 9th clock cycle to receive an acknowledge signal.

During write, the chip is always the receiver so that it outputs an acknowledge signal each time it has received eight bits of data.

During read, the chip outputs an acknowledge signal after it receives an address following a start condition. Then, it outputs read data and releases the bus to wait for an acknowledge signal from the master. When it detects an acknowledge signal, it outputs data at the next address if it does not detect a stop condition. If the chip does not detect an acknowledge signal, it stops read operation and enters the standby state wherein a stop condition occurs subsequently.

If the chip does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

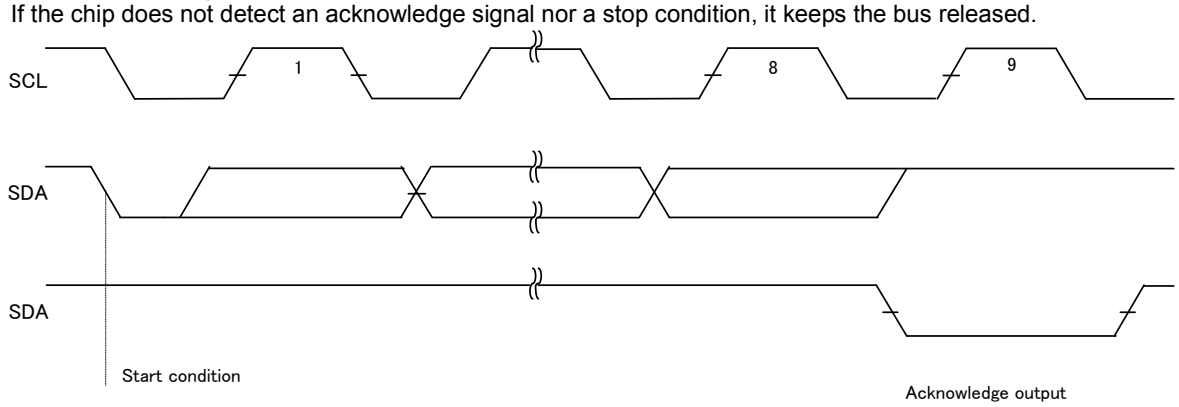


Figure 20. Acknowledge

(4) Device Addressing

After a start condition occurs, a 7-bit device address and a 1-bit read/write instruction code are sent as input to the chip. The device address occupies the upper seven bits, which must always be “1001011”.

The least significant bit (R/W:READ/WRITE) indicates a read instruction when set to 1 and a write instruction when set to 0. An instruction is not executed if the device address does not match the specified value.

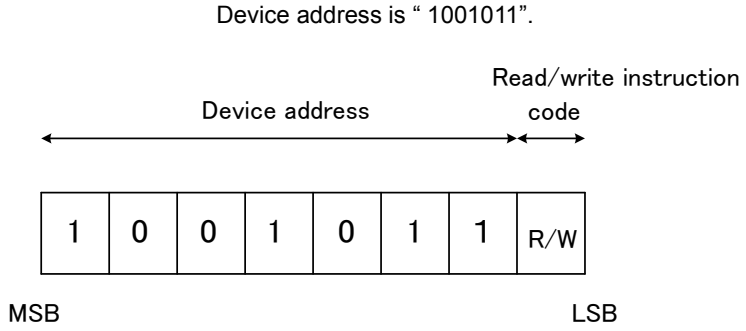


Figure 21. Device Addressing

(5) Write/Read operation

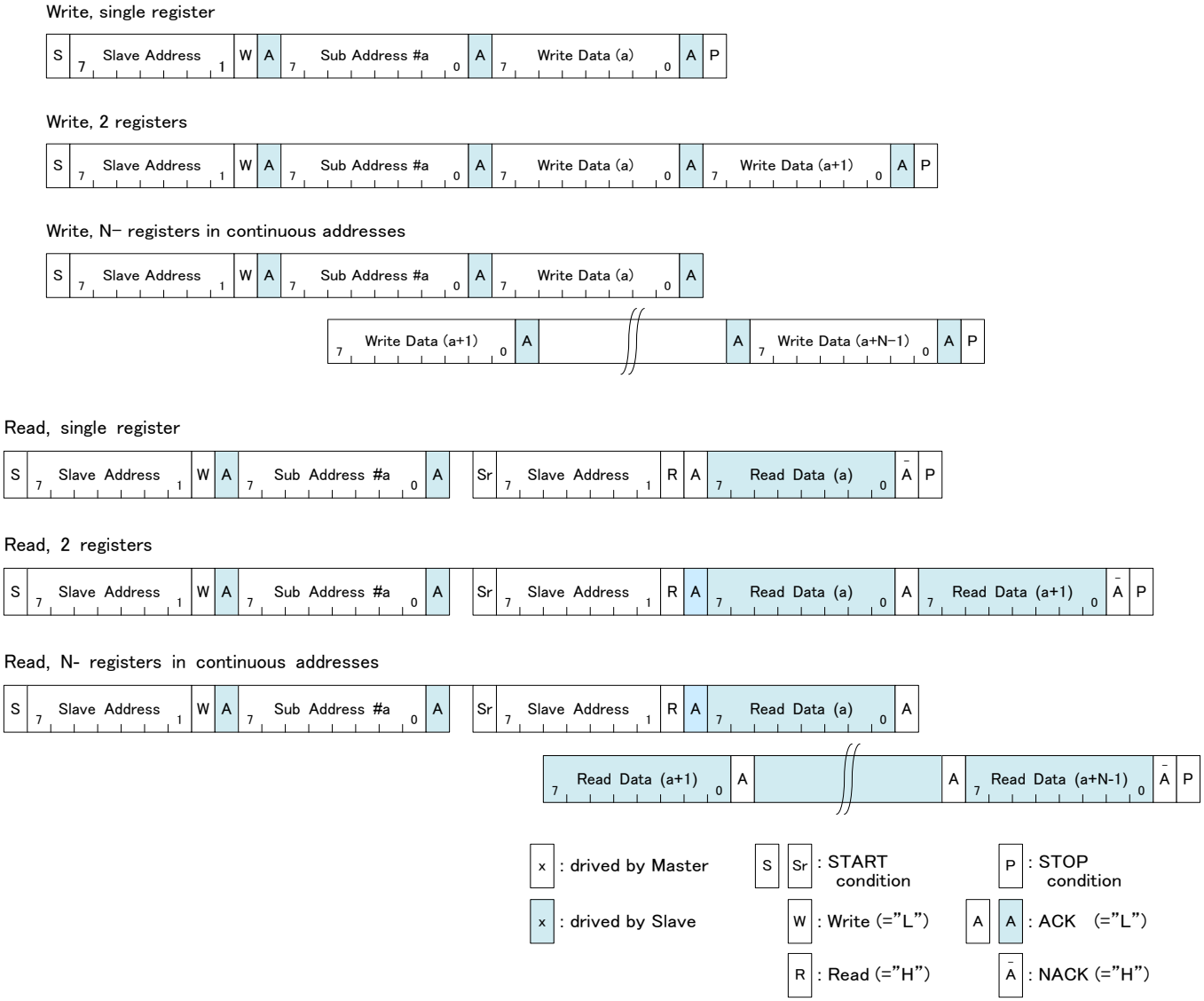


Figure 22. I2C Write / Read Operation

(6) Pulling up the SDA and SCL pins

This IC requires SDA and SCL pins to be pulled up with an external resistor. The values of the pull-up resistors are determined by the capacitance of the bus. Exceedingly large resistance combined with a given bus capacitance will result to a rise time that would violate the maximum rise time specification. On the other hand, insufficiently small resistance will result in a contention with the pull-down transistor on either slave or master. The recommended pull-up resistance range is 1kohm to 5kohm.

Consider the DVDD related input threshold of VIH = 0.7xVDD and VIL = 0.3xVDD for the purposes of RC time constant calculation.

$V(t1) = 0.3 \times DVDD = DVDD\ (1 - e^{-t1\ /\ RC})$; then $t1 = 0.3566749 \times RC$

$V(t2) = 0.7 \times DVDD = DVDD\ (1 - e^{-t2\ /\ RC})$; then $t2 = 1.2039729 \times RC$

$T = t2 - t1 = 0.8473 \times RC$

To determine the value of the pull-up resistance, you can calculate it by using the equation R=t/(0.8473C).

t : SDA, SCL rise time to meet the I2C AC specification

C : Total bus capacitance on each SDA, SCL line

(7) Limitation of I2C

Write data is synchronized with the internal clock (32.768 kHz RTC crystal clock). If internal FIFO is full, an acknowledge is not generated for write operations. An example of this situation is continuous addressing access with more than 294 kHz in I2C.

With I2C single write mode, BD71815AGW write the register after 3 or 4 RTC crystal clock time when stop condition is happened.

14. Interrupt Handling

The system is informed about important events through interrupts. Enabled interrupt events are signaled to the processor by driving the INTB pin low.
Each interrupt can be disabled by setting the corresponding enable bit to 0.
Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing “1” to the appropriate bit in the Interrupt Status register; this will also cause the INTB pin to go high. If there are multiple interrupt bits, the INTB pin will remain low until all are cleared. If a new interrupt occurs while the processor clears an existing interrupt bit, the INTB pin will remain low.
The IC powers up with all interrupts disabled, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can enable the interrupt bits of interest.
Interrupts generated by external events are debounced; therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are documented in the Interrupt summary. Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

Table 11. Interrupt summary

Interrupt Event	Register Map				Debounce Interval (3 times match)	Interrupt Event	Register Map				Debounce Interval (3 times match)
	Enable		Status/Clear				Enable		Status/Clear		
	Address	bit	Address	bit			Address	bit	Address	bit	
LED_SCP	8B	7	98	7	1kHz	BAT_RMV	90	4	9D	4	128Hz
LED_OCP	8B	6	98	6	1kHz	TMP_OUT_DET	90	1	9D	1	1Hz
LED_OVP	8B	5	98	5	1kHz	TMP_OUT_RES	90	0	9D	0	1Hz
BUCK5FAULT	8B	4	98	4	1kHz	VBAT_OV_DET	91	7	9E	7	128Hz
BUCK4FAULT	8B	3	98	3	1kHz	VBAT_OV_RES	91	6	9E	6	128Hz
BUCK3FAULT	8B	2	98	2	1kHz	VBAT_LO_DET	91	5	9E	5	128Hz
BUCK2FAULT	8B	1	98	1	1kHz	VBAT_LO_RES	91	4	9E	4	128Hz
BUCK1FAULT	8B	0	98	0	1kHz	VBAT_SHT_DET	91	3	9E	3	128Hz
DCIN_OV_DET	8C	5	99	5	1kHz	VBAT_SHT_RES	91	2	9E	2	128Hz
DCIN_OV_RES	8C	4	99	4	1kHz	DBAT_DET	91	1	9E	1	128Hz
DCIN_CLPS_IN	8C	3	99	3	4kHz	VBAT_MON_DET	92	1	9F	1	128Hz
DCIN_CLPS_OUT	8C	2	99	2	4kHz	VBAT_MON_RES	92	0	9F	0	128Hz
DCIN_RMV	8C	1	99	1	1kHz	CC_MON3_DET	93	2	A0	2	1Hz
WDOGB	8D	6	9A	6	RTC	CC_MON2_DET	93	1	A0	1	1Hz
DCIN_MON_DET	8D	1	9A	1	4kHz	CC_MON1DET	93	0	A0	0	1Hz
DCIN_MON_RES	8D	0	9A	0	4kHz	OCUR3_DET	94	5	A1	5	4kHz
VSYS_MON_DET	8E	7	9B	7	128Hz	OCUR3_RES	94	4	A1	4	4kHz
VSYS_MON_RES	8E	6	9B	6	128Hz	OCUR2_DET	94	3	A1	3	4kHz
VSYS_LO_DET	8E	3	9B	3	128Hz	OCUR2_RES	94	2	A1	2	4kHz
VSYS_LO_RES	8E	2	9B	2	128Hz	OCUR1_DET	94	1	A1	1	4kHz
VSYS_UV_DET	8E	1	9B	1	128Hz	OCUR1_RES	94	0	A1	0	4kHz
VSYS_UV_RES	8E	0	9B	0	128Hz	VF_DET	95	7	A2	7	1Hz
CHG_TRNS	8F	7	9C	7	none	VF_RES	95	6	A2	6	1Hz
TMP_TRNS	8F	6	9C	6	none	VF125_DET	95	5	A2	5	128Hz
BAT_MNT_IN	8F	5	9C	5	1kHz	VF125_RES	95	4	A2	4	128Hz
BAT_MNT_OUT	8F	4	9C	4	1kHz	OVTMP_DET	95	3	A2	3	1Hz
CHG_WDT_EXP	8F	3	9C	3	RTC	OVTMP_RES	95	2	A2	2	1Hz
EXTEMP_TOUT	8F	2	9C	2	RTC	LOTMP_DET	95	1	A2	1	1Hz
BTA_ILIM	8F	0	9C	0	128Hz	LOTMP_RES	95	0	A2	0	1Hz
TH_DET	90	7	9D	7	1Hz	ALM2	96	2	A3	2	128Hz
TH_RMV	90	6	9D	6	1Hz	ALM1	96	1	A3	1	128Hz
BAT_DET	90	5	9D	5	128Hz	ALM0	96	0	A3	0	128Hz

Note1: 1 kHz of this table means 1.024 kHz, and 4 kHz of this table means 4.096 kHz.

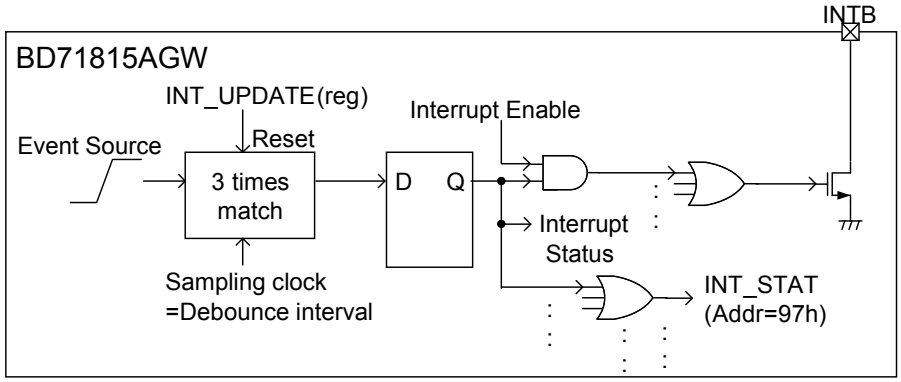


Figure 23 Interrupt Block Diagram

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Maximum Supply Voltage 1 DCIN	$VDCIN_{MAX}$	30	V
Maximum Supply Voltage 2 VIN, PVIN1,2,3,4,5,6 VINL1, VINL2, VBAT	VIN_{MAX} $PVIN_{MAX}$ $VINL_{MAX}$ $VBAT_{MAX}$	6	V
Maximum Supply Voltage 3 DVDD	$VDVDD_{MAX}$	4.5	V
Maximum Input Voltage 1 VO6, LX6	$VO6IN_{MAX}$ $LX6IN_{MAX}$	30	V
Maximum Input Voltage 2 FB1,2,3,4,5,6, LX1,2,3,4,5, HX6, VO1,2,3,4,5,VOLPSR, DVREFIN, VODVREF, CLK32KOUT, POR, INTB, READY, VSYS, PGATE, CHGLED, GPO1, PWRON, STANDBY, RESETINB, WDOGB, LDO4VEN, LDO5VSEL, SDA, SCL, XIN, XOUT, TS, BATTP, BATTM	$VMAXIN_{MAX}$	6	V
Maximum Input Voltage 3 SNVSC	$VSNVSCIN_{MAX}$	4.5	V
Maximum Input Voltage 4 CHGREF	$VCHGREF_{MAX}$	$VSNVSCIN_{MAX}$ + 0.3	V
Operating Temperature Range	Topr	-40 to +85	℃
Storage Temperature Range	Tstg	-55 to +125	℃

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)	Unit
UCSP55M4C(BD71815AGW)			
Junction to Ambient	θ_{JA}	69.0	°C/W

*(Note 1)*Based on Rohm's standard board

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
Input Voltage Range 1 DCIN	VDCIN	3.5 to 28	V
Input Voltage Range 2(Note2) VIN, PVIN1,2,3,4	VIN PVIN	2.9 to 5.5	V
Input Voltage Range 3 VINL1, VINL2	VINL1 VINL2	1.8 to 5.5	V
Input Voltage Range 4 DVDD	VDVDD	1.5 to 3.4	V

(Note2) It is necessary to supply the same voltage to VIN, and PVIN1,2,3,4

Electrical Characteristics

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
Quiescent Circuit Current						
VBAT Circuit Current 1 (SNVS Mode)	IQVB1	-	20	70	μA	RTC, Coulomb Counter, and LDO_SNVS are ON DCINOK=L, DVDD=0V
VBAT Circuit Current 2 (LPSR Mode)	IQVB2	-	50	150	μA	RTC, Coulomb Counter, LDO_SNVS, LDO_LPSR, and LDO1 are ON DCINOK=L, DVDD=0V
VBAT Circuit Current 3 (SUSPEND Mode)	IQVB3	-	150	200	μA	RTC, Coulomb Counter, BUCK2,3,4 (Auto Mode), LDO_SNVS, LDO_LPSR, and LDO1,2,3 are ON DCINOK=L, DVDD=0V
VBAT Circuit Current 4 (RUN Mode)	IQVB4	-	45	70	mA	RTC, Coulomb Counter, BUCK1,2,3,4,5 (PWM fix Mode), LDO_SNVS, LDO_LPSR, LDO_DVREF and LDO1,2,4,5 are ON DCINOK=L, DVDD=0V
DVDD Circuit Current	IQDVDD	-	-	1	μA	
Voltage Detector – VIN Under Voltage						
Detect Voltage	UVLOVIN	2.4	2.5	2.6	V	VIN sweep down SNVS to Coin state
Release Voltage	RUVLOVIN	2.7	2.8	2.9	V	VIN sweep up Coin to SNVS state
Voltage Detector – SNVS Under Voltage						
Detect Voltage	UVLOSNVS	2.0	2.2	2.4	V	VIN sweep down Coin to Shutdown state
Release Voltage	RUVLOSNVS	2.15	2.35	2.55	V	VIN sweep up Shutdown to Coin state
GPO1						
Output L Level	VOL_GPO	-	-	0.4	V	I_{IN} = 1mA
Output Off Leak current	IOFF_GPO	-1	0	1	μA	VIN=VGPO=5.5V
Digital pin characteristics - Input1 (PWRON, STANDBY, WDOGB, LDO5_VSEL, LDO4_EN)						
Input "H" level	VIH1	1.44	-	-	V	
Input "L" level	VIL1	-	-	0.4	V	
STANDBY, WDOGB, LDO4_VEN, LDO5_VSEL Pull Down Resistance	RPD1	-	1.5	-	MΩ	
Digital pin characteristics – Input2 (RESETINB)						
RESETINB Input "H" level	VIH2	2.1	-	-	V	SNVS*0.7V
RESETINB Input "L" level	VIL2	-	-	0.9	V	SNVS*0.3V
RESETINB Pull Up Resistance	RPU2	-	10	-	kΩ	
Digital pin characteristics – Input3 (SCL, SDA)						
SCL,SDA Input "H" level	VIH3	DVDD x0.7	-	DVDD + 0.3	V	
SCL,SDA Input "L" level	VIL3	-0.3	-	DVDD x0.3	V	
SCL,SDA Input leak current	IIC3	-1	0	1	μA	
Digital pin characteristics - Output (SDA, POR, INTB,READY)						
SDA Output "L" level voltage	VOL1	-	-	0.4	V	IOL=6mA
POR, INTB,READY Output "L" level voltage	VOL2	-	-	0.4	V	IOL=1mA
Output Off Leak current	IOFF_NO	-1	0	1	μA	VIN=VO=5.5V

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
BUCK1 – VDD_ ARM						
Output Voltage	VOSW1	1.084	1.100	1.117	V	Initial value Io = 200mA, PWM Mode
Programmable Output Voltage Range	VORSW1	0.8	-	2	V	25mV step
Output Current	IOSW1	-	-	800	mA	
Load Stability	ΔVLSW1	-	10	20	mV	Io=1mA ~800mA
Efficiency	ηSW11	-	84	-	%	VIN =PVIN=3.6V, Io = 1mA, Vo = 1.1V Inductor Rdc=40mΩ
	ηSW12	-	88	-	%	VIN=PVIN = 3.6V, Io = 200mA, Vo = 1.1V Inductor Rdc=40mΩ
Oscillating Frequency	FOSW1	-	6	-	MHz	VIN=4.0V, Vo = 1.1V PWM mode, Io = 0mA
Turn-on Time	TONSW1	-	-	500	usec	
Discharge Resistance	RDISSW1	-	600	-	Ω	
Output Inductance	LBUCK1	0.22	0.47	1.0	μH	Ta = -40℃～85℃
Output Capacitance	CBUCK1	4.7	10	100	μF	Ta = -40℃～85℃ with BUCK's DC bias
BUCK2 – VDD_ SOC						
Output Voltage	VOSW2	0.985	1.000	1.015	V	Initial value Io = 200mA, PWM Mode
Programmable Output Voltage Range	VORSW2	0.8	-	2	V	25mV step
Output Current	IOSW2	-	-	1000	mA	
Load Stability	ΔVLSW2	-	10	20	mV	Io=1mA ~800mA
Efficiency	ηSW21	-	84	-	%	VIN =PVIN=3.6V, Io = 1mA, Vo = 1.0V Inductor Rdc=40mΩ
	ηSW22	-	88	-	%	VIN=PVIN = 3.6V, Io = 200mA, Vo = 1.0V Inductor Rdc=40mΩ
Oscillating Frequency	FOSW2	-	6	-	MHz	VIN=4.0V, Vo = 1.0V PWM mode, Io = 0mA
Turn-on Time	TONSW2	-	-	500	usec	
Discharge Resistance	RDISSW2	-	600	-	Ω	
Output Inductance	LBUCK2	0.22	0.47	1.0	μH	Ta = -40℃～85℃
Output Capacitance	CBUCK2	4.7	10	100	μF	Ta = -40℃～85℃ with BUCK's DC bias
BUCK3 – NVCC_1P8, VDDA_1P8						
Output Voltage	VOSW3	1.773	1.800	1.827	V	Initial value Io = 200mA, PWM Mode
Programmable Output Voltage Range	VORSW3	1.2	-	2.7	V	50mV step
Output Current	IOSW3	-	-	500	mA	
Load Stability	ΔVLSW3	-	10	20	mV	Io=1mA ~800mA
Efficiency	ηSW31	-	84	-	%	VIN =PVIN=3.6V, Io = 1mA, Vo = 1.8V Inductor Rdc=40mΩ
	ηSW32	-	88	-	%	VIN=PVIN = 3.6V, Io = 200mA, Vo = 1.8V Inductor Rdc=40mΩ
Oscillating Frequency	FOSW3	-	6	-	MHz	VIN=4.0V, Vo = 1.8V PWM mode, Io = 0mA
Turn-on Time	TONSW3	-	-	500	usec	
Discharge Resistance	RDISSW3	-	600	-	Ω	
Output Inductance	LBUCK3	0.22	0.47	1.0	μH	Ta = -40℃～85℃
Output Capacitance	CBUCK3	4.7	10	100	μF	Ta = -40℃～85℃ with BUCK's DC bias

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
BUCK4 – NVCC_DRAM						
Output Voltage	VOSW4	1.182	1.200	1.218	V	Initial value Io = 200mA, PWM Mode
Programmable Output Voltage Range	VORSW4	1.1	-	1.85	V	25mV step
Output Current	IOSW4	-	-	1000	mA	
Load Stability	ΔVLSW4	-	10	20	mV	Io=1mA ~800mA
Efficiency	ηSW41	-	84	-	%	VIN =PVIN=3.6V, Io = 1mA, Vo = 1.2V Inductor Rdc=40mΩ
	ηSW42	-	88	-	%	VIN=PVIN = 3.6V, Io = 200mA, Vo = 1.2V Inductor Rdc=40mΩ
Oscillating Frequency	FOSW4	-	6	-	MHz	VIN=4.0V, Vo = 1.2V PWM mode, Io = 0mA
Turn-on Time	TONSW4	-	-	500	usec	
Discharge Resistance	RDISSW4	-	600	-	Ω	
Output Inductance	LBUCK4	0.22	0.47	1.0	μH	Ta = -40℃～85℃
Output Capacitance	CBUCK4	4.7	10	100	μF	Ta = -40℃～85℃ with BUCK's DC bias
BUCK5 – Peripheral						
Output Voltage	VOSW5	3.251	3.300	3.350	V	Initial value Io = 200mA, PWM Mode
Programmable Output Voltage Range	VORSW5	1.8	-	3.3	V	50mV step
Output Current	IOSW5	-	-	1000	mA	
Load Stability	ΔVLSW5	-	10	20	mV	Io=1mA ~800mA
Efficiency	ηSW51	-	92	-	%	VIN =PVIN=3.6V, Io = 1mA, Vo = 3.3V Inductor Rdc=40mΩ
	ηSW52	-	94	-	%	VIN=PVIN = 3.6V, Io = 200mA, Vo = 3.3V Inductor Rdc=40mΩ
Oscillating Frequency	FOSW5	-	6	-	MHz	VIN=4.0V, Vo = 3.3V PWM mode, Io = 0mA
Turn-on Time	TONSW5	-	-	500	usec	
Discharge Resistance	RDISSW5	-	600	-	Ω	
Output Inductance	LBUCK5	0.22	0.47	1.0	μH	Ta = -40℃～85℃
Output Capacitance	CBUCK5	4.7	10	100	μF	Ta = -40℃～85℃ with BUCK's DC bias

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
LDO1 - NVCC_GPIO2						
Output Voltage	VOL1	3.250	3.300	3.350	V	Initial value Io=50mA
Programmable Output Voltage Range	VORL1	0.8	-	3.3	V	50mV step
Output Current	IOL1	-	-	100	mA	
Dropout Voltage	VODPL1	-	0.04	-	V	Io=50mA VINL1=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔVIL1	-	2	5	mV	VIN =PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL1	-	10	20	mV	Io=1mA～100mA
Discharge Resistance	RDISL1	-	600	-	Ω	
Ripple rejection ratio	RRL1	-	60	-	dB	VIN=PVIN=4.2V, VR=-20dBV, fR=120Hz, Io=50mA, Vo=1.2V, BW=20Hz～20kHz
Output Capacitor	COL1	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias
LDO2 - NVCC_3P3						
Output Voltage	VOL2	3.250	3.300	3.350	V	Initial value Io=50mA
Programmable Output Voltage Range	VORL2	0.8	-	3.3	V	50mV step
Output Current	IOL2	-	-	100	mA	
Dropout Voltage	VODPL2	-	0.04	-	V	Io=50mA VINL1=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔVIL2	-	2	5	mV	VIN =PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL2	-	10	20	mV	Io=1mA～100mA
Discharge Resistance	RDISL2	-	600	-	Ω	
Ripple rejection ratio	RRL2	-	60	-	dB	VIN=PVIN=4.2V, VR=-20dBV, fR=120Hz, Io=50mA, Vo=1.2V, BW=20Hz～20kHz
Output Capacitor	COL2	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias
LDO3 - VDDA_USB1,2_3P3						
Output Voltage	VOL3	3.250	3.300	3.350	V	Initial value Io=50mA
Programmable Output Voltage Range	VORL3	0.8	-	3.3	V	50mV step
Output Current	IOL3	-	-	50	mA	
Dropout Voltage	VODPL3	-	0.08	-	V	Io=50mA VINL1=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔVIL3	-	2	5	mV	VIN =PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL3	-	10	20	mV	Io=1mA～50mA
Discharge Resistance	RDISL3	-	600	-	Ω	
Ripple rejection ratio	RRL3	-	60	-	dB	VIN=PVIN=4.2V, VR=-20dBV, fR=120Hz, Io=50mA, Vo=1.2V, BW=20Hz～20kHz
Output Capacitor	COL3	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
LDO4 - SD Card / eMMC						
Output Voltage	VOL4L	3.250	3.300	3.350	V	Io=50mA
Programmable Output Voltage Range	VORL4	0.8	-	3.3	V	50mV step
Output Current	IOL4	-	-	400	mA	
Dropout Voltage	VODPL4	-	0.03	-	V	Io=50mA VINL2=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔVIL4	-	2	5	mV	VIN =PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL4	-	10	20	mV	Io=1mA～400mA
Discharge Resistance	RDISL4	-	600	-	Ω	
Ripple rejection ratio	RRL4	-	60	-	dB	VIN=PVIN=4.2V, VR=-20dBV, fR=120Hz, Io=50mA, Vo=1.2V, BW=20Hz～20kHz
Output Capacitor	COL4	1.0	2.2	-	μF	Ta=-40～85°C, with LDO's DC bias
LDO5 - SD Card / eMMC Interface						
Output Voltage	VOL5L	3.250	3.300	3.350	V	LDO5VSEL=L Io=50mA
	VOL5H	1.773	1.800	1.827	V	LDO5VSEL=H Io=50mA
Programmable Output Voltage Range	VORL5	0.8	-	3.3	V	50mV step
Output Current	IOL5	-	-	250	mA	
Dropout Voltage	VODPL5	-	0.04	-	V	Io=50mA VINL2=3.2V (Vo=3.3V setting)
Input Voltage Stability	ΔVIL5	-	2	5	mV	VIN =PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL5	-	10	20	mV	Io=1mA～250mA
Discharge Resistance	RDISL5	-	600	-	Ω	
Ripple rejection ratio	RRL5	-	60	-	dB	VIN=PVIN=4.2V, VR=-20dBV, fR=120Hz, Io=50mA, Vo=1.2V, BW=20Hz～20kHz
Output Capacitor	COL5	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias
LDO_SNVS - SNVS						
Output Voltage	VOL6	2.94	3.00	3.06	V	Io=10mA
Output Current	IOL6	-	-	25	mA	
Input Voltage Stability	ΔVIL6	-	2	5	mV	VIN= PVIN=3.5~4.5V, Io=10mA
Load Stability	ΔVLL6	-	10	20	mV	Io=1mA～25mA
Discharge Resistance	RDISL6	-	600	-	Ω	
Output Capacitor	COL6	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias
LDO_LPSR - LPSR, NVCC_GPO1						
Output Voltage	VOL7	1.773	1.800	1.827	V	Io=50mA
Output Current	IOL7	-	-	100	mA	
Input Voltage Stability	ΔVIL7	-	2	5	mV	VIN= PVIN=3.5~4.5V, Io=50mA
Load Stability	ΔVLL7	-	10	20	mV	Io=1mA～100mA
Discharge Resistance	RDISL7	-	600	-	Ω	
Output Capacitor	COL7	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
LDO_DVREF - DDR_VREF						
Output Voltage	VOL8	DVREFIN x0.49	DVREFIN x0.50	DVREFIN x0.51	V	Io=5mA
Output Current	IOL8	-	-	10	mA	
Input Voltage Stability	ΔVIL8	-	2	5	mV	VIN= PVIN=3.5~4.5V, Io=5mA
Load Stability	ΔVLL8	-	10	20	mV	Io=1mA ~ 10mA
Discharge Resistance	RDISL8	-	600	-	Ω	
Output Capacitor	COL8	0.47	1	-	μF	Ta=-40～85°C, with LDO's DC bias
RTC						
Input Clock Frequency	RTCLKIN	-	32.768	-	kHz	
Output Clock Frequency Drift	RTCLKD	−100	-	100	ppm	(Note1)
Oscillator Stabilization Time	STBTIME	-	-	1000	msec	Within 3% of target frequency
Oscillator Stop Detection	STPDET	-	-	150	μsec	
RTC Output Buffer (CLK32KOUT)						
Output Frequency	RTCLK	-	32.768	-	KHz	With external crystal
Output Duty Cycle	RTCDTY	30	50	70	%	
Output L Level Voltage	VOL32K	-	-	0.4	V	I_{IN} = 1mA
Output Off Leak current	IOFF32K	-1	0	1	μA	VIN=VCLK32KOUT=5.5V Open drain output OFF mode
RTC Calibration Characteristics						
Calibration Range	RTCCR	−126	-	126	ppm	
Step Size	RTCCSTP	-	2	-	ppm	
Correction Interval	RTCCCI	-	30	-	sec	
Li-ion Battery Charger – OVP						
DCIN UVLO release voltage	RUVLODCIN	3.7	3.8	3.9	V	DCIN rising
DCIN UVLO hysteresis range	HUVLODCIN	100	150	200	mV	DCIN falling
DCIN OVP detection voltage	OVPDCIN	6.3	6.5	6.7	V	DCIN rising
DCIN OVP hysteresis range	HOVPDCIN	100	150	200	mV	
VSYS Output Voltage	VOVSYS	4.55	4.75	4.95	V	DCIN=5.0V input
Voltage Output turn-on time	TDCIN_ON	-	5	10	msec	
DCIN leakage current in OVP state	ILDCIN	-	-	2	mA	DCIN < 28V

(Note1) Frequency stability over temperature depends on the characteristics of the crystal unit which is expressed as a quadratic function. Recommended crystal unit is FC-135(Seiko Epson).

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V, DCIN=5.0V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
Li-ion Battery Charger						
Fast Charging current range	IBATR_INT	100	-	500	mA	100mA step Internal MOS mode
	IBATR_EXT	100	-	2000	mA	100mA step External MOS mode
Fast Charging current accuracy	IBATCHG _ACC	-	±10	-	%	Ichg=500mA VBAT=3.6V
Pre Charging current	IBATPRE	70	100	130	mA	Initial value VBAT=3.3V
Pre Charging current range	IBATPRER	50	-	375	mA	
Trickle Charging current	IBATTRI	5	10	15	mA	Initial value VBAT=3.0V
TricKle Charging Current range	IBATTRKR	2.5	-	25	mA	10mA step
Transition Voltage from Trickle Charging to Pre Charging	VPRE_LOW	2.9	3.0	3.1	V	Initial value VBAT rising
Transition Voltage range from Trickle Charging to Pre Charging	VPRE_LOWR	2.1	-	3.6	V	VBAT rising, 100mV step
Transition Voltage from Pre Charging to Fast Charging	VPRE_HIGH	3.2	3.3	3.4	V	Initial value VBAT rising
Transition Voltage range from Pre Charging to Fast Charging	VPRE_HIGHR	2.1	-	3.6	V	VBAT rising, 100mV step
Battery Charging voltage	VCHG	4.18	4.2	4.22	V	Initial value
Battery Charging voltage range	VCHGR	3.72	-	4.34	V	20mV step
Battery OVP detection	VBOVP	4.15	4.25	4.35	V	Initial value
Battery OVP detection range	VBOVPR	4.2	-	4.6	V	50mV step
Charging termination current range	ICHGTRMR	10	-	200	mA	
Charging termination current accuracy	ICHGTRM _ACC	-	±5	-	%	Ichg_term=50mA setting
Enter Supplement mode voltage threshold	ΔVBS	20	60	100	mV	VBAT-VSYS voltage
Exit supplement mode voltage threshold（Hysteresis）	ΔVBSTH	-	40	-	mV	
ON-state resistance between SYSTEM and VBAT	RON_VBAT	80	150	200	mΩ	
Battery Error Detection Time (Pre Charge)	TPRE	116	129	142	min	
Battery Error Detection Time (Fast Charge)	TFAST	577	641	705	min	
Battery Error Detection Time (High Temperature protection)	THTPRO	116	129	142	min	Over 58°C
Charging termination delay time	TTOPOFF	13	15	17	sec	
CHGLED output toggling frequency	TCHGLED	0.4	0.5	0.6	Hz	At Temp Error1, 2, or 5
Battery short-circuit detection voltage	VBATSHT	1.4	1.5	1.6	V	
Battery short-circuit detection hysteresis range	HSVBATSHT	-	0.1	-	V	
Battery temperature threshold HOT	VTH_HOT	-	58	-	°C	
Battery temperature threshold COLD	VTH_COLD	-	2	-	°C	
Battery temperature measurement accuracy	TBAT_ACC	-2	-	2	°C	
TS threshold disable voltage	VTS_DIS	0.06	0.1	0.17	V	
Battery Open detection voltage	VTS_BATOPN	1.25	1.39	1.53	V	Measure TS voltage

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
White LED Boost Converter-Switching Regurator						
LED Output Current range	ILEDR	0.01	-	25	mA	
LED Output Current accuracy	ILED_ACC	-20	0	20	%	ILED=10mA
Inducor Current limit	ILEDLIM	-	900	1200	mA	
Boost Over Voltage limit	VLEDOV	24	26	28	V	
Switching Frequency	fSW_LED	20	-	800	kHz	ILED=10mA
Turn-on Time	TONLED	-	-	500	usec	
Output Inductance	LLED	1.0	2.2	4.7	μH	Ta = -40℃～85℃
Output Capacitance	CLED	0.22	0.47	-	μF	Ta = -40℃～85℃ with BOOST DC bias
Coulomb counter						
Resolution	CCRES	-	-	15	bit	Sign + 14-bits
Operating Clock Frequency	CCFCLK	-	32.768	-	kHz	xtal
Integration Period	CCTCONV	-	1	-	sec	
Analog Input Voltage Range	CCVAIN	−30	-	30	mV	
Least Significant Bit of ΔΣ-ADC output	CCLSB	-	0.33	-	mA	Sense resister 30mΩ
Current Measurement Range	CCIAIN	−1.0	-	1.0	A	Sense resister 30mΩ
DC Offset current after calibration	CCOFSCALIB	-3.6	0	3.6	mA	Sense resister 30mΩ Ta=+25°C
Offset current over temperature	CCOFSCALBT	-3.6	0	3.6	mA	Sense resister 30mΩ Offset current variation from Ta=0°C to 60°C
Integral Non-Linearity (note1)	CCLIN	-4	-	4	LSB	CCINAIN rante Endpoint Method
12-bit SAR ADC						
Resolution	SAR_RES	-	-	12	bit	
Operating Clock Frequency	SAR_FCLK	-	400	-	kHz	
Conversion Period	SAR_TCONV	-	40	-	μsec	16 clocks
Analog Input Voltage Range 1	SAR_VAIN1	0.6	-	5.6	V	VBAT input
Analog Input Voltage Range 2	SAR_VAIN2	0.2	-	1.2	V	TS input
Analog Input Voltage Range 3	SAR_VAIN3	-30	-	30	mV	BATTP input
Differential Non-Linearity	SAR_DNL	-	±3	-	LSB	TS input
Integral Non-Linearity	SAR_INL	-	±6	-	LSB	TS input

(Unless otherwise specified, Ta=+25℃, VIN =PVIN=VINL=3.6V, DVDD=1.8V)

Parameter	Symbol	Target Spec.			Unit	Condition
		Min	Typ	Max		
I2C Bus Interface						
I2C_CLK clock frequency	f_{SCLH}	0	-	400	kHz	
Hold time START condition	$t_{HD;STA}$	160	-	-	nsec	
LOW period of I2C_CLK clock	t_{LOW}	160	-	-	nsec	
HIGH period of I2C_CLK clock	t_{HIGH}	60	-	-	nsec	
Set-up time for a repeated START condition	$t_{SU;STA}$	160	-	-	nsec	
Data hold time	$t_{HD;DAT}$	0	-	70	nsec	
Data set-up time	$t_{SU;DAT}$	10	-	-	nsec	
Set-up time for STOP condition	$t_{SU;STO}$	160	-	-	nsec	
Capacitive load for each bus line	C_b	-	-	100	pF	
Pulse width of spikes that are suppressed by the input filter *	t_{SP}	0	-	10	ns	
Bus Free Time	t_{BUFF}	1.3	-	-	us	

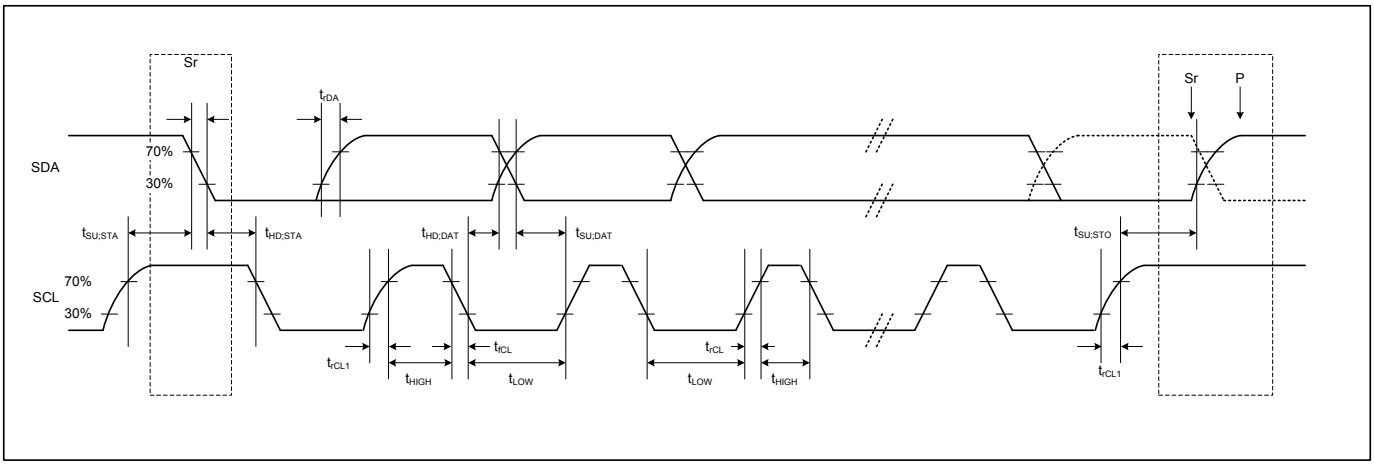


Figure 24. I2C AC Timing – High Speed Mode

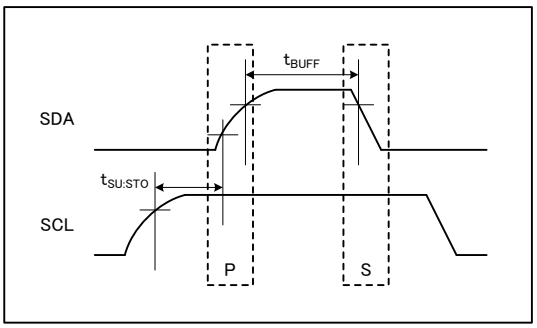


Figure 25. I2C AC Timing – Bus Free Time

Register Map

ADRS.	Register Name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0	OTP (note 4)
00h	DEVICE	R, R/W	41h	I2C_UNEMPTY	LSIVER [2:0]			DEVICEID[3:0]				NA
01h	PWRCTRL	R/W	22h	INHIBIT_0(note1)	STBY_INV	INHIBIT_0(note1)	LPSR_MODE	PWRON_DBNC[1:0]		WDOGB_PWROFF	INHIBIT_0(note1)	x
02h	BUCK1_MODE	R/W	05h	BUCK1_RAMPRATE[1:0]		-	BUCK1_PWM_FIX	BUCK1_SNVS_ON	BUCK1_RUN_ON	BUCK1_LPSR_ON	BUCK1_LP_ON	x
03h	BUCK2_MODE	R/W	05h	BUCK2_RAMPRATE[1:0]		-	BUCK2_PWM_FIX	BUCK2_SNVS_ON	BUCK2_RUN_ON	BUCK2_LPSR_ON	BUCK2_LP_ON	x
04h	BUCK3_MODE	R/W	05h	-	-	-	BUCK3_PWM_FIX	BUCK3_SNVS_ON	BUCK3_RUN_ON	BUCK3_LPSR_ON	BUCK3_LP_ON	x
05h	BUCK4_MODE	R/W	05h	-	-	-	BUCK4_PWM_FIX	BUCK4_SNVS_ON	BUCK4_RUN_ON	BUCK4_LPSR_ON	BUCK4_LP_ON	x
06h	BUCK5_MODE	R/W	05h	-	-	-	BUCK5_PWM_FIX	BUCK5_SNVS_ON	BUCK5_RUN_ON	BUCK5_LPSR_ON	BUCK5_LP_ON	x
07h	BUCK1_VOLT_H	R/W	8Ch	BUCK1_DVSSEL	BUCK1_STBY_DVS	BUCK1_H[5:0]						x
08h	BUCK1_VOLT_L	R/W	08h	-	-	BUCK1_L[5:0]						x
09h	BUCK2_VOLT_H	R/W	88h	BUCK2_DVSSEL	BUCK2_STBY_DVS	BUCK2_H[5:0]						x
0Ah	BUCK2_VOLT_L	R/W	08h	-	-	BUCK2_L[5:0]						x
0Bh	BUCK3_VOLT	R/W	0Ch	-	-	-	BUCK3[4:0]					x
0Ch	BUCK4_VOLT	R/W	04h	-	-	-	BUCK4[4:0]					x
0Dh	BUCK5_VOLT	R/W	1Eh	-	-	-	BUCK5[4:0]					x
0Eh	LED_CTRL	R/W	00h	-	-	-	CHGDONE_LED_EN	-	LED_RUN_ON	LED_LPSR_ON	LED_LP_ON	x
0Fh	LED_DIMM	R/W	00h	-	-	LED_DIMM[5:0]						NA
10h	LDO_MODE1	R/W	74h	LDO1_SNVS_ON	LDO1_RUN_ON	LDO1_LPSR_ON	LDO1_LP_ON	LDO4_REG_MODE	LDO3_REG_MODE	-	INHIBIT_0(note1)	x
11h	LDO_MODE2	R/W	F5h	LDO3_SNVS_ON	LDO3_RUN_ON	LDO3_LPSR_ON	LDO3_LP_ON	LDO2_SNVS_ON	LDO2_RUN_ON	LDO2_LPSR_ON	LDO2_LP_ON	x
12h	LDO_MODE3	R/W	57h	LDO5_SNVS_ON	LDO5_RUN_ON	LDO5_LPSR_ON	LDO5_LP_ON	LDO4_SNVS_ON	LDO4_RUN_ON	LDO4_LPSR_ON	LDO4_LP_ON	x
13h	LDO_MODE4	R/W	57h	DVREF_SNVS_ON	DVREF_RUN_ON	DVREF_LPSR_ON	DVREF_LP_ON	LDO_LPSR_SNVS_ON	LDO_LPSR_RUN_ON	LDO_LPSR_LPSR_ON	LDO_LPSR_LP_ON	x
14h	LDO1_VOLT	R/W	32h	-	-	LDO1[5:0]						x
15h	LDO2_VOLT	R/W	32h	-	-	LDO2[5:0]						x
16h	LDO3_VOLT	R/W	32h	-	-	LDO3[5:0]						x
17h	LDO4_VOLT	R/W	32h	-	-	LDO4[5:0]						NA
18h	LDO5_VOLT_H	R/W	14h	-	-	LDO5_H[5:0]						NA
19h	LDO5_VOLT_L	R/W	32h	-	-	LDO5_L[5:0]						NA
1Ah	BUCK_PD_DIS	R/W	00h	-	-	-	BUCK5_PD_DIS	BUCK4_PD_DIS	BUCK3_PD_DIS	BUCK2_PD_DIS	BUCK1_PD_DIS	NA
1Bh	LDO_PD_DIS	R/W	00h	-	DVREF_PD_DIS	LDO_LPSR_PD_DIS	LDO5_PD_DIS	LDO4_PD_DIS	LDO3_PD_DIS	LDO2_PD_DIS	LDO1_PD_DIS	NA
1Ch	GPO	R/W	03h	-	-	INHIBIT_0(note1)	GPO1_MODE	-	READY_FORCE_LOW	INHIBIT_1(note2)	GPO1_OUT	NA
1Dh	OUT32K	R, R/W	01h	OTP_STATUS	-	-	-	-	-	OUT32K_MODE	OUT32K_EN	x
1Eh	SEC	R/W	XXh	-	S40	S20	S10	S8	S4	S2	S1	NA
1Fh	MIN	R/W	XXh	-	M40	M20	M10	M8	M4	M2	M1	NA
20h	HOUR	R/W	XXh	12/24	-	H20/PA	H10	H8	H4	H2	H1	NA
21h	WEEK	R/W	0Xh	-	-	-	-	-	W4	W2	W1	NA
22h	DAY	R/W	XXh	-	-	D20	D10	D8	D4	D2	D1	NA
23h	MONTH	R/W	XXh	-	-	-	MO10	MO8	MO4	MO2	MO1	NA
24h	YEAR	R/W	XXh	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1	NA
25h	ALM0_SEC	R/W	00h	-	A0S40	A0S20	A0S10	A0S8	A0S4	A0S2	A0S1	NA
26h	ALM0_MIN	R/W	00h	-	A0M40	A0M20	A0M10	A0M8	A0M4	A0M2	A0M1	NA
27h	ALM0_HOUR	R/W	00h	A0_12/24	-	A0H20/PA	A0H10	A0H8	A0H4	A0H2	A0H1	NA
28h	ALM0_WEEK	R/W	00h	-	-	-	-	-	A0W4	A0W2	A0W1	NA
29h	ALM0_DAY	R/W	00h	-	-	A0D20	A0D10	A0D8	A0D4	A0D2	A0D1	NA
2Ah	ALM0_MONTH	R/W	00h	-	-	-	A0MO10	A0MO8	A0MO4	A0MO2	A0MO1	NA
2Bh	ALM0_YEAR	R/W	00h	A0Y80	A0Y40	A0Y20	A0Y10	A0Y8	A0Y4	A0Y2	A0Y1	NA

Register Map (continued)

ADRS.	Register Name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0	OTP (note 4)
2Ch	ALM1_SEC	R/W	00h	-	A1S40	A1S20	A1S10	A1S8	A1S4	A1S2	A1S1	NA
2Dh	ALM1_MIN	R/W	00h	-	A1M40	A1M20	A1M10	A1M8	A1M4	A1M2	A1M1	NA
2Eh	ALM1_HOUR	R/W	00h	A1_12/24	-	A1H20/PA	A1H10	A1H8	A1H4	A1H2	A1H1	NA
2Fh	ALM1_WEEK	R/W	00h	-	-	-	-	-	A1W4	A1W2	A1W1	NA
30h	ALM1_DAY	R/W	00h	-	-	A1D20	A1D10	A1D8	A1D4	A1D2	A1D1	NA
31h	ALM1_MONTH	R/W	00h	-	-	-	A1MO10	A1MO8	A1MO4	A1MO2	A1MO1	NA
32h	ALM1_YEAR	R/W	00h	A1Y80	A1Y40	A1Y20	A1Y10	A1Y8	A1Y4	A1Y2	A1Y1	NA
33h	ALM0_MASK	R/W	00h	A0_ONESEC	A0_YEAR	A0_MON	A0_DAY	A0_WEEK	A0_HOUR	A0_MIN	A0_SEC	NA
34h	ALM1_MASK	R/W	00h	A1_ONESEC	A1_YEAR	A1_MON	A1_DAY	A1_WEEK	A1_HOUR	A1_MIN	A1_SEC	NA
35h	ALM2	R/W	00h	-	-	-	-	-	-	ALM2[1:0]		NA
36h	TRIM	R/W	00h	DEV	TRIM[6:0]							NA
37h	CONF	R/W	01h	-	-	-	-	-	-	XSTB	PON	NA
38h	SYS_INIT	R/W	00h	-	-	-	-	-	-	CHGRST	-	NA
39h	CHG_STATE	R	XXh	-	CHG_STATE[6:0]							NA
3Ah	CHG_LAST_STATE	R	XXh	-	CHG_LAST_STATE[6:0]							NA
3Bh	BAT_STAT	R	XXh	-	-	BAT_DET	BAT_DET_DONE	VBAT_OV	LOW_BAT	VBAT_SHORT	DBAT_DET	NA
3Ch	DCIN_STAT	R	0Xh	-	-	-	-	DCIN_OV	IGNORE(note3)	DCIN_CLPS_DET	DCIN_DET	NA
3Dh	VSYS_STAT	R	0Xh	-	-	-	-	-	-	VSYS_LO	VSYS_UVN	NA
3Eh	CHG_STAT	R	0Xh	-	-	-	-	-	-	-	VRECHG_DET	NA
3Fh	CHG_WDT_STAT	R	XXh	CHGWDTS[7:0]								NA
40h	BAT_TEMP	R	0Xh	-	-	-	-	-	BAT_TEMP[2:0]			NA
41h	IGNORE_0	R	XXh	-	-	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	NA
42h	INHIBIT_0	R/W	E6h	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_0(note1)	x
43h	DCIN_CLPS	R/W	36h	DCIN_CLPS[11:4]								x
44h	VSYS_REG	R/W	0Bh	-	-	-	VSYS_REG[4:0]					x
45h	VSYS_MAX	R/W	33h	-	VSYS_MAX[12:6]							x
46h	VSYS_MIN	R/W	30h	-	VSYS_MIN[12:6]							x
47h	CHG_SET1	R/W	6Fh	WDT_DIS	WDT_AUTO	AUTO_FST	FST_TRG	AUTO_RECHG	BTMP_EN	COLD_ERR_EN	CHG_EN	NA
48h	CHG_SET2	R/W	98h	VF_TREG_EN	EXTMOS_EN	REBATDET_TRG	BATDET_EN	INHIBIT_1(note2)	-	TIM_CNT_SEL[1:0]		x
49h	CHG_WDT_PRE	R/W	1Eh	WDT_PRE[7:0]								x
4Ah	CHG_WDT_FST	R/W	26h	WDT_FST[10:3]								x
4Bh	CHG_IPRE	R/W	44h	ITRI[3:0]				IPRE[3:0]				x
4Ch	CHG_IFST	R/W	12h	-	-	-	IFST[4:0]					x
4Dh	CHG_IFST_TERM	R/W	05h	-	-	-	-	IFST_TERM[3:0]				x
4Eh	CHG_VPRE	R/W	C9h	VPRE_HI[3:0]				VPRE_LO[3:0]				x
4Fh	CHG_VBAT_1	R/W	18h	-	-	-	VBAT_CHG1[4:0]					x
50h	CHG_VBAT_2	R/W	13h	-	-	-	VBAT_CHG2[4:0]					x
51h	CHG_VBAT_3	R/W	10h	-	-	-	VBAT_CHG3[4:0]					x
52h	CHG_LED_1	R/W	03h	-	-	-	CHG_LED_BTA_MASK	-	TERR[2:0]			x
53h	VF_TH	R/W	00h	VF_TH[7:0]								x
54h	BAT_SET_1	R/W	00h	VBAT_HI[3:0]				VBAT_LO[3:0]				x
55h	BAT_SET_2	R/W	14h	VBAT_OVP[3:0]				-	VBAT_MNT[2:0]			x
56h	BAT_SET_3	R/W	42h	-	VBAT_DONE[2:0]			-	TIM_DBP[2:0]			x
57h	ALM_VBAT_TH_U	R/W	01h	-	-	-	-	-	-	-	VBAT_TH[12]	x

Register Map (continued)

ADRS.	Register Name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0	OTP (note 4)
58h	ALM_VBAT_TH_L	R/W	FFh	VBAT_TH[11:4]								x
59h	ALM_DCIN_TH	R/W	0Fh	DCIN_TH[11:4]								x
5Ah	ALM_VSYS_TH	R/W	FFh	VSYS_TH[12:5]								x
5Bh	VM_IBAT_U	R	00h	IBAT_DIR	-	-	-	IBAT[11:8]				NA
5Ch	VM_IBAT_L	R	00h	IBAT[7:0]								NA
5Dh	VM_VBAT_U	R	00h	-	-	-	VBAT[12:8]					NA
5Eh	VM_VBAT_L	R	00h	VBAT[7:0]								NA
5Fh	VM_BTMP	R	00h	BTMP[7:0]								NA
60h	VM_VTH	R	00h	VTH[7:0]								NA
61h	VM_DCIN_U	R	00h	-	-	-	-	DCIN[11:8]				NA
62h	VM_DCIN_L	R	00h	DCIN[7:0]								NA
63h	(reserved)	R	00h	-	-	-	-	-	-	-	-	NA
64h	VM_VF	R	00h	VF[7:0]								NA
65h	VM_OCI_PRE_U	R	00h	IBAT_OC_PRE_DIR	-	-	-	IBAT_OC_PRE[11:8]				NA
66h	VM_OCI_PRE_L	R	00h	IBAT_OC_PRE[7:0]								NA
67h	VM_OCV_PRE_U	R	00h	-	-	-	VBAT_OC_PRE[12:8]					NA
68h	VM_OCV_PRE_L	R	00h	VBAT_OC_PRE[7:0]								NA
69h	VM_OCI_PST_U	R	00h	IBAT_OC_PST_DIR	-	-	-	IBAT_OC_PST[11:8]				NA
6Ah	VM_OCI_PST_L	R	00h	IBAT_OC_PST[7:0]								NA
6Bh	VM_OCV_PST_U	R	00h	-	-	-	VBAT_OC_PST[12:8]					NA
6Ch	VM_OCV_PST_L	R	00h	VBAT_OC_PST[7:0]								NA
6Dh	VM_SA_VBAT_U	R	00h	-	-	-	VBAT_SA[12:8]					NA
6Eh	VM_SA_VBAT_L	R	00h	VBAT_SA[7:0]								NA
6Fh	VM_SA_IBAT_U	R	00h	IBAT_SA_DIR	-	-	-	IBAT_SA[11:8]				NA
70h	VM_SA_IBAT_L	R	00h	IBAT_SA[7:0]								NA
71h	CC_CTRL	R/W	40h	CCNTRST	CCNTENB	CC_CALIB	-	-	-	-	-	NA
72h	CC_BATCAP1_TH_U	R/W	00h	-	-	-	-	CC_BATCAP1_TH[11:8]				x
73h	CC_BATCAP1_TH_L	R/W	7Eh	CC_BATCAP1_TH[7:0]								x
74h	CC_BATCAP2_TH_U	R/W	00h	-	-	-	-	CC_BATCAP2_TH[11:8]				x
75h	CC_BATCAP2_TH_L	R/W	3Fh	CC_BATCAP2_TH[7:0]								x
76h	CC_BATCAP3_TH_U	R/W	00h	-	-	-	-	CC_BATCAP3_TH[11:8]				x
77h	CC_BATCAP3_TH_L	R/W	1Fh	CC_BATCAP3_TH[7:0]								x
78h	CC_STAT	R	00h	-	-	-	-	-	CC_MON3	CC_MON2	CC_MON1	NA
79h	CC_CCNTD_3	R/W	00h	-	-	-	-	CCNTD[27:24]				NA
7Ah	CC_CCNTD_2	R/W	00h	CCNTD[23:16]								NA
7Bh	CC_CCNTD_1	R/W	00h	CCNTD[15:8]								NA
7Ch	CC_CCNTD_0	R/W	00h	CCNTD[7:0]								NA
7Dh	CC_CURCD_U	R	00h	CURDIR	-	CURCD[13:8]						NA
7Eh	CC_CURCD_L	R	00h	CURCD[7:0]								NA
7Fh	VM_OCUR_THR_1	R/W	7Dh	OCURTHR1[12:5]								x
80h	VM_OCUR_DUR_1	R/W	64h	OCURDUR1[7:0]								x
81h	VM_OCUR_THR_2	R/W	5Eh	OCURTHR2[12:5]								x
82h	VM_OCUR_DUR_2	R/W	8Ch	OCURDUR2[7:0]								x
83h	VM_OCUR_THR_3	R/W	4Eh	OCURTHR3[12:5]								x

Register Map (continued)

ADRS.	Register Name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0	OTP (note 4)
84h	VM_OCUR_DUR_3	R/W	A5h	OCURDUR3[7:0]								x
85h	VM_OCUR_MON	R	0Xh	-	-	-	-	-	OCUR3	OCUR2	OCUR1	NA
86h	VM_BTMP_OV_THR	R/W	8Ch	OVBTMPTHR[7:0]								x
87h	VM_BTMP_OV_DUR	R/W	28h	OVBTMPDUR[7:0]								x
88h	VM_BTMP_LO_THR	R/W	C8h	LOBTMPTHR[7:0]								x
89h	VM_BTMP_LO_DUR	R/W	28h	LOBTMPDUR[7:0]								x
8Ah	VM_BTMP_MON	R	0Xh	-	-	-	-	-	-	OVBTMP	LOBTMP	NA
8Bh	INT_EN_01	R/W	00h	LED_SCP	LED_OCP	LED_OVP	BUCK5FAULT	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT	NA
8Ch	INT_EN_02	R/W	00h	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-	NA
8Dh	INT_EN_03	R/W	00h	-	WDOGB	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_0(note1)	DCIN_MON_DET	DCIN_MON_RES	NA
8Eh	INT_EN_04	R/W	00h	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UV_DET	VSYS_UV_RES	NA
8Fh	INT_EN_05	R/W	00h	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	INHIBIT_0(note1)	NA
90h	INT_EN_06	R/W	00h	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES	NA
91h	INT_EN_07	R/W	00h	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-	NA
92h	INT_EN_08	R/W	00h	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES	NA
93h	INT_EN_09	R/W	00h	-	-	-	-	-	CC_MON3_DET	CC_MON2_DET	CC_MON1_DET	NA
94h	INT_EN_10	R/W	00h	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES	NA
95h	INT_EN_11	R/W	00h	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES	NA
96h	INT_EN_12	R/W	00h	-	-	-	-	-	ALM2	ALM1	ALM0	NA
97h	INT_STAT	R	00h	BUCK_AST	DCIN_AST	VSYS_AST	CHG_AST	BAT_AST	BMON_AST	TMPALE	ALM_AST	NA
98h	INT_STAT_01	R/WC	00h	LED_SCP	LED_OCP	LED_OVP	BUCK5FAULT	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT	NA
99h	INT_STAT_02	R/WC	00h	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-	NA
9Ah	INT_STAT_03	R/WC	00h	-	WDOGB	INHIBIT_1(note2) & IGNORE(note3)	INHIBIT_1(note2) & IGNORE(note3)	INHIBIT_1(note2) & IGNORE(note3)	INHIBIT_1(note2) & IGNORE(note3)	DCIN_MON_DET	DCIN_MON_RES	NA
9Bh	INT_STAT_04	R/WC	00h	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UVDET	VSYS_UV_RES	NA
9Ch	INT_STAT_05	R/WC	00h	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	INHIBIT_1(note2) & IGNORE(note3)	NA
9Dh	INT_STAT_06	R/WC	00h	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES	NA
9Eh	INT_STAT_07	R/WC	00h	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-	NA
9Fh	INT_STAT_08	R/WC	00h	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES	NA
A0h	INT_STAT_09	R/WC	00h	-	-	-	-	-	CC_MON3_DET	CC_MON2_DET	CC_MON1_DET	NA
A1h	INT_STAT_10	R/WC	00h	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES	NA
A2h	INT_STAT_11	R/WC	00h	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES	NA
A3h	INT_STAT_12	R/WC	00h	-	-	-	-	-	ALM2	ALM1	ALM0	NA
A4h	INT_UPDATE	R/WC	00h	-	-	-	-	-	-	-	INT_UPDATE	NA
A5h-AFh	-	-	00h	-	-	-	-	-	-	-	-	NA
B0h	RESERVE_0	R/W	00h	RESERVE_0[7:0]								NA
B1h	RESERVE_1	R/W	00h	RESERVE_1[7:0]								NA
B2h	RESERVE_2	R/W	00h	RESERVE_2[7:0]								NA
B3h	RESERVE_3	R/W	00h	RESERVE_3[7:0]								NA
B4h	RESERVE_4	R/W	00h	RESERVE_4[7:0]								NA
B5h	RESERVE_5	R/W	00h	RESERVE_5[7:0]								NA
B6h	RESERVE_6	R/W	00h	RESERVE_6[7:0]								NA
B7h	RESERVE_7	R/W	00h	RESERVE_7[7:0]								NA
B8h	RESERVE_8	R/W	00h	RESERVE_8[7:0]								NA
B9h	RESERVE_9	R/W	00h	RESERVE_9[7:0]								NA

Register Map (continued)

ADRS.	Register Name	R/W	INIT	D7	D6	D5	D4	D3	D2	D1	D0	OTP (note 4)
BAh-BFh	-	-	00h	-	-	-	-	-	-	-	-	NA
C0h	VM_VSYS_U	R	00h	-	-	-	VSYS[12:8]					NA
C1h	VM_VSYS_L	R	00h	VSYS[7:0]								NA
C2h	VM_SA_VSYS_U	R	00h	-	-	-	VSYS_SA[12:8]					NA
C3h	VM_SA_VSYS_L	R	00h	VSYS_SA[7:0]								NA
C4h-CFh	-	-	00h	-	-	-	-	-	-	-	-	NA
D0h	VM_SA_IBAT_MIN_U	R	00h	IBAT_SA_MIN_DIR	-	-	-	IBAT_SA_MIN[11:8]				NA
D1h	VM_SA_IBAT_MIN_L	R	00h	IBAT_SA_MIN[7:0]								NA
D2h	VM_SA_IBAT_MAX_U	R	00h	IBAT_SA_MAX_DIR	-	-	-	IBAT_SA_MAX[11:8]				NA
D3h	VM_SA_IBAT_MAX_L	R	00h	IBAT_SA_MAX[7:0]								NA
D4h	VM_SA_VBAT_MIN_U	R	00h	-	-	-	VBAT_SA_MIN[12:8]					NA
D5h	VM_SA_VBAT_MIN_L	R	00h	VBAT_SA_MIN[7:0]								NA
D6h	VM_SA_VBAT_MAX_U	R	00h	-	-	-	VBAT_SA_MAX[12:8]					NA
D7h	VM_SA_VBAT_MAX_L	R	00h	VBAT_SA_MAX[7:0]								NA
D8h	VM_SA_VSYS_MIN_U	R	00h	-	-	-	VSYS_SA_MIN[12:8]					NA
D9h	VM_SA_VSYS_MIN_L	R	00h	VSYS_SA_MIN[7:0]								NA
DAh	VM_SA_VSYS_MAX_U	R	0Fh	-	-	-	VSYS_SA_MAX[12:8]					NA
DBh	VM_SA_VSYS_MAX_L	R	FFh	VSYS_SA_MAX[7:0]								NA
DCh	VM_SA_MINMAX_CLR	R/WC	8Fh	-	-	VSYS_SA_MAX_CLR	VSYS_SA_MIN_CLR	IBAT_SA_MAX_CLR	IBAT_SA_MIN_CLR	VBAT_SA_MAX_CLR	VBAT_SA_MIN_CLR	NA
DDh-DFh	-	-	FFh	-	-	-	-	-	-	-	-	NA
E0h	REX_CCNTD_3	R	00h	-	-	-	-	REX_CCNTD[27:24]				NA
E1h	REX_CCNTD_2	R	00h	REX_CCNTD[23:16]								NA
E2h	REX_CCNTD_1	R	1Fh	REX_CCNTD[15:8]								NA
E3h	REX_CCNTD_0	R	FFh	REX_CCNTD[7:0]								NA
E4h	REX_SA_VBAT_U	R	00h	-	-	-	REX_VBAT_SA[12:8]					NA
E5h	REX_SA_VBAT_L	R	00h	REX_VBAT_SA[7:0]								NA
E6h	REX_CTRL_1	R/W	00h	-	-	-	REX_CLR	REX_EN	REX_PMU_STATE_MASK	REX_DUR[1:0]		NA
E7h	REX_CTRL_2	R/W	00h	REX_CURCD_TH[7:0]								NA
E8h	FULL_CCNTD_3	R	00h	-	-	-	-	FULL_CCNTD[27:24]				NA
E9h	FULL_CCNTD_2	R	00h	FULL_CCNTD[23:16]								NA
EAh	FULL_CCNTD_1	R	00h	FULL_CCNTD[15:8]								NA
EBh	FULL_CCNTD_0	R	00h	FULL_CCNTD[7:0]								NA
ECh	FULL_CTRL	R/WC	00h	-	-	-	FULL_CLR	-	-	-	-	NA
EDh-Efh	-	-	00h	-	-	-	-	-	-	-	-	NA
F0h	CCNTD_CHG_3	R/W	09h	CHG_CCNTD[31:24]								NA
F1h	CCNTD_CHG_2	R/W	0Ah	CHG_CCNTD[23:16]								NA
BAh-FFh	-	-	00h	-	-	-	-	-	-	-	-	NA

(note1) Please always write "0" to the INHIBIT-0 register when in use.
(note2) Please always write "1" to the INHIBIT-1 register when in use.
(note3) Please always ignore the read data.
(note4) Legend of the “OTP" Column: “NA“=Not OTP target, “x”=OTP target

Address 00h: DEVICE Register (R, R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	DEVICE	R, R/W	I2C_UNEMPTY	LSIVER [2:0]			DEVICEID[3:0]			
	Initial Value	41h	0	1	0	0	0	0	0	1

Bit 7 : I2C_UNEMPTY [Read only]
0: The buffer passed to RTC from I2C is empty.
1: The buffer passed to RTC from I2C is not empty.

Bit 6-4 : LSIVER [2:0] LSI Version

Bit 3-0 : DEVICE ID[3:0] Device ID

Address 01h: PWRCTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	PWRCTRL	R/W	INHIBIT_0(note1)	STBY_INV	INHIBIT_1(note2)	LPSR_MODE	PWRON_DBNC[1:0]		WDOGB_PWROFF	INHIBIT_0(note1)
	Initial Value	22h	0	0	1	0	0	0	1	0

Bit 7 : INHIBIT_0(note1) For ROHM factory only

Bit 6 : STBY_INV STANDBY pin polarity setting
0: STANDBY pin HIGH active
1: STANDBY pin LOW active

Bit 5 : INHIBIT_1(note1) For ROHM factory only

Bit 4 : LPSR_MODE
0: Change from RUN state to SNVS state when PWRON H -> L.
1: Change from RUN state to LPSR state when PWRON H -> L.

Bit 3-2 : PWRON_DBNC[1:0] PWRON hardware debounce time setting

PWRON_DBNC[1:0]	Time (ms)
00	0
01	31
10	125
11	750

Bit 1 : WDOGB_PWROFF Select the reset mode triggered by assertion of WDOGB pin.
0: Warm Reset When WDOGB is asserted to L, Warm Reset event occurs.
PORB is asserted to low for 1ms.
1: Cold Reset When WDOGB is asserted to L, Cold Reset event occurs.
All voltage rails will be initialized and then re-boot.
And the all OTP configurable registers will be initialized.

Bit 0 : INHIBIT_0(note1) For ROHM factory only

Address 02h: BUCK1_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	BUCK1_MODE	R/W	BUCK1_RAMPRATE[1:0]		-	BUCK1_PWM_FIX	BUCK1_SNVS_ON	BUCK1_RUN_ON	BUCK1_LPSR_ON	BUCK1_LP_ON
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 7-6 : BUCK1_RAMPRATE[1:0] BUCK1RAMPRATE[1:0] BUCK1 DVS ramp rate setting
00: 10.00mV/usec
01: 5.00mV/usec
10: 2.50mV/usec
11: 1.25mV/usec

Bit 4 : BUCK1_PWM_FIX
0: BUCK1 operates in auto mode.
1: BUCK1 operates in PWM mode.
Cleared BUCK1_PWM_FIX bit to 0, when BUCK1 OCP failure is detected.

Bit 3 : BUCK1_SNVS_ON
0: BUCK1 is OFF at SNVS state.
1: BUCK1 is ON at SNVS state.
Cleared BUCK1_SNVS_ON bit to 0, when BUCK1 OCP failure is detected.

Bit 2 : BUCK1_RUN_ON
0: BUCK1 is OFF at RUN state.
1: BUCK1 is ON at RUN state.
Cleared BUCK1_RUN_ON bit to 0, when BUCK1 OCP failure is detected.

Bit 1 : BUCK1_LPSR_ON
0: BUCK1 is OFF at LPSR state.
1: BUCK1 is ON at LPSR state.
Cleared BUCK1_LPSR_ON bit to 0, when BUCK1 OCP failure is detected.

Bit 0 : BUCK1_LP_ON
0: BUCK1 is OFF at SUSPEND state.
1: BUCK1 is ON at SUSPEND state.
Cleared BUCK1_LP_ON bit to 0, when BUCK1 OCP failure is detected.

Address 03h: BUCK2_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	BUCK2_MODE	R/W	BUCK2_RAMPRATE[1:0]		-	BUCK2_PWM_FIX	BUCK2_SNVS_ON	BUCK2_RUN_ON	BUCK2_LPSR_ON	BUCK2_LP_ON
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 7-6 : BUCK2_RAMPRATE[1:0] BUCK2RAMPRATE[1:0] BUCK2 DVS ramp rate setting
00: 10.00mV/usec
01: 5.00mV/usec
10: 2.50mV/usec
11: 1.25mV/usec

Bit 4 : BUCK2_PWM_FIX
0: BUCK2 operates in auto mode.
1: BUCK2 operates in PWM mode.
Cleared BUCK2_PWM_FIX bit to 0, when BUCK2 OCP failure is detected.

Bit 3 : BUCK2_SNVS_ON
0: BUCK2 is OFF at SNVS state.
1: BUCK2 is ON at SNVS state.
Cleared BUCK2_SNVS_ON bit to 0, when BUCK2 OCP failure is detected.

Bit 2 : BUCK2_RUN_ON
0: BUCK2 is OFF at RUN state.
1: BUCK2 is ON at RUN state.
Cleared BUCK2_RUN_ON bit to 0, when BUCK2 OCP failure is detected.

Bit 1 : BUCK2_LPSR_ON
0: BUCK2 is OFF at LPSR state.
1: BUCK2 is ON at LPSR state.
Cleared BUCK2_LPSR_ON bit to 0, when BUCK2 OCP failure is detected.

Bit 0 : BUCK2_LP_ON
0: BUCK2 is OFF at SUSPEND state.
1: BUCK2 is ON at SUSPEND state.
Cleared BUCK2_LP_ON bit to 0, when BUCK2 OCP failure is detected.

Address 04h: BUCK3_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	BUCK3_MODE	R/W	-	-	-	BUCK3_PWM_FIX	BUCK3_SNVS_ON	BUCK3_RUN_ON	BUCK3_LPSR_ON	BUCK3_LP_ON
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 4 : BUCK3_PWM_FIX
0: BUCK3 operates in auto mode.
1: BUCK3 operates in PWM mode.
Cleared BUCK3_PWM_FIX bit to 0, when BUCK3 OCP failure is detected.

Bit 3 : BUCK3_SNVS_ON
0: BUCK3 is OFF at SNVS state.
1: BUCK3 is ON at SNVS state.
Cleared BUCK3_SNVS_ON bit to 0, when BUCK3 OCP failure is detected.

Bit 2 : BUCK3_RUN_ON
0: BUCK3 is OFF at RUN state.
1: BUCK3 is ON at RUN state.
Cleared BUCK3_RUN_ON bit to 0, when BUCK3 OCP failure is detected.

Bit 1 : BUCK3_LPSR_ON
0: BUCK3 is OFF at LPSR state.
1: BUCK3 is ON at LPSR state.
Cleared BUCK3_LPSR_ON bit to 0, when BUCK3 OCP failure is detected.

Bit 0 : BUCK3_LP_ON
0: BUCK3 is OFF at SUSPEND state.
1: BUCK3 is ON at SUSPEND state.
Cleared BUCK3_LP_ON bit to 0, when BUCK3 OCP failure is detected.

Address 05h: BUCK4_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
05h	BUCK4_MODE	R/W	-	-	-	BUCK4_PWM_FIX	BUCK4_SNVS_ON	BUCK4_RUN_ON	BUCK4_LPSR_ON	BUCK4_LP_ON
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 4 : BUCK4_PWM_FIX
0: BUCK4 operates in auto mode.
1: BUCK4 operates in PWM mode.
Cleared BUCK4_PWM_FIX bit to 0, when BUCK4 OCP failure is detected.

Bit 3 : BUCK4_SNVS_ON
0: BUCK4 is OFF at SNVS state.
1: BUCK4 is ON at SNVS state.
Cleared BUCK4_SNVS_ON bit to 0, when BUCK4 OCP failure is detected.

Bit 2 : BUCK4_RUN_ON
0: BUCK4 is OFF at RUN state.
1: BUCK4 is ON at RUN state.
Cleared BUCK4_RUN_ON bit to 0, when BUCK4 OCP failure is detected.

Bit 1 : BUCK4_LPSR_ON
0: BUCK4 is OFF at LPSR state.
1: BUCK4 is ON at LPSR state.
Cleared BUCK4_LPSR_ON bit to 0, when BUCK4 OCP failure is detected.

Bit 0 : BUCK4_LP_ON
0: BUCK4 is OFF at SUSPEND state.
1: BUCK4 is ON at SUSPEND state.
Cleared BUCK4_LP_ON bit to 0, when BUCK4 OCP failure is detected.

Address 06h: BUCK5_MODE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	BUCK5_MODE	R/W	-	-	-	BUCK5_PWM_FIX	BUCK5_SNVS_ON	BUCK5_RUN_ON	BUCK5_LPSR_ON	BUCK5_LP_ON
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit 4 : BUCK5_PWM_FIX
0: BUCK5 operates in auto mode.
1: BUCK5 operates in PWM mode.
Cleared BUCK5_PWM_FIX bit to 0, when BUCK5 OCP failure is detected.

Bit 3 : BUCK5_SNVS_ON
0: BUCK5 is OFF at SNVS state.
1: BUCK5 is ON at SNVS state.
Cleared BUCK5_SNVS_ON bit to 0, when BUCK5 OCP failure is detected.

Bit 2 : BUCK5_RUN_ON
0: BUCK5 is OFF at RUN state.
1: BUCK5 is ON at RUN state.
Cleared BUCK5_RUN_ON bit to 0, when BUCK5 OCP failure is detected.

Bit 1 : BUCK5_LPSR_ON
0: BUCK5 is OFF at LPSR state.
1: BUCK5 is ON at LPSR state.
Cleared BUCK5_LPSR_ON bit to 0, when BUCK5 OCP failure is detected.

Bit 0 : BUCK5_LP_ON
0: BUCK5 is OFF at SUSPEND state.
1: BUCK5 is ON at SUSPEND state.
Cleared BUCK5_LP_ON bit to 0, when BUCK5 OCP failure is detected.

Address 07h: BUCK1_VOLT_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
07h	BUCK1_VOLT_H	R/W	BUCK1_DVSSEL	BUCK1_STBY_DVS	BUCK1_H[5:0]					
	Initial Value	8Ch	1	0	0	0	1	1	0	0

Bit 7 : BUCK1_DVSSEL Select BUCK1 output voltage
0: Use BUCK1_L bits setting for BUCK1 output voltage.
1: Use BUCK1_H bits setting for BUCK1 output voltage.

Bit 6 : BUCK1_STBY_DVS Select the DVS control event
0 : DVS fucntion for BUCK1 is handled according to BUCK1_DVSSEL bit.
1 : DVS fucntion for BUCK1 is handled according to Power State: RUN/CLEAN=BUCK1_H voltage setting, SUSPEND/LPSR=BUCK1_L voltage setting.

Bit 5-0 : BUCK1_H[5:0] Sets the BUCK1 output voltage.
See Table 4 for all possible configurations.

Address 08h: BUCK1_VOLT_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	BUCK1_VOLT_L	R/W	-	-	BUCK1_L[5:0]					
	Initial Value	08h	0	0	0	0	1	0	0	0

Bit 5-0 : BUCK1_L[5:0] Sets the BUCK1 output voltage.
See Table 4 for all possible configurations.

Address 09h: BUCK2_VOLT_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	BUCK2_VOLT_H	R/W	BUCK2_DVSSEL	BUCK2_STBY_DVS	BUCK2_H[5:0]					
	Initial Value	88h	1	0	0	0	1	0	0	0

Bit 7 : BUCK2_DVSSEL Select BUCK2 output voltage
0: Use BUCK2_L bits setting for BUCK2 output voltage.
1: Use BUCK2_H bits setting for BUCK2 output voltage.

Bit 6 : BUCK2_STBY_DVS Select the DVS control event
0 : DVS fucntion for BUCK2 is handled according to BUCK2_DVSSEL bit.
1 : DVS fucntion for BUCK2 is handled according to Power State: RUN/CLEAN=BUCK2_H voltage setting, SUSPEND/LPSR=BUCK2_L voltage setting.

Bit 5-0 : BUCK2_H[5:0] Sets the BUCK2 output voltage.
See Table 4 for all possible configurations.

Address 0Ah: BUCK2_VOLT_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	BUCK2_VOLT_L	R/W	-	-	BUCK2_L[5:0]					
	Initial Value	08h	0	0	0	0	1	0	0	0

Bit 5-0 : BUCK2_L[5:0] Sets the BUCK2 output voltage.
See Table 4 for all possible configurations.

Address 0Bh: BUCK3_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Bh	BUCK3_VOLT	R/W	-	-	-	BUCK3[4:0]				
	Initial Value	0Ch	0	0	0	0	1	1	0	0

Bit 5-0 : BUCK3[4:0] Sets the BUCK3 output voltage.
See Table 4 for all possible configurations.

Address 0Ch: BUCK4_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	BUCK4_VOLT	R/W	-	-	-	BUCK4[4:0]				
	Initial Value	04h	0	0	0	0	0	1	0	0

Bit 5-0 : BUCK4[4:0] Sets the BUCK4 output voltage.
See Table 4 for all possible configurations.

Address 0Dh: BUCK5_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Dh	BUCK5_VOLT	R/W	-	-	-	BUCK5[4:0]				
	Initial Value	1Eh	0	0	0	1	1	1	1	0

Bit 5-0 : BUCK5[4:0] Sets the BUCK5 output voltage.
See Table 4 for all possible configurations.

Address 0Eh: LED_CTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	LED_CTRL	R/W	-	-	-	CHGDONE_LED_EN	-	LED_RUN_ON	LED_LPSR_ON	LED_LP_ON
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit4 : CHGDONE_LED_EN Select the LED (Shared with READY output pin) control mode with charge completion status
0: Disable Not automatically indicate charge competion status, but can be controlled by READY_FORCE_LOW bit.
1: Enable Automatically indicate charge completion status , READY output goes L. But READY_FORCE_LOW bit control is prioritized.

Bit2 : LED_RUN_ON
0: White LED boost converter is OFF at RUN state.
1: White LED boost converter is ON at RUN state.

Bit1 : LED_LPSR_ON
0: White LED boost converter is OFF at LPSR state.
1: White LED boost converter is ON at LPSR state.

Bit0 : LED_LP_ON
0: White LED boost converter is OFF at SUSPEND state.
1: White LED boost converter is ON at SUSPEND state.

Address 0Fh: LED_DIMM Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Fh	LED_DIMM	R/W	-	-	LED_DIMM[5:0]					
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5-0 : LED_DIMM[5:0] Select White LED boost converter dimming

LED_DIMM[5:0]	LED current
00h	10 uA
01h	20 uA
02h	30 uA
03h	50 uA
04h	70 uA
05h	100 uA
06h	200 uA
07h	300 uA
08h	500 uA
09h	700 uA
0Ah	1 mA
0Bh	2 mA
0Ch	3 mA
0Dh	4 mA
0Eh	5 mA
0Fh	6 mA
10h	7 mA
11h	8 mA
12h	9 mA
13h	10 mA
14h	11 mA
15h	12 mA
16h	13 mA
17h	14 mA
18h	15 mA
19h	16 mA
1Ah	17 mA
1Bh	18 mA
1Ch	19 mA
1Dh	20 mA
1Eh	21 mA
1F	22 mA
20h	23 mA
21h	24 mA
22h	25 mA
23～3Fh	don't use

Address 10h: LDO_MODE1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	LDO_MODE1	R/W	LDO1_SNVS_ON	LDO1_RUN_ON	LDO1_LPSR_ON	LDO1_LP_ON	LDO4_REG_MODE	LDO3_REG_MODE	-	INHIBIT_0(note1)
	Initial Value	74h	0	1	1	1	0	1	0	0

Bit 7 : LDO1_SNVS_ON
0: LDO1 is OFF at SNVS state.
1: LDO1 is ON at SNVS state.

Bit 6 : LDO1_RUN_ON
0: LDO1 is OFF at RUN state.
1: LDO1 is ON at RUN state.

Bit 5 : LDO1_LPSR_ON
0: LDO1 is OFF at LPSR state.
1: LDO1 is ON at LPSR state.

Bit 4 : LDO1_LP_ON
0: LDO1 is OFF at SUSPEND state.
1: LDO1 is ON at SUSPEND state.

Bit 3 : LDO4_REG_MODE
0: LDO4 is controlled via external pin (LDO4VEN).
1: LDO4 is controlled via register.

Bit 2 : LDO3_REG_MODE
0: LDO3 starts when DCIN is supplied.
1: LDO3 is controlled via register.

Bit 0 : INHIBIT_0(note1) For ROHM factory only

Address 11h: LDO_MODE2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
11h	LDO_MODE2	R/W	LDO3_SNVS_ON	LDO3_RUN_ON	LDO3_LPSR_ON	LDO3_LP_ON	LDO2_SNVS_ON	LDO2_RUN_ON	LDO2_LPSR_ON	LDO2_LP_ON
	Initial Value	F5h	1	1	1	1	0	1	0	1

Bit 7 : LDO3_SNVS_ON
0: LDO3 is OFF at SNVS state.
1: LDO3 is ON at SNVS state.

Bit 6 : LDO3_RUN_ON
0: LDO3 is OFF at RUN state.
1: LDO3 is ON at RUN state.

Bit 5 : LDO3_LPSR_ON
0: LDO3 is OFF at LPSR state.
1: LDO3 is ON at LPSR state.

Bit 4 : LDO3_LP_ON
0: LDO3 is OFF at SUSPEND state.
1: LDO3 is ON at SUSPEND state.

Bit 3 : LDO2_SNVS_ON
0: LDO2 is OFF at SNVS state.
1: LDO2 is ON at SNVS state.

Bit 2 : LDO2_RUN_ON
0: LDO2 is OFF at RUN state.
1: LDO2 is ON at RUN state.

Bit 1 : LDO2_LPSR_ON
0: LDO2 is OFF at LPSR state.
1: LDO2 is ON at LPSR state.

Bit 0 : LDO2_LP_ON
0: LDO2 is OFF at SUSPEND state.
1: LDO2 is ON at SUSPEND state.

Address 12h: LDO_MODE3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
12h	LDO_MODE3	R/W	LDO5_SNVS_ON	LDO5_RUN_ON	LDO5_LPSR_ON	LDO5_LP_ON	LDO4_SNVS_ON	LDO4_RUN_ON	LDO4_LPSR_ON	LDO4_LP_ON
	Initial Value	57h	0	1	0	1	0	1	1	1

Bit 7 : LDO5_SNVS_ON
0: LDO5 is OFF at SNVS state.
1: LDO5 is ON at SNVS state.

Bit 6 : LDO5_RUN_ON
0: LDO5 is OFF at RUN state.
1: LDO5 is ON at RUN state.

Bit 5 : LDO5_LPSR_ON
0: LDO5 is OFF at LPSR state.
1: LDO5 is ON at LPSR state.

Bit 4 : LDO5_LP_ON
0: LDO5 is OFF at SUSPEND state.
1: LDO5 is ON at SUSPEND state.

Bit 3 : LDO4_SNVS_ON
0: LDO4 is OFF at SNVS state.
1: LDO4 is ON at SNVS state.

Bit 2 : LDO4_RUN_ON
0: LDO4 is OFF at RUN state.
1: LDO4 is ON at RUN state.

Bit 1 : LDO4_LPSR_ON
0: LDO4 is OFF at LPSR state.
1: LDO4 is ON at LPSR state.

Bit 0 : LDO4_LP_ON
0: LDO4 is OFF at SUSPEND state.
1: LDO4 is ON at SUSPEND state.

Address 13h: LDO_MODE4 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13h	LDO_MODE4	R/W	DVREF_SNVS_ON	DVREF_RUN_ON	DVREF_LPSR_ON	DVREF_LP_ON	LDO_LPSR_SNVS_ON	LDO_LPSR_RUN_ON	LDO_LPSR_LPSR_ON	LDO_LPSR_LP_ON
	Initial Value	57h	0	1	0	1	0	1	1	1

Bit 7 : DVREF_SNVS_ON
0: DVREF is OFF at SNVS state.
1: DVREF is ON at SNVS state.

Bit 6 : DVREF_RUN_ON
0: DVREF is OFF at RUN state.
1: DVREF is ON at RUN state.

Bit 5 : DVREF_LPSR_ON
0: DVREF is OFF at LPSR state.
1: DVREF is ON at LPSR state.

Bit 4 : DVREF_LP_ON
0: DVREF is OFF at SUSPEND state.
1: DVREF is ON at SUSPEND state.

Bit 3 : LDO_LPSR_SNVS_ON
0: LDO_LPSR is OFF at SNVS state.
1: LDO_LPSR is ON at SNVS state.

Bit 2 : LDO_LPSR_RUN_ON
0: LDO_LPSR is OFF at RUN state.
1: LDO_LPSR is ON at RUN state.

Bit 1 : LDO_LPSR_LPSR_ON
0: LDO_LPSR is OFF at LPSR state.
1: LDO_LPSR is ON at LPSR state.

Bit 0 : LDO_LPSR_LP_ON
0: LDO_LPSR is OFF at SUSPEND state.
1: LDO_LPSR is ON at SUSPEND state.

Address 14h: LDO1_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	LDO1_VOLT	R/W	-	-	LDO1[5:0]					
	Initial Value	32h	0	0	1	1	0	0	1	0

Bit5-0 : LDO1[5:0] Sets the LDO1 output voltage.
See Table 4 for all possible configurations.

Address 15h: LDO2_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
15h	LDO2_VOLT	R/W	-	-	LDO2[5:0]					
	Initial Value	32h	0	0	1	1	0	0	1	0

Bit5-0 : LDO2[5:0] Sets the LDO2 output voltage.
See Table 4 for all possible configurations.

Address 16h: LDO3_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
16h	LDO3_VOLT	R/W	-	-	LDO3[5:0]					
	Initial Value	32h	0	0	1	1	0	0	1	0

Bit5-0 : LDO3[5:0] Sets the LDO3 output voltage.
See Table 4 for all possible configurations.

Address 17h: LDO4_VOLT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17h	LDO4_VOLT	R/W	-	-	LDO4[5:0]					
	Initial Value	32h	0	0	1	1	0	0	1	0

Bit5-0 : LDO4[5:0] Sets the LDO4 output voltage.
See Table 4 for all possible configurations.

Address 18h: LDO5_VOLT_H Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18h	LDO5_VOLT_H	R/W	-	-	LDO5_H[5:0]					
	Initial Value	14h	0	0	0	1	0	1	0	0

Bit5-0 : LDO5_H[5:0] LDO5 output voltage
See the description of LDO5_VOLT_L register below.

Address 19h: LDO5_VOLT_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19h	LDO5_VOLT_L	R/W	-	-	LDO5_L[5:0]					
	Initial Value	32h	0	0	1	1	0	0	1	0

Bit5-0 : LDO5_L[5:0] LDO5 output voltage
If LDO5VSEL = L, LDO5 output voltage corresponds to the setting of LDO5_L bits.
If LDO5VSEL = H, LDO5 output voltage corresponds to the setting of LDO5_H bits.

Address 1Ah: BUCK_PD_DIS Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ah	BUCK_PD_DIS	R/W	-	-	-	BUCK5_PD_DIS	BUCK4_PD_DIS	BUCK3_PD_DIS	BUCK2_PD_DIS	BUCK1_PD_DIS
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit4 : BUCK5_PD_DIS
0: Discharge for BUCK5 turn off is enabled.
1: Discharge for BUCK5 turn off is disabled.

Bit3 : BUCK4_PD_DIS
0: Discharge for BUCK4 turn off is enabled.
1: Discharge for BUCK4 turn off is disabled.

Bit2 : BUCK3_PD_DIS
0: Discharge for BUCK3 turn off is enabled.
1: Discharge for BUCK3 turn off is disabled.

Bit1 : BUCK2_PD_DIS
0: Discharge for BUCK2 turn off is enabled.
1: Discharge for BUCK2 turn off is disabled.

Bit0 : BUCK1_PD_DIS
0: Discharge for BUCK1 turn off is enabled.
1: Discharge for BUCK1 turn off is disabled.

Address 1Bh: LDO_PD_DIS Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Bh	LDO_PD_DIS	R/W	-	DVREF_PD_DIS	LDO_LPSR_PD_DIS	LDO5_PD_DIS	LDO4_PD_DIS	LDO3_PD_DIS	LDO2_PD_DIS	LDO1_PD_DIS
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6 : DVREF_PD_DIS
0: Discharge for DVREF turn off is enabled
1: Discharge for DVREF turn off is disabled.

Bit 5 : LDO_LPSR_PD_DIS
0: Discharge for LDO_LPSR turn off is enabled
1: Discharge for LDO_LPSR turn off is disabled.

Bit 4 : LDO5_PD_DIS
0: Discharge for LDO5 turn off is enabled
1: Discharge for LDO5 turn off is disabled.

Bit 3 : LDO4_PD_DIS
0: Discharge for LDO4 turn off is enabled
1: Discharge for LDO4 turn off is disabled.

Bit 2 : LDO3_PD_DIS
0: Discharge for LDO3 turn off is enabled
1: Discharge for LDO3 turn off is disabled.

Bit 1 : LDO2_PD_DIS
0: Discharge for LDO2 turn off is enabled
1: Discharge for LDO2 turn off is disabled.

Bit 0 : LDO1_PD_DIS
0: Discharge for LDO1 turn off is enabled
1: Discharge for LDO1 turn off is disabled.

Address 1Ch: GPO Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Ch	GPO	R/W	-	-	INHIBIT_0(note1)	GPO1_MODE	-	READY_FORCE_LOW	INHIBIT_1(note2)	GPO1_OUT
	Initial Value	03h	0	0	0	0	0	0	1	1

Bit 5 : INHIBIT_0 (note1) For ROHM factory only

Bit 4 : GPO1_MODE GPO1 Output mode setting
0: Open drain output mode
1: CMOS output mode

Bit 2 : READY_FORCE_LOW Force READY pin to be L output
0: Normal READY pin be controlled as per Power State, Power Sequence, DVS and PWRON push status.
1: Low

Bit 1 : INHIBIT_1 (note2) For ROHM factory only

Bit 0 : GPO1_OUT GPO1 Output setting
0: Low
1: Hi-Z [Open drain output mode] / High [CMOS output mode]

Address 1Dh: OUT32K Register (R,R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Dh	OUT32K	R,R/W	OTP_STATUS	-	-	-	-	-	OUT32K_MODE	OUT32K_EN
	Initial Value		01h	0	0	0	0	0	0	1

Bit 7 : OTP_STATUS OTP test status [Read only]
0: Already stored sample
1: Not stored sample

Bit 1 : OUT32K_MODE CLK32KOUT output mode setting
0: Open drain output mode
1: CMOS output mode

Bit 0 : OUT32K_EN CLK32KOUT clock output enable
0: Disable [Hi-Z at Open drain mode, H at CMOS mode]
1: Enable

Address 1Eh: SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Eh	SEC	R/W	-	S40	S20	S10	S8	S4	S2	S1
	Initial Value	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : S1 to S40 Second Counter.
The second digits range from 00 to 59 and are carried to the minute digit in transition from 59 to 00.Configured in BCD（Binary-Coded Decimal)
Any writing to the second counter resets divider units of less than 1 second.
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address 1Fh: MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1Fh	MIN	R/W	-	M40	M20	M10	M8	M4	M2	M1
	Initial Value	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : M1 to M40 Minute Counter.
The minute digits range from 00 to 59 and are carried to the hour digits in transition from 59 to 00.Configured in BCD（Binary-Coded Decimal)
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address 20h: HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	HOUR	R/W	12/24	-	H20/PA	H10	H8	H4	H2	H1
	Initial Value	XXh	0	0	x	x	x	x	x	x

Bit 7 : 12/24 Selects whether 12-hour clock or 24-hour clock is used.
0: 12hour clock
1: 24hour clock

Bit 5-0 : H20 to H1 Hour Counter.
The hour digits' range are as shown in this table and are carried to the day-of-month and day-of-week digits in transition from PM11 to AM12 or from 23 to 00. Configured in BCD（Binary-Coded Decimal)
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

24-hour clock	12-hour clock	24-hour clock	12-hour clock
0	12(AM12)	12	32(PM12)
1	01(AM1)	13	21(PM1)
2	02(AM2)	14	22(PM2)
3	03(AM3)	15	23(PM3)
4	04(AM4)	16	24(PM4)
5	05(AM5)	17	25(PM5)
6	06(AM6)	18	26(PM6)
7	07(AM7)	19	27(PM7)
8	08(AM8)	20	28(PM8)
9	09(AM9)	21	29(PM9)
10	10(AM10)	22	30(PM10)
11	11(AM11)	23	31(PM11)

Address 21h: WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
21h	WEEK	R/W	-	-	-	-	-	W4	W2	W1
	Initial Value	0Xh	0	0	0	0	0	x	x	x

Bit 2-0 : W4 to W1 Day-of-week Counter.
The day-of-week counter is incremented by 1 when the hour digits are carried to the day-of-month digits. Configured in BCD（Binary-Coded Decimal)
Correspondences between days of the week and the day-of-week digit are user-definable.
(Ex. Sunday = 0, 0, 0)
The writing of (1, 1, 1) to (W4, W2, W1) is prohibited except when days of the week are unused.
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 22h: DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
22h	DAY	S/W	-	-	D20	D10	D8	D4	D2	D1
	Initial Value	XXh	0	0	x	x	x	x	x	x

Bit 5-0 : D20 to D1 Day-of-month Counter
The day-of-month digits (D20 to D1) range from 1 to 31 for January, March, May, July, August, October, and December, from 1 to 30 for April, June, September, and November, from 1 to 29 for February in leap years, from 1 to 28 for February in ordinary years.
The day-of-month digits are carried to the month digits in reversion from the last day of the month to 1. Configured in BCD（Binary-Coded Decimal)
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 23h: MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	MONTH	R/W	-	-	-	MO10	MO8	MO4	MO2	MO1
	Initial Value	XXh	0	0	0	x	x	x	x	x

Bit 4-0 : MO10 to MO1 Month Counter.
The month digits (MO10 to MO1) range from 1 to 12 and are carried to the year digits in reversion from 12 to 1. Configured in BCD（Binary-Coded Decimal)
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 24h: YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24h	YEAR	R/W	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	Initial Value	XXh	x	x	x	x	x	x	x	x

Bit 7-0 : Y80 to Y1 Year Counter.
The year digits (Y80 to Y1) range from 00 to 99 and are carried to the 19/20 digits in reversion from 99 to 00.
00, 04, 08, ..., 92 and 96 in leap years. Configured in BCD（Binary-Coded Decimal)
RTC calendar and time information (address from 1Eh to 24h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 25h: ALM0_SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	ALM0_SEC	R/W	-	A0S40	A0S20	A0S10	A0S8	A0S4	A0S2	A0S1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A0S40 to A0S1 Alarm0 Second threshold value.Configured in BCD（Binary-Coded Decimal)

Address 26h: ALM0_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
26h	ALM0_MIN	R/W	-	A0M40	A0M20	A0M10	A0M8	A0M4	A0M2	A0M1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A0M40 to A0M1 Alarm0 Minute threshold value.Configured in BCD（Binary-Coded Decimal)

Address 27h: ALM0_HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
27h	ALM0_HOUR	R/W	A0_12/24	-	A0H20/PA	A0H10	A0H8	A0H4	A0H2	A0H1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : A0_12/24 12hour clock / 24hour clock select bit.

Bit 5-0 : A0H20/PA, A0H40 to A0H1 Alarm0 Hour threshold value.Configured in BCD（Binary-Coded Decimal)

Address 28h: ALM0_WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28h	ALM0_WEEK	R/W	-	-	-	-	-	A0W4	A0W2	A0W1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 2-0 : : A0W4 to A0W1 Alarm0 day of the Week threshold value.Configured in BCD（Binary-Coded Decimal)

Address 29h: ALM0_DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
29h	ALM0_DAY	R/W	-	-	A0D20	A0D10	A0D8	A0D4	A0D2	A0D1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5-0 : A0D20 to A0D1 Alarm0 Day threshold value.Configured in BCD（Binary-Coded Decimal)

Address 2Ah: ALM0_MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	ALM0_MONTH	R/W	-	-	-	A0MO10	A0MO8	A0MO4	A0MO2	A0MO1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 4-0 : A0MO10 to A0MO1 Alarm0 Month threshold value.Configured in BCD（Binary-Coded Decimal)

Address 2Bh: ALM0_YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Bh	ALM0_YEAR	R/W	A0Y80	A0Y40	A0Y20	A0Y10	A0Y8	A0Y4	A0Y2	A0Y1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : A0Y80 to A0Y1 Alarm0 Year threshold value

Address 2Ch: ALM1_SEC Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ch	ALM1_SEC	R/W	-	A1S40	A1S20	A1S10	A1S8	A1S4	A1S2	A1S1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A1S40 to A1S1 Alarm1 Second threshold value.Configured in BCD（Binary-Coded Decimal)

Address 2Dh: ALM1_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Dh	ALM1_MIN	R/W	-	A1M40	A1M20	A1M10	A1M8	A1M4	A1M2	A1M1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 6-0 : A1M80 to A1M1 Alarm1 Minute threshold value.Configured in BCD（Binary-Coded Decimal)

Address 2Eh: ALM1_HOUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Eh	ALM1_HOUR	R/W	A1_12/24	-	A1H20/PA	A1H10	A1H8	A1H4	A1H2	A1H1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : A1 12/24, 12hour clock / 24hour clock select bit.

Bit 5-0 : A1H20/PA, A1H10 to A1H1 Alarm1 Hour threshold value.Configured in BCD（Binary-Coded Decimal)

Address 2Fh: ALM1_WEEK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Fh	ALM1_WEEK	R/W	-	-	-	-	-	A1W4	A1W2	A1W1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 2-0 : : A1W4 to A1W1 Alarm1 day of the Week threshold value.Configured in BCD（Binary-Coded Decimal)

Address 30h: ALM1_DAY Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
30h	ALM1_DAY	R/W	-	-	A1D20	A1D10	A1D8	A1D4	A1D2	A1D1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5-0 : A1D20 to A1D1 Alarm1 Day threshold value.Configured in BCD（Binary-Coded Decimal)

Address 31h: ALM1_MONTH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
31h	ALM1_MONTH	R/W	-	-	-	A1MO10	A1MO8	A1MO4	A1MO2	A1MO1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 4-0 : A1MO10 to A1MO1 Alarm1 Month threshold value.Configured in BCD（Binary-Coded Decimal)

Address 32h: ALM1_YEAR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
32h	ALM1_YEAR	R/W	A1Y80	A1Y40	A1Y20	A1Y10	A1Y8	A1Y4	A1Y2	A1Y1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : A1Y80 to A1Y1 Alarm1 Year threshold value.Configured in BCD（Binary-Coded Decimal)

Address 33h: ALM0_MASK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
33h	ALM0_MASK	R/W	A0_ONESEC	A0_YEAR	A0_MON	A0_DAY	A0_WEEK	A0_HOUR	A0_MIN	A0_SEC
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : A0_ONESEC Alarm0 interrupt occurs once every second. (Synchronized with second counter increment)
0: Disable
1: Enable
When A0_ONESEC is set to "1", regardless of any other setting in the ALM0_MASK register and the contents of the respective ALM0_SEC to ALM0_YEAR registers.

Bit 6-0 : A0_YEAR to A0_SEC Alarm0 interrupt threshold mask bit.
0: Mask
1: Not masked

Address 34h: ALM1_MASK Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	ALM1_MASK	R/W	A1_ONESEC	A1_YEAR	A1_MON	A1_DAY	A1_WEEK	A1_HOUR	A1_MIN	A1_SEC
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : A1_ONESEC Alarm1 interrupt occur once every second. (Synchronized with second counter increment)
0: Disable
1: Enable
When A1_ONESEC is set to "1", regardless of any other setting in the ALM1_MASK register and the contents of the respective ALM1_SEC to ALM1_YEAR registers.

Bit 6-0 : A1_YEAR to A1_SEC Alarm1 interrupt threshold mask bit.
0: Mask
1: Not masked

Address 35h: ALM2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h	ALM2	R/W	-	-	-	-	-	-	ALM2[1:0]	
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 1-0 : ALM2[1:0]
00: OFF (Initial State)
01: Once per 1 second (Synchronized with second counter increment)
10: Once per minute (at 00 seconds of every minute)
11: Once per hour (at 00 minutes, and 00 seconds of every hour)

Invalidate Alarm2 when changing the value of clock and calendar.

Address 36h: TRIM Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	TRIM	R/W	DEV	TRIM[6:0]						
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : DEV
When DEV is set to '0', the Oscillation Adjustment Circuit operates at 00, 30 seconds.
When DEV is set to '1', the Oscillation Adjustment Circuit operates at 00 seconds only.

Bit 6-0 : TRIM[6:0]
The Oscillation Adjustment Circuit is configured to change time counts of 1 second on the basis of the settings of the Oscillation Adjustment Register at the timing set by DEV.
The Oscillation Adjustment Circuit will not operate with the same timing (00, or 30 seconds) as the timing of writing to the Oscillation Adjustment Register.
The TRIM 6 : bit setting of '0' causes an increment of (TRIM[5:0]-1) x 2 of time counts.
The TRIM 6 : bit setting of '1' causes a decrement of (invert(TRIM[5:0])+1) x 2 of time counts.
The TRIM 6-0 : bit setting of "x00000x" causes neither an increment nor decrement of time counts.

Address 37h: CONF Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	CONF	R/W	-	-	-	-	-	-	XSTB	PON
	Initial Value	01h	0	0	0	0	0	0	0	1

Bit 1 : XSTB Oscillator Stop Flag
0: RTC clock has been stopped.
1: RTC clock is normallyOscillator operating normally.
The XSTB bit is used to check the status of the Real Time Clock (RTC). This bit accepts R/W for "1" and "0".
If "1" is written to this bit, the XSTB bit will change value to "0" when the RTC is stopped.

Bit 0 : PON Power-on-reset Flag.
0: Normal condition.
1: Power-on-reset detected
The PON bit is used to check for a power-on-reset condition. Only "0" values may be written to this bit.
A power-on-reset condition is detected when the supply voltage rises above the SNVS undervoltage lockout (UVLO) value.
When a power-on-reset condition is detected, the PON bit is set to "1".
When the PON bit is set to "0", SNVS UVLO operates in intermittent monitoring mode.

Address 38h: SYS_INIT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	SYS_INIT	R/W	-	-	-	-	-	-	CHGRST	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 1(W) : CHGRST
Writing "0" releases reset operation.
Writing "1" resets Battery Charger States. Charger state is returned to SUSPEND state, and timers of charger are reset.

Bit 1(R) : CHGRST Reset status for CHGRST
0: Reset released
1: Reset asserted

Address 39h: CHG_STATE Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39h	CHG_STATE	R	-	CHG_STATE[6:0]						
	Initial Value	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : CHG_STATE[6:0] The current state of the battery charger. Table below shows the details of the register values.

Address 3Ah: CHG_LAST_STATE Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Ah	CHG_LAST_STATE	R	-	CHG_LAST_STATE[6:0]						
	Initial Value	XXh	0	x	x	x	x	x	x	x

Bit 6-0 : CHG_LAST_STATE[6:0] The previous state of the battery charger. Table shows the details of the register values.

CHG_STATE[6:0] CHG_LAST_STATE[6:0]	State	Description
00h	SUSPEND	Suspend charging
01h	TRICKLE CHARGE	Trickle charging (Pre-conditioning)
02h	PRE CHARGE	Pre-charging
03h	FAST CHARGE	Fast Charging
0Dh	BATDET	Battery detection
0Eh	TOP OFF	Termination Current reached
0Fh	DONE	Charging finished
10h	Temp Err 1	Out of standard temperature while in PRE CHARGE State
11h	Temp Err 2	Out of standard temperature while in FAST CHARGE or TOP OFF State
12h	Temp Err 3	Out of standard temperature while in DONE State
13h	Temp Err 4	Out of standard temperature while in SUSPEND State
14h	Temp Err 5	Out of standard temperature while in PRE CHARGE State
20h	TSD 1	Thermal Shut Down while in PRE CHARGE State (> 135℃)
21h	TSD 2	Thermal Shut Down while in FAST CHARGE State (> 135℃)
22h	TSD 3	Thermal Shut Down while in TOP OFF State (> 135℃)
23h	TSD 4	Thermal Shut Down while in DONE State (> 135℃)
24h	TSD 5	Thermal Shut Down while in TRICKLE CHARGE State (> 135℃)
30h	BATT ASSIST 1	VSYS < VBAT while in FAST CHARGE State
31h	BATT ASSIST 2	VSYS < VBAT while in TOP OFF State
32h	BATT ASSIST 3	VSYS < VBAT after TOP OFF State (DONE)
7Fh	Batt Error	Battery Error
others	(reserved)	-

Address 3Bh: BAT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Bh	BAT_STAT	R	-	-	BAT_DET	BAT_DET_DONE	VBAT_OV	LOW_BAT	VBAT_SHORT	DBAT_DET
	Initial Value	XXh	0	0	x	x	x	x	x	x

Bit 5 : BAT_DET Battery detection result
0 : Battery removed or no battery detected
1 : Battery present

Bit 4 : BAT_DET_DONE Battery detection status
0 : Detection running
1 : Detection finished

Bit 3 : VBAT_OV VBAT over-voltage Status
0 : VBAT ≦ VBAT_OVP - 150mV (Hysteresis)
1 : VBAT ≧ VBAT_OVP
For example, VBAT_OV might be detected when the battery is removed while Fast charging.

Bit 2 : LOW_BAT Battery low-voltage Status
0 : VBAT > VBAT_LO
1 : VBAT ≦VBAT_LO

Bit 1 : VBAT_SHORT Battery short-circuit detection status
0 : VBAT ≧ 1.6V (Hysteresis)
1 : VBAT ≦ 1.5V

Bit 0 : DBAT_DET Dead Battery detection status
0 : Not detected
1 : Detected
If VBAT is below VBAT_LO until the timer is expired, the battery is assumed as a weak or dead battery.
The timer expiration time is set by TIM_DBP register.

Address 3Ch: DCIN_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Ch	DCIN_STAT	R	-	-	-	-	DCIN_OV	IGNORE(note3)	DCIN_CLPS_DET	DCIN_DET
	Initial Value	0Xh	0	0	0	0	x	x	x	x

Bit 3 : DCIN_OV DCIN over-voltage status
0 : Normal voltage
1 : DCIN > 6.5V

Bit 2 : IGNORE (note3) For ROHM factory only

Bit 1 : DCIN_CLPS_DET DCIN anti-collapse status
0 : Normal operation
1 : Anti-collapse

Bit 0 : DCIN_DET DCIN detection status
0 : Not detected or low level
1 : DCIN detected (over UVLO level)

Address 3Dh: VSYS_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Dh	VSYS_STAT	R	-	-	-	-	-	-	VSYS_LO	VSYS_UVN
	Initial Value	0Xh	0	0	0	0	0	0	x	x

Bit 1 : VSYS_LO — VSYS low voltage detection status. The threshold voltage is configurable by VSYS_MIN and VSYS_MAX. The higher voltage of among VSYS(Addr.C0h-C1h) and VSYS_SA(Addr.C2h-C3h) are used for VSYS voltage.
0:VSYS ≦ VSYS_MIN
1:VSYS ≧ VSYS_MAX

Bit 0 : VSYS_UVN — VSYS UVLO detection status
0:Low voltage
1:Normal voltage

Address 3Eh: CHG_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Eh	CHG_STAT	R	-	-	-	-	-	-	-	VRECHG_DET
	Initial Value	0Xh	0	0	0	0	0	0	0	x

Bit 0 : VRECHG_DET — Re-charge voltage detection status voltage.
0:VBAT > VBAT_MNT
1:VBAT ≦ VBAT_MNT

Address 3Fh: CHG_WDT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Fh	CHG_WDT_STAT	R	CHGWDTS[7:0]							
	Initial Value	XXh	x	x	x	x	x	x	x	x

Bit 7-0 : CHGWDTS[7:0] — Actual watch-dog timer counter value for Pre-charging & Tricle-Charging or Fast Charging & Top Off.
PCHG(or TCHG) : (CHGWDTS -1) X (64/60) min.
FCHG(or TOFF) : (CHGWDTS * 8 -240) * (64/60/2) min.
FCHG(or TOFF) COLD1 condition : (CHGWDTS * 8 -3) * (64/60) min.

Address 40h: BAT_TEMP Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
40h	BAT_TEMP	R	-	-	-	-	-	BAT_TEMP[2:0]		
	Initial Value	0Xh	0	0	0	0	0	x	x	x

The temperature thresholds have hysteresis. Table lists the temperature threshold values.

BAT_TEMP[2:0]	Temperature Range	Description
0h	Room Temp	T2 < Tbat < T3
1h	HOT1	T3 < Tbat < T5
2h	HOT2	T5 < Tbat < T4
3h	HOT3	T4 < Tbat
4h	COLD1	T1 < Tbat < T2
5h	COLD2	Tbat < T1
6h	Temp. Disable	Disable thermal control (No Thermistor)
7h	Battery Open	TS port is open

No.	Description	Default Value	Note
1	Lower threshold of T1	2 deg.	T1 in JEITA profile
2	Upper threshold of T1	5 deg.	T1 in JEITA profile
3	Lower threshold of T2	10 deg.	T2 in JEITA profile
4	Upper threshold of T2	13 deg.	T2 in JEITA profile
5	Lower threshold of T3	42 deg.	T3 in JEITA profile
6	Upper threshold of T3	45 deg.	T3 in JEITA profile
7	Lower threshold of T4	55 deg.	T4 in JEITA profile
8	Upper threshold of T4	58 deg.	T4 in JEITA profile
9	Lower threshold of T5	47 deg.	Between T3 and T4
10	Upper threshold of T5	50 deg.	Between T3 and T4

Measured/Preset Battery Temperature. -55 to 200 deg. Celsius, 1-degree steps.
Degree Celsius = 200 - BTMP[7:0](address 5Fh)

Address 41h: IGNORE_0 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41h	IGNORE_0	R	-	-	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)	IGNORE(note3)
	Initial Value	XXh	0	0	x	x	x	x	x	x

Bit 5-0 : IGNORE(note3) — For ROHM factory only

Address 42h: INHIBIT_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42h	INHIBIT_0	R/W	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_1(note2)	INHIBIT_1(note2)	INHIBIT_1(note2)
	Initial Value	E6h	1	1	1	0	0	1	1	0

Bit 7-0 : INHIBIT_0/1(note1/2) — For ROHM factory only

Address 43h: DCIN_CLPS Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h	DCIN_CLPS	R/W	DCIN_CLPS[11:4]							
	Initial Value	36h	0	0	1	1	0	1	1	0

Bit 7-0 : DCIN_CLPS[11:4] DCIN Anti-collapse entry voltage threshold 0.0V to 20.4V range, 80 mV steps.
When DCINOK = L, Anti-collapse detection is invalid.
When DCIN < DCIN_CLPS is detected, the charger decreases the input current restriction value.
DCIN_CLPS voltage must be set higher than VBAT_CHG1, VBAT_CHG2, and VBAT_CHG3.
If DCIN_CLPS set lower than these value, can't detect removing DCIN.

Address 44h: VSYS_REG Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
44h	VSYS_REG	R/W	-	-	-	VSYS_REG[4:0]				
	Initial Value	0Bh	0	0	0	0	1	0	1	1

Bit 7-0 : VSYS_REG[4:0] VSYS regulation voltage setting. 4.2V to 5.25V range, 50mV step.

VSYS_REG	VSYS Voltage
00h	4.20V
01h	4.25V
02h	4.30V
03h	4.35V
04h	4.40V
05h	4.45V
06h	4.50V
07h	4.55V
08h	4.60V
09h	4.65V
0Ah	4.70V
0Bh	4.75V
0Ch	4.80V
0Dh	4.85V
0Eh	4.90V
0Fh	4.95V
10h	5.00V
11h	5.05V
12h	5.10V
13h	5.15V
14h	5.20V
15h	5.25V

Address 45h: VSYS_MAX Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
45h	VSYS_MAX	R/W	-	VSYS_MAX[12:6]						
	Initial Value	33h	0	0	1	1	0	0	1	1

Bit 6-0 : VSYS_MAX[12:6] VSYS voltage rising detection threshold. 0.0V to 8.128V range, 64mV steps.

Address 46h: VSYS_MIN Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
46h	VSYS_MIN	R/W	-	VSYS_MIN[12:6]						
	Initial Value	30h	0	0	1	1	0	0	0	0

Bit 6-0 : VSYS_MIN[12:6] VSYS voltage falling detection threshold. 0.0V to 8.128V range, 64mV steps.

VSYS_MAX VSYS_MIN	VSYS Voltage
08h-28h	0.512V - 2.56 V
29h	2.624V
2Ah	2.688V
2Bh	2.752V
2Ch	2.816V
2Dh	2.880V
2Eh	2.944V
2Fh	3.008V
30h	3.072V
31h	3.136V
32h	3.200V
33h	3.264V
34h	3.328V
35h	3.392V
36h	3.456V
37h	3.520V
38h-6Dh	3.584V - 6.976V

Address 47h: CHG_SET1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
47h	CHG_SET1	R/W	WDT_DIS	WDT_AUTO	AUTO_FST	FST_TRG	AUTO_RECHG	BTMP_EN	COLD_ERR_EN	CHG_EN
	Initial Value	6Fh	0	1	1	0	1	1	1	1

Bit 7 : WDT_DIS Disable Charger Watch Dog Timer(WDT). This control is valid for watch dog timer of Trickle-charging, Pre-charging, Fast-charging and Top
0 : Normal operation
1 : Disable
When WDT_DIS = "0", the charger will stop charging when the WDT expired, indicating an error has occurred.
When WDT_DIS = "1", the Host should handle any error by its software.

Bit 6 : WDT_AUTO WDT setting mode
0 : Manual setting
1 : Auto setting
In auto setting mode, the WDT expiration time is set to 128 minutes for Pre-charging and 640 minites for Fast-charging.
In manual setting mode, the WDT expiration time is set by the register WDT_PRE for Pre-charging and the register WDT_FST for Fast-charging.

Bit 5 AUTO_FST Fast charging transition mode
0 : Manual control
1 : Auto control
When VBAT > VPRE_HI is detected at Pre-charging, the charger goes to Fast Charging.
In the Manual control mode, the Host should write FST_TRG = "1" to move the charger to Fast Charging.

Bit 4 FST_TRG Trigger Fast Charging
0 : No action
1 : Trigger to Fast Charging at Pre-Charge state with AUTO_FST='0'
The positive edge of FST_TRG is needed for the trigger.

Bit 3 AUTO_RECHG Automatic re-charging mode
0 : Manual control
1 : Auto control
In the auto control mode, the charger will re-start charging when the maintenance voltage is detected
(VBAT < VBAT_MNT).
While in manual control mode, VBAT_MNT can be detected but re-charging should be triggered by the software.

Bit 2 BTMP_EN Charging voltage is reduced by battery temperature.
0 : Disable
1 : Enable

Bit 1 COLD_ERR_EN Slow down the watch-dog timer counter in COLD1 condition.
0 : Disable Count down every 4.27min.
1 : Enable Count down every 8.53min.

Bit 0 CHG_EN Enabling charger operation.
0 : Disable
1 : Enable

Address 48h: CHG_SET2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
48h	CHG_SET2	R/W	VF_TREG_EN	EXTMOS_EN	REBATDET_TRG	BATDET_EN	INHIBIT_1(note2)	-	TIM_CNT_SEL[1:0]	
	Initial Value	98h	1	0	0	1	1	0	0	0

Bit7 : VF_TREG_EN Thermal shutdown for charger
0 : Disable
1 : Enable

Bit6 : EXTMOS_EN Select Internal/External MOSFET. Change this register after CHG_EN is set to '0' (charge disable)
0 : Charger uses Internal MOSFET.
1 : Charger uses External MOSFET.

Bit5 : REBATDET Trigger for re-trial of Battery detection
When REBATDET_TRG bit is set to 1, battery detection trial will start.
REBATDET TRG needs to be set 1 again after set to 0 for next battery detection.

Bit4 : BATDET_EN Enable Battery detection
0 : Disable
1 : Enable

Bit3 : INHIBIT_1(note2) For ROHM factory only

Bit1-0 : TIME_CNT_SEL[1:0] Transition Timer Setting from the Suspend State to the Trickle state.

TIM_CNT_SEL[2:0]	Timer Setting (CLK32K Cycle)
0h	1600 (48.8ms)
1h	3200 (97.7ms)
2h	4800 (146.5ms)
3h	6400 (195.3ms)

Address 49h: CHG_WDT_PRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
49h	CHG_WDT_PRE	R/W	WDT_PRE[7:0]							
	Initial Value	1Eh	0	0	0	1	1	1	1	0

Bit7-0 : WDT PRE[7:0] Watch Dog Timer setting for Pre-charging 1 to 272 minutes range, 64-sec steps.
This register is effective only when '0' is written to WDT_AUTO(address 47h Bit6).
PCHG(or TCHG) : (WDT_PRE -1) * (64/60) min.
It can be invalid with WDT_PRE set to '1' and expire immediately with WDT_PRE set to '0'.

Address 4Ah: CHG_WDT_FST Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Ah	CHG_WDT_FST	R/W	WDT_FST[10:3]							
	Initial Value	26h	0	0	1	0	0	1	1	0

Bit7-0 : WDT_FST[10:3] Watch Dog Timer setting for Fast Charging 8.5 to 2176 minutes range, 512-sec steps.
This register is effective only when '0' is written to WDT_AUTO(address 42h Bit6).
FCHG(or TOFF) : (WDT_FST * 8 -240) * (64/60/2) min.
FCHG(or TOFF) COLD1 condition : (WDT_FST * 8 -3) X (64/60) min.
The timer can be invalid with WDT_FST set to '0'.
In case of COLD1 condition, it can expire immediately with WDT_FST set to '30' or less.

Address 4Bh: CHG_IPRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Bh	CHG_IPRE	R/W	ITRI[3:0]				IPRE[3:0]			
	Initial Value	44h	0	1	0	0	0	1	0	0

Bit 4-0 : IPRI[3:0] Trickle charge current setting 20 mA to 100 mA range, 10 mA steps.

Bit 4-0 : ITRI[3:0] Pre-charging current setting 100 mA to 500 mA range, 50 mA steps.

ITRI	Trickle charging current
0h	0.0 mA
1h	2.5 mA
2h	5.0 mA
3h	7.5 mA
4h	10.0 mA
5h	12.5 mA
6h	15.0 mA
7h	17.5 mA
8h	20.0 mA
9h	22.5 mA
Ah	25.0 mA
Bh-Fh	(reserved)

IPRE	Pre-charging current
0h	0 mA
1h	25 mA
2h	50 mA
3h	75 mA
4h	100 mA
5h	125 mA
6h	150 mA
7h	175 mA
8h	200 mA
9h	225 mA
Ah	250 mA
Bh	275 mA
Ch	300 mA
Dh	325 mA
Eh	350 mA
Fh	375 mA

Address 4Ch: CHG_IFST Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Ch	CHG_IFST	R/W	-	-	-	IFST[4:0]				
	Initial Value	12h	0	0	0	1	0	0	1	0

Bit 4-0 : IFST[4:0] Battery Charging Current for Fast Charge 100 mA to 2000 mA range, 100 mA steps.

IFST	Fast charging Current	
	Internal MOSFET	External MOSFET
00h	0 mA	0 mA
01h	25 mA	100 mA
02h	50 mA	200 mA
03h	75 mA	300 mA
04h	100 mA	400 mA
05h	125 mA	500 mA
06h	150 mA	600 mA
07h	175 mA	700 mA
08h	200 mA	800 mA
09h	225 mA	900 mA
0Ah	250 mA	1000 mA
0Bh	275 mA	1100 mA
0Ch	300 mA	1200 mA
0Dh	325 mA	1300 mA
0Eh	350 mA	1400 mA
0Fh	375 mA	1500 mA
10h	400 mA	1600 mA
11h	425 mA	1700 mA
12h	450 mA	1800 mA
13h	475 mA	1900 mA
14h	500 mA	2000 mA
15h-1Fh	(reserved)	(reserved)

Address 4Dh: CHG_IFST_TERM Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Dh	CHG_IFST_TERM	R/W	-	-	-	-	IFST_TERM[3:0]			
	Initial Value	05h	0	0	0	0	0	1	0	1

Bit3-0 : IFST_TERM[3:0] Charging Termination Current for Fast Charge 10 mA to 200 mA range.

IFST_TERM	Termination Current	
	RSEN=10mohm	RSEN=30mohm
0h	0 mA	0 mA
1h	10 mA	3.33 mA
2h	20 mA	6.67 mA
3h	30 mA	10.0 mA
4h	40 mA	13.3 mA
5h	50 mA	16.7 mA
6h	100 mA	33.3 mA
7h	150 mA	50.0 mA
8h	200 mA	66.7 mA
9h-Fh	(reserved)	(reserved)

Address 4Eh: CHG_VPRE Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Eh	CHG_VPRE	R/W	VPRE_HI[3:0]				VPRE_LO[3:0]			
	Initial Value	C9h	1	1	0	0	1	0	0	1

Bit7-4 : VPRE_HI[3:0] Upper threshold of Pre-charging voltage 2.1V to 3.6V range, 0.1V steps.

Bit3-0 : VPRE_LO[3:0] Lower threshold of Pre-charging voltage 2.1V to 3.6V range, 0.1V steps.
VPRE_LO is also the upper threshold of Trickle Charging voltage.

VPRE_HI VPRE_LO	Setting Voltage
0h	2.1 V
1h	2.2 V
2h	2.3 V
3h	2.4 V
4h	2.5 V
5h	2.6 V
6h	2.7 V
7h	2.8 V
8h	2.9 V
9h	3.0 V
Ah	3.1 V
Bh	3.2 V
Ch	3.3 V
Dh	3.4 V
Eh	3.5 V
Fh	3.6 V

Address 4Fh: CHG_VBAT_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Fh	CHG_VBAT_1	R/W	-	-	-	VBAT_CHG1[4:0]				
	Initial Value	18h	0	0	0	1	1	0	0	0

Bit4-0 : VBAT_CHG1[4:0] Fast Charging Voltage for the temperature range ROOM.
3.72V to 4.34V range, 20mV step

VBAT_CHGx	Setting Voltage
00h	3.72 V
01h	3.74 V
02h	3.76 V
03h	3.78 V
04h	3.80 V
~	~
1Dh	4.30 V
1Eh	4.32 V
1Fh	4.34 V

Address 50h: CHG_VBAT_2 Register (R/W)

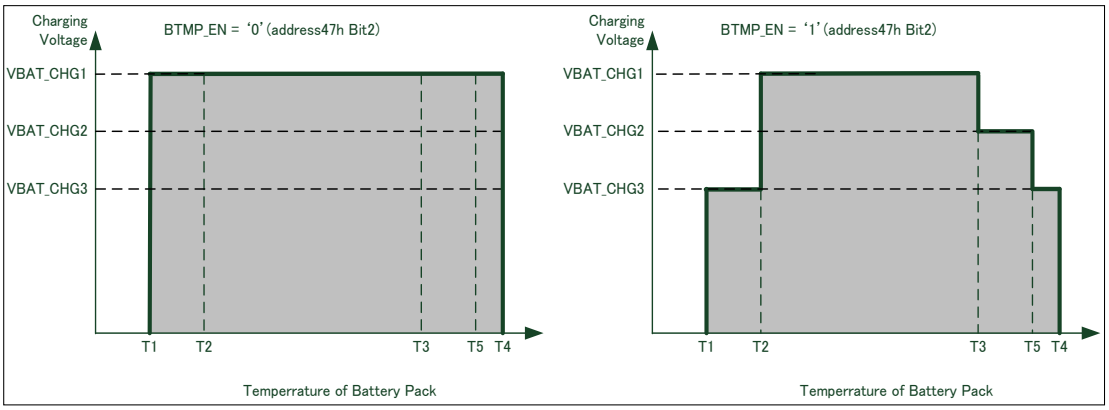
Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	CHG_VBAT_2	R/W	-	-	-	VBAT_CHG2[4:0]				
	Initial Value	13h	0	0	0	1	0	0	1	1

Bit4-0 : VBAT_CHG2[4:0] Fast Charging Voltage for the temperature range HOT1.
3.72V to 4.34V range, 20mV step

Address 51h: CHG_VBAT_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
51h	CHG_VBAT_3	R/W	-	-	-	VBAT_CHG3[4:0]				
	Initial Value	10h	0	0	0	1	0	0	0	0

Bit4-0 : VBAT_CHG3[4:0] Fast Charging Voltage for the temperature range HOT2 and COLD1.
3.72V to 4.34V range, 20mV step



Address 52h: CHG_LED_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	CHG_LED_1	R/W	-	-	-	CHG_LED_BTA_MASK	-	TERR[2:0]		
	Initial Value	03h	0	0	0	0	0	0	1	1

Bit4 : CHG LED BTA MASK
0 : Lighting
1 : Not lighting
CHGLED mask control for Battery Assist 1&2.

Bit2-0 : TERR[2:0] CHGLED lighting setting for the battery charging temperature error indication.

TERR	LED Lighting for Error Indication
0h	Always ON
1h	Blinking at 0.125 Hz
2h	Blinking at 0.25 Hz
3h	Blinking at 0.5 Hz
4h	Blinking at 1 Hz
5h	Blinking at 4 Hz
6h	Blinking at 8 Hz
7h	Light OFF

Address 53h: VF_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
53h	VF_TH	R/W	VF_TH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7-0 : VF_TH[7:0] Vf Voltage threshold for monitor. 0.100V to 1.395V range, 1.3V/256 steps.

Address 54h: BAT_SET_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
54h	BAT_SET_1	R/W	VBAT_HI[3:0]				VBAT_LO[3:0]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7-4 : VBAT_HI[3:0] Battery voltage threshold for VBAT rising 3.00V to 3.60V range, 50 mV steps.

Bit3-0 : VBAT_LO[3:0] Battery voltage threshold for VBAT falling 2.50V to 3.10V range, 50 mV steps.
VBAT_LO is also the lower threshold of dead battery detection.

VBAT_HI	Setting Voltage
0h	3.00 V
1h	3.05 V
2h	3.10 V
3h	3.15 V
4h	3.20 V
5h	3.25 V
6h	3.30 V
7h	3.35 V
8h	3.40 V
9h	3.45 V
Ah	3.50 V
Bh	3.55 V
Ch	3.60 V
Dh	3.65 V
Eh	3.70 V
Fh	3.75 V

VBAT_LO	Setting Voltage
0h	2.50 V
1h	2.55 V
2h	2.60 V
3h	2.65 V
4h	2.70 V
5h	2.75 V
6h	2.80 V
7h	2.85 V
8h	2.90 V
9h	2.95 V
Ah	3.00 V
Bh	3.05 V
Ch	3.10 V
Dh	3.15 V
Eh	3.20 V
Fh	3.25 V

Address 55h: BAT_SET_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
55h	BAT_SET_2	R/W	VBAT_OVP[3:0]				-	VBAT_MNT[2:0]		
	Initial Value	14h	0	0	0	1	0	1	0	0

Bit7-4 : VBAT_OVP[3:0] Battery over-voltage detection threshold. 4.20V to 4.60V range, 50 mV steps.

Bit2-0 : VBAT_MNT[2:0] Battery voltage maintenance threshold.
The charger starts re-charging when VBAT ≦ VBAT_MNT.

VBAT_OVP	Setting Voltage
0h	4.20 V
1h	4.25 V
2h	4.30 V
3h	4.35 V
4h	4.40 V
5h	4.45 V
6h	4.50 V
7h	4.55 V
8h	4.60 V
9h - Fh	(reserved)

VBAT_MNT	Setting Voltage
0h	VBAT_CHG1/2/3 - 0.35V
1h	VBAT_CHG1/2/3 - 0.30V
2h	VBAT_CHG1/2/3 - 0.25V
3h	VBAT_CHG1/2/3 - 0.20V
4h	VBAT_CHG1/2/3 - 0.15V
5h	VBAT_CHG1/2/3 - 0.10V
6h	VBAT_CHG1/2/3 - 0.05V
7h	VBAT_CHG1/2/3 - 0.00V

Address 56h: BAT_SET_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
56h	BAT_SET_3	R/W	-	VBAT_DONE[2:0]			-	TIM_DBP[2:0]		
	Initial Value	42h	0	1	0	0	0	0	1	0

Bit2-0 : VBAT_DONE[2:0] Charging Termination Battery voltage threshold for Fast Charge.
The charger accepts VBAT > VBAT_DONE as one of the condition for end of Fast Charge.

Bit2-0 : TIM_DBP[2:0] Dead Battery Provisioning timer setting
Refer to the description for DBAT_DET bit.

VBAT_DONE	Setting Voltage
0h	VBAT_CHG1/2/3 - 0.112V
1h	VBAT_CHG1/2/3 - 0.096V
2h	VBAT_CHG1/2/3 - 0.080V
3h	VBAT_CHG1/2/3 - 0.064V
4h	VBAT_CHG1/2/3 - 0.048V
5h	VBAT_CHG1/2/3 - 0.032V
6h	VBAT_CHG1/2/3 - 0.016V
7h	VBAT_CHG1/2/3 - 0.000V

TIM_DBP	DBP Timer Setting
0h	12 min
1h	32 min
2h	45 min
3h	64 min
4h	128 min
5h	5 min
6h	1 min
7h	0 min

Address 57h: ALM_VBAT_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
57h	ALM_VBAT_TH_U	R/W	-	-	-	-	-	-	-	VBAT_TH[12]
	Initial Value	01h	0	0	0	0	0	0	0	1

Address 58h: ALM_VBAT_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
58h	ALM_VBAT_TH_L	R/W	VBAT_TH[11:4]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

VBAT_TH[12:0] Battery Voltage Alarm Threshold.
Setting Range is from 0.000V to 8.176V, 16mV steps. It will be compared with VM_VBAT[12:4] (concatenated VM_VBAT_U[12:8] and VM_\
See also VBAT_MON_DET/RES alarm.

Address 59h: ALM_DCIN_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
59h	ALM_DCIN_TH	R/W	DCIN_TH[11:4]							
	Initial Value	0Fh	0	0	0	0	1	1	1	1

DCIN TH[11:4] DCIN Voltage Alarm Threshold.
Setting Range is from 0.0V to 20.4V, 80mV steps. It will be compared with VM_DCIN[11:4] (concatenated VM_DCIN_U[11:8] and VM_DCIN

Address 5Ah: ALM_VSYS_TH Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ah	ALM_VSYS_TH	R/W	VSYS_TH[12:5]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

Bit 7-0 : VSYS_TH[12:5] VSYS Voltage Alarm Threshold.
Setting Range is from 0.00V to 8.16V, 32mV steps.

Address 5Bh: VM_IBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Bh	VM_IBAT_U	R	IBAT_DIR	-	-	-	IBAT[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 5Ch: VM_IBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ch	VM_IBAT_L	R	IBAT[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Measured Battery Current
IBAT_DIR Current Direction
0 : Charging
1 : Discharging

IBAT[11:0] Absolute Current , 0.000A to 4.095A range(0.00A to 4.063A clamp), 1mA steps (RSENS=10mohm).
Absolute Current , 0.000A to 1.365A range(0.00A to 4.063A clamp), 0.33mA steps (RSENS=30mohm).
Series of IBAT_DIR and IBAT[11:0] (address from 5Bh to 5Ch) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address 5Dh: VM_VBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Dh	VM_VBAT_U	R	-	-	-	VBAT[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 5Eh: VM_VBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Eh	VM_VBAT_L	R	VBAT[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VBAT[12:0] Measured Battery Voltage. 0.000V to 8.191V range(0.4V to 5.6V clamp), 1mV steps.
This register value is also used for Over-Voltage detection and some Charger functions.
Series of VBAT[12:0] (address from 5Dh to 5Eh) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address 5Fh: VM_BTMP Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Fh	VM_BTMP	R	BTMP[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : BTMP[7:0] Measured Battery Temperature. -55 to 200 deg. Celsius, 1-degree steps.
Degree Celsius = 200 - BTMP[7:0]

Address 60h: VM_VTH Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60h	VM_VTH	R	VTH[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : VTH[7:0] Thermistor terminal (TS) voltage. 0.100V to 1.395V range, 1.3/256V steps.

Address 61h: VM_DCIN_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
61h	VM_DCIN_U	R	-	-	-	-	DCIN[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 62h: VM_DCIN_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
62h	VM_DCIN_L	R	DCIN[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

DCIN[11:0] Measured DCIN Voltage 0.000V to 20.475V range(1.200V to 16.80V clamp), 5mV steps.
Series of DCIN[11:0] (address from 61h to 62h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 64h: VM_VF Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64h	VM_VF	R	VF[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7-0 : VF[7:0] Die Vf Voltage monitor. 0.100V to 1.395V range, 1.3V/256 steps.

Address 65h: VM_OCI_PRE_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
65h	VM_OCI_PRE_U	R	IBAT_OC_PRE_DIR	-	-	-	IBAT_OC_PRE[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 66h: VM_OCI_PRE_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
66h	VM_OCI_PRE_L	R	IBAT_OC_PRE[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Measured Battery Current (1st time) at PMIC boot.
IBAT_OC_PRE_DIR Current Direction
0 : Charging
1 : Discharging

IBAT_OC_PRE[11:0] Absolute Current, 0.00A to 4.063A range, 1mA steps (RSENS=10mohm).
Absolute Current, 0.00A to 1.354A range, 0.33mA steps (RSENS=30mohm).
Series of IBAT_OC_PRE_DIR and IBAT_OC_PRE[11:0] (address from 65h to 66h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 67h: VM_OCV_PRE_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
67h	VM_OCV_PRE_U	R	-	-	-	VBAT_OC_PRE[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 68h: VM_OCV_PRE_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68h	VM_OCV_PRE_L	R	VBAT_OC_PRE[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VBAT_OC_PRE[11:0] Measured Battery Voltage (1st time) at boot, 0.000V to 8.191V range (0.6V to 5.6V clamp), 1mV steps.
Series of VBAT_OC_PRE[12:0] (address from 67h to 68h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 69h: VM_OCI_PST_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
69h	VM_OCI_PST_U	R	IBAT_OC_PST_DIR	-	-	-	IBAT_OC_PST[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 6Ah: VM_OCI_PST_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Ah	VM_OCI_PST_L	R	IBAT_OC_PST[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Measured Battery Current (2nd time) at PMIC boot.
IBAT_OC_PST_DIR Current Direction
0 : Charging
1 : Discharging

IBAT_OC_PST[11:0] Absolute Current, 0.00A to 4.063A range, 1mA steps (RSENS=10mohm).
Absolute Current, 0.00A to 1.354A range, 0.33mA steps (RSENS=30mohm).

Address 6Bh: VM_OCV_PST_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Bh	VM_OCV_PST_U	R	-	-	-	VBAT_OC_PST[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 6Ch: VM_OCV_PST_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Ch	VM_OCV_PST_L	R	VBAT_OC_PST[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VBAT_OC_PST[11:0] Measured Battery Voltage (2nd time) at boot, 0.000V to 8.191V range (0.6V to 5.6V clamp), 1mV steps.
Series of VBAT_OC_PST[12:0] (address from 6Bh to 6Ch) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 6Dh: VM_SA_VBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Dh	VM_SA_VBAT_U	R	-	-	-	VBAT_SA[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 6Eh: VM_SA_VBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Eh	VM_SA_VBAT_L	R	VBAT_SA[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VBAT SA[12:0] Measured Battery Voltage calculated simple average, 0.000V to 8.191V range(0.6V to 5.6V clamp), 1mV steps.
Series of VBAT_SA[12:0] (address from 6Dh to 6Eh) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 6Fh: VM_SA_IBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6Fh	VM_SA_IBAT_U	R	IBAT_SA_DIR	-	-	-	IBAT_SA[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 70h: VM_SA_IBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
70h	VM_SA_IBAT_L	R	IBAT_SA[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Measured Battery Current calculated simple average, 0.00A to 4.063A range, 1mA steps.
IBAT_SA_DIR Current Direction
0 : Charging
1 : Discharging

IBAT_SA[11:0] Absolute Current, 0.00A to 4.063A range, 1mA steps (RSENS=10mohm).
Absolute Current, 0.00A to 1.354A range, 0.33mA steps (RSENS=30mohm).
Series of IBAT_SA_DIR and IBAT_SA[11:0] (address from 6Fh to 70h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 71h: CC_CTRL Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
71h	CC_CTRL	R/W	CCNTRST	CCNTENB	CC_CALIB	-	-	-	-	-
	Initial Value	40h	0	1	0	0	0	0	0	0

Bit7 : CCNTRST Reset the Coulomb Counter
0 : Release reset
1 : Reset CC_CCNTD_3-0

Bit6 : CCNTENB Enable the Coulomb Counter
0 : Disable (stop counting)
1 : Enable (counting)

Bit5 : CC_CALIB
0: Automatic calibration
1: Force calibration
Writing 1 to CC_CALIB bit, then CC_CALIB bit is cleared to 0.

Address 72h: CC_BATCAP1_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72h	CC_BATCAP1_TH_U	R/W	-	-	-	-	CC_BATCAP1_TH[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 73h: CC_BATCAP1_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
73h	CC_BATCAP1_TH_L	R/W	CC_BATCAP1_TH[7:0]							
	Initial Value	7Eh	0	1	1	1	1	1	1	0

CC_BATCAP1_TH[11:0] Battery capacity monitor threshold1.
CC_BATCAP1_TH[11:0] is compared with CCNTD[27:16].

Address 74h: CC_BATCAP2_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74h	CC_BATCAP2_TH_U	R/W	-	-	-	-	CC_BATCAP2_TH[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 75h: CC_BATCAP2_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75h	CC_BATCAP2_TH_L	R/W	CC_BATCAP2_TH[7:0]							
	Initial Value	3Fh	0	0	1	1	1	1	1	1

CC_BATCAP2_TH[11:0] Battery capacity monitor threshold2.
CC_BATCAP2_TH[11:0] is compared with CCNTD[27:16].

Address 76h: CC_BATCAP3_TH_U Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
76h	CC_BATCAP3_TH_U	R/W	-	-	-	-	CC_BATCAP3_TH[11:8]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 77h: CC_BATCAP3_TH_L Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
77h	CC_BATCAP3_TH_L	R/W	CC_BATCAP3_TH[7:0]							
	Initial Value	1Fh	0	0	0	1	1	1	1	1

CC_BATCAP3_TH[11:0] Battery capacity monitor threshold3.
CC_BATCAP3_TH[11:0] is compared with CCNTD[27:16].

Address 78h: CC_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
78h	CC_STAT	R	-	-	-	-	-	CC_MON3	CC_MON2	CC_MON1
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 2 : CC_MON3 It indicates that the CCNTD[27:16] goes below the CC_BATCAP3_TH.
Bit 1 : CC_MON2 It indicates that the CCNTD[27:16] goes below the CC_BATCAP2_TH.
Bit 0 : CC_MON1 It indicates that the CCNTD[27:16] goes above the CC_BATCAP1_TH.

Address 79h: CC_CCNTD_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
79h	CC_CCNTD_3	R/W	-	-	-	-	CCNTD[27:24]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 7Ah: CC_CCNTD_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Ah	CC_CCNTD_2	R/W	CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 7Bh: CC_CCNTD_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Bh	CC_CCNTD_1	R/W	CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 7Ch: CC_CCNTD_0 Register (R/W)

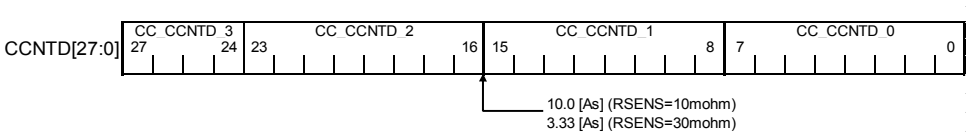
Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Ch	CC_CCNTD_0	R/W	CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CCNTD[27:0] Coulomb Counter

It indicates the Coulomb Counter accumulated result. CCNTD[27:16] means the battery capacity in 10 [As] (Ampere-second) unit when RSENS=10mohm is used, and CCNTD[1:0] is always "00". For example, when the battery capacity is 1350 [mAh], the register value will be shown as below
1350 [mAh] / 1000 [mA/A] x 3600 [s/h] = 4860 [As]. CCNTD[27:16] = 4860 / 10 = 486 (1E6h)

When CCNTENB = "1", the Coulomb Counter accumulates the charge or discharge current value.
In battery charging, the measured current value is added to the Coulomb Counter at every conversion period. Before battery charging starts, CCNTD must be reset to zero or initialized with an estimated SoC (State of Charge) value by software. If an empty battery is full-charged, CCNTD value indicates the actual battery capacity.

During battery discharging, the Coulomb Counter decreases in value. Before discharging, CCNTD must be initialized with BATCAP value by software, if the remaining battery capacity is unknown.



Series of CCNTD[27:0] (address from 79h to 7Ch) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 7Dh: CC_CURCD_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Dh	CC_CURCD_U	R	CURDIR	-	CURCD[13:8]					
	Initial Value	00h	0	0	0	0	0	0	0	0

Address 7Eh: CC_CURCD_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Eh	CC_CURCD_L	R	CURCD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CURDIR Battery current direction. "1": Discharging / "0": Charging.

CURCD[13:0] Battery current value converted from DS-ADC output, 0mA to 16,384mA range, 1 mA units (RSENS=10mohm).(0mA to 13,000mA)
Battery current value converted from DS-ADC output, 0mA to 5,461mA range, 0.33 mA units (RSENS=30mohm).(0mA to 4,333mA)

Series of CURCD[13:0] (address from 7Dh to 7Eh) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address 7Fh: VM_OCUR_THR_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Fh	VM_OCUR_THR_1	R/W	OCURTHR1[12:5]							
	Initial Value	7Dh	0	1	1	1	1	1	0	1

Bit 7-0 : OCURTHR1[12:5] Battery over-current threshold. The value is set in 64 mA units (RSENS=10mohm).
Battery over-current threshold. The value is set in 21.3 mA units (RSENS=30mohm).

Address 80h: VM_OCUR_DUR_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
80h	VM_OCUR_DUR_1	R/W	OCURDUR1[7:0]							
	Initial Value	64h	0	1	1	0	0	1	0	0

Bit 7-0 : OCURDUR1[7:0] The duration time(typ) for the battery over-current detection. The value is set in 250 us units.
If CURRD > OCURTHR1 for the duration of OCURDUR1, the register bit OCUR1 will be asserted.

Address 81h: VM_OCUR_THR_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
81h	VM_OCUR_THR_2	R/W	OCURTHR2[12:5]							
	Initial Value	5Eh	0	1	0	1	1	1	1	0

Bit 7-0 : OCURTHR2[12:5] Battery over-current threshold. The value is set in 64 mA units (RSENS=10mohm).
Battery over-current threshold. The value is set in 21.3 mA units (RSENS=30mohm).

Address 82h: VM_OCUR_DUR_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
82h	VM_OCUR_DUR_2	R/W	OCURDUR2[7:0]							
	Initial Value	8Ch	1	0	0	0	1	1	0	0

Bit 7-0 : OCURDUR2[7:0] The duration time(typ) for the battery over-current detection. The value is set in 250 us units.
If CURRD > OCURTHR2 for the duration of OCURDUR1, the register bit OCUR2 will be asserted.

Address 83h: VM_OCUR_THR_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
83h	VM_OCUR_THR_3	R/W	OCURTHR3[12:5]							
	Initial Value	4Eh	0	1	0	0	1	1	1	0

Bit 7-0 : OCURTHR3[12:5] Battery over-current threshold. The value is set in 64 mA units (RSENS=10mohm).
Battery over-current threshold. The value is set in 21.3 mA units (RSENS=30mohm).

Address 84h: VM_OCUR_DUR_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
84h	VM_OCUR_DUR_3	R/W	OCURDUR3[7:0]							
	Initial Value	A5h	1	0	1	0	0	1	0	1

Bit 7-0 : OCURDUR3[7:0] The duration time(typ) for the battery over-current detection. The value is set in 250 us units.
If CURRD > OCURTHR3 for the duration of OCURDUR3, the register bit OCUR3 will be asserted.

Address 85h: VM_OCUR_MON Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
85h	VM_OCUR_MON	R	-	-	-	-	-	OCUR3	OCUR2	OCUR1
	Initial Value	0Xh	0	0	0	0	0	x	x	x

Bit 2 : OCUR3 Battery over-current 3 detection status. “1”: Detected / “0”: Not detected.
Bit 1 : OCUR2 Battery over-current 2 detection status. “1”: Detected / “0”: Not detected.
Bit 0 : OCUR1 Battery over-current 1 detection status. “1”: Detected / “0”: Not detected.

Address 86h: VM_BTMP_OV_THR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
86h	VM_BTMP_OV_THR	R/W	OVBTMPTHR[7:0]							
	Initial Value	8Ch	1	0	0	0	1	1	0	0

Bit7-0 : OVBTMPTHR[7:0] Battery over-temperature threshold. The value is set in 1-degree units, -55 to 200 degree range.

Address 87h: VM_BTMP_OV_DUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
87h	VM_BTMP_OV_DUR	R/W	OVBTMPDUR[7:0]							
	Initial Value	28h	0	0	1	0	1	0	0	0

Bit 7-0 : OVBTMPDUR[7:0] The duration time(typ) for the battery over-temperature detection. The value is set in 244 us units.
If BTMPD > OVTMPTHR for the duration of OVTMPDUR, the register bit OVTMP will be asserted.

Address 88h: VM_BTMP_LO_THR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
88h	VM_BTMP_LO_THR	R/W	LOBTMPTHR[7:0]							
	Initial Value	C8h	1	1	0	0	1	0	0	0

Bit7-0 : LOBTMPTHR[7:0] : Battery low-temperature threshold. The value is set in 1-degree units, -55 to 200 degree range.

Address 89h: VM_BTMP_LO_DUR Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
89h	VM_BTMP_LO_DUR	R/W	LOBTMPDUR[7:0]							
	Initial Value	28h	0	0	1	0	1	0	0	0

Bit 7-0 : LOBTMPDUR[7:0] The duration time(typ) of the battery over-temperature detection. The value is set in 244 us units.
If BTMPD < LOTMPTHR for the duration of LOTMPDUR, the register bit LOTMP will be asserted.

Address 8Ah: VM_BTMP_MON Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ah	VM_BTMP_MON	R	-	-	-	-	-	-	OVBTMP	LOBTMP
	Initial Value	0Xh	0	0	0	0	0	0	x	x

Bit1 : OVBTMP : Battery over-temperature detection status. “1”: Detected / “0”: Not detected.
Bit0 : LOBTMP : Battery low-temperature detection status. “1”: Detected / “0”: Not detected.

Address 8Bh: INT_EN_01 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Bh	INT_EN_01	R/W	LED_SCP	LED_OCP	LED_OVP	BUCK5FAULT	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 : LED_SCP Enable LED SCP detection 1: Enable / 0: Disable.
Bit6 : LED_OCP Enable LED OCP detection 1: Enable / 0: Disable.
Bit5 : LED_OVP Enable LED OVP detection 1: Enable / 0: Disable.
Bit4 : BUCK5FAULT Enable BUCK5 output current limit detection interrupt 1: Enable / 0: Disable.
Bit3 : BUCK4FAULT Enable BUCK4 output current limit detection interrupt 1: Enable / 0: Disable.
Bit2 : BUCK3FAULT Enable BUCK3 output current limit detection interrupt 1: Enable / 0: Disable.
Bit1 : BUCK2FAULT Enable BUCK2 output current limit detection interrupt 1: Enable / 0: Disable.
Bit0 : BUCK1FAULT Enable BUCK1 output current limit detection interrupt 1: Enable / 0: Disable.

Address 8Ch: INT_EN_02 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Ch	INT_EN_02	R/W	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit5 : DCIN_OV_DET Interrupt Enable : DCIN Over-Voltage Detection : DCIN >= 6.5V(typ) 1: Enable / 0: Disable.
Bit4 : DCIN_OV_RES Interrupt Enable : DCIN Over-Voltage Resume : DCIN <= 6.5V-150mV(typ) 1: Enable / 0: Disable.
Bit3 : DCIN_CLPS_IN Interrupt Enable : DCIN Anti-Collapse Detection : DCIN(61h+62h) ≧ DCIN_CLPS(43h) 1: Enable / 0: Disable.
Bit2 : DCIN_CLPS_OUT Interrupt Enable : DCIN Anti-Collapse Resume : DCIN(61h+62h) < DCIN_CLPS(43h) 1: Enable / 0: Disable.
Bit1 : DCIN_RMV Interrupt Enable : DCIN Removal 1: Enable / 0: Disable.

Address 8Dh: INT_EN_03 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Dh	INT_EN_03	R/W	-	WDOGB	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_0(note1)	INHIBIT_0(note1)	DCIN_MON_DET	DCIN_MON_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit6 : WDOGB Interrupt Enable : WDOGB Detection 1: Enable / 0: Disable.
Bit5 : INHIBIT_0(note1) For ROHM factory only
Bit4 : INHIBIT_0(note1) For ROHM factory only
Bit3 : INHIBIT_0(note1) For ROHM factory only
Bit2 : INHIBIT_0(note1) For ROHM factory only
Bit1 : DCIN_MON_DET Interrupt Enable : DCIN General Alarm Detection : DCIN(61h+62h) ≦ DCIN_TH(59h) 1: Enable / 0: Disable.
Bit0 : DCIN_MON_RES Interrupt Enable : DCIN General Alarm Resume : DCIN(61h+62h) > DCIN_TH(59h) 1: Enable / 0: Disable.

Address 8Eh: INT_EN_04 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Eh	INT_EN_04	R/W	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UV_DET	VSYS_UV_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 : VSYS_MON_DET Interrupt Enable : VSYS General Alarm Detection : VSYS(63h) ≦ VSYS_TH(5Ah) 1: Enable / 0: Disable.
Bit6 : VSYS_MON_RES Interrupt Enable : VSYS General Alarm Resume : VSYS(63h) > VSYS_TH(5Ah) 1: Enable / 0: Disable.
Bit3 : VSYS_LO_DET Interrupt Enable : VSYS Low Voltage Detection : VSYS(63h) ≦ VSYS_MIN(46h) 1: Enable / 0: Disable.
Bit2 : VSYS_LO_RES Interrupt Enable : VSYS Low Voltage Resume : VSYS(63h) ≧ VSYS_MAX(45h) 1: Enable / 0: Disable.
Bit1 : VSYS_UV_DET Interrupt Enable : VSYS Under-Voltage Detection : VSYS ≦ 2.9V(typ) 1: Enable / 0: Disable.
Bit0 : VSYS_UV_RES Interrupt Enable : VSYS Under-Voltage Resume : VSYS ≧ 3.2V(typ) 1: Enable / 0: Disable.

Address 8Fh: INT_EN_05 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
8Fh	INT_EN_05	R/W	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	INHIBIT_0(NOTE1)
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 :	CHG_TRNS	Interrupt Enable : Battery Charger State Transition : CHG_STATE(39h)	1: Enable / 0: Disable.
Bit6 :	TMP_TRNS	Interrupt Enable : Ranged Battery Temperature Transition : BAT_TEMP(40h)	1: Enable / 0: Disable.
Bit5 :	BAT_MNT_IN	Interrupt Enable : Battery Maintenance(Re-Charging) Condition Detection :	1: Enable / 0: Disable.
		VBAT(5Dh+5Eh) ≦ VBAT_MNT(55h)	1: Enable / 0: Disable.
Bit4 :	BAT_MNT_OUT	Interrupt Enable : Battery Maintenance(Re-Charging) Condition Resume :	1: Enable / 0: Disable.
		VBAT(5Dh+5Eh) < VBAT_MNT(55h)	1: Enable / 0: Disable.
Bit3 :	CHG_WDT_EXP	Interrupt Enable : Charging Watch Dog Timer Expiration for abnormal long charging :	1: Enable / 0: Disable.
		CHG_WDT_PRE(49h), CHG_WDT_FST(4Ah)	1: Enable / 0: Disable.
Bit2 :	EXTEMP_TOUT	Interrupt Enable : Charging Watch Dog Timer Expiration for abnormal temperature protection :	1: Enable / 0: Disable.
		refer to "Battery Charger Block - Four Watch Dog Timers" section.	1: Enable / 0: Disable.
Bit0 :	INHIBIT_0(note1)	For ROHM factory only	

Address 90h: INT_EN_06 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
90h	INT_EN_06	R/W	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 :	TH_DET	Interrupt Enable : External Thermistor Detection	1: Enable / 0: Disable.
Bit6 :	TH_RMV	Interrupt Enable : External Thermister Removal	1: Enable / 0: Disable.
Bit5 :	BAT_DET	Interrupt Enable : Battery Detection :	1: Enable / 0: Disable.
		BAT_SET(3Bh) [5]BAT_DET, [4]BAT_DET_DONE and CHG_SET2(48h) [4]BATDET_E	1: Enable / 0: Disable.
Bit4 :	BAT_RMV	Interrupt Enable : Battery Removal : "	1: Enable / 0: Disable.
		BAT_SET(3Bh) [5]BAT_DET, [4]BAT_DET_DONE and CHG_SET2(48h) [4]BATDET_E	1: Enable / 0: Disable.
Bit1 :	TMP_OUT_DET	Interrupt Enable : "Out of Battery Charging Temperature Range" Detection :	1: Enable / 0: Disable.
		BAT_TEMP(40h) is HOT3 or COLD2	1: Enable / 0: Disable.
Bit0 :	TMP_OUT_RES	Interrupt Enable : "Out of Battery Charging Temperature Range" Resume :	1: Enable / 0: Disable.
		BAT_TEMP(40h) is except HOT3 and COLD2	1: Enable / 0: Disable.

Address 91h: INT_EN_07 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
91h	INT_EN_07	R/W	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 :	VBAT_OV_DET	Interrupt Enable : VBAT Over-Voltage Detection : VBAT(5Dh+5Eh) ≧ VBAT_OVP(55h)	1: Enable / 0: Disable.
Bit6 :	VBAT_OV_RES	Interrupt Enable : VBAT Over-Voltage Resume : VBAT(5Dh+5Eh) ≦ VBAT_OVP(55h)-150mV	1: Enable / 0: Disable.
Bit5 :	VBAT_LO_DET	Interrupt Enable : VBAT Low-Voltage Detection : VBAT(5Dh+5Eh) ≦ VBAT_LO(54h)	1: Enable / 0: Disable.
Bit4 :	VBAT_LO_RES	Interrupt Enable : VBAT Low-Voltage Resume : VBAT(5Dh+5Eh) ≧ VBAT_HI(54h)	1: Enable / 0: Disable.
Bit3 :	VBAT_SHT_DET	Interrupt Enable : VBAT Short-Circuit Detection : VBAT(5Dh+5Eh) ≦ 1.5V(typ)	1: Enable / 0: Disable.
Bit2 :	VBAT_SHT_RES	Interrupt Enable : VBAT Short-Circuit Resume : VBAT(5Dh+5Eh) > 1.6V(typ)	1: Enable / 0: Disable.
Bit1 :	DBAT_DET	Interrupt Enable : VBAT Dead-Battery Detection :	1: Enable / 0: Disable.
		VBAT(5Dh+5Eh) ≦ VBAT_LO(54h) with duration timer TIM_DBP(56h)	1: Enable / 0: Disable.

Address 92h: INT_EN_08 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
92h	INT_EN_08	R/W	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit1 :	VBAT_MON_DET	Interrupt Enable : VBAT General Alarm Detection : VBAT(5Dh+5Eh) ≦ VBAT_TH(57h+58h)	1: Enable / 0: Disable.
Bit0 :	VBAT_MON_RES	Interrupt Enable : VBAT General Alarm Resume : VBAT(5Dh+5Eh) > VBAT_TH(57h+58h)	1: Enable / 0: Disable.

Address 93h: INT_EN_09 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
93h	INT_EN_09	R/W	-	-	-	-	-	CC_MON3_DET	CC_MON2_DET	CC_MON1_DET
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit2 :	CC_MON3_DET	Interrupt Enable : Battery Capacity Alarm 3 :	1: Enable / 0: Disable.
		CCNTD(79h+7Ah+7Bh+7Ch) ≦ CC_BATCAP3_TH(76h+77h) (lower than equal)	1: Enable / 0: Disable.
Bit1 :	CC_MON2_DET	Interrupt Enable : Battery Capacity Alarm 2 :	1: Enable / 0: Disable.
		CCNTD(79h+7Ah+7Bh+7Ch) ≦ CC_BATCAP2_TH(74h+75h) (lower than equal)	1: Enable / 0: Disable.
Bit0 :	CC_MON1_DET	Interrupt Enable : Battery Capacity Alarm 1 :	1: Enable / 0: Disable.
		CCNTD(79h+7Ah+7Bh+7Ch) ≧ CC_BATCAP1_TH(72h+73h) (greater than equal)	1: Enable / 0: Disable.

Address 94h: INT_EN_10 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
94h	INT_EN_10	R/W	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit5 : OCUR3_DET Interrupt Enable : Battery Over-Current 3 Detection : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) ≧ OCURTHR3(83h) with duration timer OCURDUR3(84h) 1: Enable / 0: Disable.
Bit4 : OCUR3_RES Interrupt Enable : Battery Over-Current 3 Resume : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) < OCURTHR3(83h) with duration timer OCURDUR3(84h) 1: Enable / 0: Disable.
Bit3 : OCUR2_DET Interrupt Enable : Battery Over-Current 2 Detection : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) ≧ OCURTHR2(81h) with duration timer OCURDUR2(82h) 1: Enable / 0: Disable.
Bit2 : OCUR2_RES Interrupt Enable : Battery Over-Current 2 Resume : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) < OCURTHR2(81h) with duration timer OCURDUR2(82h) 1: Enable / 0: Disable.
Bit1 : OCUR1_DET Interrupt Enable : Battery Over-Current 1 Detection : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) ≧ OCURTHR1(7Fh) with duration timer OCURDUR1(80h) 1: Enable / 0: Disable.
Bit0 : OCUR1 RES Interrupt Enable : Battery Over-Current 1 Resume : 1: Enable / 0: Disable.
CURCD(7Dh+7Eh) < OCURTHR1(7Fh) with duration timer OCURDUR1(80h) 1: Enable / 0: Disable.

Address 95h: INT_EN_11 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
95h	INT_EN_11	R/W	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit7 : VF_DET Interrupt Enable : Die temp.(VF) General Alarm Detection : VF(64h) ≦ VF_TH(53h) 1: Enable / 0: Disable.
Bit6 : VF_RES Interrupt Enable : Die temp.(VF) General Alarm Resume : VF(64h) > VF_TH(53h) 1: Enable / 0: Disable.
Bit5 : VF125_DET Interrupt Enable : Die temp(VF) Over 125 degC Detection : VF(64h) ≦ 125 degC(typ) 1: Enable / 0: Disable.
Bit4 : VF125_RES Interrupt Enable : Die temp(VF) Over 125 degC Resume : VF(64h) > 125 degC(typ) 1: Enable / 0: Disable.
Bit3 : OVTMP_DET Interrupt Enable : Battery Over-Temperature Detection : 1: Enable / 0: Disable.
BTMP(5Fh) < OVBTMPTHR(86h) with duration timer OVBTMPDUR(87h) 1: Enable / 0: Disable.
Bit2 : OVTMP_RES Interrupt Enable : Battery Over-Temperature Resume : 1: Enable / 0: Disable.
BTMP(5Fh) ≧ OVBTMPTHR(86h) with duration timer OVBTMPDUR(87h) 1: Enable / 0: Disable.
Bit1 : LOTMP_DET Interrupt Enable : Battery Low-Temperature Detection : 1: Enable / 0: Disable.
BTMP(5Fh) > LOBTMPTHR(88h) with duration timer LOBTMPDUR(89h) 1: Enable / 0: Disable.
Bit0 : LOTMP_RES Interrupt Enable : Battery Low-Temperature Resume : 1: Enable / 0: Disable.
BTMP(5Fh) ≦ LOBTMPTHR(88h) with duration timer LOBTMPDUR(89h) 1: Enable / 0: Disable.

Address 96h: INT_EN_12 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
96h	INT_EN_12	R/W	-	-	-	-	-	ALM2	ALM1	ALM0
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit2 : ALM2 Interrupt Enable : RTC Alarm 2 : ALM2(35h) 1: Enable / 0: Disable.
Bit1 : ALM1 Interrupt Enable : RTC Alarm 1 : ALM0(2Ch-32h) with ALM0_MASK(34h) 1: Enable / 0: Disable.
Bit0 : ALM0 Interrupt Enable : RTC Alarm 0 : ALM0(25h-2Bh) with ALM0 MASK(33h) 1: Enable / 0: Disable.

Address 97h: INT_STAT Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
97h	INT_STAT	R	BUCK_AST	DCIN_AST	VSYS_AST	CHG_AST	BAT_AST	BMON_AST	TMPALE	ALM_AST
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7(R) : BUCK_AST Merged status of INT_STAT_01, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_01.

Bit 6(R) : DCIN_AST Merged status of INT_STAT_02-03, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_02-03.

Bit 5(R) : VSYS_AST Merged status of INT_STAT_04, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_04.

Bit 4(R) : CHG_AST Merged status of INT_STAT_05, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_05.

Bit 3(R) : BAT_AST Merged status of INT_STAT_06, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_06.

Bit 2(R) : BMON_AST Merged status of INT_STAT_07-10, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_07-10.

Bit 1(R) : TMP_AST Merged status of INT_STAT_11, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_11.

Bit 0(R) : ALM_AST Merged status of INT_STAT_12, 1: Event occurred / 0: No event.
Indicates the read data from all bits of INT_STAT_12.

Address 98h: INT_STAT_01 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
98h	INT_STAT_01	R/WC	LED_SCP	LED_OCP	LED_OVP	BUCK5FAULT	BUCK4FAULT	BUCK3FAULT	BUCK2FAULT	BUCK1FAULT
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :LED_SCP Interrupt Status : A bit is set when LED driver detects SCP. 1: Event occurred / 0: No event.
Bit 7 (W) LED_SCP Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :LED_OCP Interrupt Status : A bit is set when LED driver detects OCP. 1: Event occurred / 0: No event.
Bit 6 (W) LED_OCP Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 5 (R) :LED_OVP Interrupt Status : A bit is set when LED driver detects OVP. 1: Event occurred / 0: No event.
Bit 5 (W) LED_OVP Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :BUCK5FAULT Interrupt Status : A bit is set when BUCK5 detects OCP. 1: Event occurred / 0: No event.
Bit 4 (W) BUCK5FAULT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :BUCK4FAULT Interrupt Status : A bit is set when BUCK4 detects OCP. 1: Event occurred / 0: No event.
Bit 3 (W) BUCK4FAULT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :BUCK3FAULT Interrupt Status : A bit is set when BUCK3 detects OCP. 1: Event occurred / 0: No event.
Bit 2 (W) BUCK3FAULT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :BUCK2FAULT Interrupt Status : A bit is set when BUCK2 detects OCP. 1: Event occurred / 0: No event.
Bit 1 (W) BUCK2FAULT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :BUCK1FAULT Interrupt Status : A bit is set when BUCK1 detects OCP. 1: Event occurred / 0: No event.
Bit 0 (W) BUCK1FAULT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 99h: INT_STAT_02 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
99h	INT_STAT_02	R/WC	-	-	DCIN_OV_DET	DCIN_OV_RES	DCIN_CLPS_IN	DCIN_CLPS_OUT	DCIN_RMV	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5 (R) :DCIN_OV_DET Interrupt Status : A bit is set when detecting DCIN Over-Voltage : DCIN ≧ 6.5V(typ) 1: Event occurred / 0: No event.
Bit 5 (W) DCIN_OV_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :DCIN_OV_RES Interrupt Status : A bit is set when recovering from DCIN Over-Voltage : DCIN ≦ 6.5V-150mV(typ) 1: Event occurred / 0: No event.
Bit 4 (W) DCIN_OV_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :DCIN_CLPS_IN Interrupt Status : A bit is set when detecting DCIN Anti-Collapse : DCIN(61h+62h) ≧ DCIN_CLPS(43h) 1: Event occurred / 0: No event.
Bit 3 (W) DCIN_CLPS_IN Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :DCIN_CLPS_OUT Interrupt Status : A bit is set when recovering DCIN Anti-Collapse : DCIN(61h+62h) < DCIN_CLPS(43h) 1: Event occurred / 0: No event.
Bit 2 (W) DCIN_CLPS_OUT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :DCIN_RMV Interrupt Status : A bit is set when removing DCIN 1: Event occurred / 0: No event.
Bit 1 (W) DCIN_RMV Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 9Ah: INT_STAT_03 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Ah	INT_STAT_03	R/WC	-	WDOGB	INHIBIT_1(NOTE2) & IGNORE(NOTE3)	INHIBIT_1(NOTE2) & IGNORE(NOTE3)	INHIBIT_1(NOTE2) & IGNORE(NOTE3)	INHIBIT_1(NOTE2) & IGNORE(NOTE3)	DCIN_MON_DET	DCIN_MON_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit6 (R) : WDOGB Interrupt Status : A bit is set when detecting WDOGB input. 1: Event occurred / 0: No event.
Bit6 (W) :WDOGB Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit5 (R) : IGNORE(note3) For ROHM factory only
Bit5 (W) :INHIBIT_1(note2) For ROHM factory only

Bit4 (R) : IGNORE(note3) For ROHM factory only
Bit4 (W) :INHIBIT_1(note2) For ROHM factory only

Bit3 (R) : IGNORE(note3) For ROHM factory only
Bit3 (W) :INHIBIT_1(note2) For ROHM factory only

Bit2 (R) : IGNORE(note3) For ROHM factory only
Bit2 (W) :INHIBIT_1(note2) For ROHM factory only

Bit 1 (R) :DCIN_MON_DET Interrupt Status : A bit is set when detecting DCIN General Alarm : DCIN(61h+62h) ≦ DCIN_TH(59h) 1: Event occurred / 0: No event.
Bit 1 (W) DCIN_MON_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :DCIN_MON_RES Interrupt Status : A bit is set when recovering from DCIN General Alarm : DCIN(61h+62h) > DCIN_TH(59h 1: Event occurred / 0: No event.
Bit 0 (W) DCIN_MON_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 9Bh: INT_STAT_04 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Bh	INT_STAT_04	R/WC	VSYS_MON_DET	VSYS_MON_RES	-	-	VSYS_LO_DET	VSYS_LO_RES	VSYS_UVDET	VSYS_UV_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :VSYS_MON_DET Interrupt Status : A bit is set when detecting VSYS General Alarm : VSYS(63h) ≦ VSYS_TH(5Ah) 1: Event occurred / 0: No event.
Bit 7 (W) VSYS_MON_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :VSYS_MON_RES Interrupt Status : A bit is set when recovering from VSYS General Alarm : VSYS(63h) > VSYS_TH(5Ah) 1: Event occurred / 0: No event.
Bit 6 (W) VSYS_MON_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :VSYS_LO_DET Interrupt Status : A bit is set when detecting VSYS Low Voltage : VSYS(63h) ≦ VSYS_MIN(46h) 1: Event occurred / 0: No event.
Bit 3 (W) VSYS_LO_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :VSYS_LO_RES Interrupt Status : A bit is set when recovering VSYS Low Voltage : VSYS(63h) ≧ VSYS_MAX(45h) 1: Event occurred / 0: No event.
Bit 2 (W) VSYS_LO_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :VSYS_UVDET Interrupt Status : A bit is set when detecting VSYS Under-Voltage : VSYS ≦ 2.9V(typ) 1: Event occurred / 0: No event.
Bit 1 (W) VSYS_UVDET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :VSYS_UV_RES Interrupt Status : A bit is set when recovering VSYS Under-Voltage : VSYS ≧ 3.2V(typ) 1: Event occurred / 0: No event.
Bit 0 (W) VSYS_UV_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 9Ch: INT_STAT_05 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Ch	INT_STAT_05	R/WC	CHG_TRNS	TMP_TRNS	BAT_MNT_IN	BAT_MNT_OUT	CHG_WDT_EXP	EXTEMP_TOUT	-	INHIBIT_1(NOTE2) & IGNORE(NOTE3)
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :CHG_TRNS Interrupt Status : A bit is set when Battery Charger State translated : CHG_STATE(39h) 1: Event occurred / 0: No event.
Bit 7 (W) CHG_TRNS Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :TMP_TRNS Interrupt Status : A bit is set when Ranged Battery Temperature translated : BAT_TEMP(40h) 1: Event occurred / 0: No event.
Bit 6 (W) TMP_TRNS Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 5 (R) :BAT_MNT_IN Interrupt Status : A bit is set when detecting Battery Maintenance(Re-Charging) Condition : 1: Event occurred / 0: No event.
VBAT(5Dh+5Eh) ≦ VBAT_MNT(55h)
Bit 5 (W) BAT_MNT_IN Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :BAT_MNT_OUT Interrupt Status : A bit is set when recovering Battery Maintenance(Re-Charging) Condition : 1: Event occurred / 0: No event.
VBAT(5Dh+5Eh) < VBAT_MNT(55h)
Bit 4 (W) BAT_MNT_OUT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :CHG_WDT_EXP Interrupt Status : A bit is set when detecting Watch Dog Timeout for abnormal long charging : 1: Event occurred / 0: No event.
CHG_WDT_PRE(49h), CHG_WDT_FST(4Ah)
Bit 3 (W) CHG_WDT_EXP Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :EXTEMP_TOUT Interrupt Status : A bit is set when detecting Watch Dog Timeout for abnormal temperature protection : 1: Event occurred / 0: No event.
refer to "Battery Charger Block - Four Watch Dog Timers" section.
Bit 2 (W) EXTEMP_TOUT Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :IGNORE(note3) For ROHM factory only
Bit 0 (W) INHIBIT_1(note2) For ROHM factory only

Address 9Dh: INT_STAT_06 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Dh	INT_STAT_06	R/WC	TH_DET	TH_RMV	BAT_DET	BAT_RMV	-	-	TMP_OUT_DET	TMP_OUT_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :TH_DET Interrupt Status : A bit is set when detecting External Thermistor. 1: Event occurred / 0: No event.
Bit 7 (W) TH_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :TH_RMV Interrupt Status : A bit is set when removing External Thermister. 1: Event occurred / 0: No event.
Bit 6 (W) TH_RMV Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 5 (R) :BAT_DET Interrupt Status : A bit is set when detecting Battery : 1: Event occurred / 0: No event.
BAT_SET(3Bh) [5]BAT_DET, [4]BAT_DET_DONE and CHG_SET2(48h) [4]BATDET_EN
Bit 5 (W) BAT_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :BAT_RMV Interrupt Status : A bit is set when removing Battery : 1: Event occurred / 0: No event.
BAT_SET(3Bh) [5]BAT_DET, [4]BAT_DET_DONE and CHG_SET2(48h) [4]BATDET_EN
Bit 4 (W) BAT_RMV Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :TMP_OUT_DET Interrupt Status : A bit is set when detecting "Out of Battery Charging Temperature Range" : 1: Event occurred / 0: No event.
BAT_TEMP(40h) is HOT3 or COLD2
Bit 1 (W) TMP_OUT_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :TMP_OUT_RES Interrupt Status : A bit is set when recovering from "Out of Battery Charging Temperature Range" : 1: Event occurred / 0: No event.
BAT_TEMP(40h) is except HOT3 and COLD2
Bit 0 (W) TMP_OUT_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 9Eh: INT_STAT_07 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Eh	INT_STAT_07	R/WC	VBAT_OV_DET	VBAT_OV_RES	VBAT_LO_DET	VBAT_LO_RES	VBAT_SHT_DET	VBAT_SHT_RES	DBAT_DET	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :VBAT_OV_DET Interrupt Status : A bit is set when detecting VBAT Over-Voltage : VBAT(5Dh+5Eh) ≧ VBAT_OVP(55h) 1: Event occurred / 0: No event.
Bit 7 (W) VBAT_OV_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :VBAT_OV_RES Interrupt Status : A bit is set when recovering from VBAT Over-Voltage : VBAT(5Dh+5Eh) ≦ VBAT_OVP(55h)-150mV 1: Event occurred / 0: No event.
Bit 6 (W) VBAT_OV_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 5 (R) :VBAT_LO_DET Interrupt Status : A bit is set when detecting VBAT Low-Voltage : VBAT(5Dh+5Eh) ≦ VBAT_LO(54h) 1: Event occurred / 0: No event.
Bit 5 (W) VBAT_LO_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :VBAT_LO_RES Interrupt Status : A bit is set when recovering from VBAT Low-Voltage : VBAT(5Dh+5Eh) ≧ VBAT_HI(54h 1: Event occurred / 0: No event.
Bit 4 (W) VBAT_LO_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :VBAT_SHT_DET Interrupt Status : A bit is set when detecting VBAT Short-Circuit : VBAT(5Dh+5Eh) ≦1.5V(typ) 1: Event occurred / 0: No event.
Bit 3 (W) VBAT_SHT_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :VBAT_SHT_RES Interrupt Status : A bit is set when recovering from VBAT Short-Circuit Detection : VBAT(5Dh+5Eh) > 1.6V 1: Event occurred / 0: No event.
Bit 2 (W) VBAT_SHT_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :DBAT_DET Interrupt Status : A bit is set when detecting VBAT Dead-Battery : VBAT(5Dh+5Eh) ≦VBAT_LO(54h) with duration timer TIM_DBP(56h) 1: Event occurred / 0: No event.
Bit 1 (W) DBAT_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address 9Fh: INT_STAT_08 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9Fh	INT_STAT_08	R/WC	-	-	-	-	-	-	VBAT_MON_DET	VBAT_MON_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 1 (R) :VBAT_MON_DET Interrupt Status : A bit is set when detecting VBAT General Alarm : VBAT(5Dh+5Eh) ≦ VBAT_TH(57h+58 1: Event occurred / 0: No event.
Bit 1 (W) VBAT_MON_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :VBAT_MON_RES Interrupt Status : A bit is set when recovering from VBAT General Alarm : VBAT(5Dh+5Eh) > VBAT_TH(57 1: Event occurred / 0: No event.
Bit 0 (W) VBAT_MON_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address A0h: INT_STAT_09 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A0h	INT_STAT_09	R/WC	-	-	-	-	-	CC_MON3_DET	CC_MON2_DET	CC_MON1_DET
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 2 (R) :CC_MON3_DET Interrupt Status : A bit is set when detecting Battery Capacity Alarm 3 : CCNTD(79h+7Ah+7Bh+7Ch) ≦ CC_BATCAP3_TH(76h+77h) (lower than equal) 1: Event occurred / 0: No event.
Bit 2 (W) CC_MON3_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :CC_MON2_DET Interrupt Status : A bit is set when detecting Battery Capacity Alarm 2 : CCNTD(79h+7Ah+7Bh+7Ch) ≦ CC_BATCAP2_TH(74h+75h) (lower than equal) 1: Event occurred / 0: No event.
Bit 1 (W) CC_MON2_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :CC_MON1_DET Interrupt Status : A bit is set when detecting Battery Capacity Alarm 1 : CCNTD(79h+7Ah+7Bh+7Ch) ≧ CC_BATCAP1_TH(72h+73h) (greater than equal) 1: Event occurred / 0: No event.
Bit 0 (W) CC_MON1_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address A1h: INT_STAT_10 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A1h	INT_STAT_10	S/WC	-	-	OCUR3_DET	OCUR3_RES	OCUR2_DET	OCUR2_RES	OCUR1_DET	OCUR1_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5 (R) :OCUR3_DET Interrupt Status : A bit is set when detecting Battery Over-Current 3 : CURCD(7Dh+7Eh) ≧ OCURTHR3(83h) with duration timer OCURDUR3(84h) 1: Event occurred / 0: No event.
Bit 5 (W) OCUR3_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 4 (R) :OCUR3_RES Interrupt Status : A bit is set when recovering from Battery Over-Current 3 : CURCD(7Dh+7Eh) < OCURTHR3(83h) with duration timer OCURDUR3(84h) 1: Event occurred / 0: No event.
Bit 4 (W) OCUR3_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :OCUR2_DET Interrupt Status : A bit is set when detecting Battery Over-Current 2 : CURCD(7Dh+7Eh) ≧ OCURTHR2(81h) with duration timer OCURDUR2(82h) 1: Event occurred / 0: No event.
Bit 3 (W) OCUR2_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :OCUR2_RES Interrupt Status : A bit is set when recovering from Battery Over-Current 2 : CURCD(7Dh+7Eh) < OCURTHR2(81h) with duration timer OCURDUR2(82h) 1: Event occurred / 0: No event.
Bit 2 (W) OCUR2_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :OCUR1_DET Interrupt Status : A bit is set when detecting Battery Over-Current 1 : CURCD(7Dh+7Eh) ≧ OCURTHR1(7Fh) with duration timer OCURDUR1(80h) 1: Event occurred / 0: No event.
Bit 1 (W) OCUR1_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :OCUR1_RES Interrupt Status : A bit is set when recovering from Battery Over-Current 1 : CURCD(7Dh+7Eh) < OCURTHR1(7Fh) with duration timer OCURDUR1(80h) 1: Event occurred / 0: No event.
Bit 0 (W) OCUR1_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address A2h: INT_STAT_11 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A2h	INT_STAT_11	S/WC	VF_DET	VF_RES	VF125_DET	VF125_RES	OVTMP_DET	OVTMP_RES	LOTMP_DET	LOTMP_RES
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 (R) :VF_DET Interrupt Status : A bit is set when detecting Die temp.(VF) General Alarm : VF(64h) ≦ VF_TH(53h) 1: Event occurred / 0: No event.
Bit 7 (W) VF_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :VF_RES Interrupt Status : A bit is set when Recovering from Die temp.(VF) General Alarm : VF(64h) > VF_TH(53h) 1: Event occurred / 0: No event.
Bit 6 (W) VF_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :VF125_DET Interrupt Status : A bit is set when detecting Die temp(VF) Over 125 degC : VF(64h) ≦125 degC(typ) 1: Event occurred / 0: No event.
Bit 6 (W) VF125_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 6 (R) :VF125_RES Interrupt Status : A bit is set when Recovering from Die temp(VF) Over 125 degC : VF(64h) > 125 degC(ty 1: Event occurred / 0: No event.
Bit 6 (W) VF125_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 3 (R) :OVTMP_DET Interrupt Status : A bit is set when detecting Battery Over-Temperature : 1: Event occurred / 0: No event.
BTMP(5Fh) < OVBTMPTHR(86h) with duration timer OVBTMPDUR(87h)
Bit 3 (W) OVTMP_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 2 (R) :OVTMP_RES Interrupt Status : A bit is set when Recovering from Battery Over-Temperature : 1: Event occurred / 0: No event.
BTMP(5Fh) ≧ OVBTMPTHR(86h) with duration timer OVBTMPDUR(87h)
Bit 2 (W) OVTMP_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :LOTMP_DET Interrupt Status : A bit is set when detecting Battery Low-Temperature : 1: Event occurred / 0: No event.
BTMP(5Fh) > LOBTMPTHR(88h) with duration timer LOBTMPDUR(89h)
Bit 1 (W) LOTMP_DET Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :LOTMP_RES Interrupt Status : A bit is set when Recovering from Battery Low-Temperature : 1: Event occurred / 0: No event.
BTMP(5Fh) ≦ LOBTMPTHR(88h) with duration timer LOBTMPDUR(89h)
Bit 0 (W) LOTMP_RES Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address A3h: INT_STAT_12 Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A3h	INT_STAT_12	S/WC	-	-	-	-	-	ALM2	ALM1	ALM0
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 2 (R) :ALM2 Interrupt Status : A bit is set when detecting RTC Alarm 2 : ALM2(35h) 1: Event occurred / 0: No event.
Bit 2 (W) ALM2 Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 1 (R) :ALM1 Interrupt Status : A bit is set when detecting RTC Alarm 1 : ALM0(2Ch-32h) with ALM0_MASK(34h) 1: Event occurred / 0: No event.
Bit 1 (W) ALM1 Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Bit 0 (R) :ALM0 Interrupt Status : A bit is set when detecting RTC Alarm 0 : ALM0(25h-2Bh) with ALM0_MASK(33h) 1: Event occurred / 0: No event.
Bit 0 (W) ALM0 Write 1 to this bit to clear the status. 1: Clear / 0: Not clear.

Address A4h: INT_UPDATE Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A4h	INT_UPDATE	R/WC	-	-	-	-	-	-	-	INT_UPDATE
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit0 : INT_UPDATE The present interruption status is updated.
0 : Interruption is not updated.
1 : Interruption is updated and INT_UPDATE bit is cleared to 0.

Address B0h: RESERVE_0 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B0h	RESERVE_0	R/W	RESERVE_0[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_0[7:0] Reserved registers which user can use

Address B1h: RESERVE_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B1h	RESERVE_1	R/W	RESERVE_1[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_1[7:0] Reserved registers which user can use

Address B2h: RESERVE_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B2h	RESERVE_2	R/W	RESERVE_2[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_2[7:0] Reserved registers which user can use

Address B3h: RESERVE_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B3h	RESERVE_3	R/W	RESERVE_3[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_3[7:0] Reserved registers which user can use

Address B4h: RESERVE_4 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B4h	RESERVE_4	R/W	RESERVE_4[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_4[7:0] Reserved registers which user can use

Address B5h: RESERVE_5 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B5h	RESERVE_5	R/W	RESERVE_5[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_5[7:0] Reserved registers which user can use

Address B6h: RESERVE_6 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B6h	RESERVE_6	R/W	RESERVE_6[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_6[7:0] Reserved registers which user can use

Address B7h: RESERVE_7 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B7h	RESERVE_7	R/W	RESERVE_7[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_7[7:0] Reserved registers which user can use

Address B8h: RESERVE_8 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B8h	RESERVE_8	R/W	RESERVE_8[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_8[7:0] Reserved registers which user can use

Address B9h: RESERVE_9 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B9h	RESERVE_9	R/W	RESERVE_9[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : RESERVE_9[7:0] Reserved registers which user can use

Address C0h: VM_VSYS_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C0h	VM_VSYS_U	S	-	-	-	VSYS[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address C1h: VM_VSYS_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C1h	VM_VSYS_L	S	VSYS[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VSYS[12:0] Measured VSYS voltage 0.00V to 8.191V(0.50V to 7.00V clamp), 1 mV steps.

Series of VSYS[12:0] (address from C0h to C1h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address C2h: VM_SA_VSYS_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C2h	VM_SA_VSYS_U	S	-	-	-	VSYS_SA[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address C3h: VM_SA_VSYS_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
C3h	VM_SA_VSYS_L	S	VSYS_SA[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VSYS_SA[12:0] Measured VSYS voltage calculated simple average 0.00V to 8.191V(0.50V to 7.00V clamp), 1 mV steps.

Series of VSYS_SA[12:0] (address from C2h to C3h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address D0h: VM_SA_IBAT_MIN_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D0h	VM_SA_IBAT_MIN_U	S	IBAT_SA_MIN_DIR	-	-	-	IBAT_SA_MIN[11:8]			
	Initial Value	0Fh	0	0	0	0	1	1	1	1

Address D1h: VM_SA_IBAT_MIN_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D1h	VM_SA_IBAT_MIN_L	S	IBAT_SA_MIN[7:0]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

Latest minimum Battery Current (simple average), 0.00A to 4.063A range, 1mA steps.
IBAT_SA_MIN_DIR Current Direction
0 : Charging
1 : Discharging

IBAT_SA_MIN[11:0] Absolute Current, 0.00A to 4.063A range, 1mA steps (RSENS=10mohm).
Absolute Current, 0.00A to 1.354A range, 0.33mA steps (RSENS=30mohm).
Series of IBAT_SA_MIN_DIR and IBAT_SA_MIN[11:0] (address from D0h to D1h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address D2h: VM_SA_IBAT_MAX_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D2h	VM_SA_IBAT_MAX_U	S	IBAT_SA_MAX_DIR	-	-	-	IBAT_SA_MAX[11:8]			
	Initial Value	8Fh	1	0	0	0	1	1	1	1

Address D3h: VM_SA_IBAT_MAX_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D3h	VM_SA_IBAT_MAX_L	S	IBAT_SA_MAX[7:0]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

Latest maximum Battery Current (simple average), 0.00A to 4.063A range, 1mA steps.
IBAT_SA_MAX_DIR Current Direction
0 : Charging
1 : Discharging

IBAT_SA_MAX[11:0] Absolute Current, 0.00A to 4.063A range, 1mA steps (RSENS=10mohm).
Absolute Current, 0.00A to 1.354A range, 0.33mA steps (RSENS=30mohm).
Series of IBAT_SA_MAX_DIR and IBAT_SA_MAX[11:0] (address from D2h to D3h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address D4h: VM_SA_VBAT_MIN_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D4h	VM_SA_VBAT_MIN_U	S	-	-	-	VBAT_SA_MIN[12:8]				
	Initial Value	1Fh	0	0	0	1	1	1	1	1

Address D5h: VM_SA_VBAT_MIN_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D5h	VM_SA_VBAT_MIN_L	S	VBAT_SA_MIN[7:0]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

VBAT_SA_MIN[12:0] Latest minimum Battery Voltage (simple average), 0.000V to 8.191V range (0.6V to 5.6V clamp), 1mV steps.
Series of VBAT_SA_MIN[12:0] (address from D4h to D5h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address D6h: VM_SA_VBAT_MAX_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D6h	VM_SA_VBAT_MAX_U	S	-	-	-	VBAT_SA_MAX[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address D7h: VM_SA_VBAT_MAX_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D7h	VM_SA_VBAT_MAX_L	S	VBAT_SA_MAX[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VBAT_SA_MAX[12:0] Latest maximum Battery Voltage (simple average), 0.000V to 8.191V range (0.6V to 5.6V clamp), 1mV steps.
Series of VBAT_SA_MAX[12:0] (address from D6h to D7h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address D8h: VM_SA_VSYS_MIN_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D8h	VM_SA_VSYS_MIN_U	S	-	-	-	VSYS_SA_MIN[12:8]				
	Initial Value	1Fh	0	0	0	1	1	1	1	1

Address D9h: VM_SA_VSYS_MIN_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
D9h	VM_SA_VSYS_MIN_L	S	VSYS_SA_MIN[7:0]							
	Initial Value	FFh	1	1	1	1	1	1	1	1

VSYS_SA_MIN[12:0] Latest minimum VSYS voltage (simple average) 0.00V to 8.191V(0.50V to 7.00V clamp), 1 mV steps.
Series of VSYS_SA_MIN[12:0] (address from D8h to D9h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address DAh: VM_SA_VSYS_MAX_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DAh	VM_SA_VSYS_MAX_U	S	-	-	-	VSYS_SA_MAX[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address DBh: VM_SA_VSYS_MAX_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DBh	VM_SA_VSYS_MAX_L	S	VSYS_SA_MAX[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

VSYS_SA_MAX[12:0] Latest maximum VSYS voltage (simple average) 0.00V to 8.191V(0.50V to 7.00V clamp), 1 mV steps.
Series of VSYS_SA_MAX[12:0] (address from DAh to DBh) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address DCh: VM_SA_MINMAX_CLR Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DCh	VM_SA_MINMAX_CLR	R/WC	-	-	VSYS_SA_MAX_CLR	VSYS_SA_MIN_CLR	IBAT_SA_MAX_CLR	IBAT_SA_MIN_CLR	VBAT_SA_MAX_CLR	VBAT_SA_MIN_CLR
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 5 : VSYS_SA_MAX_CLR Clear for VSYS_SA_MAX[12:0] register, then VSYS_SA_MAX_CLR bit is cleared to 0. 1: Clear / 0: Not clear.
Bit 4 : VSYS_SA_MIN_CLR Clear for VSYS_SA_MIN[12:0] register, then VSYS_SA_MIN_CLR bit is cleared to 0. 1: Clear / 0: Not clear.
Bit 3 : IBAT_SA_MAX_CLR Clear for IBAT_SA_MAX_DIR and IBAT_SA_MAX[11:0] register, then IBAT_SA_MAX_CLR bit is cleared t 1: Clear / 0: Not clear.
Bit 2 : IBAT_SA_MIN_CLR Clear for IBAT_SA_MIN_DIR and IBAT_SA_MIN[11:0] register, then IBAT_SA_MIN_CLR bit is cleared to (1: Clear / 0: Not clear.
Bit 1 : VBAT_SA_MAX_CLR Clear for VBAT_SA_MAX[12:0] register, then VBAT_SA_MAX_CLR bit is cleared to 0. 1: Clear / 0: Not clear.
Bit 0 : VBAT_SA_MIN_CLR Clear for VBAT_SA_MIN[12:0] register, then VBAT_SA_MIN_CLR bit is cleared to 0. 1: Clear / 0: Not clear.

Address E0h: REX_CCNTD_3 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E0h	REX_CCNTD_3	S	-	-	-	-	REX_CCNTD[27:24]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address E1h: REX_CCNTD_2 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E1h	REX_CCNTD_2	S	REX_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

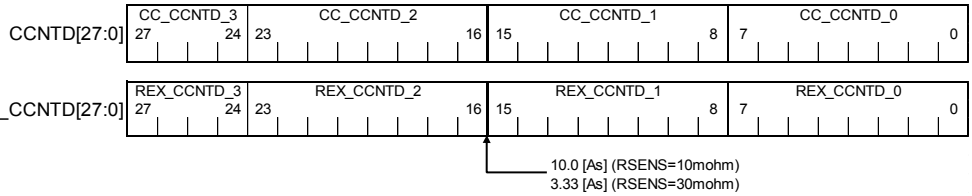
Address E2h: REX_CCNTD_1 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E2h	REX_CCNTD_1	S	REX_CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address E3h: REX_CCNTD_0 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E3h	REX_CCNTD_0	S	REX_CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

REX_CCNTD[27:0] Coulomb Counter value at Relax State detection.



Series of REX_CCNTD[27:0] (address from E0h to E3h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address E4h: REX_SA_VBAT_U Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E4h	REX_SA_VBAT_U	S	-	-	-	REX_VBAT_SA[12:8]				
	Initial Value	00h	0	0	0	0	0	0	0	0

Address E5h: REX_SA_VBAT_L Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E5h	REX_SA_VBAT_L	S	REX_VBAT_SA[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

REX_VBAT_SA[12:0] Battery Voltage at Relax State detection, 0.000V to 8.919V range (0.6V to 5.6V clamp), 1mV steps.
Series of REX_VBAT_SA[12:0] (address from E4h to E5h) should be read in accordance with continuous manner, so stop condition should not be inserted during reading these registers.

Address E6h: REX_CTRL_1 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E6h	REX_CTRL_1	R/W	-	-	-	REX_CLR	REX_EN	REX_PMU_STATE_MASK	REX_DUR[1:0]	
	Initial Value	09h	0	0	0	0	1	0	0	1

Bit 4 : REX_CLR Clear for REX_CCNTD[27:0] and REX_VBAT_SA[12:0] register.
0: Not clear.
1: Clear
Writing 1 to REX_CLR bit, then REX_CLR bit is cleared to 0.

Bit 3 : REX_EN Enable Relax State detection.
Relax State detection accepts Power State as one of the condition.
0 : Disable. Immediately exits Relax State action.
1 : Enable.

Bit 2 : REX_PMU_STATE_MASK Mask a condition according to Power State for Relax State detection.
0 : Not mask.
1: Mask.

Bit 1-0 : REX_DUR Duration Timer setting for Relax State detection.

REX_DUR	Duration time
0h	32 min
1h	64 min
2h	96 min
3h	128 min

Address E7h: REX_CTRL_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E7h	REX_CTRL_2	R/W	REX_CURCD_TH[7:0]							
	Initial Value	0Ah	0	0	0	0	1	0	1	0

Bit 7-0 : REX_CURCD_TH Battery Current threshold for Relax State detection, 1mA to 255mA range, 1mA steps (RSENS=10mohm).
Battery Current threshold for Relax State detection, 0.33mA to 85mA range, 0.33mA steps (RSENS=30mohm).

If REX_CURCD_TH bits are set to 00h, battery current (CURCD bits) is ignored for Relax State detection.
If REX_CURCD_TH bits are set to a value except 00h,
Battery current (CURCD bits ≤ REX_CURCD_TH bits) is applied as one of the conditions of Relax State detection.

Address E8h: FULL_CCNTD_3 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E8h	FULL_CCNTD_3	S	-	-	-	-	FULL_CCNTD[27:24]			
	Initial Value	00h	0	0	0	0	0	0	0	0

Address E9h: FULL_CCNTD_2 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
E9h	FULL_CCNTD_2	S	FULL_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

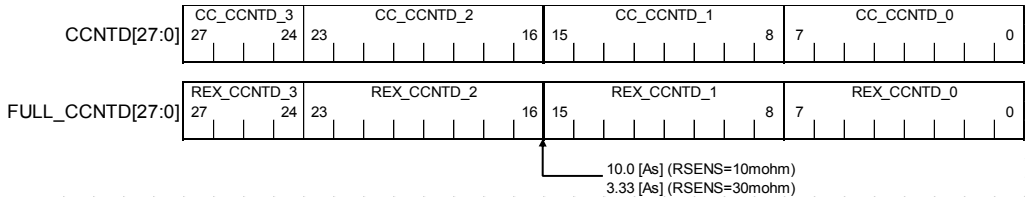
Address EAh: FULL_CCNTD_1 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EAh	FULL_CCNTD_1	S	FULL_CCNTD[15:8]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Address EBh: FULL_CCNTD_0 Register (R)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EBh	FULL_CCNTD_0	S	FULL_CCNTD[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

FULL_CCNTD[27:0] Coulomb Counter value when the charger judged end of full charging (DONE) with ROOM temperature.



Series of FULL_CCNTD[27:0] (address from E8h to EBh) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address ECh: FULL_CTRL Register (R/WC)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ECh	FULL_CTRL	R/WC	-	-	-	FULL_CLR	-	-	-	-
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 4 : FULL_CLR Clear for FULL_CCNTD[27:0] register.
0 : Not clear.
1 : Clear
Writing 1 to FULL_CLR bit, then FULL_CLR bit is cleared to 0.

Address F0h: CCNTD_CHG_3 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F0h	CCNTD_CHG_3	R/W	CHG_CCNTD[31:24]							
	Initial Value	00h	0	0	0	0	0	0	0	0

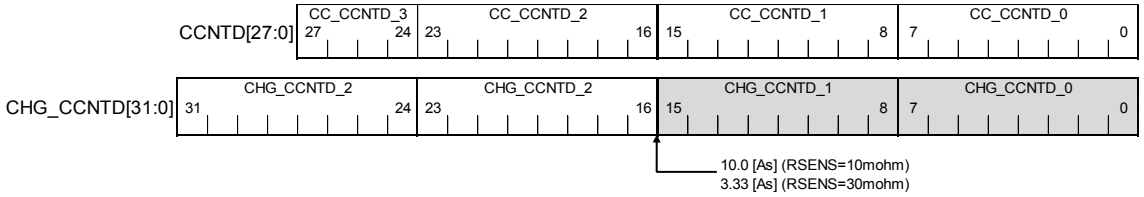
Address F1h: CCNTD_CHG_2 Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
F1h	CCNTD_CHG_2	R/W	CHG_CCNTD[23:16]							
	Initial Value	00h	0	0	0	0	0	0	0	0

CHG_CCNTD[31:16] Charging Coulomb Counter value .

When CCNTENB = "1", the Coulomb Counter accumulates the charge current value only.
In battery charging, the measured current value is added to the Coulomb Counter at every conversion period.
Before CHG_CCNTD reaches full, it regularly must be set with an caluculated charging cycle by software.

Internal register keeps CHG_CCNTD[15:0], it can clear by set CCNTRST to 1.



Series of CHG_CCNTD[31:16] (address from F0h to F1h) should be read in accordance with continuous manner,
so stop condition should not be inserted during reading these registers.

Address FEh: PROTECT Register (R/W)

Address (Index)	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FEh	PROTECT	R/W	PROTECT[7:0]							
	Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7-0 : PROTECT[7:0] This register is intend to access test area registers. Do NOT write any data to this register

Typical Performance Curves

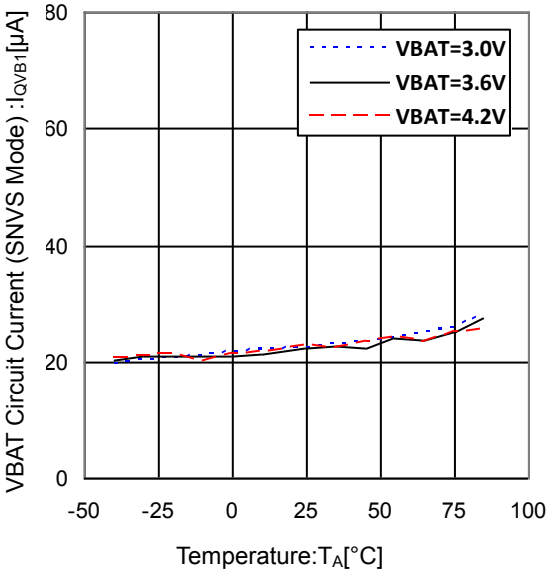


Figure 24. VBAT Circuit Current (SNVS Mode) vs Temperature

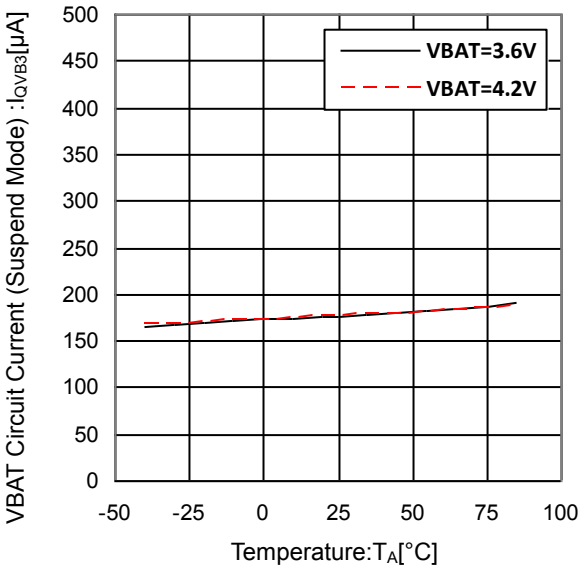


Figure 25. VBAT Circuit Current (Suspend Mode) vs Temperature

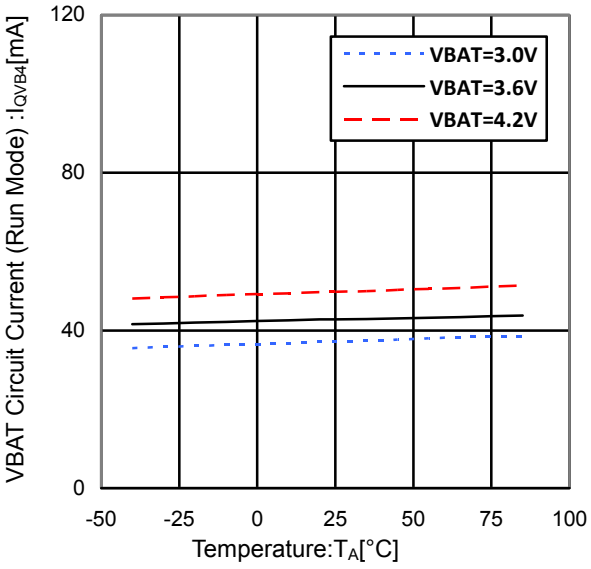


Figure 26. VBAT Circuit Current (Run Mode) vs Temperature

Typical Performance Curves - continued

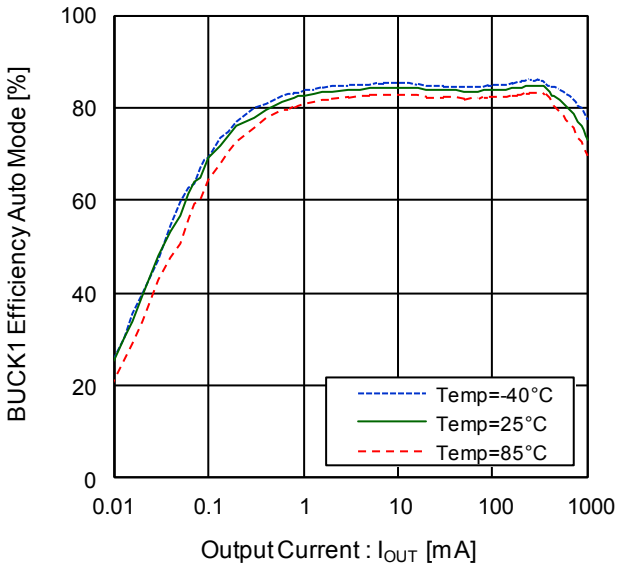


Figure 27. Efficiency vs Output Current
("BUCK1 Efficiency Auto Mode", V_{BAT}=3.6V, V_{OSW1}=1.3V)

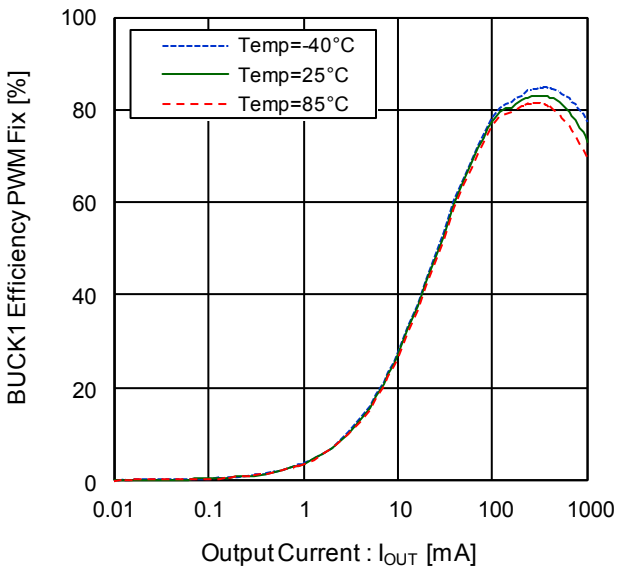


Figure 28. Efficiency vs Output Current
("BUCK1 Efficiency PWM Mode", V_{BAT}=3.6V, V_{OSW1}=1.3V)

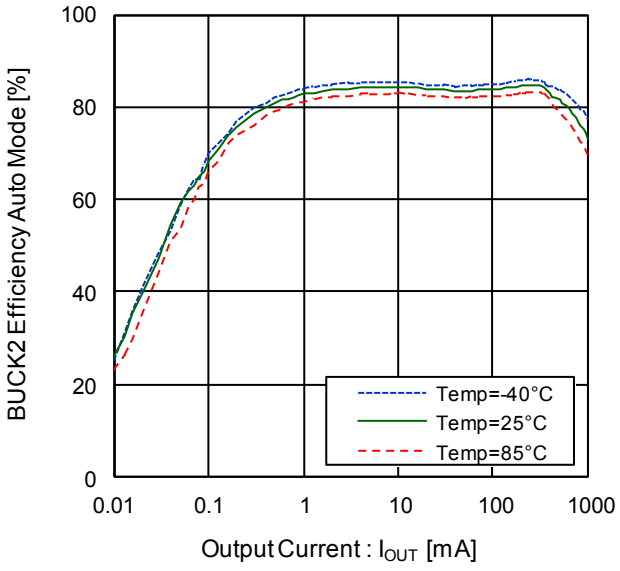


Figure 29. Efficiency vs Output Current
("BUCK2 Efficiency Auto Mode", V_{BAT}=3.6V, V_{OSW2}=1.3V)

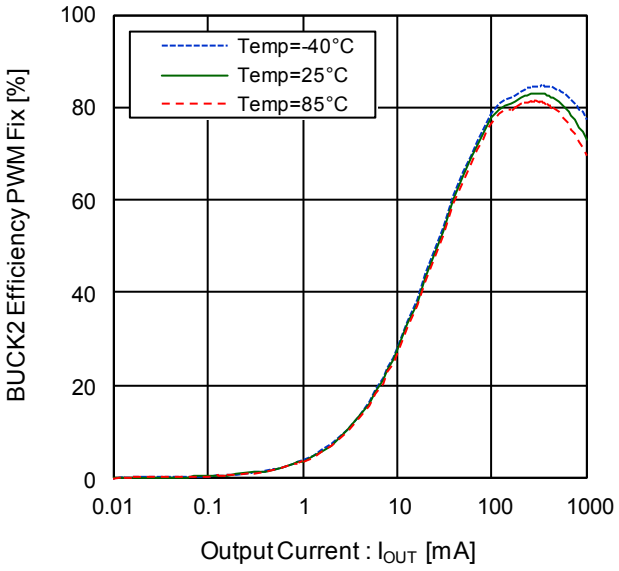


Figure 30. Efficiency vs Output Current
("BUCK2 Efficiency PWM Mode", V_{BAT}=3.6V, V_{OSW2}=1.3V)

Typical Performance Curves - continued

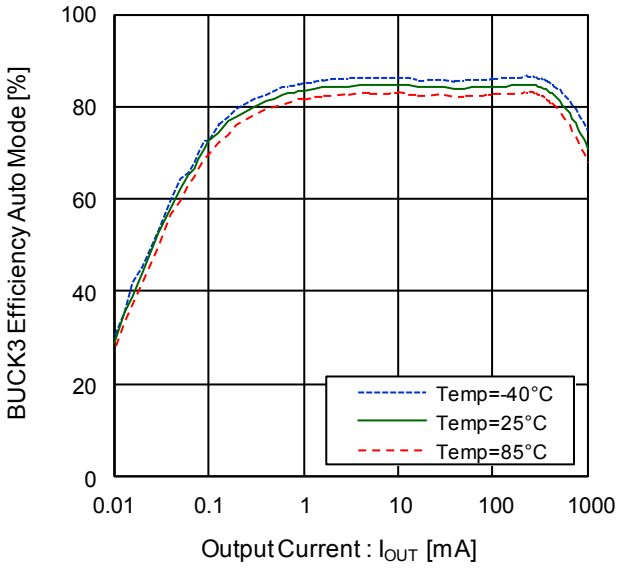


Figure 31. Efficiency vs Output Current
("BUCK3 Efficiency Auto Mode", V_{BAT}=3.6V, V_{OSW3}=1.8V)

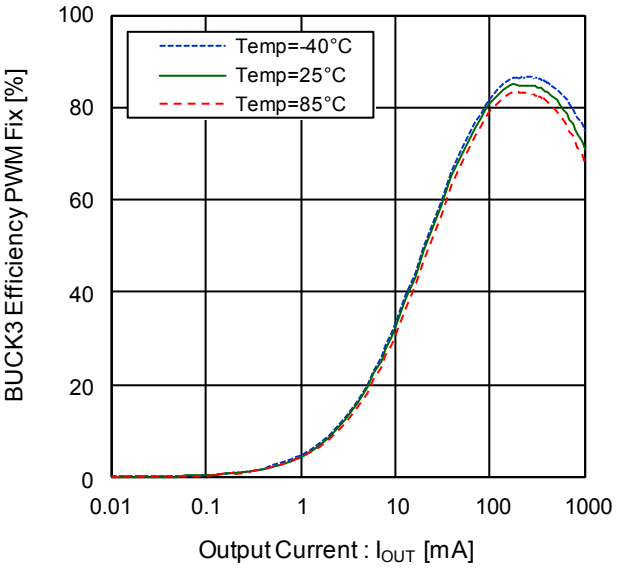


Figure 32. Efficiency vs Output Current
("BUCK3 Efficiency PWM Mode", V_{BAT}=3.6V, V_{OSW3}=1.8V)

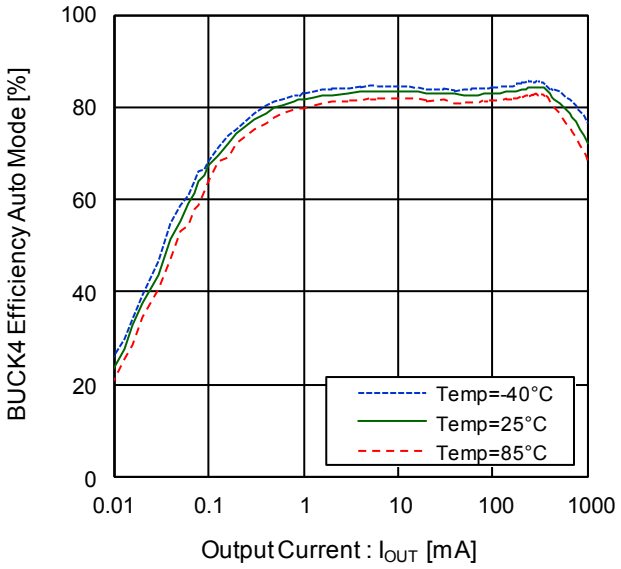


Figure 33. Efficiency vs Output Current
("BUCK4 Efficiency Auto Mode", V_{BAT}=3.6V, V_{OSW4}=1.2V)

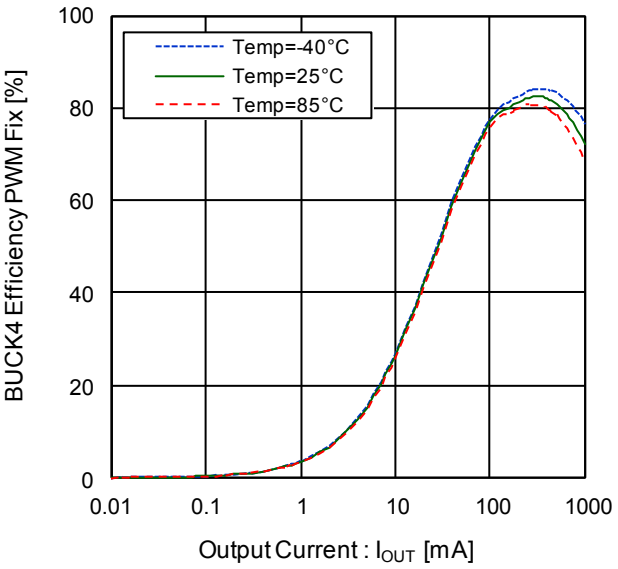


Figure 34. Efficiency vs Output Current
("BUCK4 Efficiency PWM Mode", V_{BAT}=3.6V, V_{OSW4}=1.2V)

Typical Performance Curves - continued

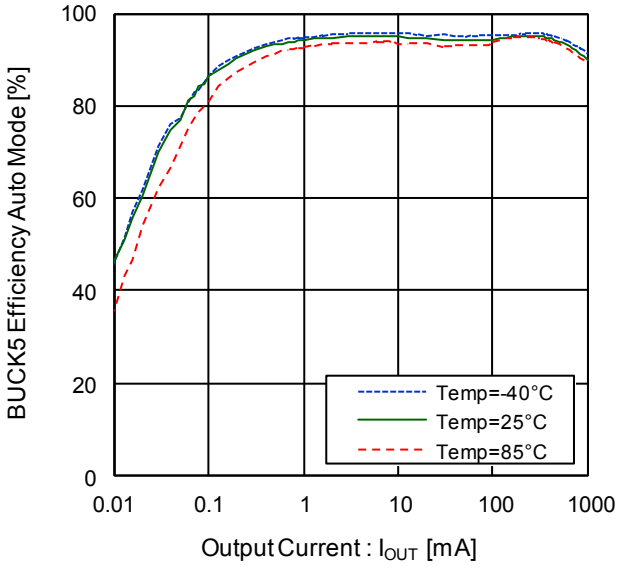


Figure 35. Efficiency vs Output Current
("BUCK5 Efficiency Auto Mode", V_{BAT}=3.6V, V_{OSW5}=3.2V)

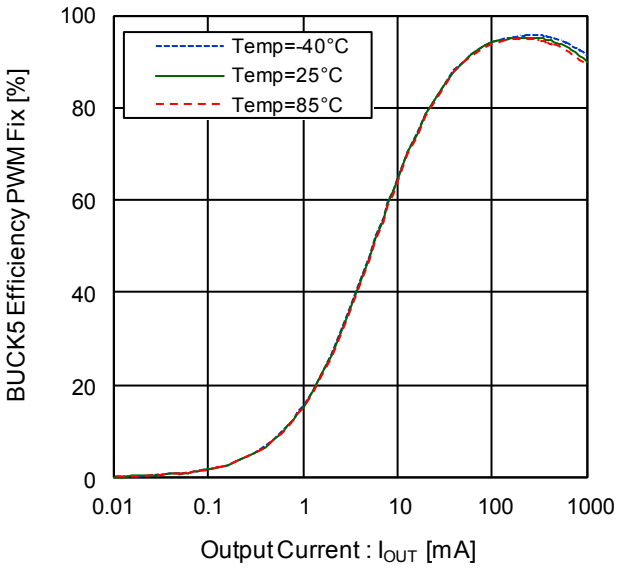


Figure 36. Efficiency vs Output Current
("BUCK5 Efficiency PWM Mode", V_{BAT}=3.6V, V_{OSW5}=3.2V)

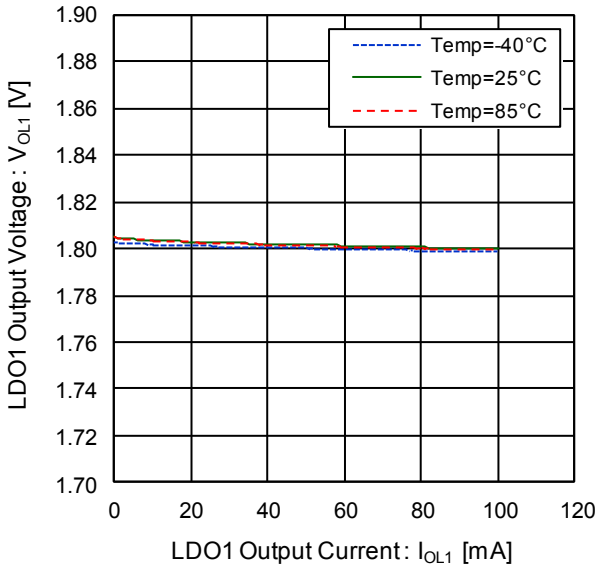


Figure 37. LDO1 Output Voltage vs
LDO1 Output Current
(V_{BAT}=3.6V, VSYS=VIN=VINL1,2)

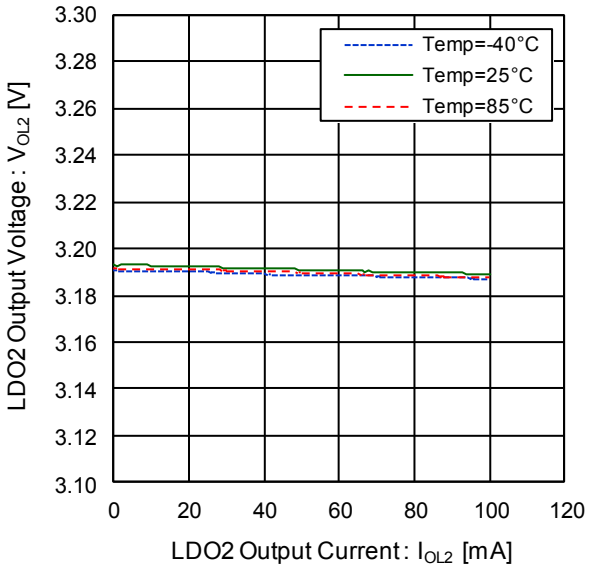


Figure 38. LDO2 Output Voltage vs
LDO2 Output Current
(VBAT=3.6V, VSYS=VIN=VINL1,2)

Typical Performance Curves - continued

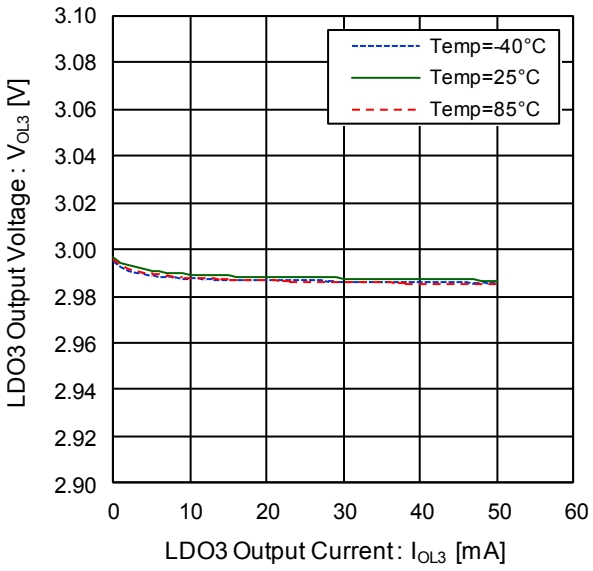


Figure 39. LDO3 Output Voltage vs LDO3 Output Current (VBAT=3.6V, VSYS=VIN=VINL1,2)

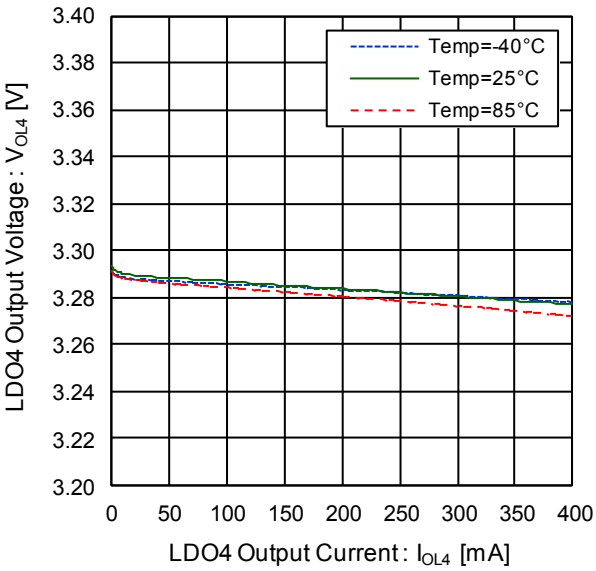


Figure 40. LDO4 Output Voltage vs LDO4 Output Current (VBAT=3.6V, VSYS=VIN=VINL1,2)

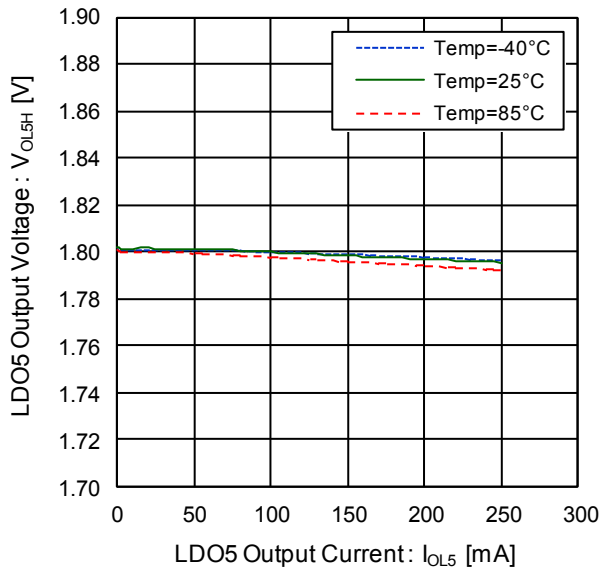


Figure 41. LDO5 Output Voltage vs LDO5 Output Current (V_{BAT}=3.6V, VSYS=VIN=VINL1,2, LDO5VSEL=H)

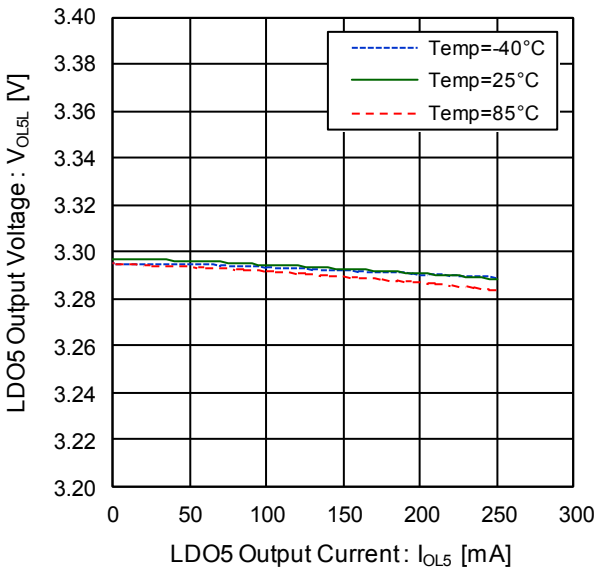


Figure 42. LDO5 Output Voltage vs LDO5 Output Current (V_{BAT}=3.6V, VSYS=VIN=VINL1,2, LDO5VSEL=L)

Typical Performance Curves - continued

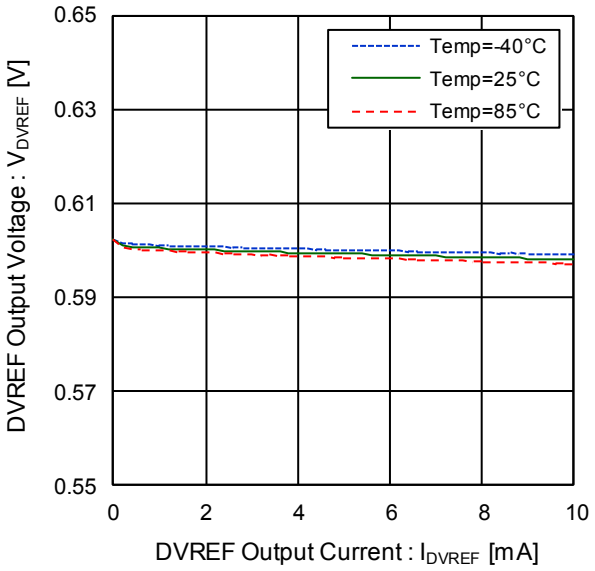


Figure 43. DVREF Output Voltage vs DVREF Output Current (V_{BAT}=3.6V, VSYS=VIN=VINL1,2)

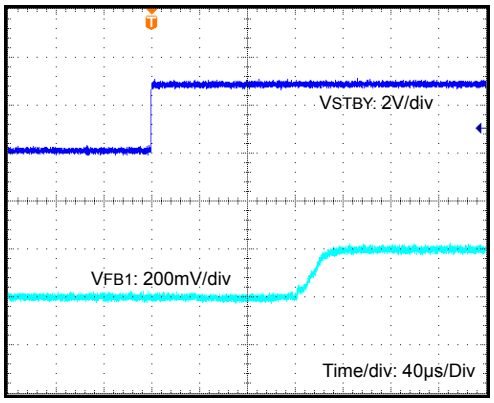


Figure 44. BUCK1 DVS Rise Time (V_{BAT}=3.6V C_L=10µF I_{OUT}=0A Ramp Rate=10mV/µs, BUCK1_MODE [02h:15h] PWM Mode)

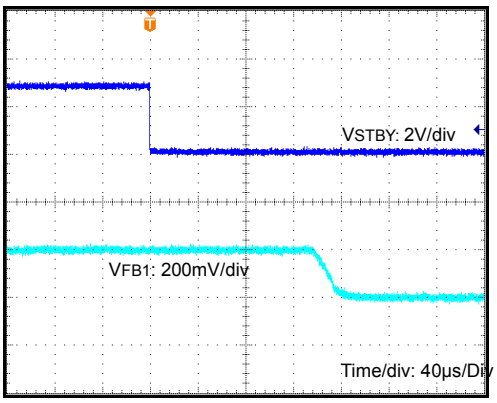


Figure 45. BUCK1 DVS Fall Time (V_{BAT}=3.6V C_L=10µF I_{OUT}=0A Ramp Rate=10mV/µs, BUCK1_MODE [02h:15h] PWM Mode)

Typical Performance Curves - continued

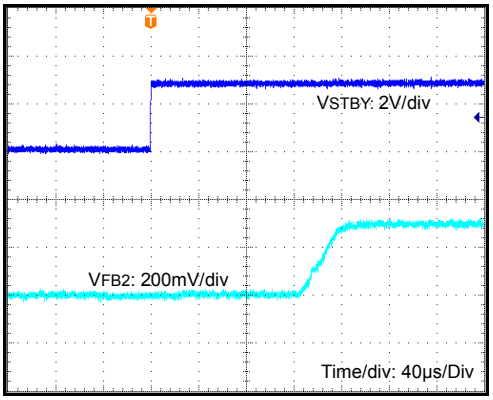


Figure 46. BUCK2 DVS Rise Time
(V_{BAT}=3.6V C_L=10µF I_{OUT}=0A
Ramp Rate=10mV/µs, BUCK2_MODE [03h:15h]
PWM Mode)

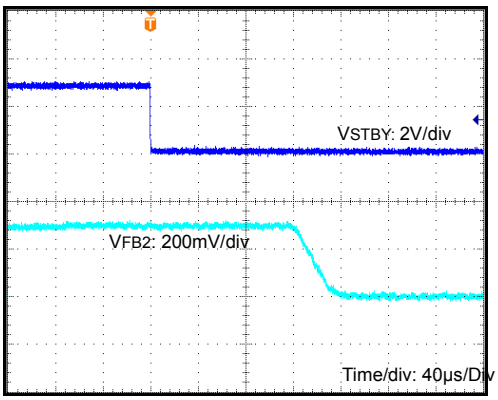


Figure 47. BUCK2 DVS Rise Time
(V_{BAT}=3.6V C_L=10µF I_{OUT}=0A
Ramp Rate=10mV/µs, BUCK2_MODE [03h:15h]
PWM Mode)

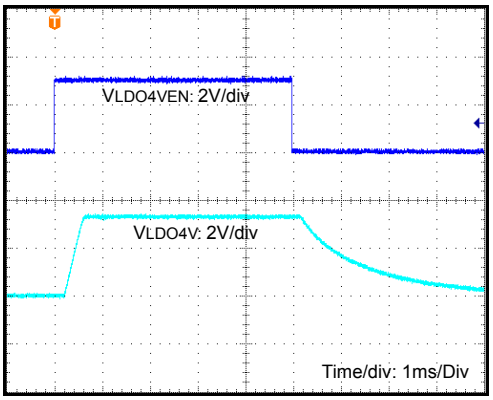


Figure 48. LDO4 Control Timing Diagram
(V_{BAT}=3.6V I_{OUT}=0A)

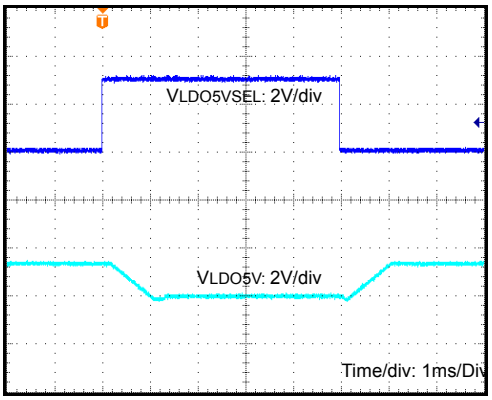


Figure 49. LDO5 Control Timing Diagram
(V_{BAT}=3.6V I_{OUT}=0A)

Typical Performance Curves - continued

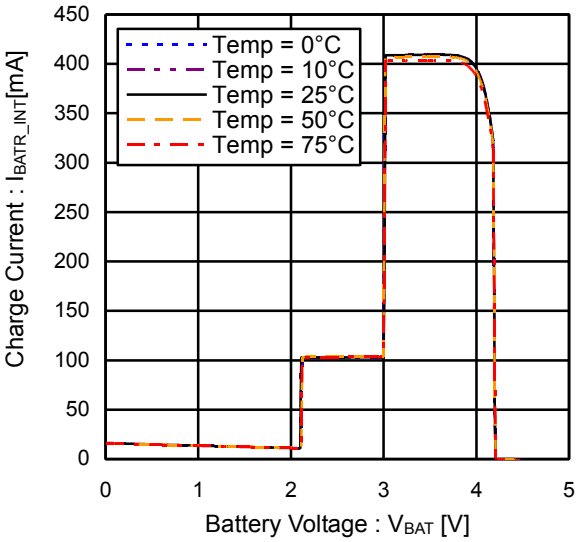


Figure 50. Charge Current (Internal MOS) vs Battery Voltage (DCIN=5V I_{FST}=400mA TS=GND)

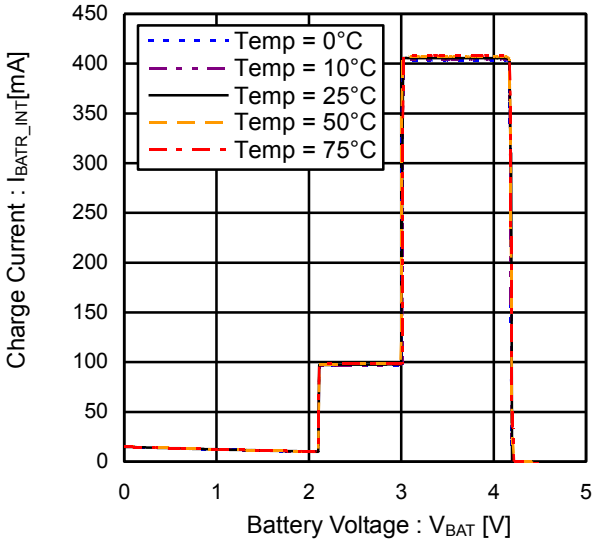


Figure 51. Charge Current (External MOS) vs Battery Voltage (DCIN=5V I_{FST}=400mA TS=GND)

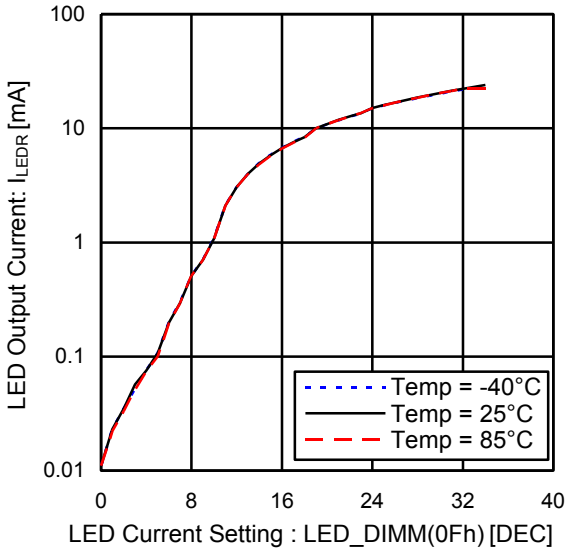
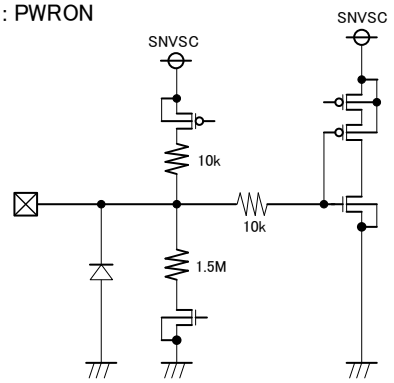


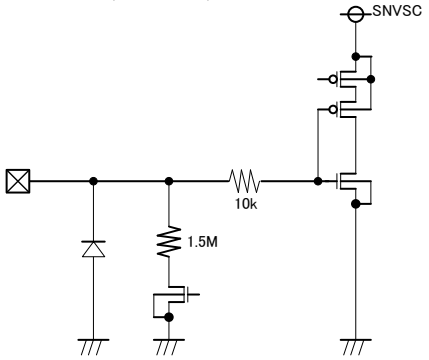
Figure 52. LED Output Current vs LED Current Setting (V_{BAT}=3.6V LEDs=6)

I/O Equivalent Circuits

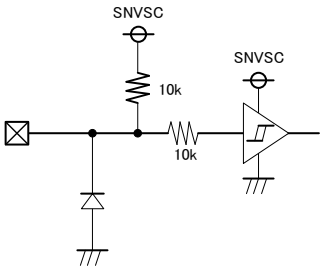
A : PWRON



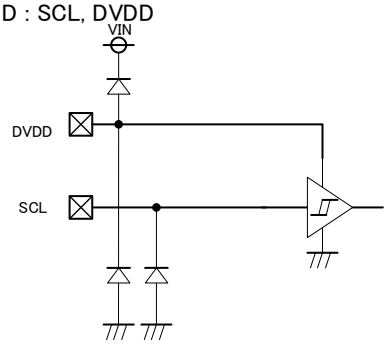
B : STANDBY, WDOGB, LDO4EN. LDO5VSEL



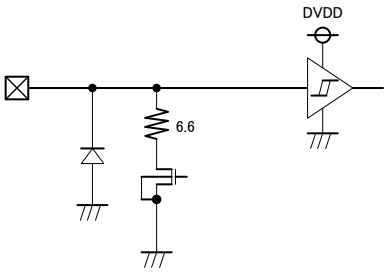
C : RESETINB



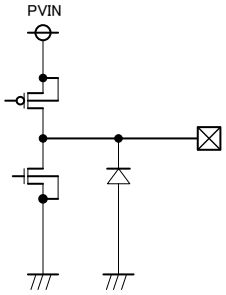
D : SCL, DVDD



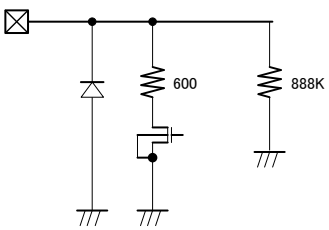
E : SDA



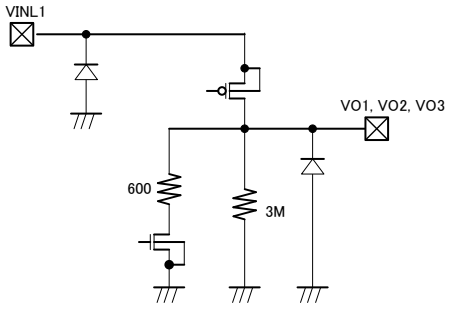
F : LX1, LX2, LX3, LX4



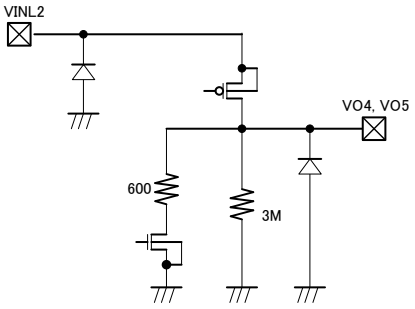
G : FB1, FB2, FB3, FB4



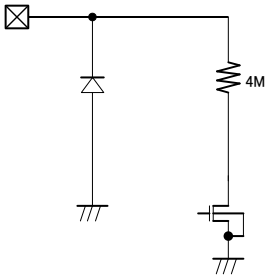
H : VINL1, VO1, VO2, VO3



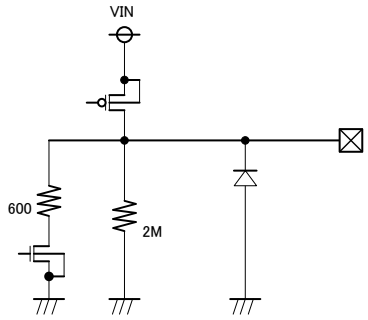
I : VINL2, VO4, VO5



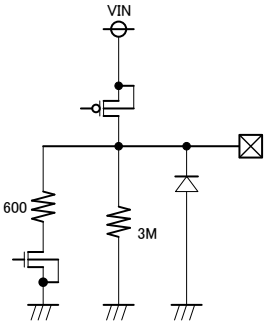
J : DVREFIN



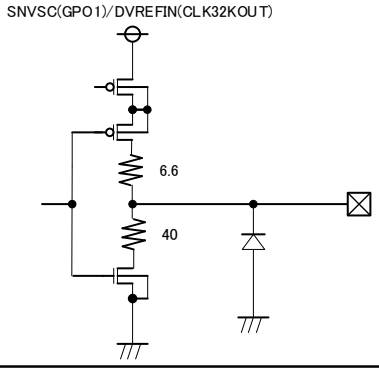
K : VODVREF



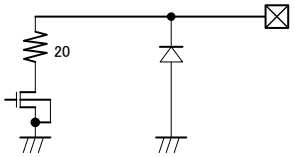
L : VOLPSR



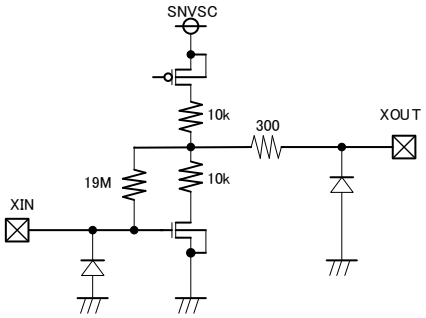
M : GPO1, CLK32KOUT



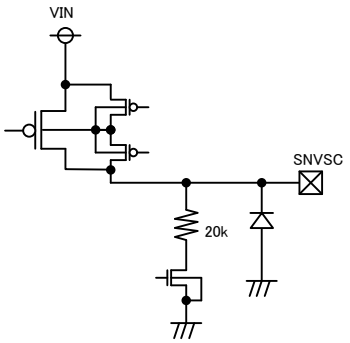
N : POR, INTB



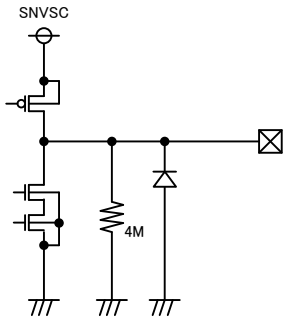
O : XIN, XOUT



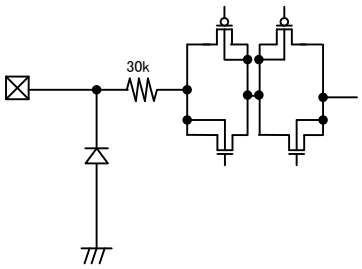
P : SNVSC



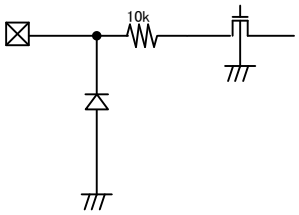
Q : CHGREF



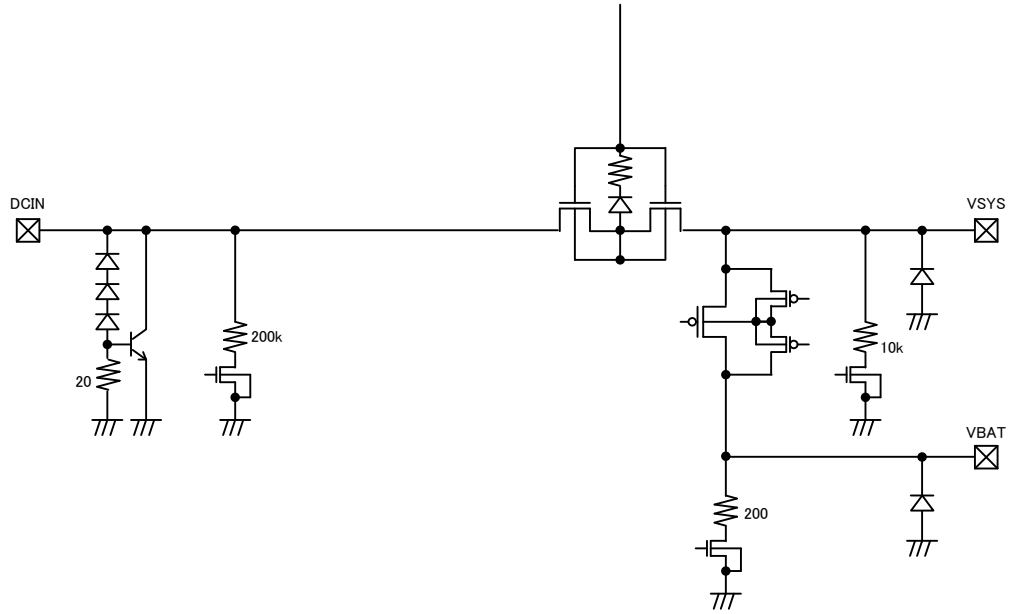
R : TS



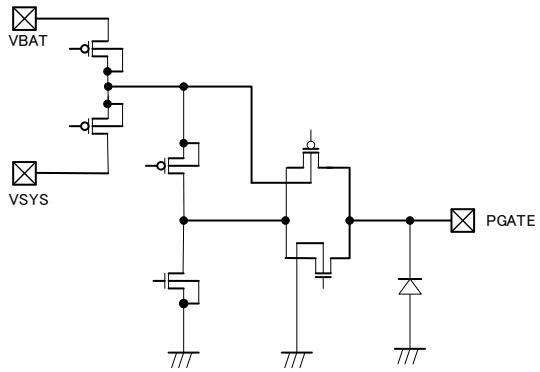
S : BATTP, BATTM



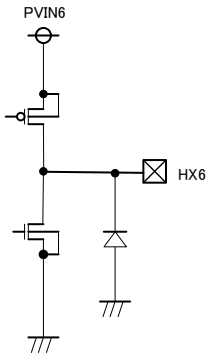
T : DCIN, VSYS, VBAT



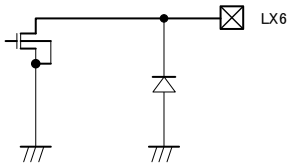
U: PGATE



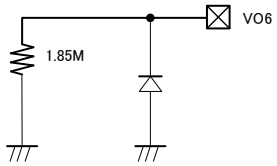
V: HX6



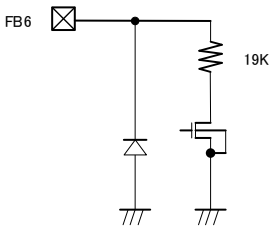
W: LX6



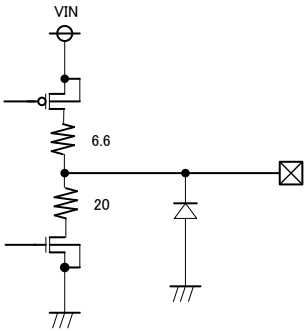
X: VO6



Y: FB6



Z: READY, CHGLED



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

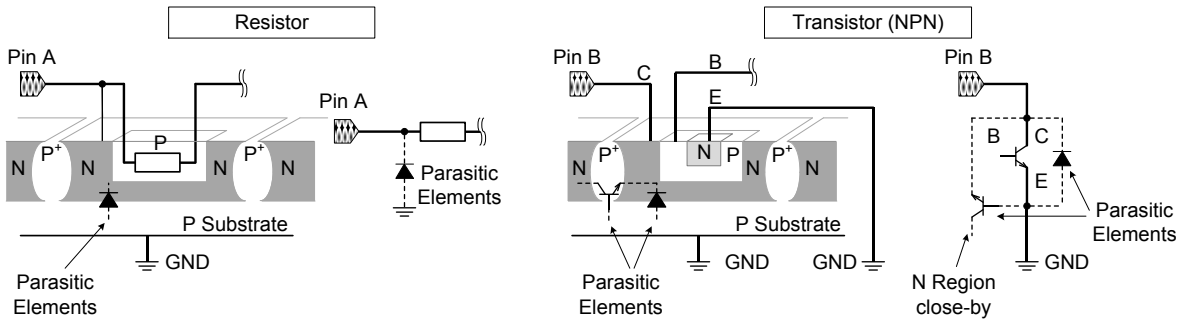


Figure 53. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

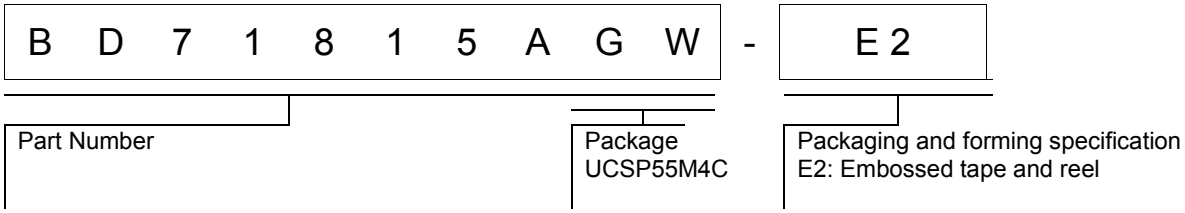
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

17. Disturbance light

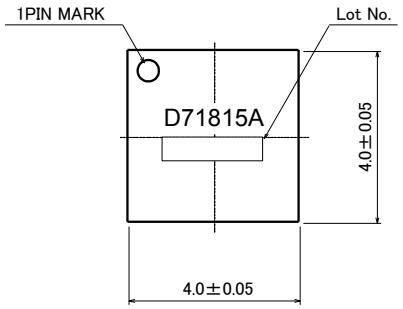
In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



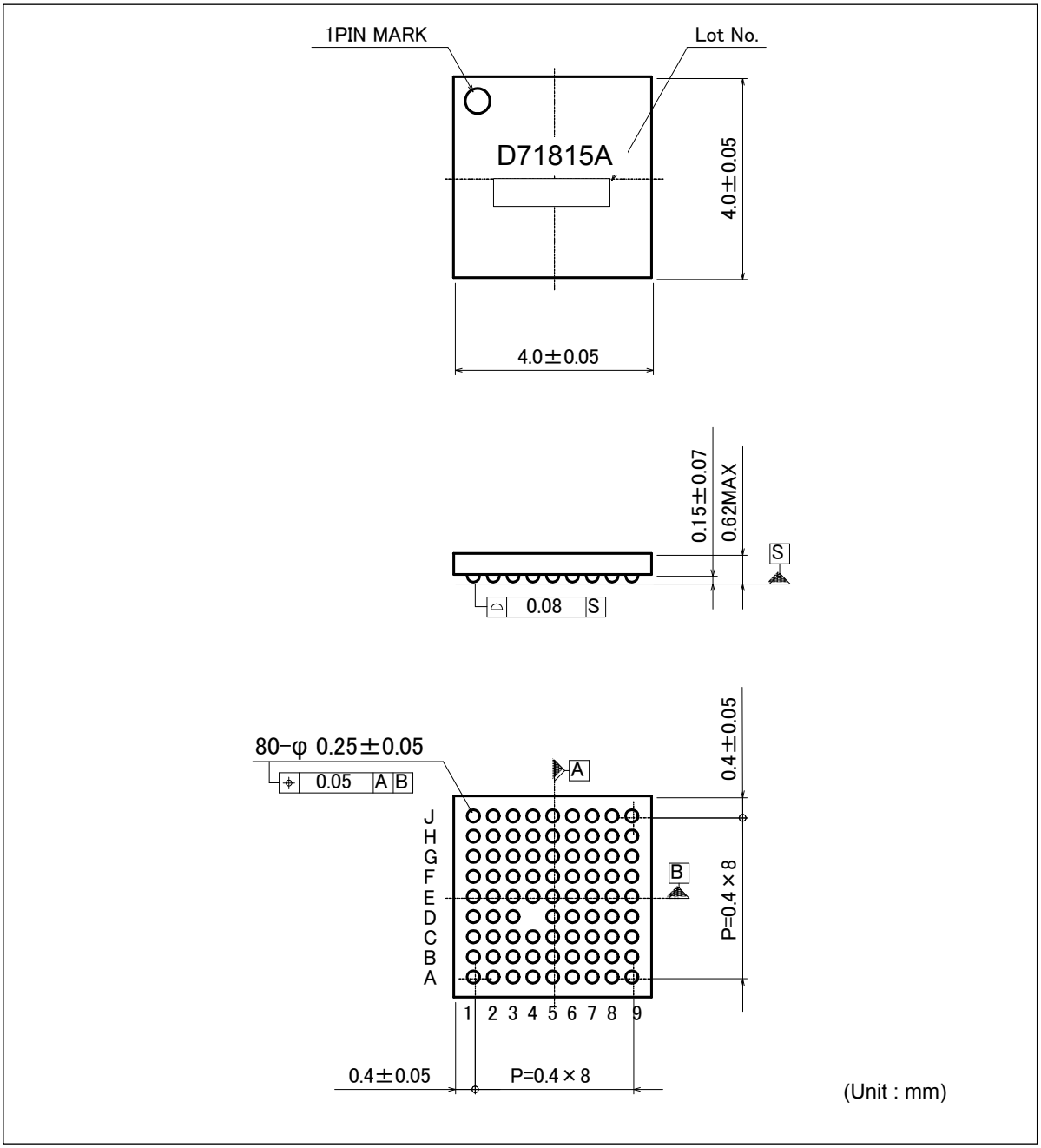
Marking Diagrams

UCSP55M4C(BD71815AGW) Top view



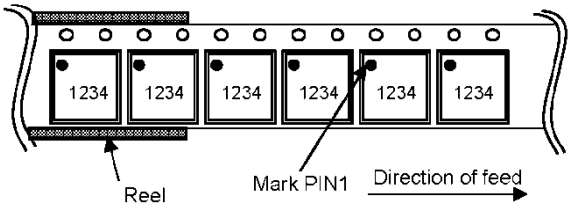
Physical Dimension Tape and Reel Information

Package Name	UCSP55M4C(BD71815AGW)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2,500 pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
5.Oct.2016	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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BD71815AGW - Web Page

Part Number	BD71815AGW
Package	UCSP55M4C
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes