Benefits of low side MOSFET drivers in SMPS

About this document

Scope and purpose

This application note provides key features and advantages of the EiceDRIVER™ family of low side MOSFET drivers from Infineon Technologies. The 1EDN/2EDN family of MOSFET drivers is intended to be used in Switch Mode Power Supplies (SMPS) where it is necessary to drive a power MOSFET into ON and OFF conditions. Different power conversion topologies used in SMPS require this driver / MOSFET combination to work effectively in order to achieve an efficient power conversion. Understanding MOSFET driver IC functions is critical to enhancing switching performance. In this application note we explain the benefits of using 1EDN/2EDN drivers to help the designer create a robust and efficient drive stage for switching the power MOSFET.

Intended audience

This document is intended for designers with entry level technical knowledge relating to SMPS, MOSFET drivers and super junction transistors.

Table of contents

1 MOSFET driver IC basic considerations

The key factor for an efficient power conversion lies in the switching that occurs within the power stage of a SMPS. Many of today's high frequency, high-performance PWM controllers, either analog or digital, do not have the capability to drive a power MOSFET directly. A MOSFET driver IC is the interface between the low-power switching signals of a PWM and the high-current demanded by the MOSFET. Once a converter topology, such as Power Factor Corrector (PFC), resonant stages like half-bridge LLC or full-bridge ZVS, or synchronous rectification is decided upon, selecting the best driver IC for the chosen topology requires an understanding of the MOSFET driver IC functions, that are most important to enhancing the switching performance.

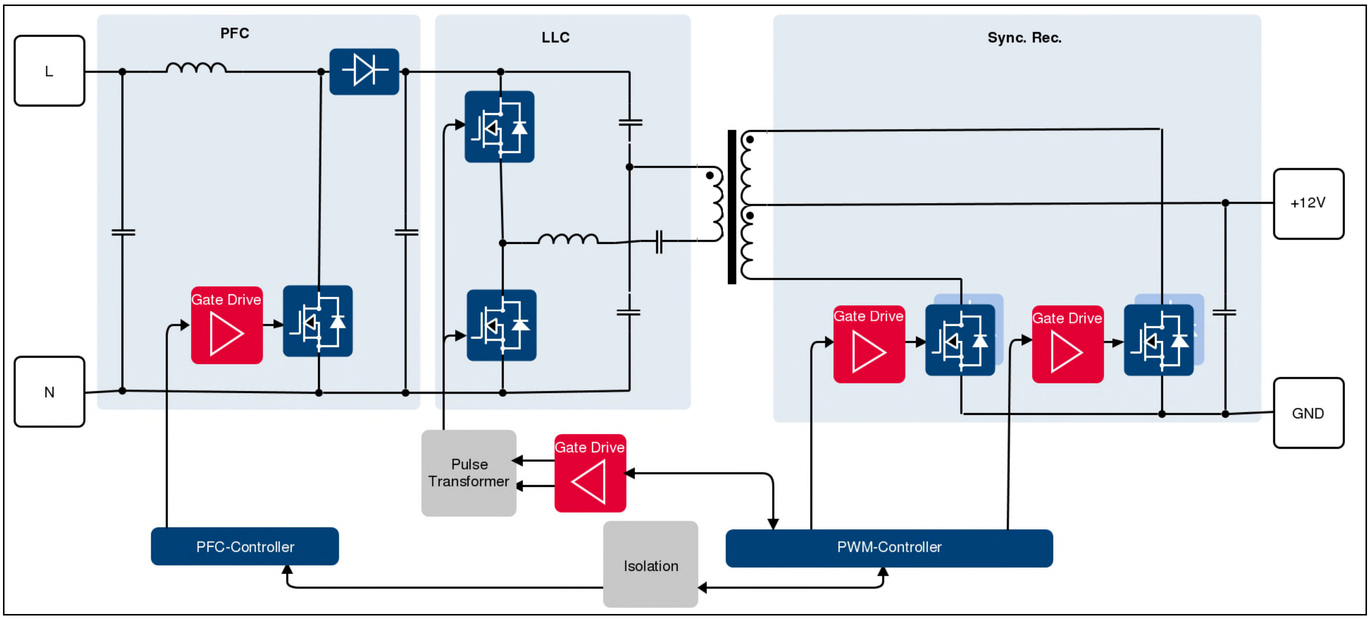


Figure 1 Typical server power supply with PFC, main and synchronous rectification stage

The various stages of a MOSFET driver IC are outlined below:

Typical application

As an example for the synchronous rectifier (SR) in Figure 1, the 2EDN driver is configured into two separate channels (see Figure 2). Each channel is connected to a PWM controller source on the input side. INA and INB carry the PWM signals. ENA and ENB are the gating signals that can be used for safety purposes. Each driver output (OUTA and OUTB) control a MOSFET M_1 and M_2 through a gate resistor R_{g1} and R_{g2}. The capacitor C_{VDD} supports the IC during the fast transitions and keeps the supporting power in the safe operation voltage levels.

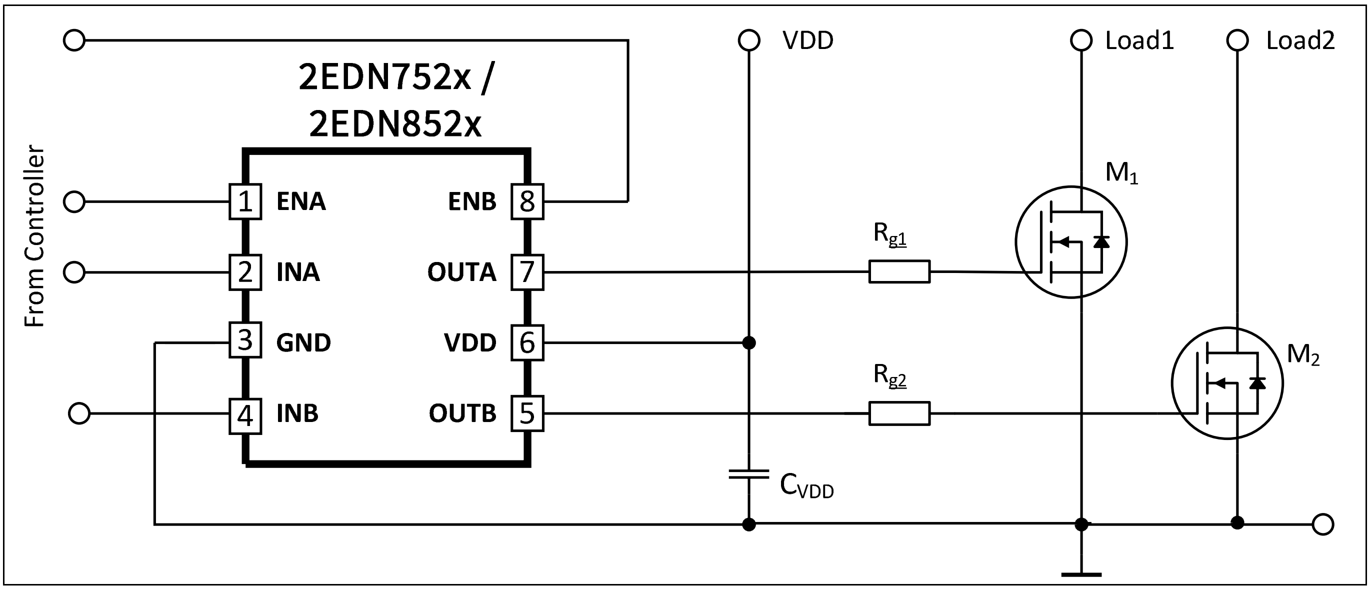


Figure 2 2EDN MOSFET drivers for high-speed switching with a robust and low $R_{DS(on)}$ MOS-only output stage

Another example of a low side PFC MOSFET driver circuit is shown in Figure 3. The 1EDN driver is configured into two separate gate driver resistor paths. The source path supports the turn-on event and limits the current via R_{g1}. The lower sink path is active during turn-off. The current is limited by R_{g2}.

This configuration enables a separate adjustment of turn-on and turn-off timing behaviors. This circuit uses less space and eliminates the diode that is needed to separate both paths in a conventional design.

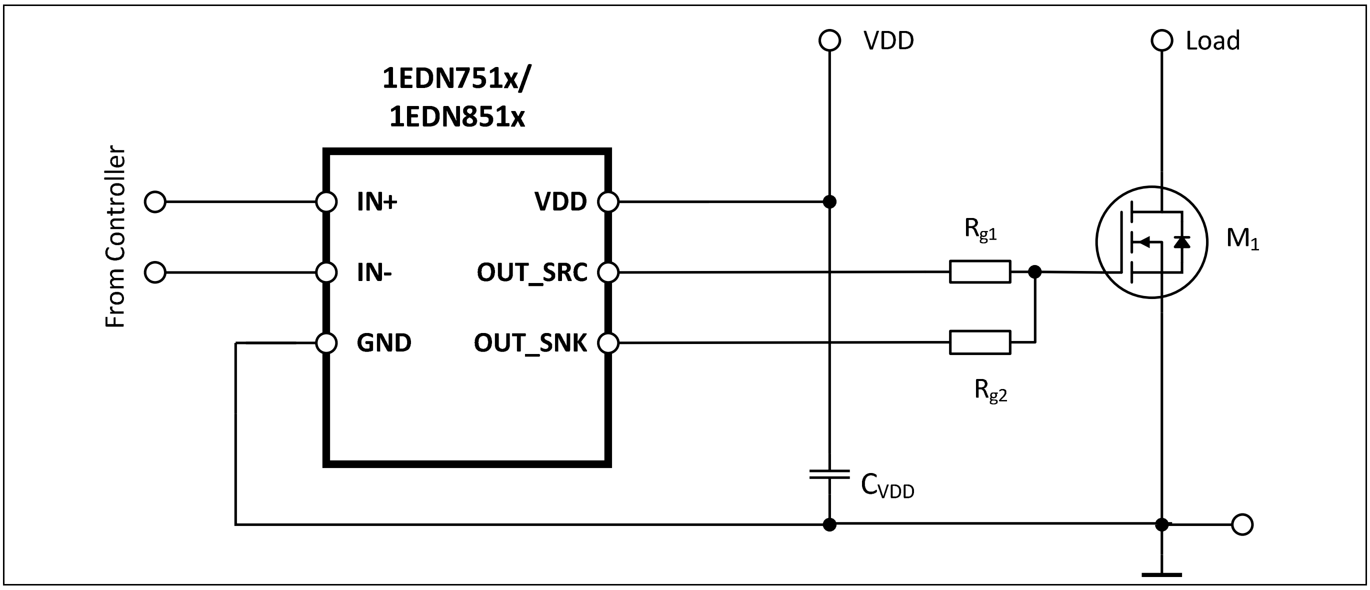


Figure 3 1EDN MOSFET drivers for high-speed switching with separate source/sink path MOS-only output stage

1.1 Driver input stage benefits

1.1.1 Negative voltage withstand ability – crucial safety margin when driven from pulse transformers or used in non-optimal PCB layouts

Voltage offset between controller GND pin and MOSFET driver GND

Typically MOSFET drivers are used between a PWM controller (such as a microcontroller) and a high voltage MOSFET. The driver's ground pin is connected close to the source pin of the MOSFET, as shown in Figure 4. Displaced from the driver and connected to the same ground network, the controller sends signals over IN and EN (1EDN: IN- / IN+ inputs). This is possible, due to a high current peak on the ground network. The ground network has a voltage drop between the driver and controller as shown with the arrow “A”. If the control IC drives to a low level (close to 0 V), the input side of the driver is driven to a voltage level below zero.

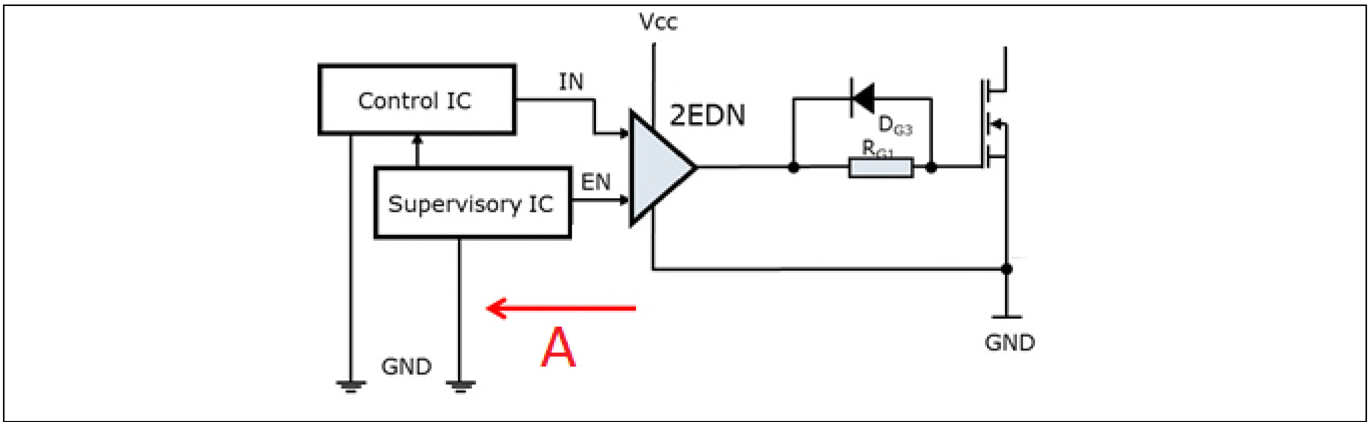


Figure 4 2EDN MOSFET drivers have ability to withstand negative voltage spikes

Dual and single channel low side MOSFET drivers (2END752x/2EDN842x, 1EDN751x/1EDN851x) can handle negative voltage spikes up to 10 V.

Standard MOSFET drivers only allow negative voltage levels down to -0.3 V. This limit is due to the ESD structure that protects the IC from electrostatic discharge during production handling. These low side MOSFET drivers have diodes that can protect against voltage spikes in the range of -10 V to 22 V, as shown in Figure 5.

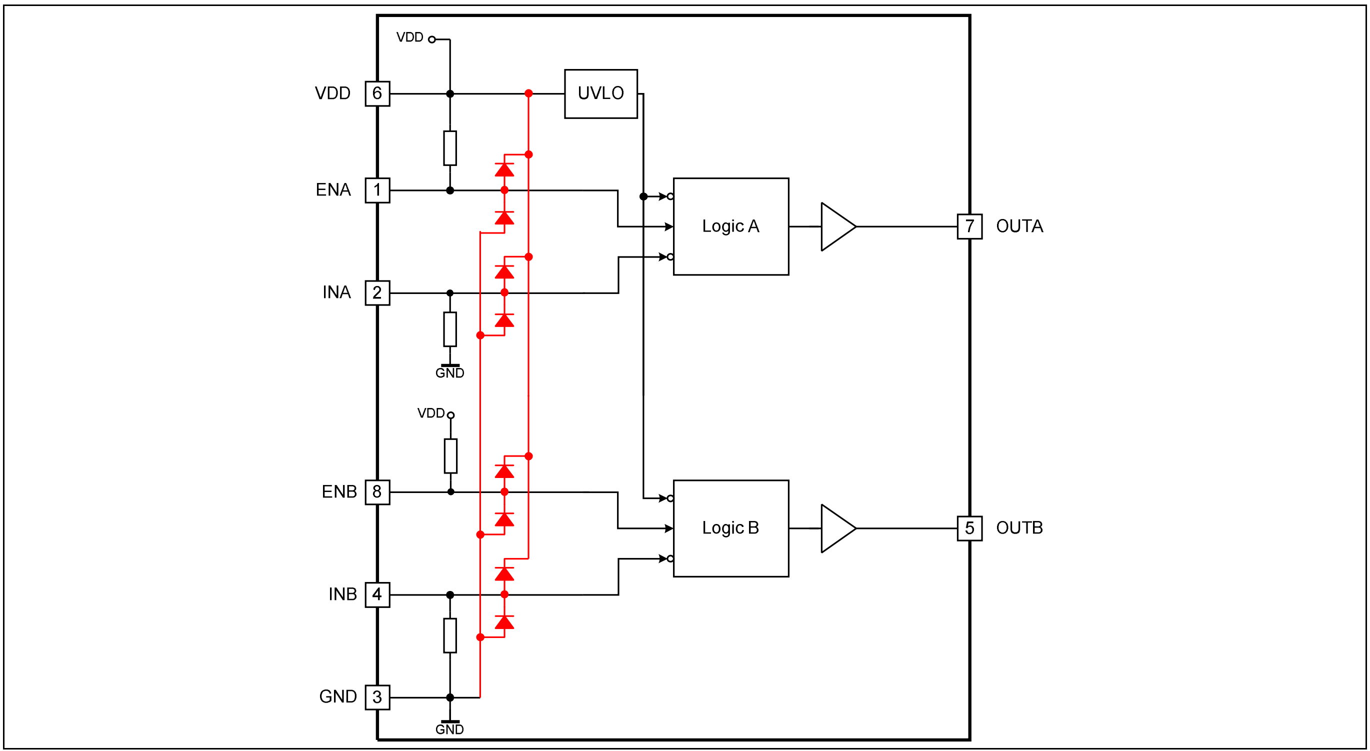


Figure 5 Standard MOSFET drivers ESD structure (red) have diodes which limit voltage range

The voltage range of the input pins is important for the connection to the PWM source. Many applications have separated power lines for controller and driver circuits. This means, that V_{cc} or GND can be displaced or, due to external influence, have voltage drops as explained in Figure 4.

The input pins of the 1EDN/2EDN family are able to cover voltage levels below zero or above V_{cc}. A driver V_{cc} voltage shutdown has no influence on the input pins. The zener diodes in Figure 6 (A, B, C and D) enable a neutral voltage zone with no interaction with V_{cc}. This is a clear benefit to other drivers, which would power the driver IC via the input pins ESD structure. This unwanted behavior can destroy the PWM controller or generate failures in the MOSFET driving circuit.

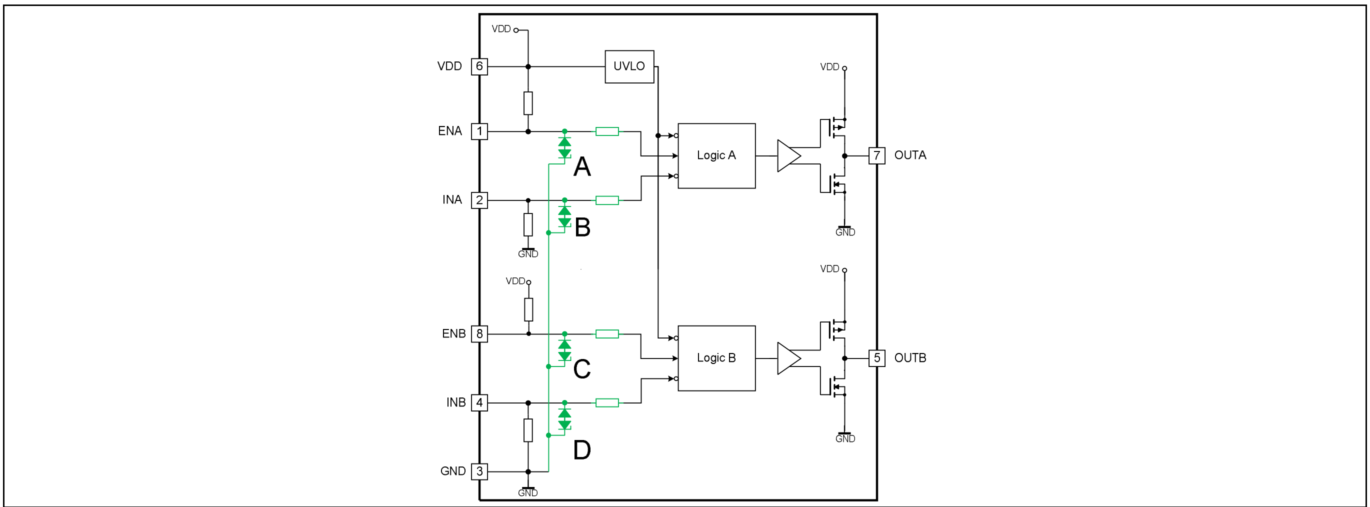


Figure 6 2EDN MOSFET drivers ESD structure (green) have ability to withstand negative voltage spikes down to -10 V

1.1.2 Sharp voltage thresholds, low tolerances and pull ups/down resistors ensure robust functionality

The input stage of a MOSFET driver should be compatible with both CMOS and TTL input signals.

CMOS input stage thresholds vary and are equal to two-thirds of V_{cc} and one-third of V_{cc}. They offer excellent noise immunity, especially for higher V_{cc} values. Accuracy of the PWM switching behavior is directly related to the precision of the supply voltage. A noisy or fluctuating Vcc generates PWM instability, thereby influencing the power supply regulation.

As a TTL input stage does not rely on the driver's V_{cc}, the designer has more flexibility in choosing a PWM controller since Undervoltage Lockout (UVLO) is not a consideration for input-switching thresholds. Exact thresholds are a guarantee for a stable and precise PWM timing. The 1EDN/2EDN family is equipped with thresholds that are stabilized for both temperature and supply voltage. This is a huge benefit for a fast and precise regulation of power supplies.

How to connect the input pins:

2END752x/2EDN842x:
If the Enable pin is not used, this pin should remain unconnected or connected to V_{DD}.

1EDN751x/1EDN851x:
IN- and IN+ have pull-up / pull-down resistors to disable the output. You have to set both inputs to enable the output.

1.2 Output stage benefits

The output current rating of the driver and the power MOSFET gate charge predominately determine how quickly the MOSFET can switch on and off. Since these switching transitions determine the switching losses within the power MOSFET, choosing a driver with a current rating correctly matched to the power MOSFET can play an essential role in improving efficiency.

All drivers use a MOS-only output stage to deliver the high current required by the power MOSFET of the power converter. ICs using MOS-only drive stages overcome the drawbacks of bipolar MOSFET drivers by fully switching the power MOSFET between the two power rails, V_{cc} and GND. The 1EDN/2EDN family uses a strong MOS-only driver stage to enable low power dissipation and fast switching. A detailed comparison is made in chapter 3.1.

1.2.1 1EDN7511B/1EDN8511B separated outputs for source and sink

“Break before Make” is a common timing recommendation in many SMPS applications. The turn-off time should be faster than the turn-on time. This prevents shoot-through current if two MOSFETs are working against each other, as in a half-bridge or push-pull configuration.

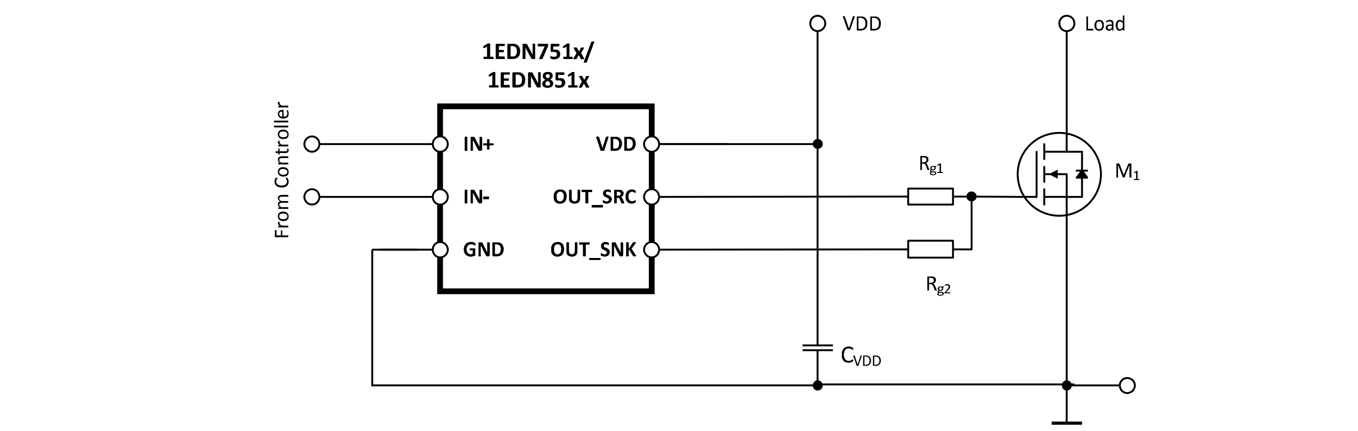


Figure 7 1EDN7511B/1EDN8511B with two output paths enables different times for on/off

Figure 7 & Figure 8 show R_{g1}, which limits the turn-on current for MOSFET M_1. For turn-off, the resistor R_{g2} is active. This is possible due to the separate power paths in the MOSFET driver IC (Figure 8).

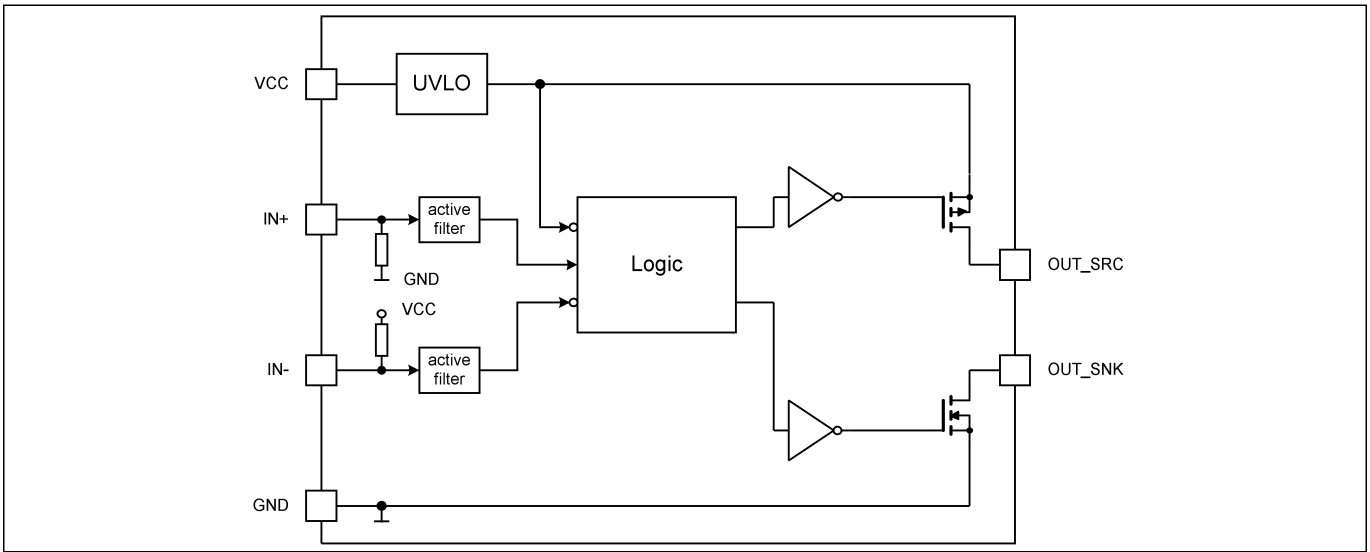


Figure 8 1EDN7511B/1EDN8511B internal circuit shows two separated output paths

1.2.2 Reverse current capability – built-in diodes in the output stage avoid using external diodes

Apart from having low $R_{DS(on)}$, the MOSFETs integrated into the internal driver stages of the 2END752x/2EDN842x and 1EDN751x/1EDN851x series also have built-in diodes for robust reverse current protection. As shown in Figure 9 below, reverse currents are generated due to parasitic inductance.

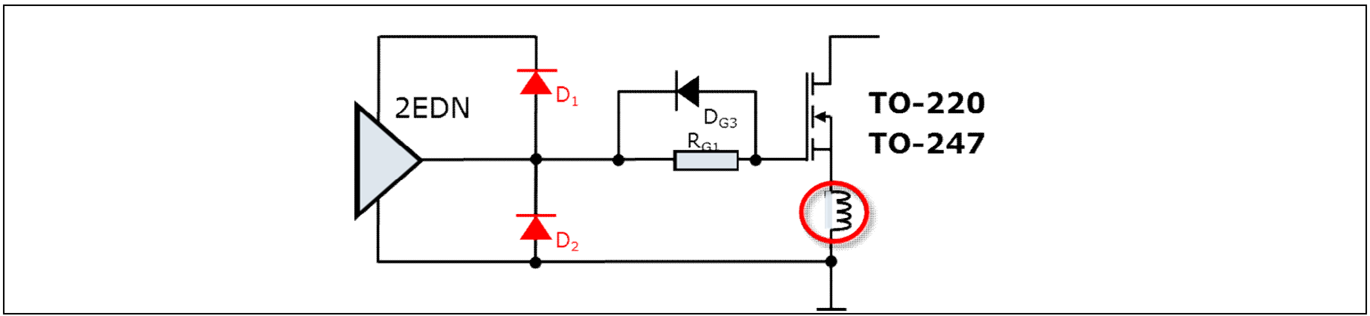


Figure 9 1EDN/2EDN MOSFET drivers have built in diodes at the output stage to withstand high reverse currents increasing the robustness

Most drivers require external diodes D_1/D_2 to protect the driver output stage from such an event. The parasitic source inductance of a TO-220/TO-247 package can be greater than 10 nH (including PCB effects). A switching current ramp (di/dt) of around 5 A/ns leads to a switching spike of +/-50 V source potential shift leading to a delta of +/-30 V on V_{gs}, causing reverse currents.

1.2.3 Power dissipation in the driver

A MOSFET driver's power dissipation is due to charging and discharging the MOSFET's gate capacitance, the driver's quiescent current and cross-conduction or shoot-through current in the MOSFET driver. Of these three factors, power dissipation due to the charging and discharging of the MOSFET's gate capacitance is the most important, especially at lower switching frequencies.

$P_{max} = C_{gs} \times V_{dd}^2 \times f_{sw}$

Where

C_g = MOSFET gate capacitance

V_{dd} = Supply voltage of MOSFET driver

f_{sw} = Switching frequency

The energy dissipated by the gate resistance and driver circuit is exactly equal to the energy stored in the MOSFET gate capacitance. The total power dissipated by the driver due to the MOSFET charging and discharging was shown above and included the power dissipated in the gate resistor.

The key point to note is that the MOSFET driver and the gate resistance will share the power dissipation linearly. Thus the power dissipation can be split between the driver and gate resistor.

Due to the low $R_{DS(on)}$ PMOS used in the driver output stage, when using the 2END752x/2EDN842x and 1EDN751x/1EDN851x series, the power dissipation in the driver and the resulting temperature rise is much smaller when compared to competitive drivers. This is shown in Figure 10 for the 2EDN7524.

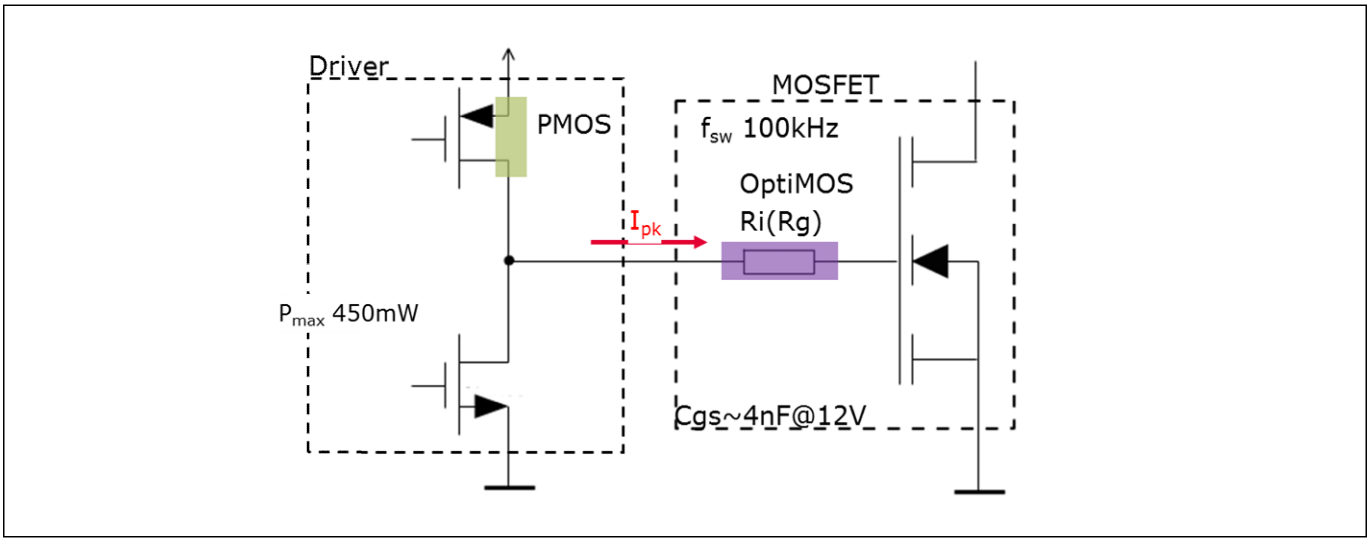


Figure 10 Thermal dissipation in a driver

Impact of a strong driver output $R_{DS(on)}$

The test set-up for measuring the thermal dissipation in the driver is shown below (Figure 11). A PWM pulse of 250 kHz is provided at the input. The load on the output is 1 Ω and 15 nF. The test was performed at an ambient temperature of 23°C.

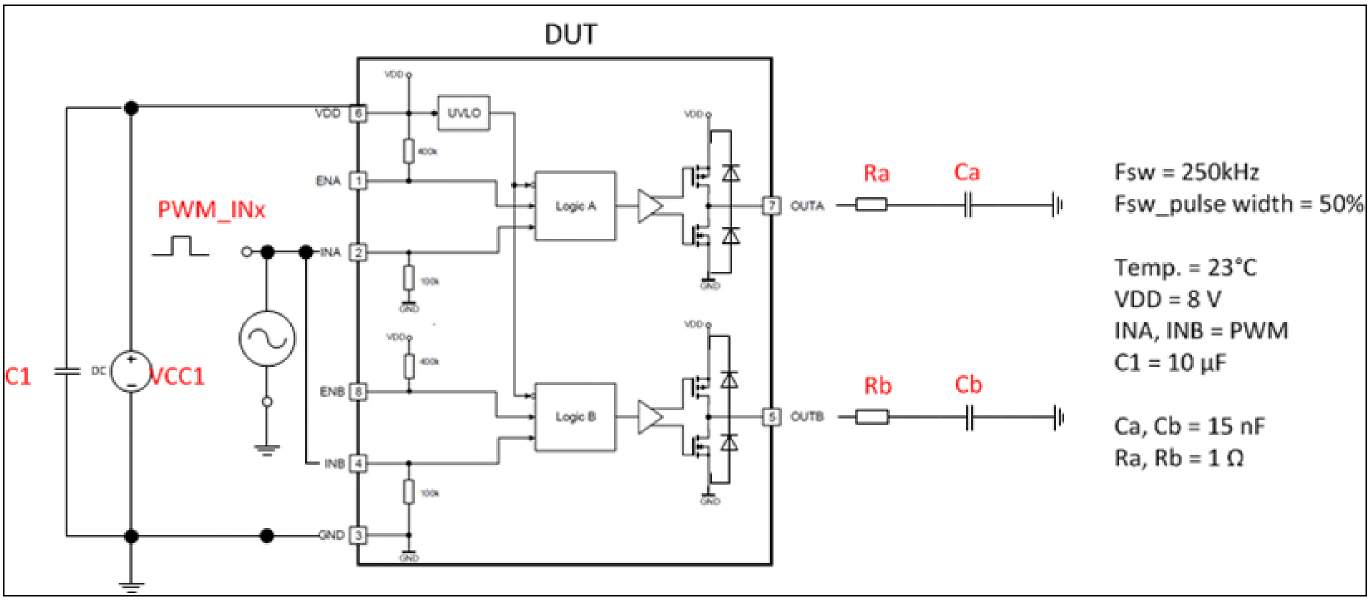


Figure 11 Test setup for thermal dissipation

The test results show that the dissipation in the competitive devices show almost 50% higher power dissipation than the 2EDN7524. As discussed earlier, the total power dissipation includes driver dissipation and gate resistor dissipation. As the 2EDN is showing lower dissipation, the gate resistor used along with the 2EDN will see higher power dissipation. A higher value of R_g will reduce its power dissipation.

Figure 12 shows the temperature hot spots at the driver IC and R_a/R_b

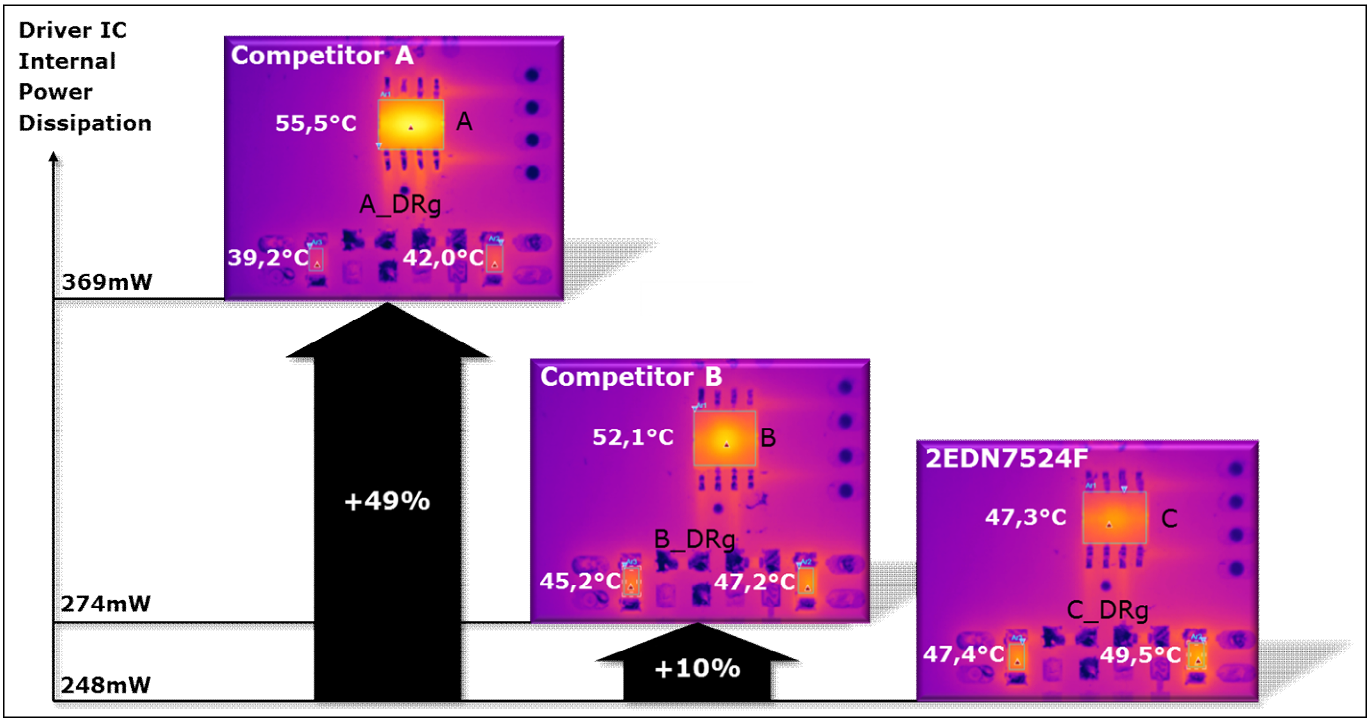


Figure 12 Test results for thermal dissipation

This clearly shows that the 2EDN7524 helps to drive a bigger transistor at an increased switching frequency and gate voltage by means of optimized power distribution. Lower IC temperature means less risk of failure and longer life. The 1EDN series has same output stage structure and the behavior is similar.

1.2.4 MOSFET drive current capability

In addition to the power dissipation, designers must understand the peak drive current. In the first moment of a switching event, the complete voltage V_{dd} is available. In the following sequence, the MOSFET capacitor C_{gs} is charged and discharged, generating a voltage drop. Less voltage is available for driving the MOSFET gate.

For a fast switching, a fast charge / discharge of the MOSFET capacitor C_{gs} is necessary, meaning there must be low resistance in the driver, external resistor R_g and MOSFET internal gate restistance R_g. This leads to a huge current peak at the first moment of a switching event, which can cause damage. Drivers have to limit this peak by an internal circuit.

The 2EDN limits this peak current in the output stage by a saturated power MOSFET. These agile output MOSFETs need no additional snubbing circuits meaning that it is very robust design.

Figure 13 shows a driver output stage with a huge load (100 nF, 0.25 Ω). V_{dd} (12 V, yellow line) is blocked by a 1 uF capacitor, which serves the circuit during the pulse. The red line is the input signal. The blue line indicates the output current.

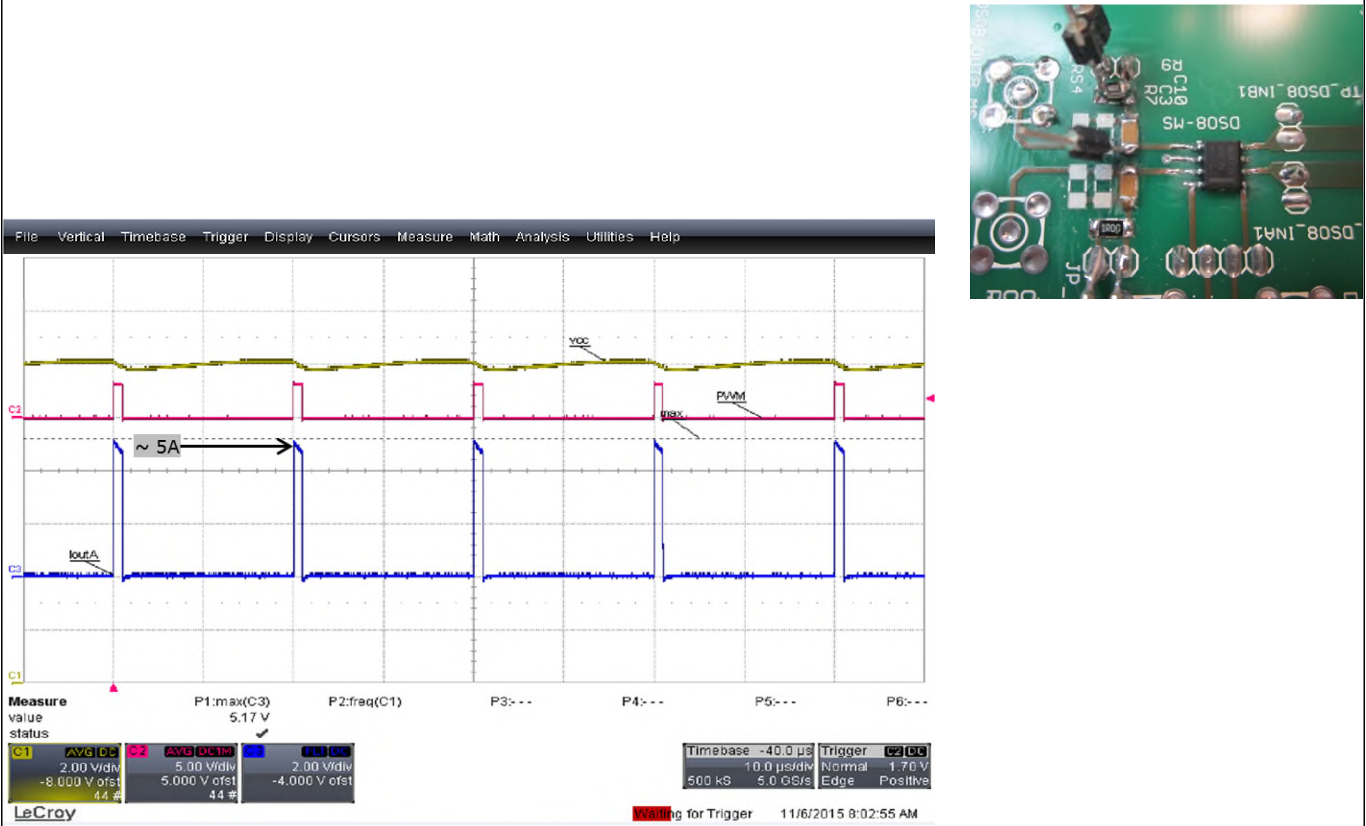


Figure 13 2EDN drive current measurement board and results

At the first moment of this switching event (on or off), the current limiter increases the limiting level by 20% and holds the max. current at 5 A. The duty cycle is limited to the maximum power dissipation to hold the junction temperature at 150°C. Each pulse is limited and there is no thermal runaway.

This benefit, related to other MOSFET drivers, is integrated by default in the strong driver output stage and reacts within nanoseconds. No additional protection circuit or limiting resistor is necessary. This enables a robust device even in critical external conditions.

1.2.5 Under voltage capability – reliable MOSFET protection

UVLO is a safety feature to protect the switching MOSFET during saturation, which means losses, high power dissipation and in some cases a thermal breakdown.

8 V UVLO for standard and super junction MOSFET like CoolMOS™ or OptiMOS™

The 2END752x/2EDN842x and 1EDN751x/1EDN851x series offers an 8 V UVLO version. This is particularly useful when used to drive super junction MOSFETs such as CoolMOS™.

Regular drivers have an under voltage lockout of 4.5 V to 5 V. Thus, under fault conditions such as a short circuit condition, they try to keep the MOSFET ON until the lockout voltage of 5 V is reached on V_{cc} or keep the MOSFET in linear mode with high I_d and low V_{gs}. The MOSFET will be stressed under this condition and its thermal dissipation will increase due to the unnecessary losses.

With 8 V UVLO, the MOSFET gate voltage is cutoff below 8 V and hence the MOSFET power dissipation is well controlled under fault conditions. Figure 14 shows two sample graphs of the MOSFET output characteristics.

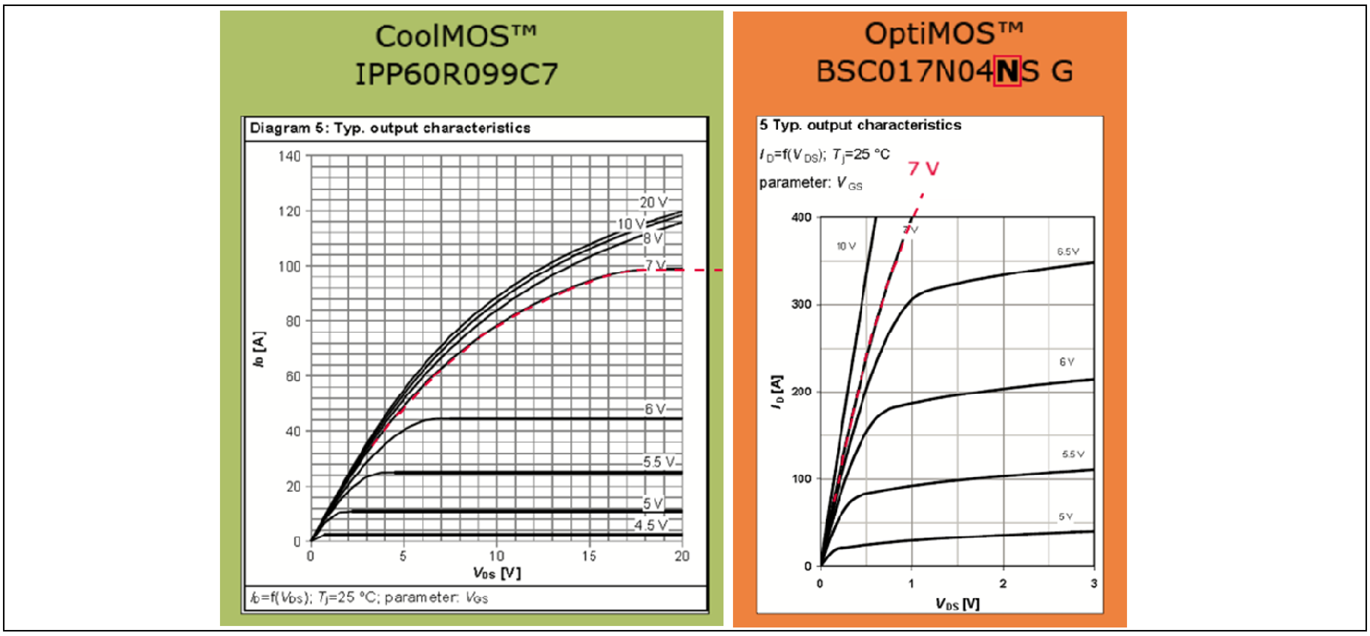


Figure 14 CoolMOS™ and OptiMOS™ output characteristics versus 8 V UVLO / gate voltage

4.2 V UVLO for MOSFETs with TTL compatible gate thresholds like OptiMOS™ L series

For MOSFETs with TTL gate thresholds, the driver offers a 4.2 V UVLO version. Figure 15 shows the typical output characteristic of the OptiMOS™ LS series.

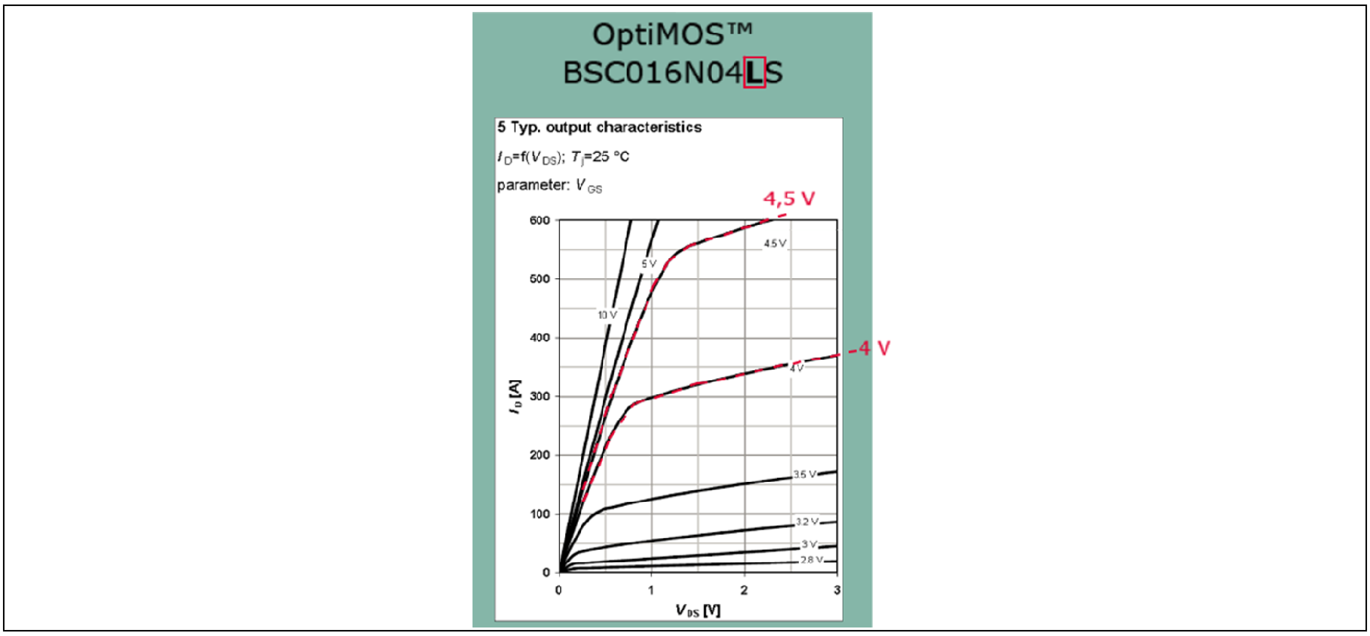


Figure 15 OptiMOS™ “LS” output characteristics versus 4.2 V UVLO / gate voltage

1.3 Propagation delay

Figure 16 shows a static enable input ENx. Propagation delay is the time it takes to pass a signal from the driver's input INx to output OUT.

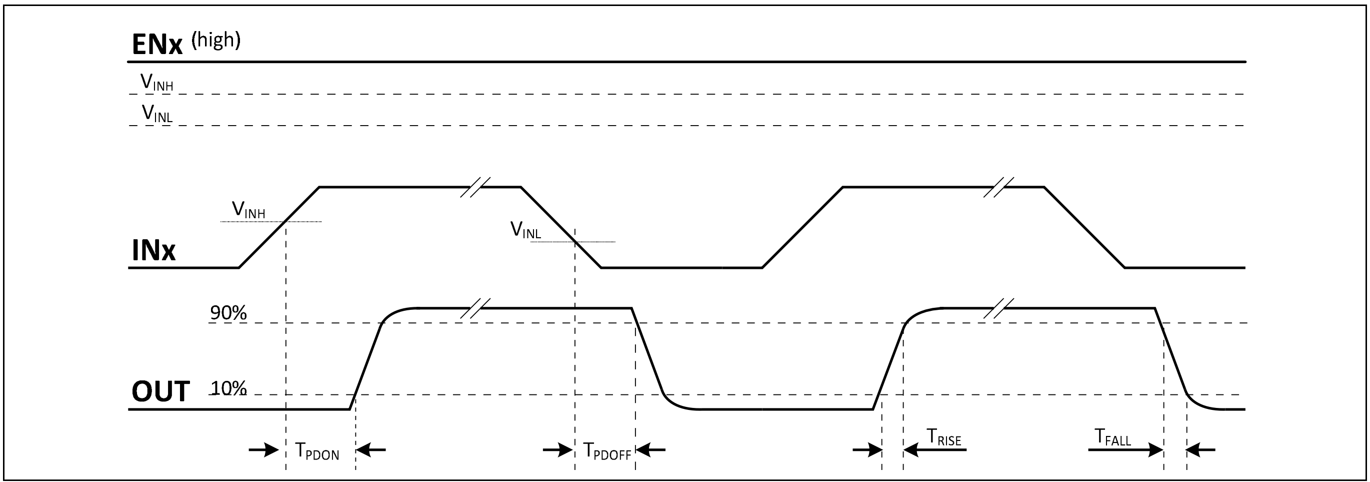


Figure 16 2EDN MOSFET drivers propagation delay definition

While propagation delays can affect the timing between the PWM and the power MOSFET, the delay is not a primary concern because it is normally accounted for within the converter's control loop.

The timing between the high side and low side switching MOSFET has to ensure "break before make" operation (turn off before the other switch turns on). This requirement prevents the cross currents that would occur when both MOSFETs are active.

Low propagation delay variation is a key for synchronous switching power converters with high efficiency. The time frame between switching conditions is dead time and degrades efficiency, which needs to be considered due to tolerances, thermal-related delays and load conditions in the SMPS. The more consistent each component is the better the performance and adverse conditions are less likely to occur.

2END752x/2EDN842x:
Consistent propagation delays in the same IC enable the device to drive both driver channels in parallel. This doubles the supported current and supports MOSFETS with high gate loads. The 2EDN driver keeps this variation of less than 4 ns and prevents destructive cross currents. The resulting low ohmic, low power dissipation enables a very efficient method of paralleling MOSFETs in a synchronous rectification stage.

For isolated converters using a primary-side PWM controller and a secondary-side synchronous rectifier MOSFET driver, the propagation delay can significantly affect the timing between the primary and the secondary side switching node. A requirement for these types of converters is that the total delay to the secondary synchronous rectifiers must be less than the delay from the PWM through the power transformer. Using a secondary-side MOSFET driver with a propagation delay larger than the primary-side PWM to MOSFET delay can make it difficult to optimize the timing between the primary and secondary. The 1EDN/2EDN family has a very low propagation delay variation therefore, precise and highly efficient power supplies can be driven.

Both the1EDN751x and 1EDN851x series have identical delay timings on each input pin pair.

1.4 Packaging

As with any power management IC, the junction temperature of the MOSFET driver must be kept safely within rated limits under all operating conditions. Industry-standard packages (Figure 17) such as TSSOP / DSO8, and VDSON are popular considerations, but high-current MOSFET drivers used in high-frequency applications require careful consideration to be given to advanced packaging techniques.

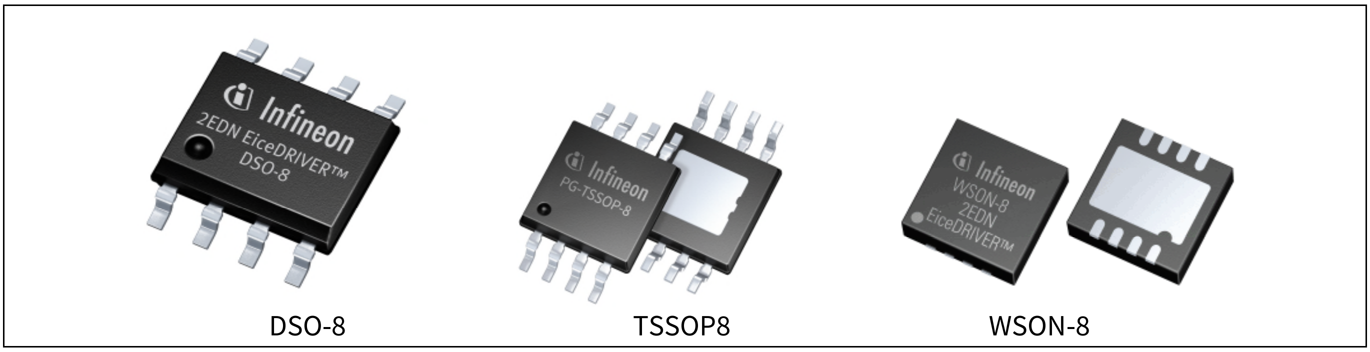


Figure 17 2EDN package variation

2EDN MOSFET drivers are placed in WSON or TSSOP packages with an exposed lead frame die pad on the bottom of the package. This is known as a Power Pad and offers thermal impedance with a junction-to-case rating as low as 2°C/W. This package version is ideal for SR applications with high switching speed and a high gate load due to super junction MOSFETs in parallel. The small package size and compact footprint enables designs with high power density.

The DSO-8 package is a well-known package. Many power supplies are based on this driver package. It is robust, solid and can be used in wave soldering processes. The wider pin pitch facilitates visual inspection during production.

For single, low side MOSFET drivers, the 1EDN751x/1EDN851x offer smaller package types. This is shown in Figure 18. These package types offer more than 60 % space reduction to a DSO-8 package.

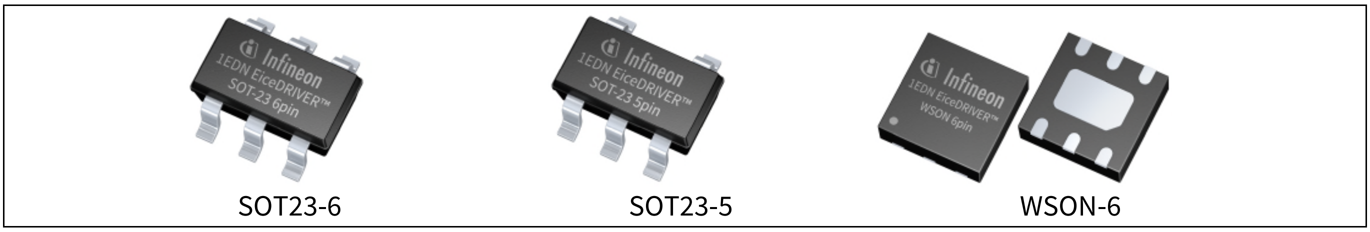


Figure 18 1EDN package variation

The driver can be placed close to the power MOSFET and reduce parasitic influences in the gate loop. Fast switching is possible.

2 PCB design considerations

2.1 Layout recommendations

Good PCB layout is essential for high-current, fast-switching devices to ensure optimal functioning of the design along with providing robustness during transient events. As explained in this application note, the 2EDN family of gate drivers has powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power MOSFET to facilitate very fast voltage transitions.

High di/dt causes significant ringing if the trace lengths and impedances are beyond recommended limits. When designing with 2EDN drivers:

- The driver should be placed as close as possible to switching MOSFET in order to minimize the length of any high-current traces between the driver output pins and the gate of MOSFET.

- The V_{DD} bypass capacitors between V_{DD} and GND should be as close as possible to the driver with minimal trace lengths to improve the noise filtering. These capacitors support high peak current being drawn from V_{DD} during turn-on of MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.

- The turn-on and turn-off current loop paths (MOSFET driver, MOSFET and V_{DD} bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops during turn-on and turn-off transients, which will induce significant voltage transients on the output pin of the driver device and the gate of the MOSFET.

- Parallel the source and return traces, taking advantage of flux cancellation, if feasible, while routing the tracks.

- Separate power traces and signal traces, such as output and input signals.

- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the MOSFET driver is connected to the other circuit nodes such as the source of the MOSFET and the ground of the PWM controller at a single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.

- Use a ground plane to provide noise shielding. Fast rise and fall times at the output may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can act as a heatsink and assist in power dissipation.

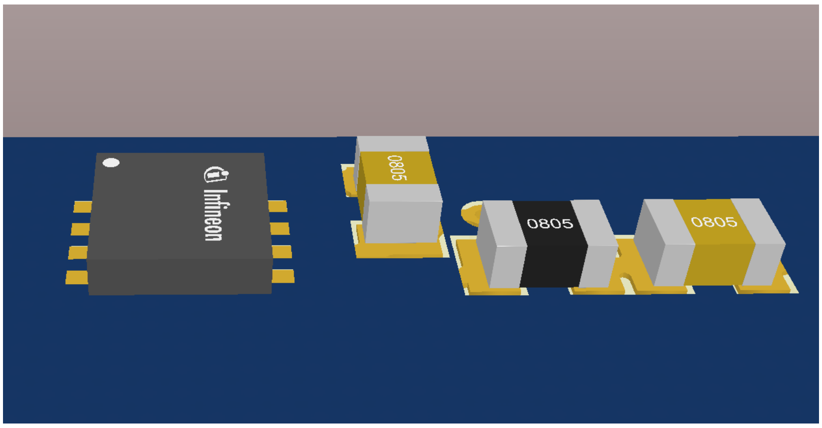
In noisy environments, connect the input of an unused channel of the 2EDN to GND (using short traces) to ensure that the output of that channel is disabled and prevent noise from causing malfunction in that output. This is particularly necessary when testing the capabilities of each channel individually.

TSSOP and WSON package – thermal conduction to PCB

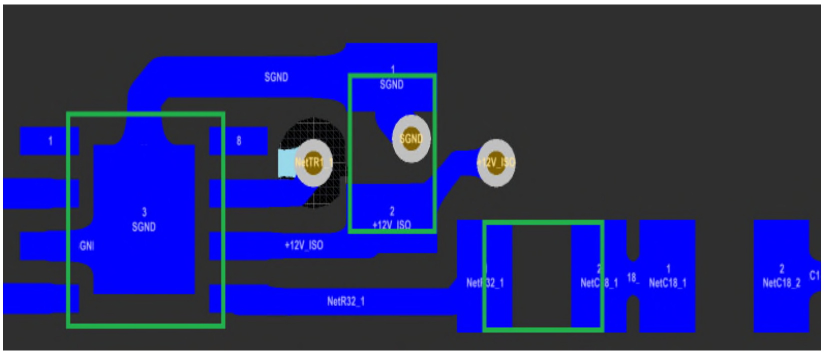
The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the TSSOP8, WSON-8 and WSON-6 (1EDN7512G) packages are not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate of the device. It is generally recommended to externally connect the exposed pads to GND in the PCB layout for better EMI immunity.

2.2 Typical 2EDN layout snapshots

Consider a 2EDN7524G in a synchronous rectification application. As shown in Figure 19, channel A is used on the top side. Channel B controls the power MOSFETS on the back side. SGND (ground) and +12V_ISO (V_{DD}) are routed from the back side to the blocking capacitor. PWM signals (INA and INB) are routed from left side top layer.



Device placement



Wiring in one layer

Figure 19 Typical layout example for WSON-8 package (2EDN7524G)

Another example with 1EDN7511B shows the benefit of a compact driver circuit design. GND and V_{DD} are on separated inner layers (Figure 20 layer 2 and 15). This enables low parasitic connections to IC. Blocking capacitor (C4) is as close as possible at the supporting pins.

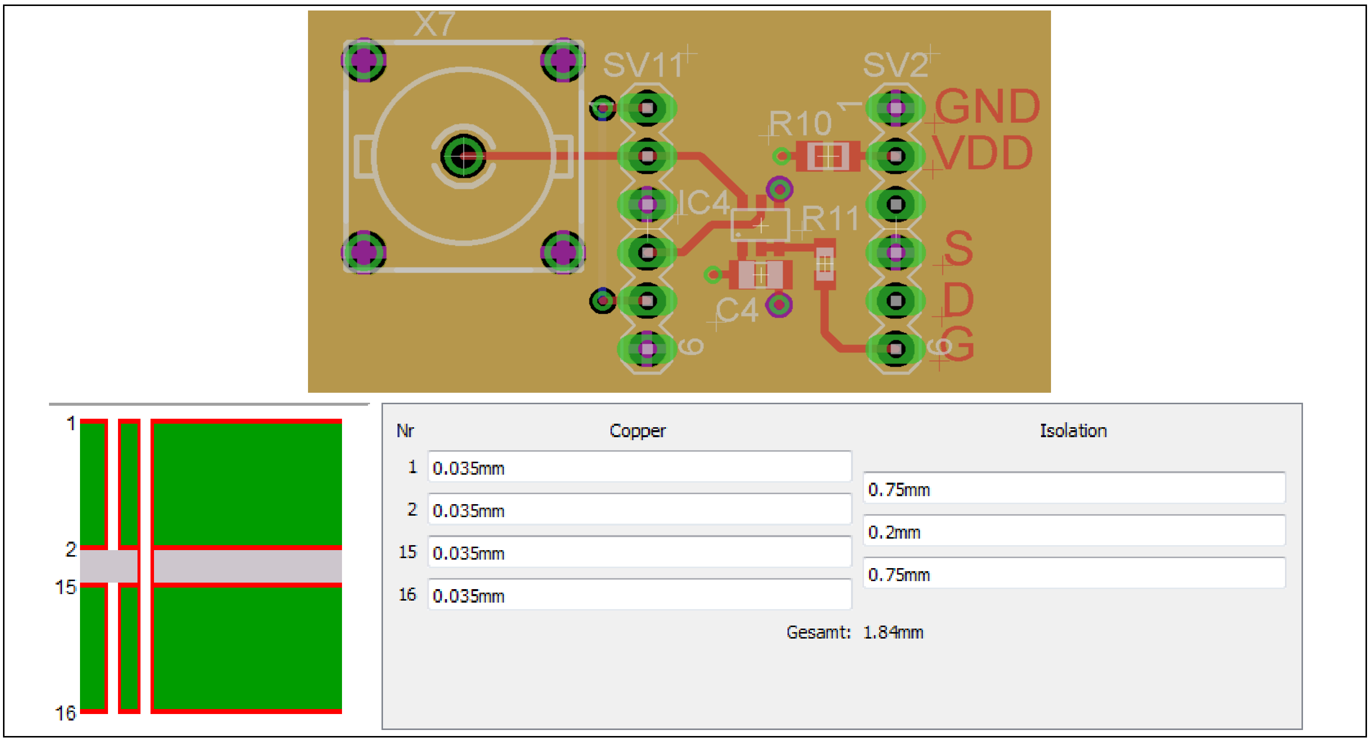


Figure 20 1EDN7511B (SOT23-6 package) in 4 layer PCB

If 4 layers or more are available, the MOSFET driver placement and wire routing can focus on space savings. A good placement, less vias and perfect routing enables high signal quality and robust functionality.

2.3 Thermal recommendations

The useful ranges of the 2END752x/2EDN842x and 1EDN751x/1EDN851x series are greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. We have earlier discussed how the strong output stage of the driver helps it to run cooler. For a gate driver to be effective over a particular temperature range, the package must allow the efficient removal of the heat produced while keeping the junction temperature within rated limits. The 2END752x/2EDN842x and 1EDN751x/1EDN851x family of drivers is available in different packages to cover a wide range of application requirements.

The TSSOP-8, WSON-8 and WSON-6 packages remove the heat from the semiconductor junction through the bottom of the package. Both of these packages offer an exposed thermal pad at the base of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows for a significant improvement in heatsinking.

3 MOSFET driver tests

3.1 Testing robustness and testing different driver output stages

As mentioned initially in this application note, there are different MOSFET drivers with different output stage configurations available in the market. Traditional MOSFET drivers were based on bipolar transistors in totem-pole configuration; newer technologies have MOSFETs. Based on the type of MOSFET technology available in the high side of the totem pole, an additional MOSFET may be required to provide the start-up current. There are also MOSFET drivers with a hybrid stage which combine MOSFET totem pole and transistor totem pole configurations to obtain an optimal drive current at high and low frequencies.

The 2END752x/2EDN842x and 1EDN751x/1EDN851x series are an all MOSFET output stage. To show the benefits of this MOSFET only configuration, a buck converter test setup is realized using the internal MOSFETs of the driver as the buck switches (Figure 21). This is not a standard test of robustness but it is used to highlight the benefit of the MOSFET only output stage of the 2EDN752x.

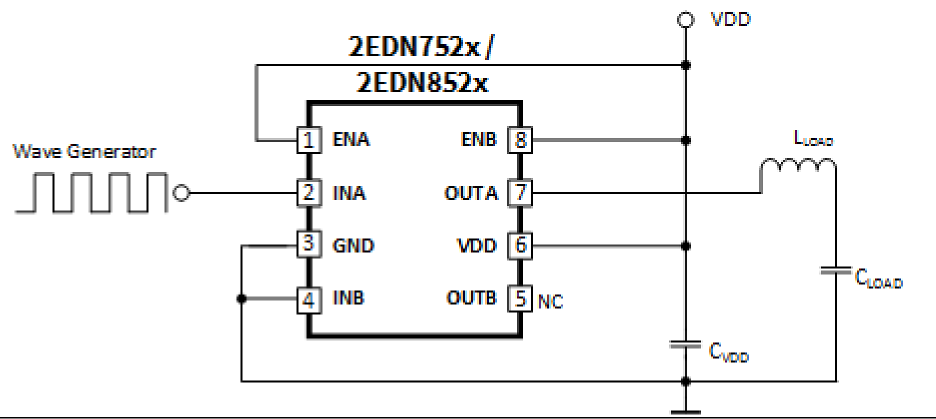


Figure 21 Buck converter to test robustness

An open loop buck converter is designed and the high side and low side switches are realized by the internal driver switches. The device performance is noted at 50 kHz to 100 kHz (50% duty-cycle, C_{LOAD} = 330 uF, L_{LOAD} = 22 uH, V_{DD} = 12 V).

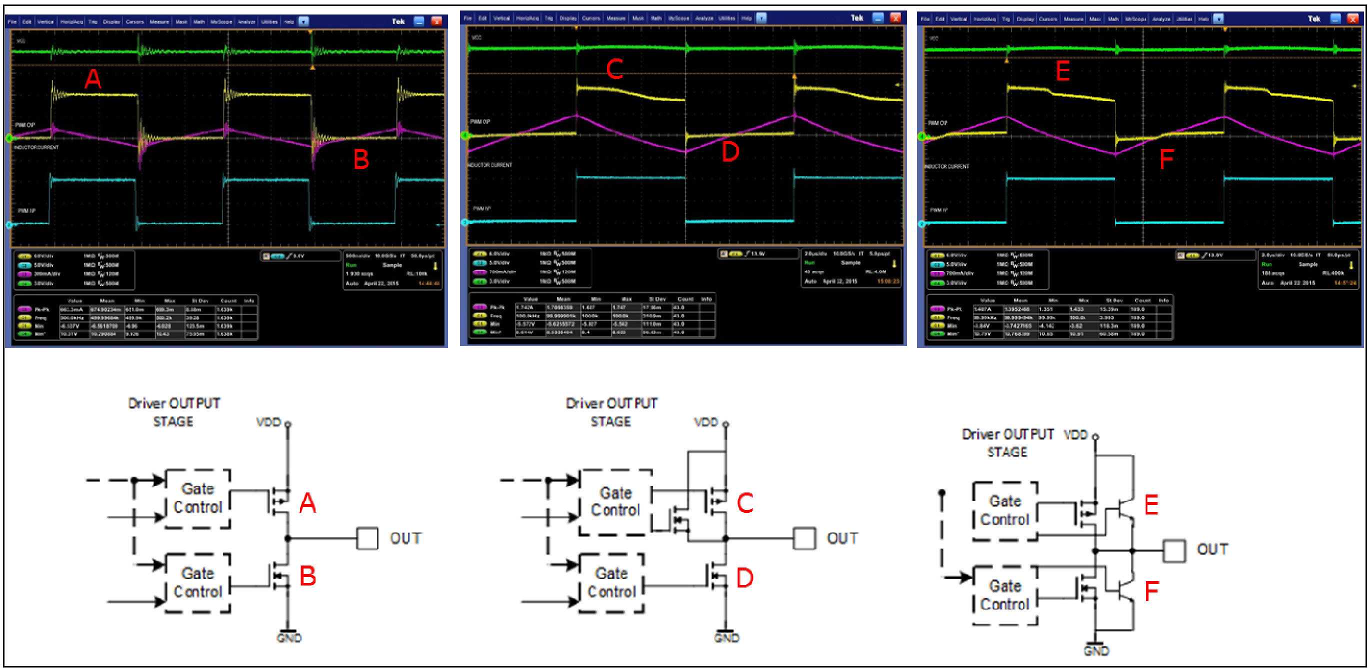


Figure 22 Robustness test results at 100 kHz

Figure 22 left side: Single totem pole MOSFET output stage (2EDN)

The advantages of the strong 0.7 Ω high side and 0.55 Ω low side MOSFET in the 2EDN752x is clearly seen at points A and B in Figure 15 above. The lack of a step on the driver output at zero current crossing shows that the drive current is carried by the MOSFET channel, not in the body diode. Very low voltage drops (flatness of the voltage waveform), decrease the power losses and makes the 2EDN robust.

Figure 22 middle: Totem pole MOSFET output stage with boost n-channel FET

As seen at points C and D, the step on the driver output reflects the zero current crossing. Here the current changes from being carried by the body diode to the MOSFET active channel. This is due to a weak high side and good low side MOSFET being used in the drive output stage. The resulting voltage drop causes the power dissipation to rise.

Figure 22 right side: Dual totem pole output stage with bipolar transistor and MOSFET

The bipolar stage drives the current; due to the "pn"-structure, it is not possible to drive rail to rail. This weakness is compensated by a second small totem pole MOSFET stage. In points E and F, the current is carried in the body diode due to the weak bipolar stage at the output - in the hybrid driver output stages. The resulting voltage drop causes the power dissipation to rise faster and to higher levels than the other two stages.

3.2 Output reverse current test and comparison with other MOSFET drivers

The test setup below (Figure 23) is used to test the robustness of the output stage of 2EDN MOSFET drivers.

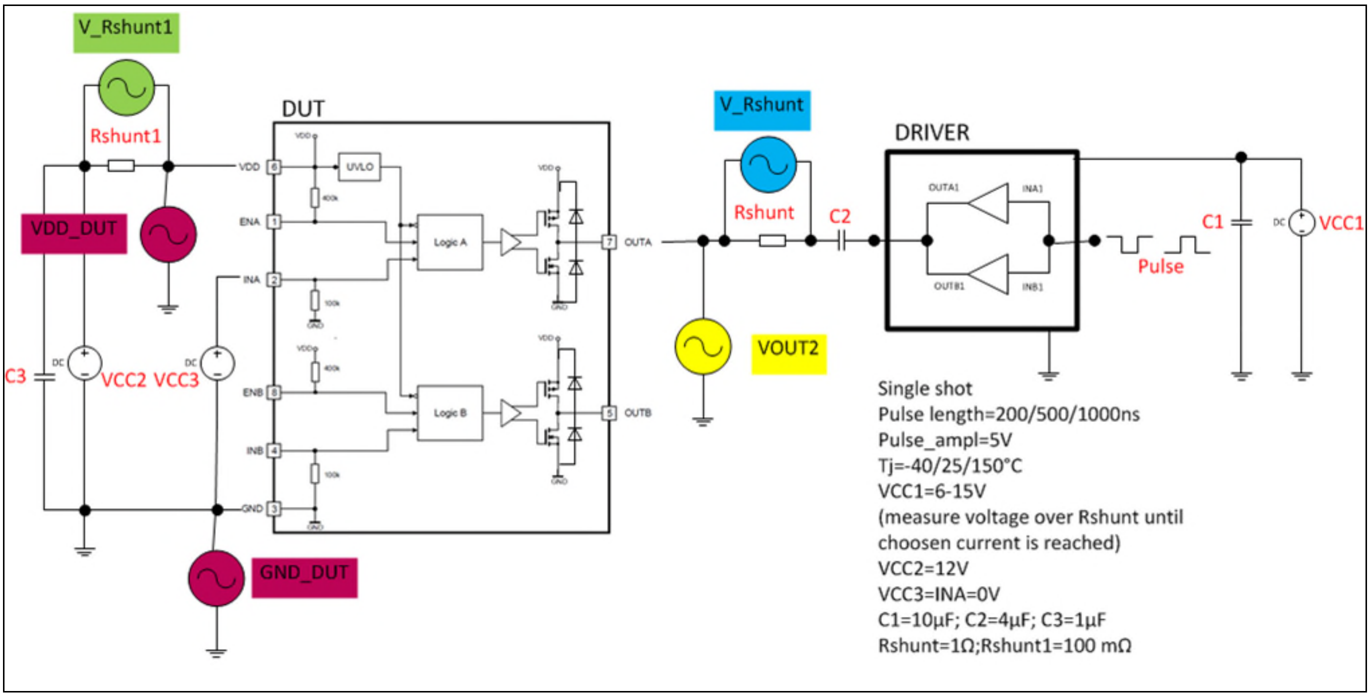


Figure 23 Measurement setup for reverse current robustness

Positive pulse:

The device under test (DUT) drives output OUTA static high via a logic "high" signal (VCC3, INA). The DRIVER output is low (0 V) and C2 is charged via R_{shunt}. Now, the DRIVER sends a reverse current pulse to DUT OUTA when toggling the DRIVER output from low to high. C2 will be discharged.

Negative pulse:

In this case, DUT OUT A is low and the DRIVER output is high. C2 is charged in the opposite way. A high to low pulse from the DRIVER discharges C2 and sends a reverse current to DUT OUTA.

Single shot, 5 V amplitude pulses of different lengths are injected from the output side and the response is measured on the output shunt and input shunt resistors. This is performed at various junction temperatures. The table below (Figure 24) along with relevant waveforms summarizes the test results.

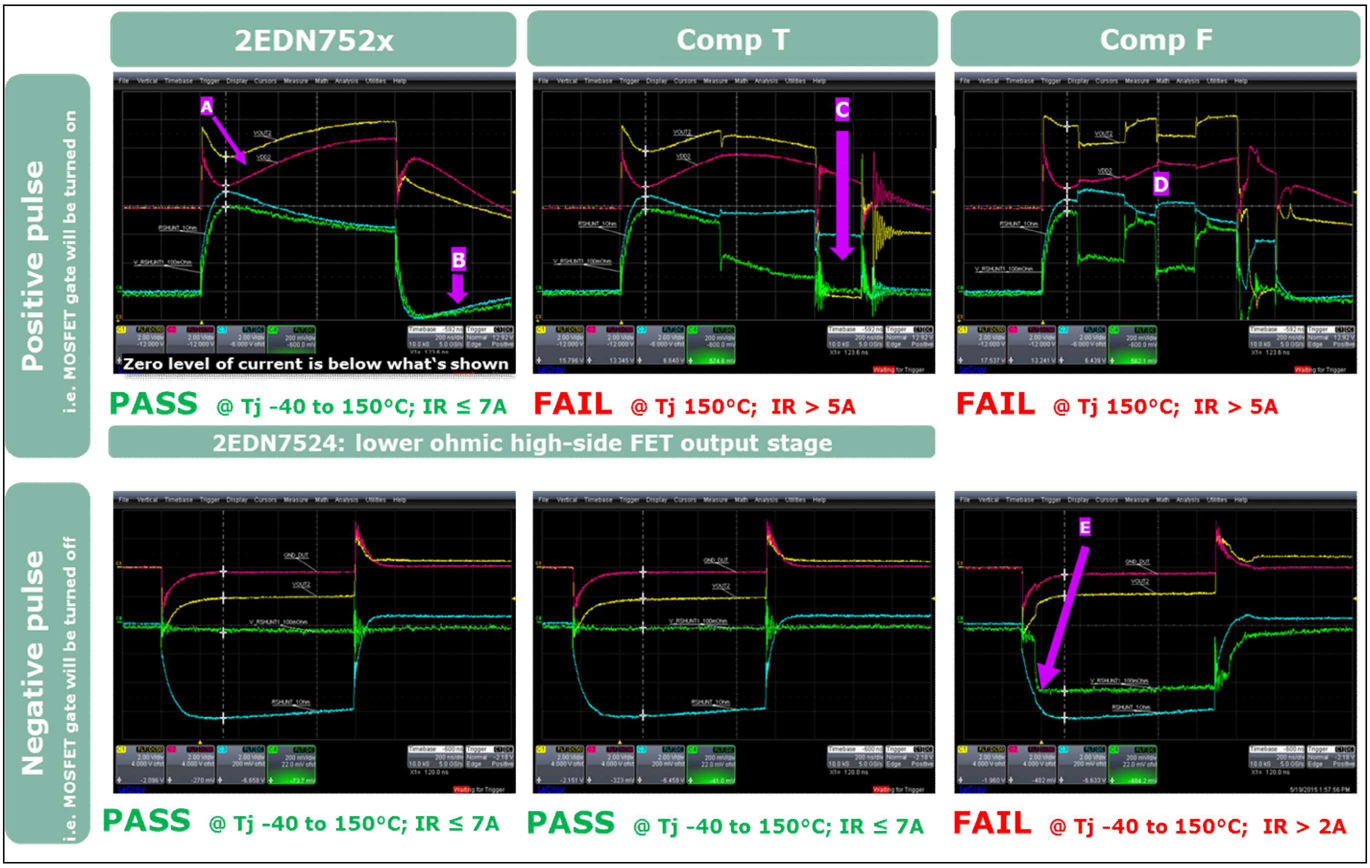


Figure 24 2EDN reverse current robustness explained as compared to different competition

Point A in the 2EDN752x shows the forward voltage diode drop. In an ideal case the reverse current which flows into OUT A returns out at V_{dd} and only the forward voltage drop of one diode leads to power dissipation. Reverse currents due to parasitic inductance can be seen at point A. At point B, a clean recovery is observed with the 2EDN752x.

With a competitive MOSFET driver, at point C we have an undefined recovery with high current. This is due to the parasitic pnp-BJT turning on, leading to two-thirds of the reverse current flowing out via GND as opposed to through V_{dd}. This leads to five times more power dissipation than with the 2EDN752x.

At point D the situation is far worse than above. As shown at point E, after 50 ns, the parasitic npn-BJT turns on and almost 75% of the reverse current flows through V_{dd} leading to high power dissipation that causes failure.

From these figures, it can be seen that the 2EDN752x driver can withstand 7 A of reverse current due to transients in either MOSFET turn on or turn off conditions.

3.3 Output reverse current protection test with diodes

Based on the output voltage drop across external diodes D_1/D_2 (typically BAT54 when used), it can be seen that the BAT54 carries a very small share of the reverse current. Most of the reverse current flows through the output stage of the MOSFET driver (Figure 25).

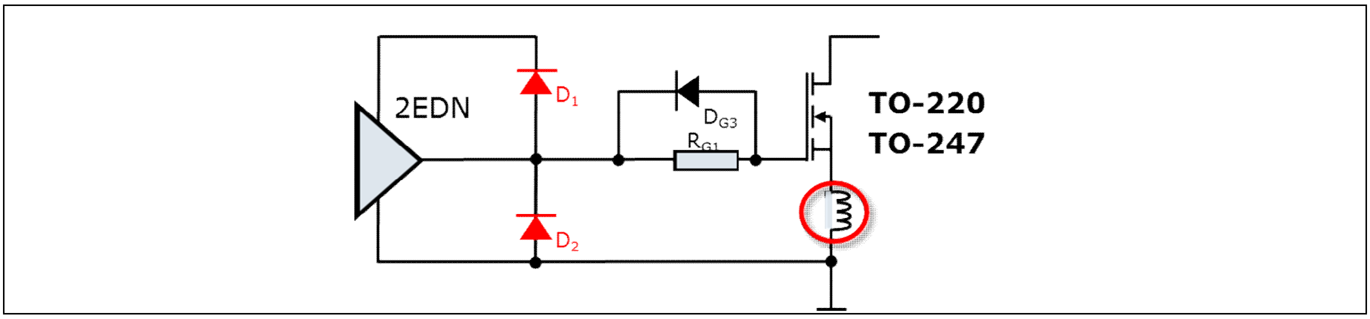


Figure 25 1EDN/2EDN MOSFET drivers have built in diodes at the output stage to withstand high reverse currents increasing the robustness

As an example, the 2EDN752x can carry most of the reverse current and is robust. It does not need external protection diodes as seen in Figure 26 below.

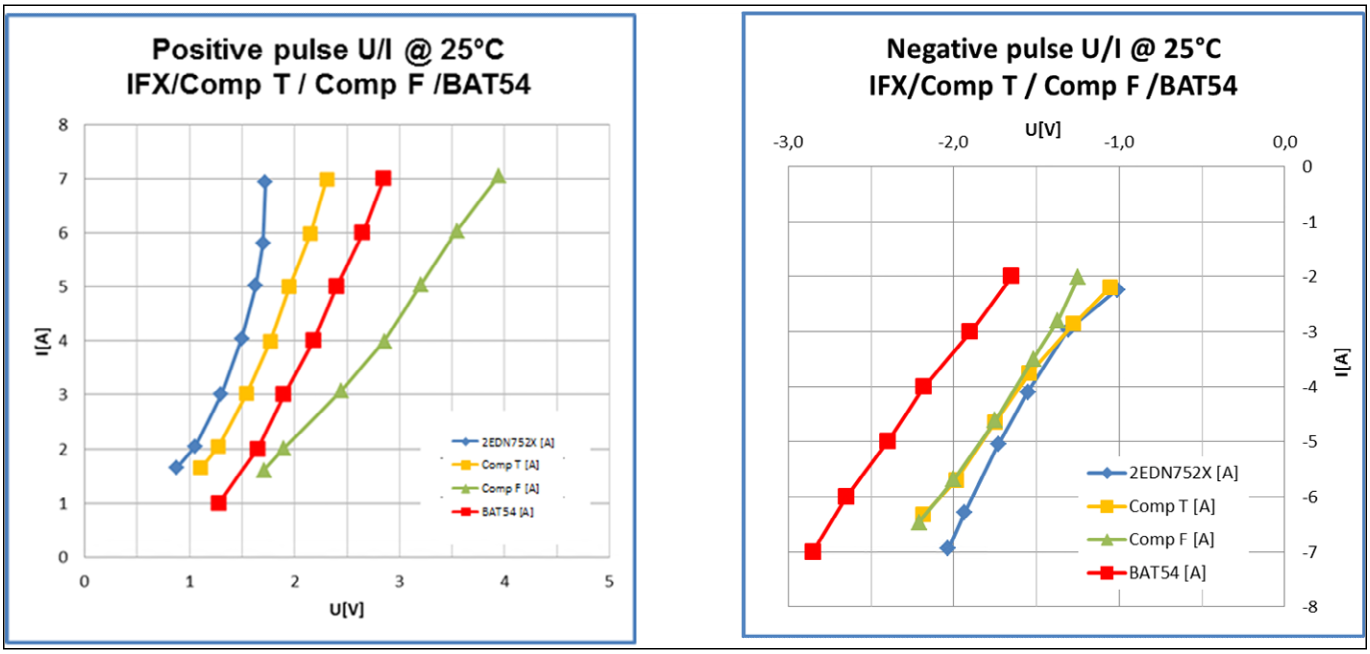


Figure 26 2EDN does not need external protection diodes at the output

The 1EDNx family reverse current behavior is similar. Due to the asymmetric driver bridge, the positive graph has a less deep increase, still stronger than Comp T. The negative graph has an even stronger increase of the reverse current, related to the voltage drop.

4 Conclusion

The 2END752x/2EDN842x and 1EDN751x/1EDN851x families of MOSFET drivers can be used effectively in different power supply topologies, requiring a low side gate drive such as PFC, secondary synchronous rectification, primary MOSFET gate drivers in combination with a pulse transformer for isolation.

The huge benefit of this driver family is

- A negative voltage withstand ability with crucial safety margin when driven from pulse transformers or used in non-optimal PCB layouts,
- Sharp voltage thresholds, low tolerances and pull ups/down resistors for robust functionality,
- Separated outputs for source and sink (1EDN7511B), which lower the bill of material (BOM)
- Reverse current capability with built-in diodes in the output stage to avoid using external diodes
- Low power dissipation in the driver due to a strong output stage with low ohmic p-channel MOSFETS and
- Under voltage lockout capability for comprehensive and reliable MOSFET protection.

Along with proper layout techniques and component selection around the driver, the 2END752x/2EDN842x and 1EDN751x/1EDN851x series makes a perfect complement to CoolMOS™ and OptiMOS™ and other similar MOSFETs when designing high efficiency power supplies.

5 References and proposed links

[1] Obtaining information about junction temperature by using the thermal coefficient – Infineon EiceDRIVER™ IC Application Note
http://www.infineon.com/dgdl/Infineon-AN2013_09_Junction_temperature_using_thermal_coefficient-AN-v2.0-en.pdf?fileId=db3a30434208e5fd01420933214a0116

[2] EiceDRIVER™ 2EDN family main page
http://www.infineon.com/2edn

[3] EiceDRIVER™ 1EDN family main page
http://www.infineon.com/1edn

[4] EiceDRIVER™ product main page
http://www.infineon.com/non-isolated-gate-driver-ic

6 Revision history

Major changes since the last revision

Page or reference	Description of change
	Initial version

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, Infineon™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SIL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Trademarks updated August 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2016-11-11

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_201609_PL52_031