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FDS8333C

30V N & P-Channel PowerTrench[®] MOSFETs

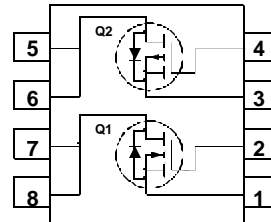
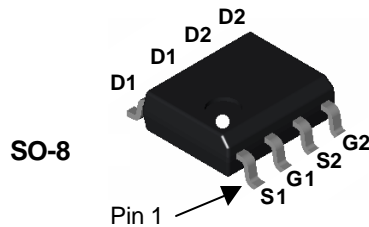
General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- **Q1** 4.1 A, 30V. $R_{DS(ON)} = 80\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 130\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- **Q2** -3.4 A, 30V. $R_{DS(ON)} = 130\text{ m}\Omega @ V_{GS} = -10\text{ V}$
 $R_{DS(ON)} = 200\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and handling capability in a widely used surface mount package.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V _{DSS}	Drain-Source Voltage	30	-30	V
V _{GSS}	Gate-Source Voltage	±16	±20	
I _b	Drain Current – Continuous (Note 1a)	4.1	-3.4	A
	– Pulsed	20	-20	
P _D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8333C	FDS8333C	7"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
Off Characteristics							
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_b = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_b = -250\ \mu\text{A}$	Q1 30 Q2 -30			V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_b = 250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$ $I_b = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$	Q1 Q2	25 -22		mV/°C	
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2		1 -1	μA	
I_{GSSF}/I_{GSSR}	Gate–Body Leakage, Forward	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA	
I_{GSSF}/I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA	
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_b = 250\ \mu\text{A}$	Q1 Q2	1 -1	1.7 -1.8	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_b = 250\ \mu\text{A}, \text{Ref. To } 25^\circ\text{C}$ $I_b = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$	Q1 Q2		-4.2 3.7		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_b = 4.1\text{ A}$ $V_{GS} = 4.5\text{ V}, I_b = 3.2\text{ A}$ $V_{GS} = 10\text{ V}, I_b = 4.1\text{ A}, T_J = 125^\circ\text{C}$	Q1 Q2		67 81 103	80 130 145	m Ω
		$V_{GS} = -10\text{ V}, I_b = -3.4\text{ A}$ $V_{GS} = -4.5\text{ V}, I_b = -2.5\text{ A}$ $V_{GS} = -10\text{ V}, I_b = -3.4\text{ A}, T_J = 125^\circ\text{C}$			105 167 147	130 200 220	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	Q1 Q2	10 -5			A
		$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$					
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_b = 4.1\text{ A}$	Q1 Q2		9 5		S
		$V_{DS} = -5\text{ V}, I_b = -3.4\text{ A}$					
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1 Q2		282 185		pF
		$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$					
C_{oss}	Output Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1 Q2		49 56		pF
		$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$					
C_{rSS}	Reverse Transfer Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	Q1 Q2		20 26		pF
		$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$					
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$	Q1 Q2		2.3 -9.6		Ω
		$V_{GS} = -15\text{ mV}, f = 1.0\text{ MHz}$					
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn–On Delay Time	For Q1 : $V_{DS} = 10\text{ V}, I_{DS} = 1\text{ A}$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		4.5 4.5	9 9	ns
t_r	Turn–On Rise Time		Q1 Q2		6 13	12 23	ns
$t_{d(off)}$	Turn–Off Delay Time	For Q2 : $V_{DS} = -10\text{ V}, I_{DS} = -1\text{ A}$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		19 11	34 20	ns
t_f	Turn–Off Fall Time		Q1 Q2		1.5 2	3 4	ns
Q_g	Total Gate Charge	For Q1 : $V_{DS} = 10\text{ V}, I_{DS} = 4.1\text{ A}$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$	Q1 Q2		4.7 4.1	6.6 5.7	nC
Q_{gs}	Gate–Source Charge		Q1 Q2		0.9 0.8		nC
Q_{gd}	Gate–Drain Charge	For Q2 : $V_{DS} = -10\text{ V}, I_{DS} = -3.4\text{ A}$ $V_{GS} = -4.5\text{ V}$	Q1 Q2		0.6 0.4		nC

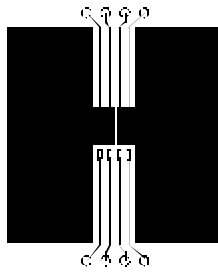
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

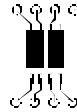
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain–Source Diode Forward Voltage	Q1 $V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.8	1.2	V
		Q2 $V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		0.8	-1.2	
t_{rr}	Diode Reverse Recovery Time	Q1 $I_F = 4.1\text{ A}, d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		16.3		nS
		Q2 $I_F = -3.4\text{ A}, d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		14.5		
Q_{rr}	Diode Reverse Recovery Charge	Q1 $I_F = 4.1\text{ A}, d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		26.7		nC
		Q2 $I_F = -3.4\text{ A}, d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		21.1		

Notes:

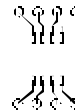
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 0.5 in^2 pad of 2 oz copper



b) $125^\circ\text{C}/\text{W}$ when mounted on a 0.02 in^2 pad of 2 oz copper



c) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics: N-Channel

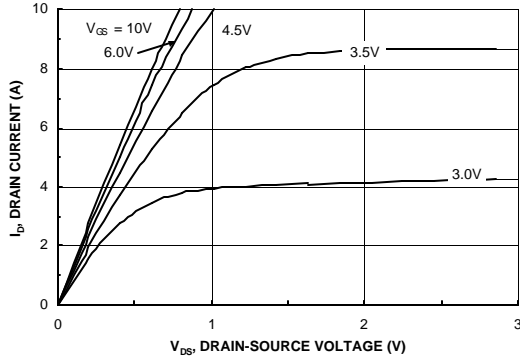


Figure 1. On-Region Characteristics.

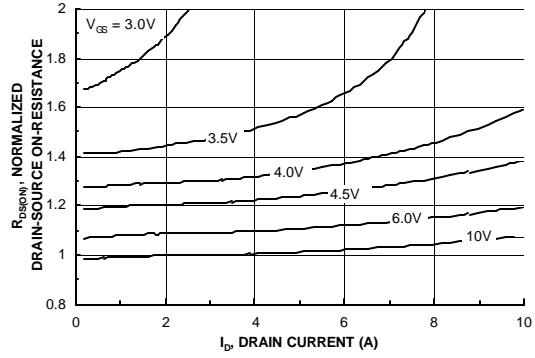


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

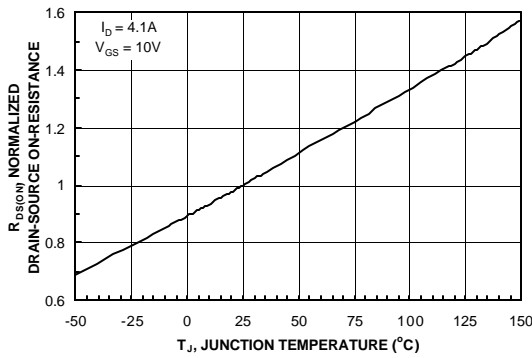


Figure 3. On-Resistance Variation with Temperature.

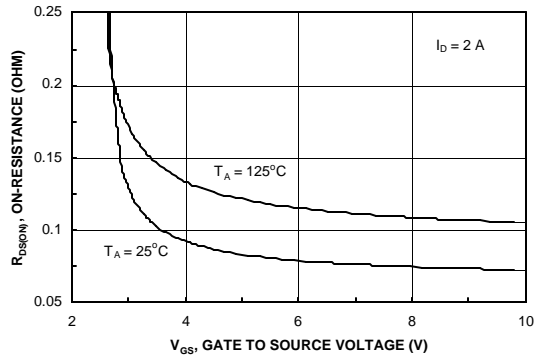


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

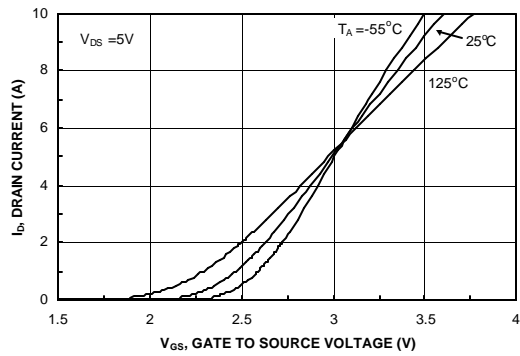


Figure 5. Transfer Characteristics.

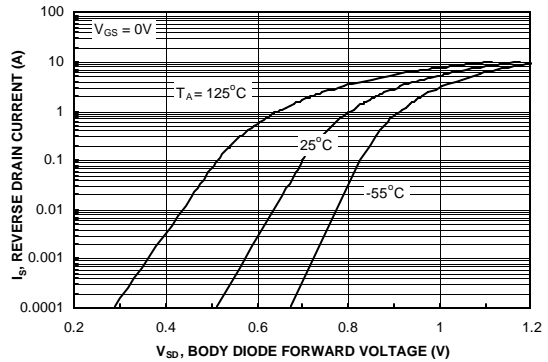


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

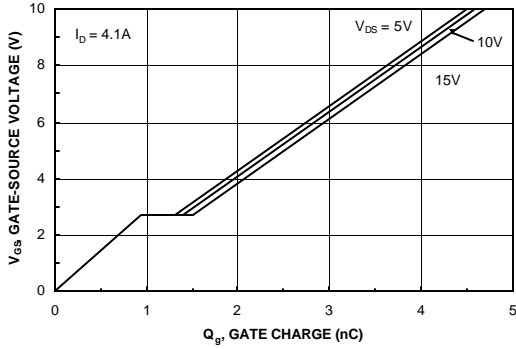


Figure 7. Gate Charge Characteristics.

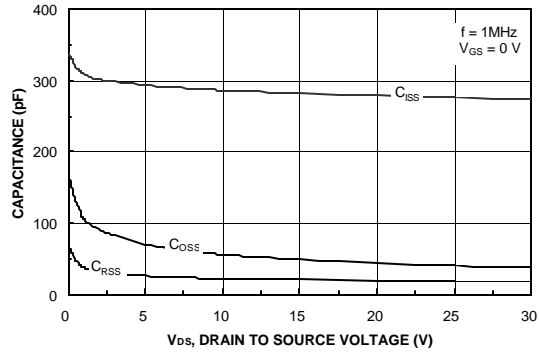


Figure 8. Capacitance Characteristics.

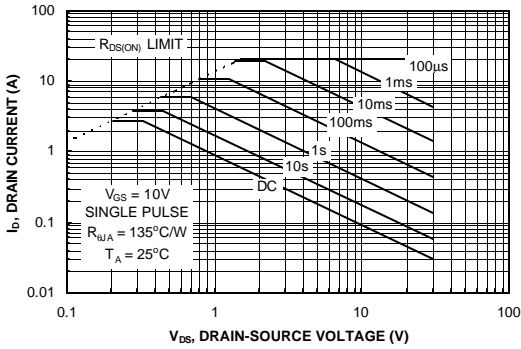


Figure 9. Maximum Safe Operating Area.

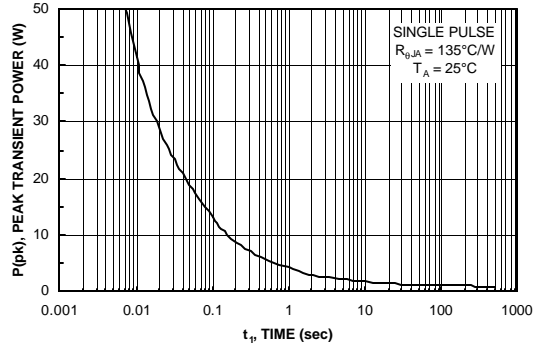


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

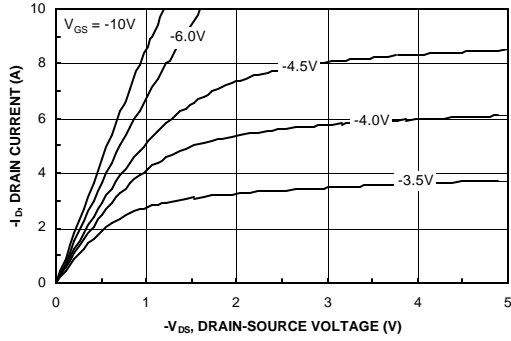


Figure 11. On-Region Characteristics.

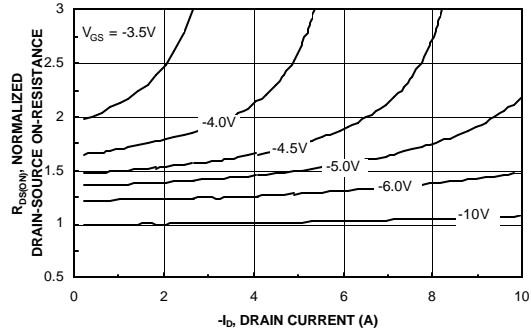


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

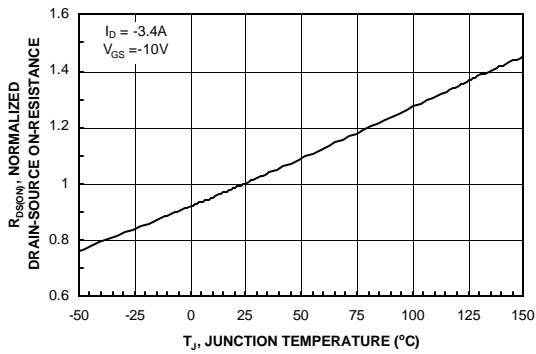


Figure 13. On-Resistance Variation with Temperature.

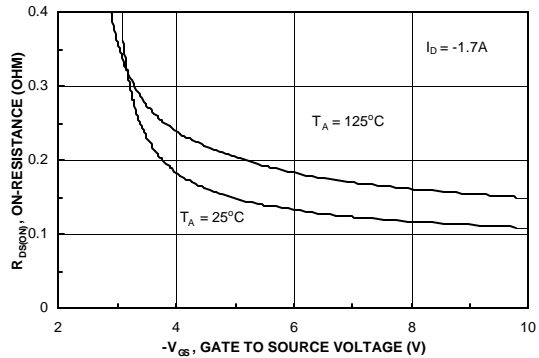


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

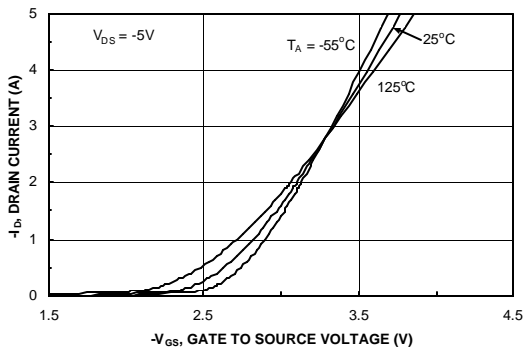


Figure 15. Transfer Characteristics.

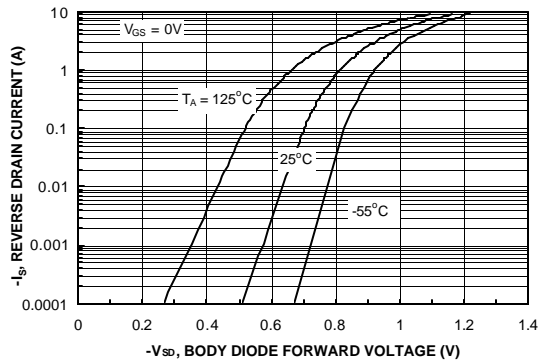


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: P-Channel (continued)

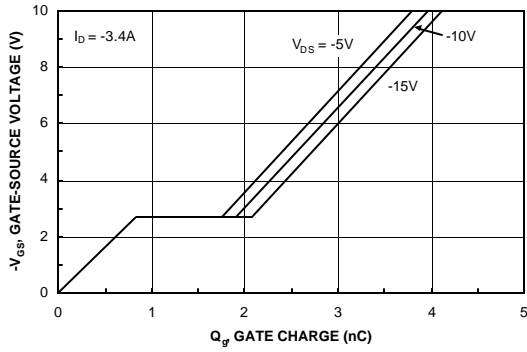


Figure 17. Gate Charge Characteristics.

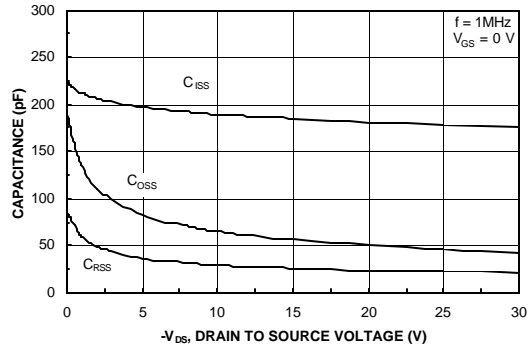


Figure 18. Capacitance Characteristics.

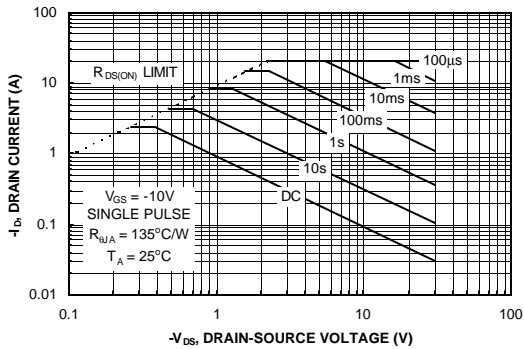


Figure 19. Maximum Safe Operating Area.

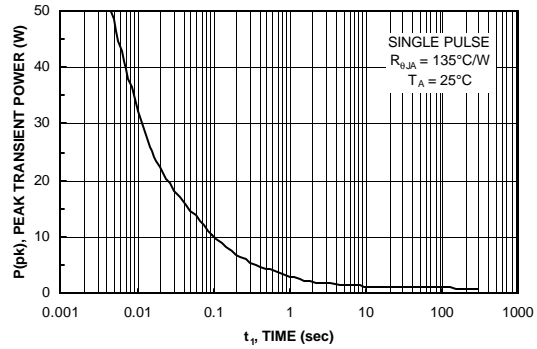


Figure 20. Single Pulse Maximum Power Dissipation.

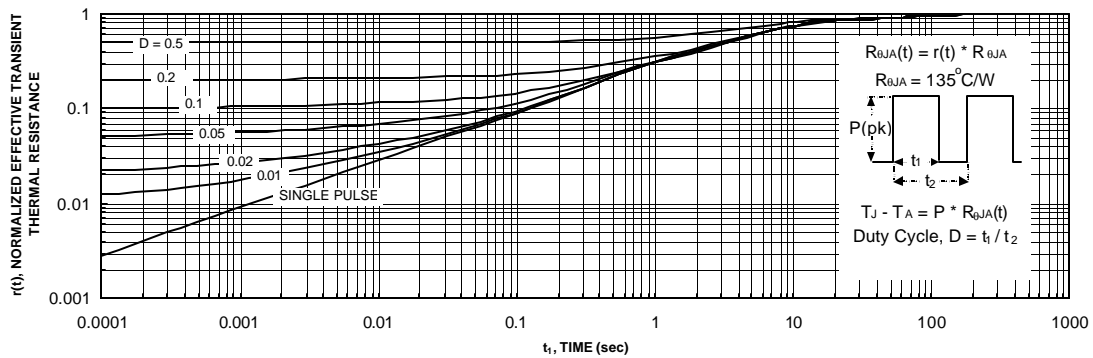


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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