

NXH5104

4 Mbit Serial EEPROM

Rev. 6 — 8 March 2017

Product data sheet

1. General description

The NXP NXH5104 is a 4 Mbit serial electrically erasable and programmable read-only memory (EEPROM). It provides byte level and page level serial EEPROM functions, sector level protection and power-down functions. The device has been developed for low-power low-voltage applications and is provided with a Serial Peripheral Interface (SPI) compatible interface.

2. Features and benefits

- Compact Wafer Level Chip Scale Package (WLCSP) package
 - ◆ 7.8 mm², 380 μm thick
 - ◆ 13 bumps with 400 μm pitch
- Integrated Power Management Unit (PMU)
 - ◆ V_{DD} supply range 1.0 V to 2.0 V
 - ◆ V_{DD(I/O)} supply range: V_{DD} to 2.6 V
 - ◆ Direct operation from ZnAir, NiMH, Silver-Zinc batteries
 - ◆ Active peak current limiting
- Low current consumption
 - ◆ Average power down current < 5 μA
 - ◆ Average read current 0.6 mA (V_{DD} = V_{DD(I/O)} = 1.8 V, F_{SPI} = 5 MHz)
 - ◆ Average write current 0.7 mA (V_{DD} = V_{DD(I/O)} = 1.8 V, F_{SPI} = 5 MHz)
- Low-power CMOS technology
- Auxiliary supply voltage enabling direct LED drive
- Self-timed program cycle
 - ◆ 256 byte page write buffer
 - ◆ Partial page write allowed
- Write Protect
 - ◆ Quarter, half or entire memory array
- Serial Peripheral Interface (SPI)
 - ◆ Speed up to 5 MHz for 1.2 V signaling level
 - ◆ Speed up to 10 MHz for 1.8 V signaling level
 - ◆ SPI Mode 0 (0,0) and 3 (1,1) support
 - ◆ SPI 3-wire support for SPI mode 0
- Fixed High Supply mode for faster start-up
- Space-saving 2.80 mm × 2.74 mm Wafer Level Chip Scale Package (WLCSP)
- Highly integrated: 1 external cap



- High Reliability
 - ◆ 10-year data retention
 - ◆ 500000 program cycles
 - ◆ Wear-out management
- Operating temperature $-20\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$
- Support for different supply configurations
- Device ID and Unique ID
- Pb-free and RoHS compliant

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
NXH5104UK/A1	WLCSP13	wafer level chip-scale package; 13 bumps; $2.74 \times 2.80 \times 0.38\text{ mm}$	SOT1461-1

4. Block diagram

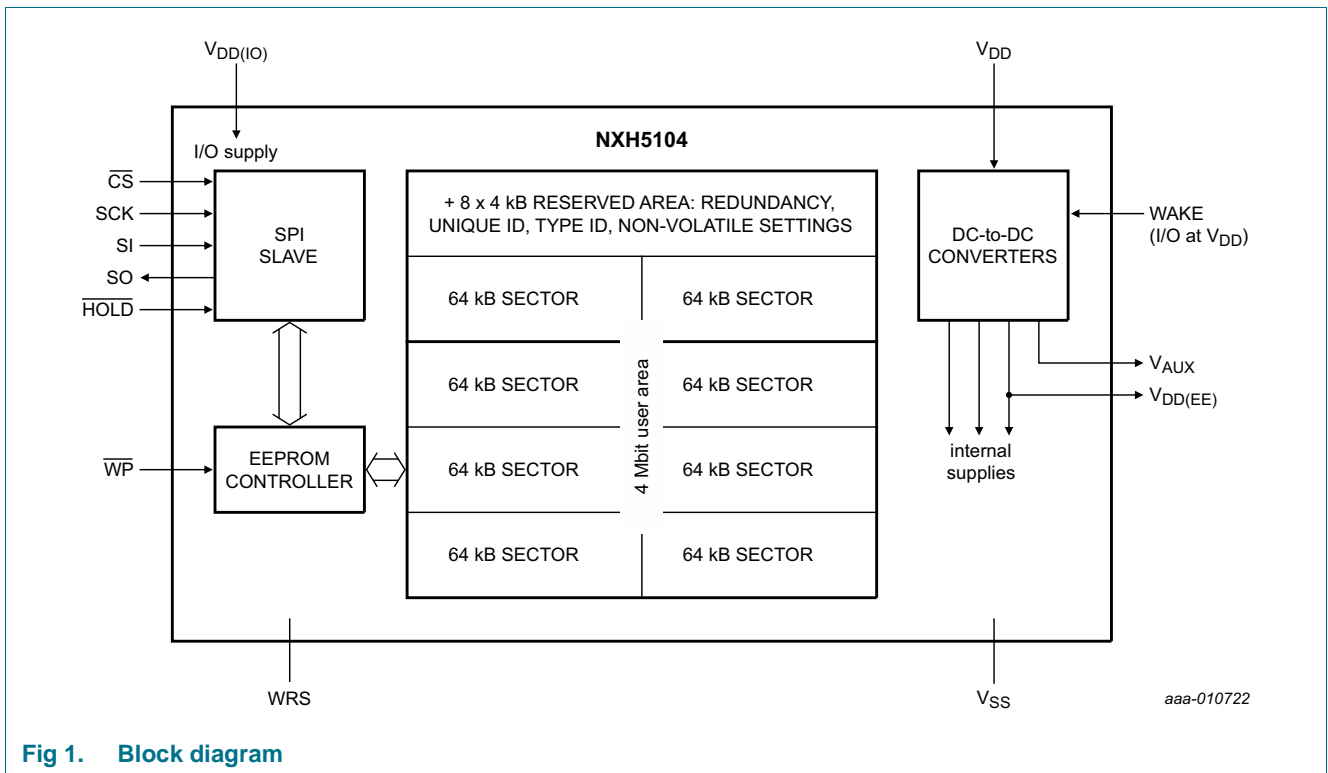


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

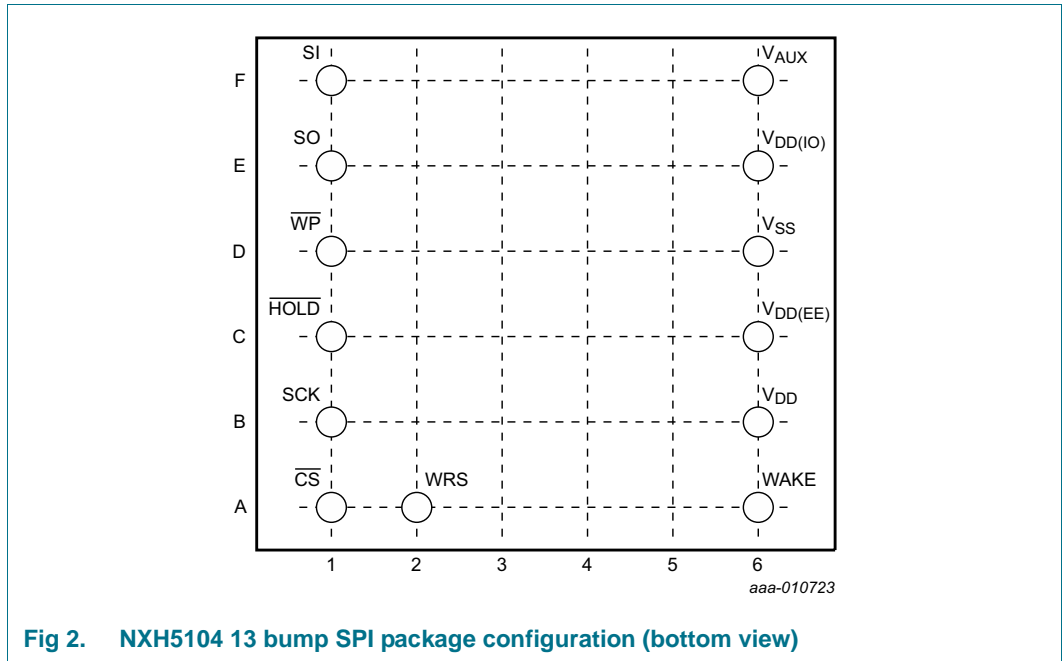


Fig 2. NXH5104 13 bump SPI package configuration (bottom view)

5.2 Pin description

Table 2. Bump allocation table

Bump	Symbol	Type	Description
SUPPLY			
B6	V _{DD}	PWR	primary supply input. The V _{DD} pin is used to supply the source voltage to the device. Operations at invalid V _{DD} voltages may produce spurious results and should not be attempted.
E6	V _{DD(IO)}	PWR	input/output supply input. The V _{DD(IO)} pin is used to supply the IO voltage to the device and hence defines the signaling voltage of the SPI slave interface. The voltage level of V _{DD(IO)} must be equal or higher than V _{DD} .
C6	V _{DD(EE)}	PWR	EEPROM array supply output. In Wide Range Supply mode, this pin requires a 470 nF decoupling capacitor. In Fixed High Supply (FHS) mode, this pin must be pulled HIGH with a 1 MΩ resistor to V _{DD} .
F6	V _{AUX}	PWR	auxiliary supply output. This pin provides a configurable voltage source for supplying other devices. Section 6.3 describes this functionality. A separate Application Note Ref. 2 provides more detailed usage information.
GROUND			
D6	V _{SS}	GND	analog/digital ground. Connect to the system GND.
CONFIGURATION			
D1	$\overline{\text{WP}}$	DI	write-protect pin. This pin is used to prevent inadvertent writes to the EEPROM array. When connected to GND, the device is write protected. When connected to V _{DD(IO)} , the device is not write protected.
A2	WRS	DI	wide-range supply pin. This pin configures the supply mode of the device. When connected to V _{DD(IO)} , the chosen supply mode is the Wide Range Supply mode. When connected to GND, the chosen supply mode is the Fixed High Supply mode. In this latter mode, a higher minimum voltage is required on V _{DD} , as described in Section 6.4 .
CONTROL			
A6	WAKE	DI	wake-up/power-down control input. To disable this functionality, the WAKE pin must be connected to GND. The SPI slave chip select input can then be used to wake up the device. To enable the WAKE functionality, the WAKE pin must be actively driven and may not be left unconnected nor floating. The input voltage level is referenced to V _{DD} .
SPI			
A1	$\overline{\text{CS}}$	DI	SPI slave chip select. Asserting the $\overline{\text{CS}}$ pin selects the device. When the device is deselected, the SPI SO output pin is in a HIGH impedance state. Commands issued to the device are not accepted. A HIGH to LOW transition on the $\overline{\text{CS}}$ pin initiates an operation, a LOW to HIGH transition ends an operation. For communication, the signaling level is referenced to V _{DD(IO)} . For waking up the device, the input level is referenced to V _{DD} .

Table 2. Bump allocation table ...continued

Bump	Symbol	Type	Description
E1	SO	DO	SPI slave serial data output. The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. The SO pin is in a high impedance state whenever the device is not selected. The signaling level is referenced to $V_{DD(I/O)}$. For EMI, it is required to pull-up the SO line at some place in the system: either the SPI master has an internal weak pull-up, either an external pull-up resistor is required.
F1	SI	DI	SPI slave serial data input. The SI pin is used the shift opcodes, addresses and data into the device and latched on the rising edge of SCK. The signaling level is referenced to $V_{DD(I/O)}$.
B1	SCK	DI	SPI clock input.
C1	$\overline{\text{HOLD}}$	DI	SPI HOLD. The $\overline{\text{HOLD}}$ pin can be used to pause an on-going SPI transaction. More information on usage can be found in Section 6.1.1 . The signaling level is referenced to $V_{DD(I/O)}$. To disable this functionality, the HOLD pin must be connected to $V_{DD(I/O)}$.

6. Functional description

6.1 SPI interface

The NXP NXH5104 acts as a slave device on the Serial Peripheral Interface (SPI) bus. It supports mode 0 (0,0) and mode 3 (1,1) transfers at standard clock speeds up to 5 MHz. It also supports high-speed operation up to 10 MHz when $V_{DD(I/O)}$ exceeds 1.8 V. Incoming data on the SI pin is latched on the rising edge of SCK. Outgoing data output on the SO pin is output on the falling edge of SCK. A leading or trailing falling edge of SCK is discarded.

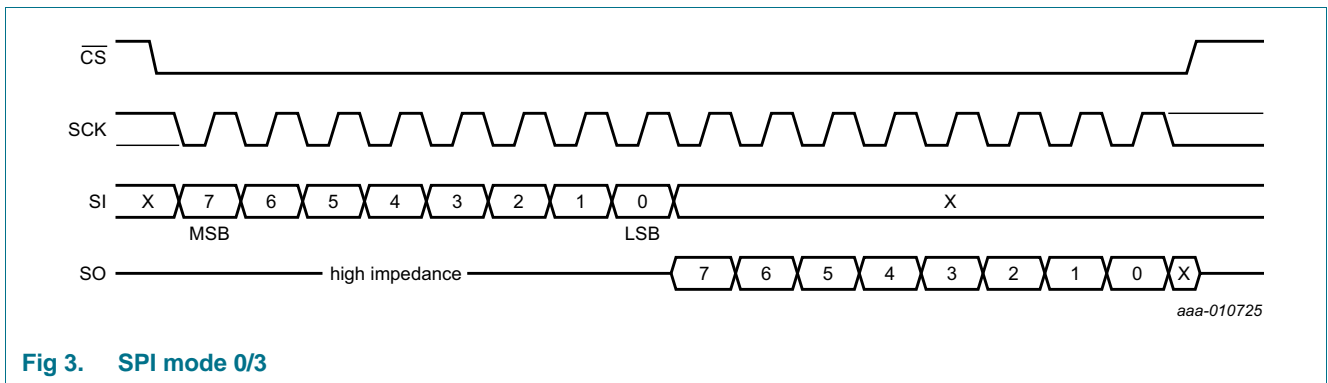


Fig 3. SPI mode 0/3

Transactions are byte-oriented, counting an integer multiple of 8-bit words, whereby the Most Significant Bit (MSB) is transmitted first, Least Significant Bit (LSB) last. The master initiates a transaction by asserting \overline{CS} low and terminates it by de-asserting \overline{CS} high, even if it is a single-byte command.

The command byte is the first byte transmitted by the master and received by the slave on the SI line after asserting low the \overline{CS} pin.

6.1.1 SPI transaction hold

A \overline{HOLD} input is provided as an extension to the SPI interface. It enables the host to suspend an ongoing transaction such as performing a high priority transaction with another slave device.

While \overline{HOLD} is asserted low, the device releases the SO line to a high impedance state and discards any transitions on SCK and SI lines. The \overline{CS} line however, must remain asserted. The suspended transaction resumes when the \overline{HOLD} input is de-asserted high.

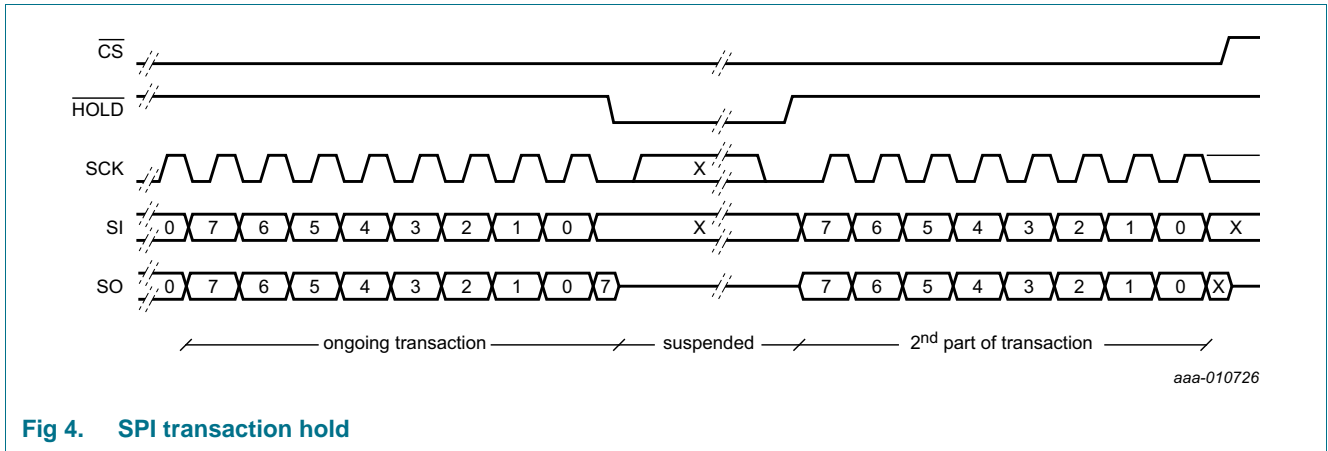


Fig 4. SPI transaction hold

The $\overline{\text{HOLD}}$ input must be asserted low when SCK is stable and must be de-asserted during the same clock phase as it was asserted.

The $\overline{\text{HOLD}}$ input must be asserted after the last bit of a byte has been asserted on SI (see [Figure 4](#)).

If this feature is not used, the $\overline{\text{HOLD}}$ input must be tied to $V_{DD(I/O)}$.

6.1.2 Overview commands

The NXP NXH5104 uses 8-bit commands. For some of these commands, the device needs time to execute the action during which no new commands can be serviced. These commands are referred to as Extended Operation Commands (EOC). For instance, the WRITE command is an EOC. The WRITE command triggers an erase-program cycle during which other commands are not serviced.

The host must poll readiness by issuing RDSR commands and must observe whether the RDY bit is asserted low.

If an invalid command byte is received, the command is ignored and the SO line remains in a high impedance state.

There are two types of write accesses: volatile and persistent. When a setting is written volatile, the change takes effect, but this setting reinitializes with its default value after a device power cycle. When a setting is written persistent, the change takes effect and the updated value is automatically loaded after a device power cycle.

Table 3. SPI command set overview

Command	Value	Description	EOC	Reference
WRSR	01h	write status register.	yes	Table 12
WRITE	02h	write data bytes to memory array.	yes	Table 7
READ	03h	read data bytes from memory array.	no	Table 4
WRDI	04h	disable write operations.	no	Table 9
RDSR	05h	read status register.	no	Table 17
WREN	06h	enable write operations.	no	Table 8
RDID	83h	read device ID and unique ID.	no	Table 18
RDR	F9h	read response.	no	Table 20
STBY	E0h	standby command.	yes	Table 26
SLEEP	E1h	sleep command.	yes	Table 25
PWDN	E2h	power-down command.	yes	Table 24
VWXS	E3h	volatile write of extended status register.	yes	Table 15
PWXS	E4h	persistent write of extended status register.	yes	
VAUXVW	E5h	volatile write of auxiliary supply configuration register (VAUXCFG).	yes	Table 27
VAUXPW	E6h	persistent write of auxiliary supply configuration register (VAUXCFG).	yes	Table 28
VAUXR	E7h	prepares a read auxiliary supply configuration register (VAUXCFG). To read the auxiliary supply configuration register value, use the RDR (Read Response) command.	yes	Table 29
WOIR	E8h	prepares a read of wear out status register. To read the wear-out status register value, use the RDR (Read Response) command.	yes	Table 21
RVDD	E9h	prepares a read of the V _{DD} supply voltage level. To read back the prepared data, use the RDR (Read Response) command.	yes	Table 23

6.1.3 SPI read operation (READ)

A read operation of the memory array is initiated when the SPI master issues a READ command, followed by the sector byte and the 16-bit address. The latter defines the offset within the chosen sector.

The NXP NXH5104 contains eight sectors; hence the SA field contains 3 bits. The remaining most-significant bits of the sector byte must be zero!

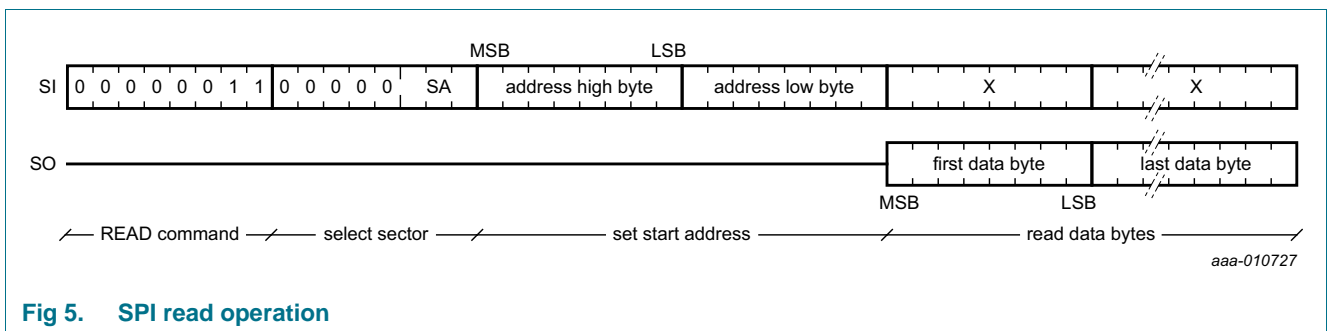


Fig 5. SPI read operation

Immediately following the last address byte (READ command), the device starts driving the SO line. It transmits consecutive data bytes read from the memory array, starting at the selected memory location, until the CS input is asserted HIGH.

During read operations, the internal address counter auto-increments. What happens at a sector boundary depends on the setting of the RAWMODE field of the Extended Status register (see Table 14). When RAWSEC is chosen, the address automatically wraps at the sector boundary. When RAWFULL is chosen, the address automatically increments beyond the sector boundary to the next sector.

If a previous program operation is in progress, the memory read/write operation is prohibited (treated as an invalid command).

A READ command is only allowed on sectors which are in Power-up mode.

Table 4. SPI READ command

Byte	Access	Command	Value	Description
0	W	READ	03h	read data bytes from memory.
1:3	W	SPI_AR	-	address register.
4:...	R	DATA	-	data bytes.

6.1.4 SPI write protection

To prevent inadvertent writes to the memory array and Status register, software and hardware protection mechanisms are included in the device.

The following protection is available for writing to the EEPROM memory array:

- The write enable bit (WEN) must be first set by issuing a write enable (WREN) command. It is cleared by issuing a write disable (WRDI) command. The write enable bit is also automatically cleared at power-up, after each WRITE command, and when the status register is written (WRSR or PWXSR).
- The corresponding sector protection bit SP(n) must be disabled.
- If a program operation is still in progress ($\overline{\text{RDY}} = 1$), writes are prohibited.

Table 5. SPI memory array write protection

RDY	WEN	WREN	$\overline{\text{WP}}$	SP(n)	WRITE command ^[1]
1	X	X	X	X	prohibited
X	0	X	X	X	prohibited
X	X	X	X	1	prohibited
0	1	X	X	0	allowed

[1] When prohibited, the WRITE command is treated as an invalid command.

The following protection is available for writing to the status register:

- The write enable bit (WEN) must be set by issuing a write enable (WREN) command. It is cleared by issuing a write disable (WRDI) command. It is also automatically cleared at power-up, after each WRITE instruction, and when the status register is written (WRSR or PWXSR).
- If the nonvolatile WPEN bit is set and the $\overline{\text{WP}}$ input is asserted low, hardware write protection is enabled.
- If a program operation is still in progress ($\overline{\text{RDY}} = 1$), writes are discarded.

Table 6. SPI Status register write protection

RDY	WEN	WPEN	WP	SP(n)	WRSR or PWXSR commands ^[1]
1	X	X	X	X	prohibited
X	0	X	X	X	prohibited
0	1	1	0	X	prohibited
0	1	0	X	X	allowed
0	1	X	1	X	allowed

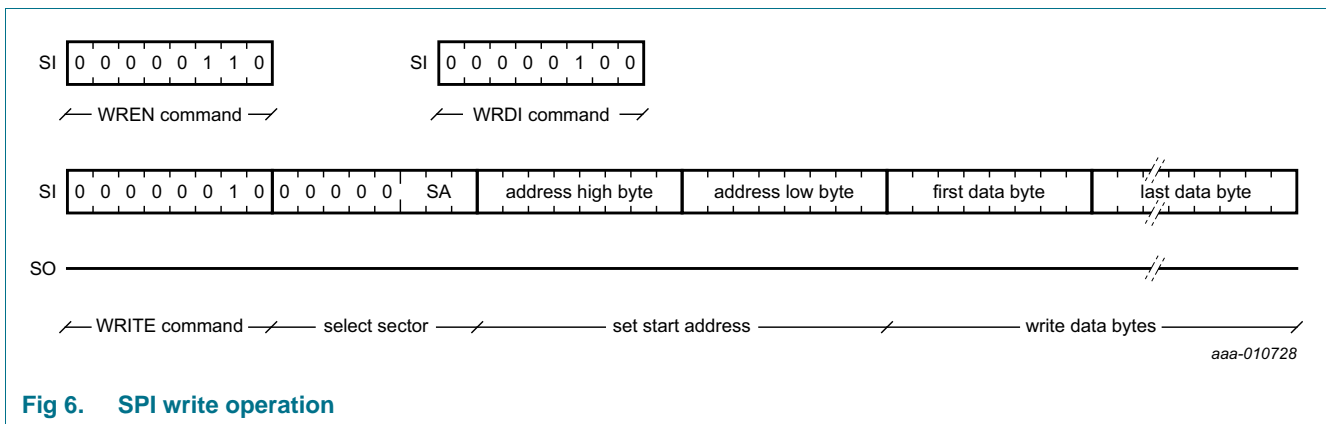
[1] When prohibited, the WRSR and PWXSR commands are treated as invalid commands.

Because the granularity of the write protection mechanisms is sector-based, it is recommended to store different types of data (e.g. firmware instructions versus data logging) in separate sectors.

6.1.5 SPI write operation (WRITE)

Since the write enable bit (WEN) is cleared after each write operation, a write enable (WREN) command must precede each WRITE command. The write enable (WREN) command and write disable command (WRDI) are single-byte commands.

A write operation is initiated when the master issues a WRITE command followed by 3 bytes. The first byte selects the sector, and the remaining 2 bytes set the 16-bit address pointer (offset within the sector).



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Fig 6. SPI write operation

Following the address bytes, any number of data bytes between 1 and 256 transmitted by the master, are written to the page write buffer. The write transfer is completed by asserting \overline{CS} high, upon which an internal self-timed program cycle is started.

The eight lower bits of the address counter, corresponding to the offset within the page buffer, auto-increment after each byte is written via SPI. Hence, the current address wraps at page boundary. If more than 256 data bytes are transferred via SPI, all bytes from byte 256 are discarded.

A write operation must be preceded by setting the write enable bit (see previous section).

A write operation is initiated when the master issues a WRITE command byte followed by the sector byte and the 16-bit (2-byte) address. The latter defines the offset within the chosen sector.

The NXP NXH5104 contains eight sectors; hence the SA field contains 3 bit. The remaining most significant bits of the sector byte must be logic 0!

If more than 256 data bytes are transferred through the SPI slave interface, these additional bytes are discarded.

Table 7. SPI WRITE command: write data bytes to memory

Byte	Access	Command/Data	Value	Description
0	W	WRITE	02h	write data bytes to memory.
1:3	W	SPI_AR	-	address register.
4:...	R	DATA	-	data bytes.

Table 8. SPI WREN command: enable write operations

Byte	Access	Command/Data	Value	Description
0	W	WREN	06h	enable write operations

Table 9. SPI WRDI command: disable write operations

Byte	Access	Command/Data	Value	Description
0	W	WRDI	04h	disable write operations

Table 10. SPI address register (SPI_AR)

Bits	Access ^[1]	Field	Value	Description
23:19	W	-	00000b	fixed SPI prefix. These bits should be written as zeros
18:16	W	SA_0	000b	sector address bits. Sector 0
		SA_1	001b	sector address bits. Sector 1
		SA_2	010b	sector address bits. Sector 2
		SA_3	011b	sector address bits. Sector 3
		SA_4	100b	sector address bits. Sector 4
		SA_5	101b	sector address bits. Sector 5
		SA_6	110b	sector address bits. Sector 6
		SA_7	111b	sector address bits. Sector 7
15:8	W	AH	-	high address bit
7:0	W	AL	-	low address bit

[1] W = volatile writable.

A write operation consists out of an erase cycle followed by a programming cycle. To guarantee the endurance, an adaptive trimming algorithm checks whether the erase cycle was successful. If not, another erase cycle is started at a higher (internal) supply level. This process leads to a longer programming time, which can be considerably higher than the typical programming time (see [Table 36](#)). It is highly recommended to poll completion through the RDSR command: as soon as the write operation is completed, the host can continue and issue new commands.

6.1.6 SPI status register

The Status Register (SR) is accessible through the RDSR and WRSR instructions. It can be read at any time to poll the device RDY status bit. The other bits of the Status Register

are not updated when the RDY is indicating busy state. They can be overwritten using the WRSR instruction. Under applicable write protection conditions (see [Section 6.1.4](#)), the WRSR command initiates a write of the Status Register

The status register can be accessed as part of the Extended Status Register (XSR).

Table 11. SPI status register

Bits	Access ^[1]	Field	Value ^[2]	Description
-	R/P	SR	(00h)	status register.
7	R/P	WPEN	(0b)	write protect enable bit.
6:4	R	-	(000b)	(reserved).
3:2	R/P	SP	(00b)	sector protection.
		SPNONE	00b	sector protection disabled.
		SPQUART	01b	protect sector 6 and 7 (upper quarter).
		SPHALF	10b	protect sectors 4 to 7 (upper half).
		SPALL	11b	protect all sectors.
1	R ^[3]	WEN	(0b)	write enable bit.
0	R	$\overline{\text{RDY}}$	(0b)	ready status bit.

[1] R = readable, P = persistent writable.

[2] Default manufacturing values between brackets.

[3] The WREN/WRDI commands set/clear the WEN bit.

Table 12. SPI write status register

Byte	Access	Command/Data	Value	Description
0	W	WRSR	01h	write status register.
1	P	SR	-	status register.

Table 13. SPI read status register

Byte	Access	Command/Data	Value	Description
0	W	RDSR	05h	read status register.
1	R	SR	-	status register.

6.1.7 SPI extended status register

An extended, 32-bit status register (XSR) can be read using the same RDSR command. The upper (first) byte corresponds to the 8-bit status register (SR). Reading beyond this first byte provides access to extended features/settings of the device.

Two functions support writing to the Extended Status Register:

- VWXSR: Volatile Write of the XSR. Only the fields indicated with W are writing.
- PWXSR: Persistent Write of the XSR. Only the fields indicated with P are writing.

Manufacturing default R/W/P fields are indicated (between brackets). A persistent write can configure the device in a mode which is unrecoverable. It is recommended that the host programs the preferred settings once at initial start-up.

Table 14. SPI XSR: extended status register

Bits	Access ^[1]	Field	Value ^[2]	Description
-	R/W/P	XSR	(0010h)	extended status register.
31:24	R/P	SR	(00h)	status register.
23:16	R/W/P	SPD	(00h)	sector power-down.
		bit 23	1b	power-down sector 7.
		bit 22	1b	power-down sector 6.
		bit 21	1b	power-down sector 5.
		bit 20	1b	power-down sector 4.
		bit 19	1b	power-down sector 3.
		bit 18	1b	power-down sector 2.
		bit 17	1b	power-down sector 1.
		bit 16	1b	power-down sector 0.
15:14	W	PMI	(00b)	power mode indicator.
		PMSB	00b	standby.
		PMS	01b	sleep.
13:12	R/W/P	IOMODE	(00b)	select $V_{DD(I/O)}$ mode.
			0xb	$V_{DD(I/O)} = V_{DD}$.
			10b	$V_{DD(I/O)}$ is fixed, > 1.5 V
			11b	$V_{DD(I/O)}$ is fixed, < 1.5 V
11:8	R	-	(00b)	(reserved).
7	R	WOI	(0b)	wear-out indication.
		WOIOK	0b	no wear-out, indication OK.
		WOINOK	1b	wear-out, indication not OK.
6:5	R	PSTAT	(00b)	result of last program operation.
		PNONE	00b	no program cycle has been started.
		PSUCCESS	01b	program cycle succeeded.
		PABORT	10b	program cycle aborted.
		PWORN	11b	page is worn out.
4	R/W/P	RAWMODE	(1b)	read address wrapping mode.
		RAWSEC	0b	wrap address at sector boundary.
		RAWFULL	1b	read across sector boundary.
3	R/W/P	WPPOL	(0b)	write protect input polarity.
		PLOW	0b	active low polarity.
		PHIGH	1b	active high polarity.
2:0	R	-	(000b)	(reserved).

[1] R = readable, W = volatile writable, P = persistent writable.

[2] Default manufacturing values between brackets.

Table 15. SPI VWXSR command: volatile write extended status register

Byte	Access	Command/Data	Value	Description
0	W	VWXSR	E3h	volatile write extended status register.
1:4	W	XSR	-	extended status register.

Table 16. SPI PWXSR command: persistent write extended status register

Byte	Access	Command/Data	Value	Description
0	W	PWXSR	E4h	persistent write extended status register.
1:4	W	XSR	-	extended status register.

Table 17. SPI read status register

Byte	Access	Command/Data	Value	Description
0	W	RDSR	05h	read status register.
1:4	R	XSR	-	extended status register.

6.1.8 SPI device identification

Device identification data comprises a fixed device ID as well as a unique ID. The identifiers can be retrieved using the RDID command. This command can only be applied if sector 0 is powered-up.

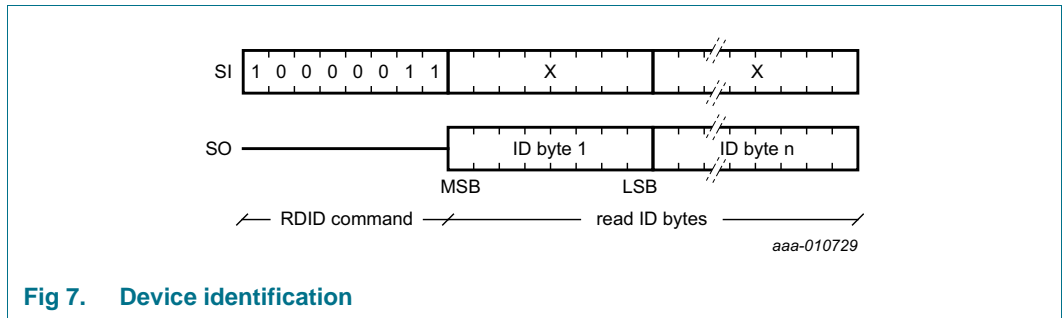


Fig 7. Device identification

Table 18. SPI RDID command: read device ID and unique ID

Byte	Access	Command/Data	Value	Description
0	W	RDID	83h	read device ID and unique ID.
1:3	R	DEVID	(001010h)	device ID.
4:15	R	UID	-	unique ID.

Table 19. SPI device ID

Bits	Access	Field	Value	Description
-	R	DEVID	(001010h)	device ID.
23:12	R	MFG	(001h)	manufacturing identification.
11:3	R	PART	(000000010b)	part identification.
2:0	R	REV	(000b)	revision number.

6.1.9 SPI read response (RDR)

Reads a 32-bit register after the extended commands: VAUXR or WOIR.

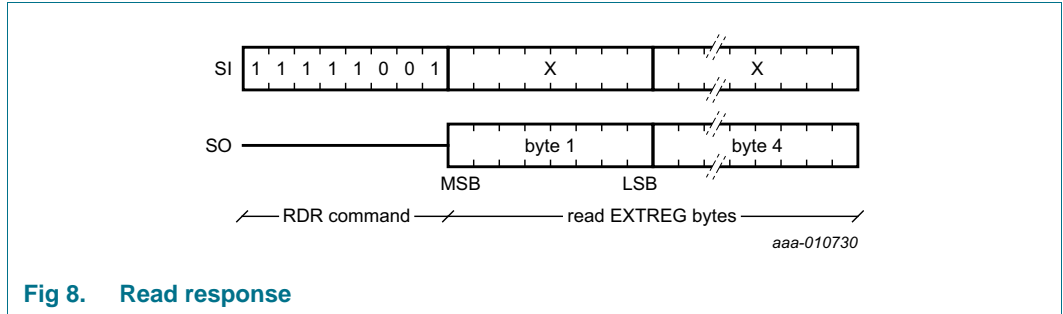


Fig 8. Read response

Table 20. SPI RDR command: read response

Byte	Access	Command/Data	Value	Description
0	W	RDR	F9h	read extended register.
1:4	R	EXTREG	-	extended register.

6.1.10 SPI wear-out status register (WOIR)

If the bit WOI in the XSR is set, a part of the EEPROM has reached its maximal endurance level. The host can request more details by consulting the Wear-Out Status Register (WOSR).

The register gives details informing which sector has reached the maximal endurance level.

The command WOIR prepares the wear-out status register.

The host must poll readiness by issuing RDSR commands and observing that the $\overline{\text{RDY}}$ bit is asserted low. To read the wear-out status register value, use RDR.

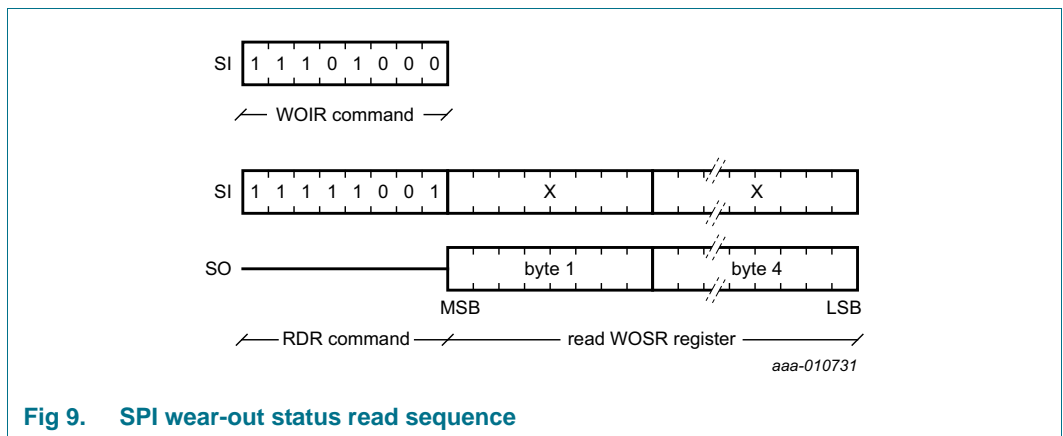


Fig 9. SPI wear-out status read sequence

Table 21. SPI wear-out status register

Bits	Access	Field	Value	Description
-	R	WOSR	-	wear-out status register.
31:24	R	SPD	(00h)	wear-out indicator.
		bit 31	1b	wear-out of sector 7 when set to 1.
		bit 30	1b	wear-out of sector 6 when set to 1.
		bit 29	1b	wear-out of sector 5 when set to 1.
		bit 28	1b	wear-out of sector 4 when set to 1.
		bit 27	1b	wear-out of sector 3 when set to 1.
		bit 26	1b	wear-out of sector 2 when set to 1.
		bit 25	1b	wear-out of sector 1 when set to 1.
		bit 24	1b	wear-out of sector 0 when set to 1.
23:0	R	-	undefined	(reserved).

Table 22. SPI RDR command: read response

Byte	Access	Command/Data	Value	Description
0	W	WOIR	E8h	Prepares a read of the wear-out status register. To read the wear-out status register value, use RDR.

6.1.11 SPI read of the V_{DD} supply (RVDD)

After the device receives the SPI read of the V_{DD} supply command, a response can be eventually read in the response register.

The command RVDD prepares the read of the V_{DD} supply.

The host must poll readiness by issuing RDSR commands and observing whether the RDY bit is asserted low.

To read the value of the V_{DD} supply, use RDR.

Table 23. SPI read of the V_{DD} supply

Bits	Access	Field	Value	Description
7:4	R	RVDD	(0h)	V_{DD} supply voltage level
			0h	0.850 V - 0.950 V
			1h	0.925 V - 1.025 V
			2h	1.000 V - 1.100 V
			3h	1.050 V - 1.150 V
			4h	1.150 V - 1.250 V
			5h	1.200 V - 1.300 V
			6h	1.250 V - 1.350 V
			7h	1.350 V - 1.450 V
			8h	1.400 V - 1.500 V
			9h	1.500 V - 1.600 V
			Ah	1.550 V - 1.650 V
			Bh	1.650 V - 1.750 V
			Ch	1.700 V - 1.800 V
			Dh	1.800 V - 1.900 V
Eh	1.850 V - 1.950 V			
Fh	1.900 V - 2.000 V			
3:0	-	(reserved)	(0h)	-

6.2 Power modes

In order to conserve power, the NXH5104 features scalable power modes as illustrated below.

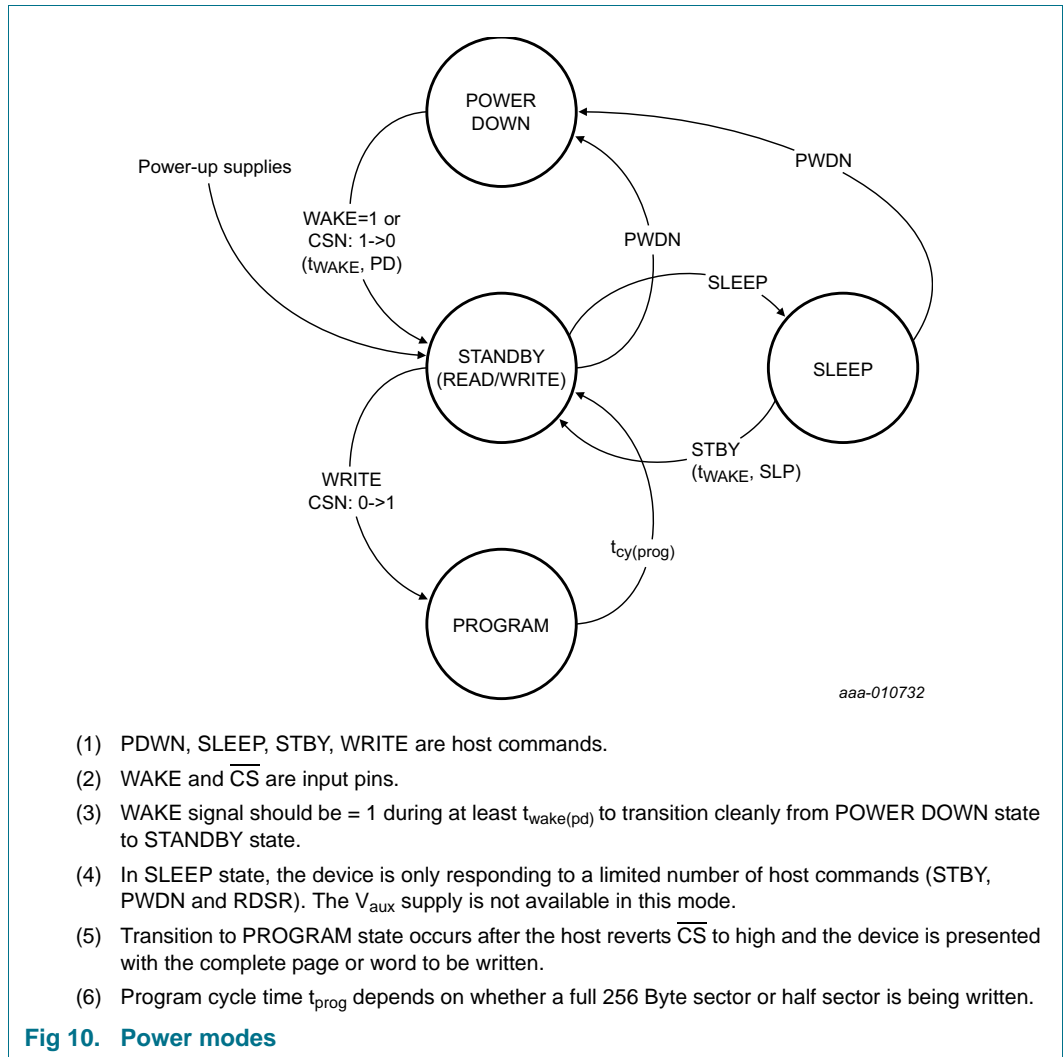


Fig 10. Power modes

6.2.1 Boot

When V_{DD} is supplied, the device by default boots into the STANDBY mode. To move the device into Sleep or Power-down mode, issue the Sleep or Power-down command over the SPI interface.

6.2.2 Power-down

The device features a Power-down mode with very low current consumption. All internal reference circuits are disabled in this mode, internally generated supplies are switched off, and output pins are in a high impedance state. The host controls the Power-down mode by using either a dedicated WAKE pin or the \overline{CS} pin. Both pins are plain inputs referenced to V_{DD} and must not float.

Wake-up using the \overline{CS} pin

When the \overline{CS} pin is used to wake the device, the WAKE pin must always be kept low. When the \overline{CS} pin is asserted low at V_{DD} start-up, the device starts ramping-up its supplies. After the wake-up time t_{wake} , the supplies are stable and the device becomes active and ready to process requests. To test it, poll the RDY bit.

When a 1 to 0 transition is detected on the \overline{CS} pin, the device ramps-up its supplies. After wake-up time t_{wake} , the supplies are stable and the device becomes active and ready to process requests. The RDY bit can be used to test that it is ready. This detection mechanism becomes active 1 ms after applying the V_{DD} .

Wake-up using the WAKE pin

If the WAKE pin is de-asserted (low) at start-up, the device remains in Power-down mode until the WAKE pin is asserted high.

When the WAKE pin is asserted high, the device ramps-up its supplies. After wake-up time $t_{wake(pd)}$, the supplies are stable and the device becomes active and ready to process requests. The RDY bit can be used to test that it is ready.

NOTE: The wake **must** be asserted low again before reverting to the Power-down mode.

When a PDWN command is issued, the device enters Power-down mode. If a program cycle is still in progress, the PDWN command is ignored. The RDY bit can first be polled to check if the command is valid.

Table 24. SPI PDWN: power-down command

Byte	Access	Command	Value	Description
0	W	PWDN	E2h	power-down command.

6.2.3 Sleep

Sleep mode is a power-saving mode in which the EEPROM array is powered down. However, internally generated supplies are maintained and the serial interfaces remain responsive to a limited set of host commands. The Auxiliary supply voltage (V_{aux}) cannot be maintained. For more information, see the Application Note: *V_{AUX} - Auxiliary voltage supply* (Ref. 2). This mode enables faster activation ($t_{wake(sleep)}$) compared to Sleep and Power-down modes. When a SLEEP command is issued, the device enters Sleep mode. If a program cycle is still in progress, the SLEEP command is ignored. The RDY bit can first be polled to check if the command is valid.

When in Sleep mode, the device only responds to STBY, RDSR and PDWN commands. The V_{aux} supply is not available in Sleep mode.

Table 25. SPI SLEEP: sleep command

Byte	Access	Command	Value	Description
0	W	SLEEP	E1h	sleep command.

6.2.4 Standby

In Standby mode, the EEPROM remains powered and ready to process read/write requests.

When an STBY command is issued in Sleep mode, the device ramps-up its internal supplies. After wake-up time $t_{\text{wake(sleep)}}$, the supplies are stable and the enabled EEPROM array sectors are switched to Power-on state. The enabled EEPROM array sectors are configured in the XSR register (non-user area). The device becomes active and ready to process read/write requests. Polling the RDY bit can be used to test it. Wake-up from Sleep mode is significantly faster ($t_{\text{wake(sleep)}}$) as it does not involve ramp-up of the supplies. It does involve switching the enabled EEPROM sectors to the Power-on state.

In STANDBY mode, the EEPROM array can be read and written with READ and WRITE commands.

Table 26. SPI STBY: standby command

Byte	Access	Command	Value	Description
0	W	STBY	E0h	standby command.

6.3 Auxiliary supply

The auxiliary supply voltage (V_{aux}) is a configurable DC-to-DC supply, generated from the primary supply voltage (V_{DD}) for supplying an external auxiliary component. It is configured using the VAUXVW, VAUXPW and VAUXR commands that configure the VAUXCFG register.

For performing a volatile write (VAUXVW) of the V_{AUX} configuration register, no preceding WREN command is required. If there is a persistent write (VAUXPW), a preceding WREN command is required.

Table 27. SPI VAUXVW command: volatile write auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXVW	E5h	volatile write auxiliary supply configuration.
1:4	W	VAUXCFG	-	auxiliary supply configuration register.

Table 28. SPI VAUXPW command: persistent write auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXPW	E6h	persistent write auxiliary supply configuration register. Persistent write of the configuration register which is used for initialization after reset.
1:4	P	VAUXCFG	-	auxiliary supply configuration register.

Table 29. SPI VAUXR command: read auxiliary supply configuration

Byte	Access	Command/Data	Value	Description
0	W	VAUXR	E7h	prepares a read auxiliary supply register. To read the auxiliary supply configuration register value, use RDR.

Table 30. SPI auxiliary supply configuration

Bits	Access	Field	Value	Description
31:17	-	-	-	(reserved)
16	R/W/P	VAUXEN	(0b)	auxiliary supply enable.
		VAUXEN_DIS	0b	disabled.
		VAUXEN_EN	1b	enabled.
15	R/W/P	VAUXBY	(0b)	auxiliary supply bypass mode.
		VAUXBY_DIS	0b	disabled.
		VAUXBY_EN	1b	enabled.
14	R/W/P	VAUXRATIO	(0b)	auxiliary supply ratio setting.
			0b	ratio 2
			1b	ratio 3
13	-	-	-	(reserved)
12:11	R/W/P	VAUXDS	(00b)	auxiliary supply drive strength.
			00b	1/4 of drive strength.
			01b	2/4 of drive strength.
			10b	3/4 of drive strength.
			11b	4/4 of drive strength.
10:8	R/W/P	VAUXDF	(000b)	auxiliary supply clock divider.
			000b	maximum clock speed
			001b	clock divided by 2
			010b	clock divided by 4
			011b	clock divided by 8
			100b	clock divided by 16
			101b	clock divided by 32
			110b	clock divided by 64
			111b	clock divided by 128
7	R/W/P	VAUXREG	(0b)	auxiliary supply enable voltage regulation
			0b	disabled (open loop).
			1b	enabled (closed loop).
6:0	R/W/P	VAUXV	(0b)	auxiliary supply comparator mode.
			00h	minimum (1.5 V)
			7Fh	maximum (3.3 V)

Remark: Details of the V_{aux} principle and operation can be found in the separate application data note: V_{AUX} - Auxiliary voltage supply ([Ref. 2](#)).

6.4 Supply mode

There are two V_{DD} supply modes available. The Wide Range Supply pin (WRS) selects the supply mode.

If the supplied V_{DD} of the device is a regulated voltage always above 1.65 V, it is possible to use the Fixed High Supply (FHS) mode. In this mode, the DC-to-DC converter that is used to generate the EEPROM array voltage ($V_{DD(EE)}$) is bypassed. The rise time of this supply is hence almost instantaneous, reducing the overall start-up time of the device by approximately 1.5 ms. For the actual values, refer to [Section 9](#). To select the Fixed High Supply mode, the WRS pin must be connected to GND.

If the minimum supplied V_{DD} of the device cannot be guaranteed to be above 1.65 V, the Wide Range Supply mode can be used. To select the Wide Range Supply mode, the WRS pin must be connected to $V_{DD(EO)}$.

6.5 Error-correcting code

The NXH5104 features an Error-Correcting Code (ECC) to improve reliability. It provides six parity bits for every 32 data bits so that a 38-bit word in memory represents four data bytes internally. Single bit read errors within a word are corrected.

Since the NXP NXH5104 supports byte level access, it is only allowed to write part of the four data bytes that make up a word. However, if a partial word is modified, the entire word is updated and endures a program cycle. To benefit from the qualified endurance optimally (500000 program cycles), write entire words (multiples of 4 bytes at word boundaries) within a single transaction.

6.6 Current measurements

The most interesting modes impacting the current consumption of the NXP NXH5104 are the READ and the WRITE mode. Measurements performed for these modes are shown in this section. The current has been measured using a differential voltage amplifier across the 10 Ω resistor, as shown in the schematic. The scale for all following graphs is 1 mA / division.

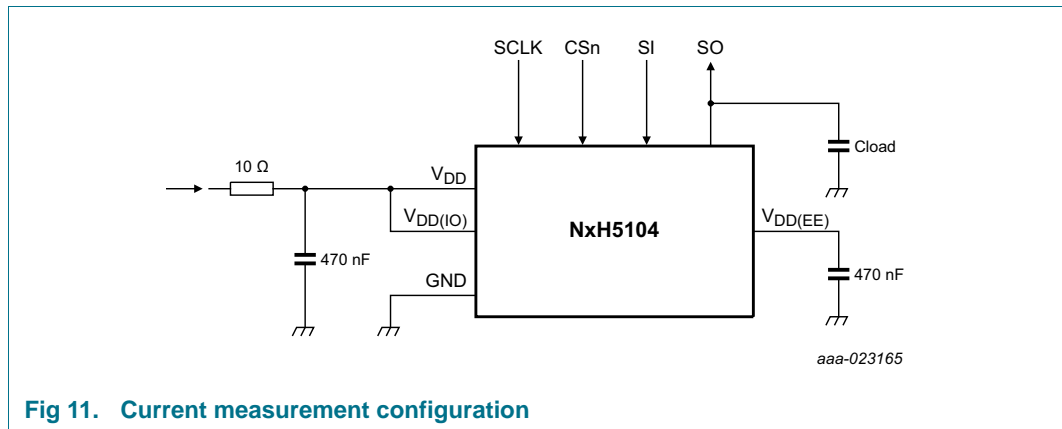
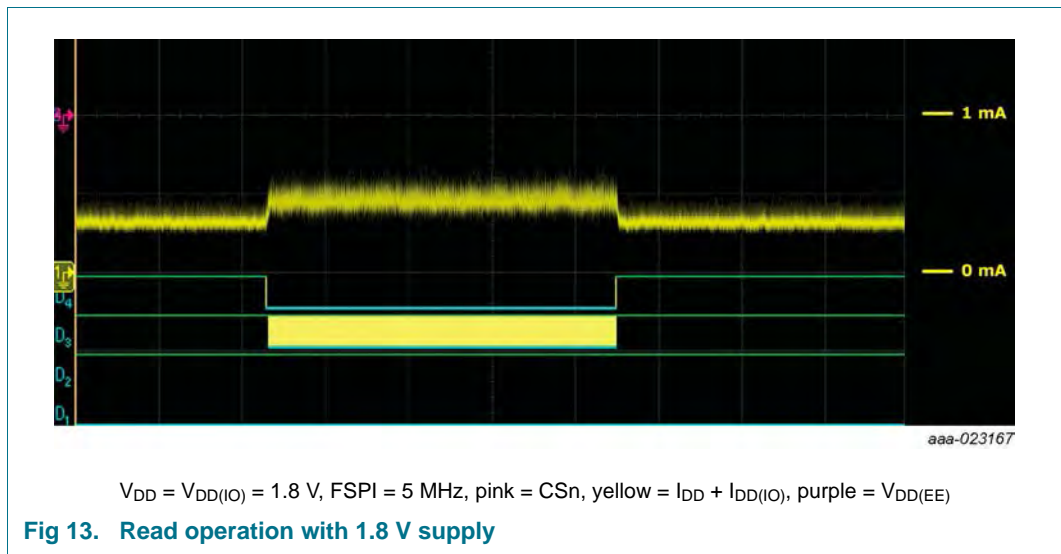
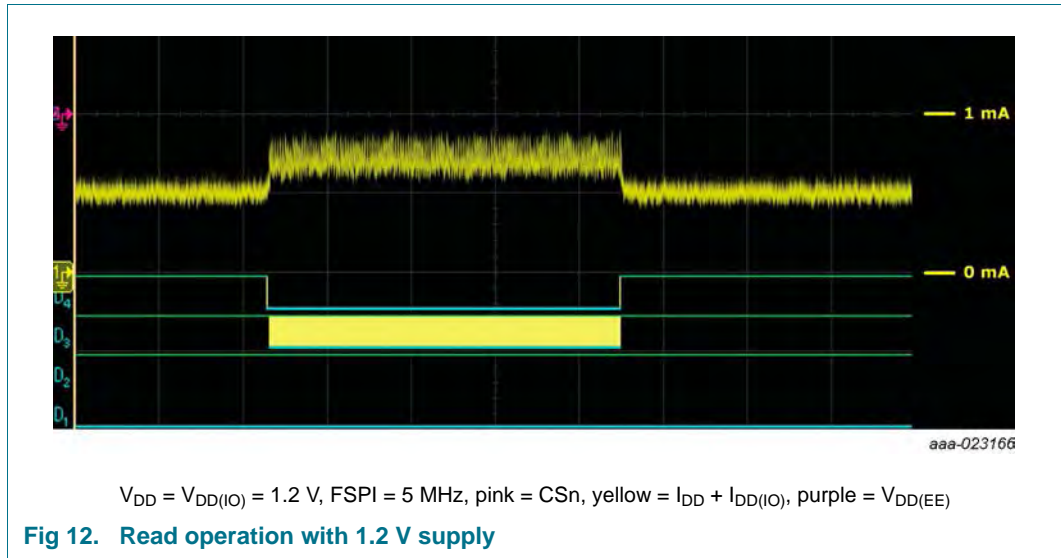


Fig 11. Current measurement configuration

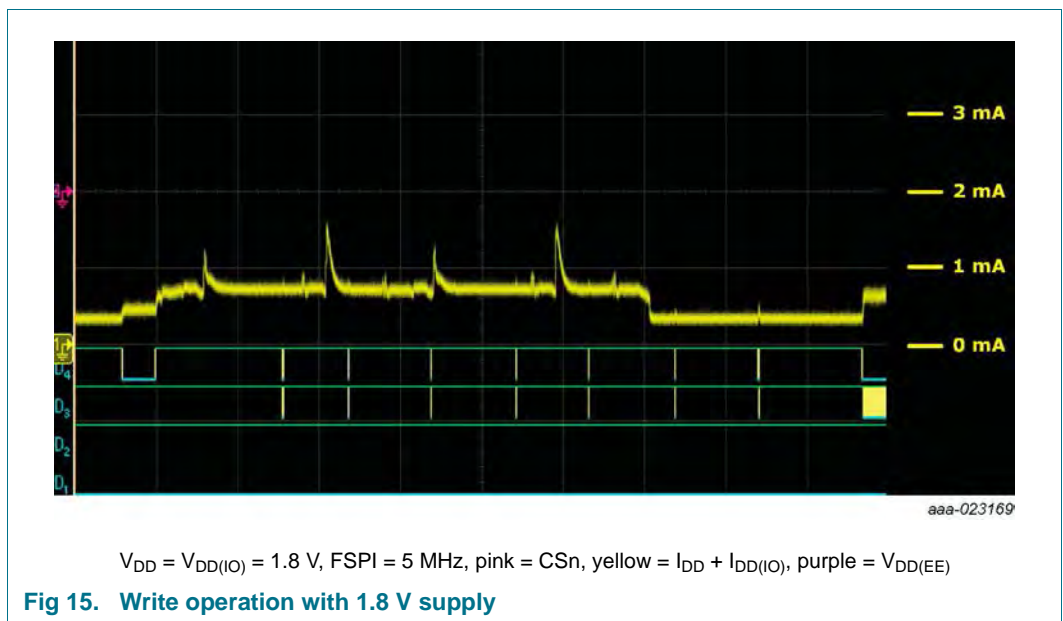
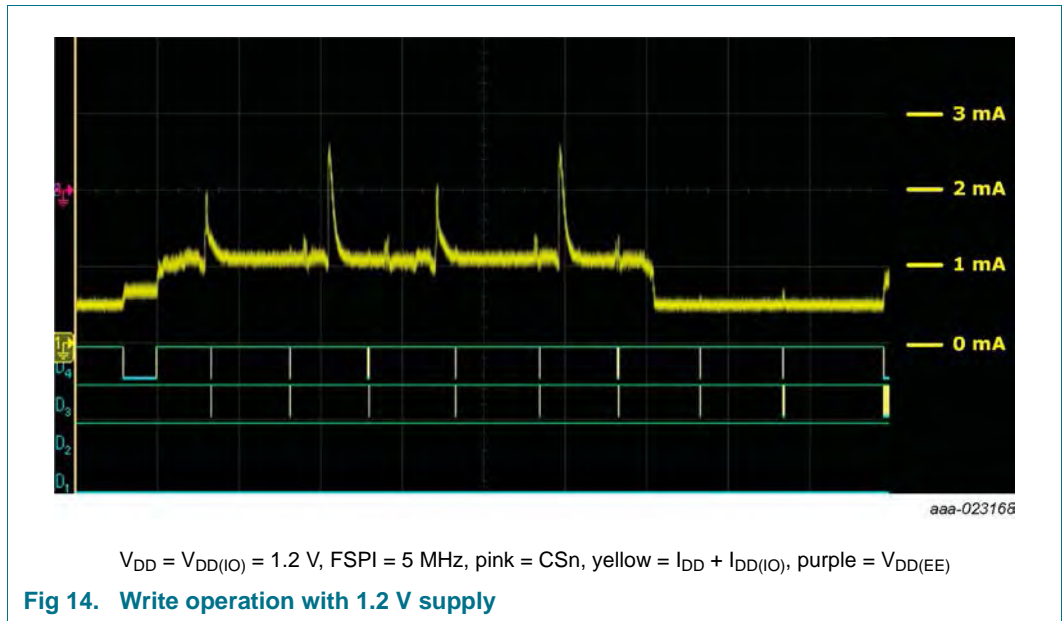
6.6.1 Read

The following graphs depict a READ operation, with varying levels of supply. Take note that the capacitive load (C_{load}) on the SO line dominates $I_{DD(IO)}$.



6.6.2 Write

The following graphs depict a WRITE operation, with varying levels of supply.



7. Limiting values

Table 31. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-50	+150	°C
V _{DD}	supply voltage	[1]	-0.5	+2.4	V
V _{DD(I/O)}	input/output supply voltage		-0.5	+5.2	V
V _{aux}	auxiliary voltage		-0.5	+5.2	V
V _{ESD}	electrostatic discharge voltage	human body model [2]	-	2	kV
		charged device model [3]	-	500	V
I _{lu}	latch-up current	[4]	-	±100	μA

[1] Maximum voltage for a lifetime of 1 hour at 60 °C, with 0.01 % failure rate and 95 % confidence bound.

[2] In accordance with JESD22-A114.

[3] In accordance with JESD22-C101.

[4] In accordance with JESD78.

7.1 Recommended operating conditions

Table 32. Operating conditions[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{oper}	operating temperature		-20	+25	+85	°C
V _{DD}	supply voltage	[2]	1.0	1.2	2.0	V
V _{DD(I/O)}	input/output supply voltage		1.0	V _{DD}	2.6	V
V _{DD(I/O)(1V2)}	input/output supply voltage (1.2 V)	1.2 V signaling	1.08	1.2	1.9	V
V _{DD(I/O)(1V8)}	input/output supply voltage (1.8 V)	1.8 V signaling	1.62	1.8	2.6	V

[1] V_{DD(I/O)} must always be equal to, or higher than, V_{DD}.

[2] During the READ and WRITE command execution the V_{DD} is allowed to dip to 0.9 V.

8. Static characteristics

Table 33. Static characteristics-1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Auxiliary supply						
V _{aux}	auxiliary voltage	regulation range	1.5	1.8	3.3	V
		regulation step	-	3.75	-	mV
I _{aux(ext)}	external auxiliary current	standby/active mode	-	0.75	2.0	mA
		pass-through mode	-	-	2.0	mA

Table 34. Static characteristics-2^[1]

Symbol	Parameter	Conditions	1.2 V		1.8 V		Unit
			Typ	Max	Typ	Max	
I _{DD(pd)}	average power-down supply current		-	5	-	5	μA
I _{DD(sleep)}	average sleep supply current		80	-	70	-	μA
I _{DD(stb)}	average standby supply current	all sectors powered down ^[2]	400	-	350	-	μA
		4 sectors active ^[2]	635	-	475	-	μA
		all sectors active ^[2]	870	-	600	-	μA
I _{DD(RW)}	average read supply current	4 sectors active and 5 MHz SPI ^[2]	800	-	600	-	μA
I _{DD(prog)}	average write supply current	4 sectors active and 5 MHz SPI ^[2]	1.1	-	0.7	-	mA

[1] Current from V_{DD}, excluding external current sourced through supply or I/O pads.

[2] Sectors powered down according to the SPD field in the External Status Register (XSR).

[3] With recommended supply decoupling of 470 nF.

Table 35. Static characteristics-3

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages and currents						
V _{DD(EEPROM)}	EEPROM supply voltage		1.5	1.6	2.0	V
Input characteristics^[1]						
V _{IH}	HIGH-level input voltage		0.7 × V _S	-	2.6	V
V _{IL}	LOW-level input voltage		-0.5	-	+0.3 × V _S	V
V _{hys}	hysteresis voltage		0.1 × V _S	-	-	V
Output characteristics 1.2 V signaling						
I _{OH}	HIGH-level output current	current sourcing capability; V _{OH} = 0.8 × V _{DD(IO)(1V2)}	2.0	-	-	mA
I _{OL}	LOW-level output current	current sinking capability; V _{OL} = 0.2 × V _{DD(IO)(1V2)}	2.0	-	-	mA
Output characteristics 1.8 V signaling						
I _{OH}	HIGH-level output current	current sourcing capability; V _{OH} = 0.8 × V _{DD(IO)(1V8)}	4.0	-	-	mA
I _{OL}	LOW-level output current	current sinking capability; V _{OL} = 0.2 × V _{DD(IO)(1V8)}	4.0	-	-	mA

[1] For WAKE pin and WRS pin, V_S = V_{DD}. For all other I/Os, V_S = V_{DD(IO)}.

9. Dynamic characteristics

Table 36. Dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output characteristics – 1.2 V signaling						
$t_{r(io)}$	input/output rise time		[1] 1.0	-	10	ns
$t_{f(io)}$	input/output fall time		[1] 1.0	-	10	ns
Output characteristics 1.8 V signaling						
$t_{r(io)}$	input/output rise time		[1] 1.0	-	10	ns
$t_{f(io)}$	input/output fall time		[1] 1.0	-	10	ns
Input characteristics						
f_{SPI}	SPI frequency	1.2 V signaling	[2] 5	-	-	MHz
		1.8 V signaling	[2] 10	-	-	MHz
Reliability						
$N_{endu(W)}$	write endurance	number of program cycles	[3] 500 000	-	-	cycles
$t_{ret(data)}$	data retention time		10	-	-	years
Input characteristics						
t_{prog}	programming time	full 256 Byte sector	[4] -	6.4	-	ms
		half sector	-	3.7	-	ms
$t_{wake(pd)}$	power-down mode wake-up time	Wide Range Supply mode	-	5	-	ms
		Fixed High Supply mode	-	3.5	-	ms
$t_{wake(sleep)}$	sleep mode wake-up time		-	500	-	μ s

[1] 5 nH bond wire inductance and 15 pF external capacitive load.

[2] $V_{DD} > 1.0$ V.

[3] Endurance qualified at word level (4 bytes).

[4] The programming time is consisting out of an erase cycle followed by a program cycle. To guarantee the endurance, an adaptive trimming algorithm could retry erasing, which leads to a longer programming time. The typical value given is for a programming time without erase retry. Very rarely (on average once in 200 000 write operations) such an additional erase/program cycle is performed, which increases the programming time to 11.3 ms. The user is strongly advised to use the available control flow. This control flow always provides the shortest access time by polling completion of the programming operation by using the RDSR command.

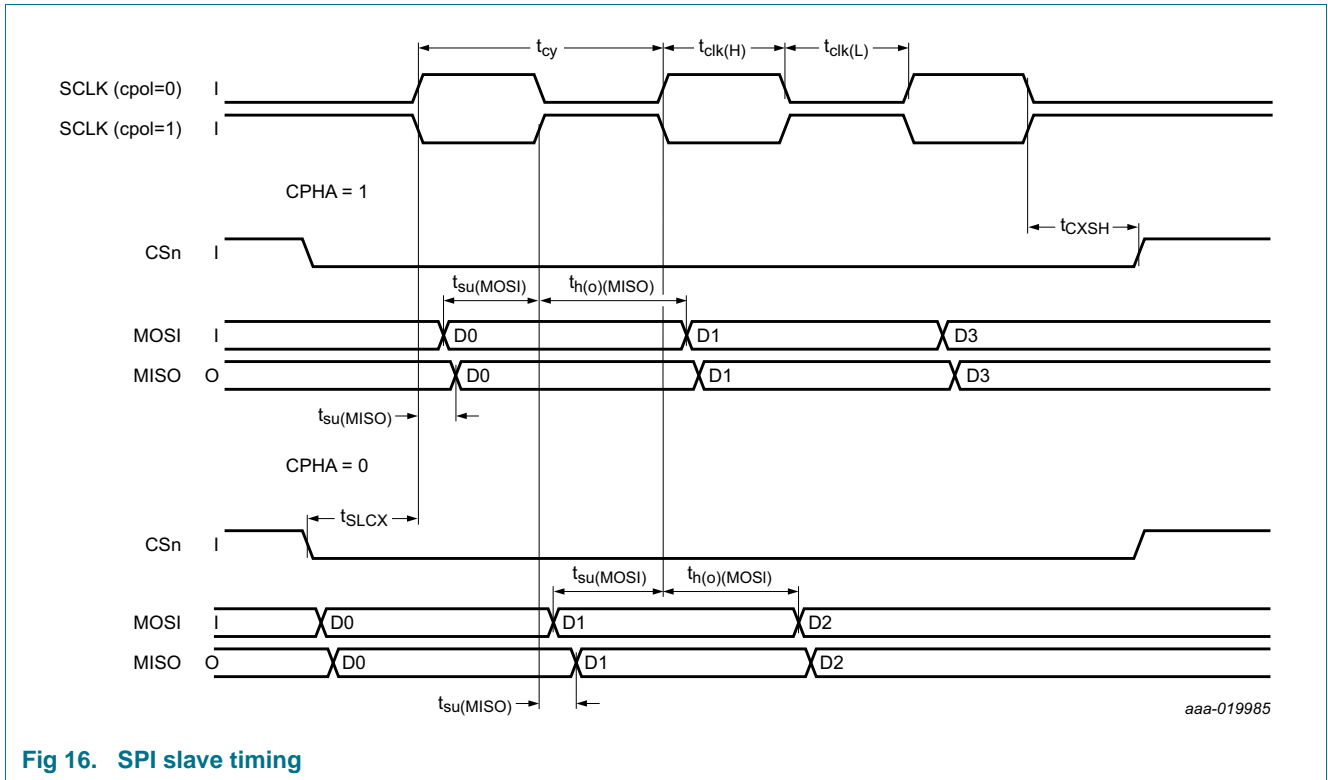


Fig 16. SPI slave timing

Table 37. SPI slave timing - 1.8 V signaling level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy}	cycle time	$V_{DD(IO)} = 1.8\text{ V}$, $C_{LOAD} = 4\text{ pF}$	100	-	-	ns
$t_{clk(H)}$	clock HIGH time		50	-	-	ns
$t_{clk(L)}$	clock LOW time		50	-	-	ns
t_{su}	set-up time	To the rising edge of PCLK. MOSI	20	-	-	ns
$t_{h(o)}$	output hold time	MOSI	20	-	-	ns
$t_{d(o)}$	output delay time	MISO	-	-	22.5	ns
t_{SLCX}	chip select LOW to clock changing		50	-	-	ns
t_{CXSH}	clock changing to chip select HIGH		50	-	-	ns

Table 38. SPI slave timing - 1.2 V signaling level

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{cy}	cycle time	$V_{DD(10)} = 1.2\text{ V}$, $C_{LOAD} = 4\text{ pF}$	200	-	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	-	ns
$t_{clk(L)}$	clock LOW time		100	-	-	ns
t_{su}	set-up time	To the rising edge of PCLK. MOSI	20	-	-	ns
$t_{h(o)}$	output hold time	MOSI	20	-	-	ns
$t_{d(o)}$	output delay time	MISO	-	-	64.0	ns
t_{SLCX}	chip select LOW to clock changing		100	-	-	ns
t_{CXSH}	clock changing to chip select HIGH		100	-	-	ns

10. Application information

The primary supply input (V_{DD}) accepts a voltage in range 1.0 V to 2.0 V and supports battery powered operation with various battery chemistries. Three configurations are demonstrated to connect the Input/Output supply ($V_{DD(I/O)}$).

The auxiliary supply (V_{aux}) is available as an independent, configurable supply for auxiliary components.

In the following application diagrams, a 470 nF decoupling capacitor is proposed for decoupling V_{DD} and $V_{DD(I/O)}$. This value is not strictly mandatory, another value may be chosen depending on the system integration.

10.1 Configuration 1 - Wide range single supply

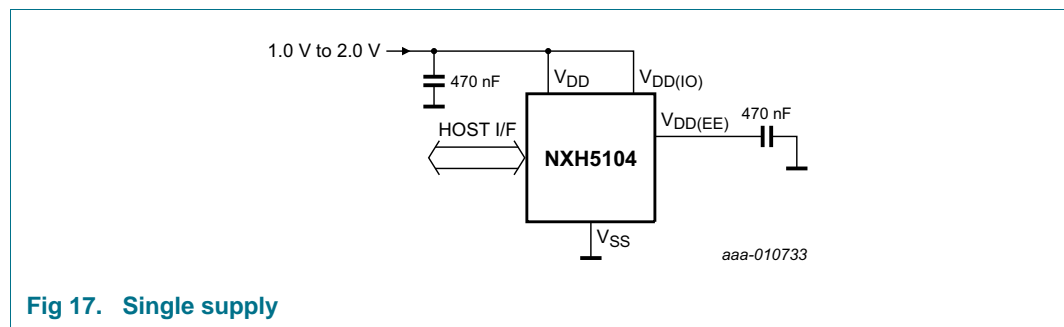


Fig 17. Single supply

According to application configuration 1 (Figure 17), the Input/Output signaling voltage ($V_{DD(I/O)}$) can equal the primary supply. It enables single supply operation according to the specified voltage range.

10.2 Configuration 2 - Wide range dual supply

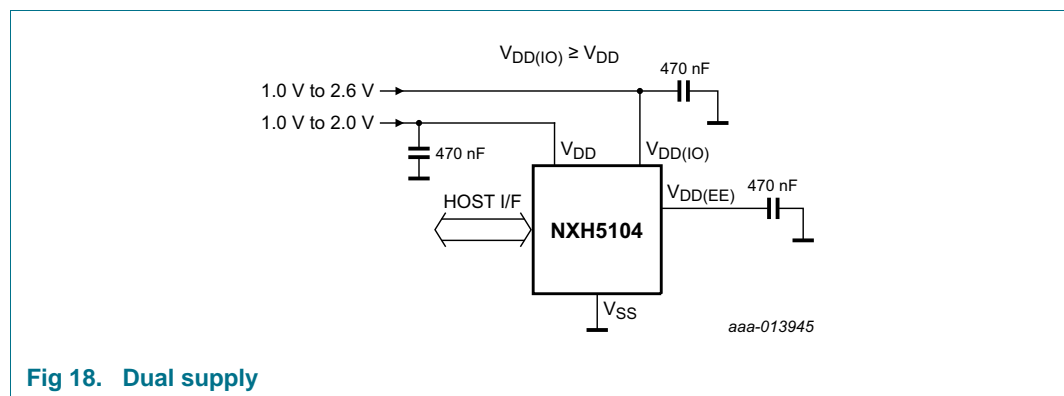


Fig 18. Dual supply

For configuration 2 (Figure 18), the I/O supply is different from the primary supply. The primary supply is typically connected to the battery.

The I/O supply can be disabled while the primary supply stays powered. The I/O supply should be valid as long as the device is not powered down.

10.3 Configuration 3 - Fixed high supply mode

If V_{DD} is $>1.65\text{ V}$ in the WRS mode, configurations 1 (Figure 17) and 2 (Figure 18) can be used. In this case, capacitor C1 is not required.

If V_{DD} is a regulated voltage always above 1.65 V , it is possible to use the WRS mode. In this mode, the DC-to-DC converter used to generate the V_{EE} voltage is bypassed. For this reason, the rise of this supply is almost instantaneous, reducing the overall start-up time of the device by approximately 1.5 ms . For the actual values, refer to Section 9.

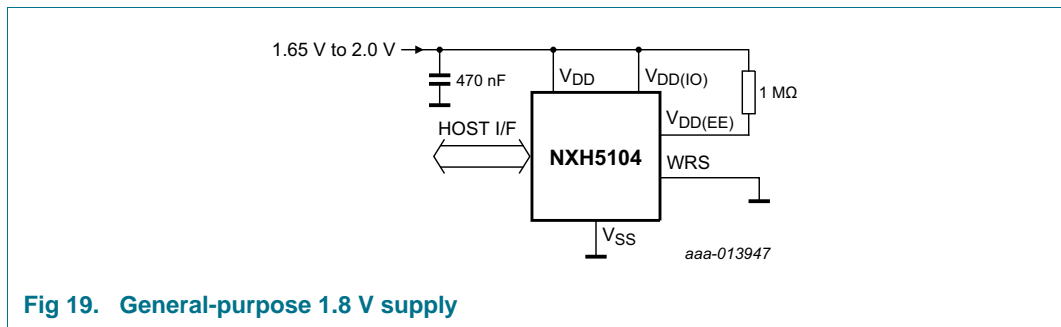


Fig 19. General-purpose 1.8 V supply

10.4 Configuration 4 - Auxiliary supply feeding $V_{DD(IO)}$

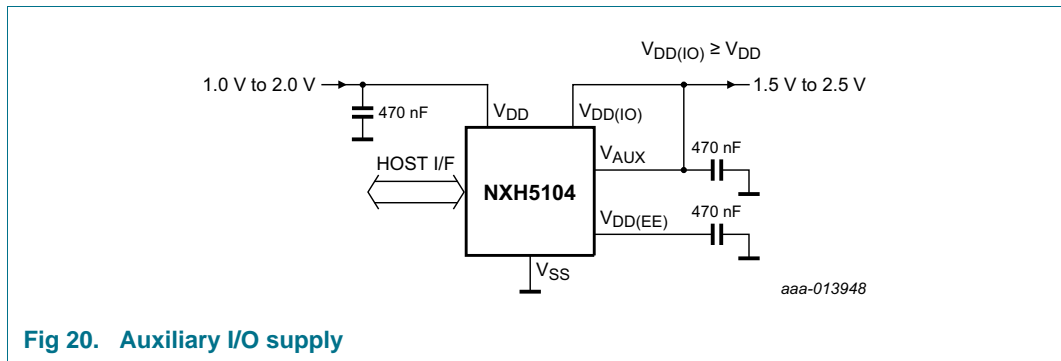


Fig 20. Auxiliary I/O supply

In this configuration, the auxiliary output V_{aux} can be used to feed $V_{DD(IO)}$. The V_{aux} output needs a 470 nF decoupling capacitor.

10.5 Application diagram - driving an LED

Figure 21 shows the application diagram for driving an LED. An additional capacitor may be required between V_{aux} and ground, depending on the application.

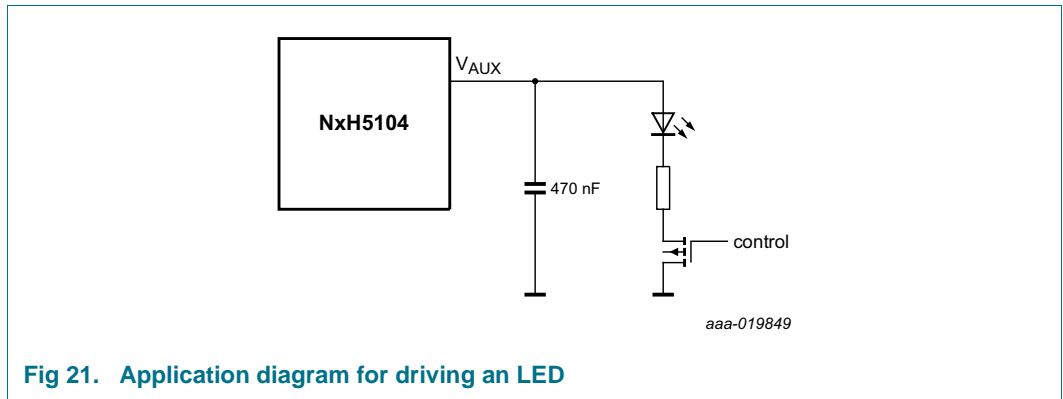


Fig 21. Application diagram for driving an LED

11. Packing information

Default packing for the WLCSP devices is tape and reel according to T1 taping orientation as depicted below.

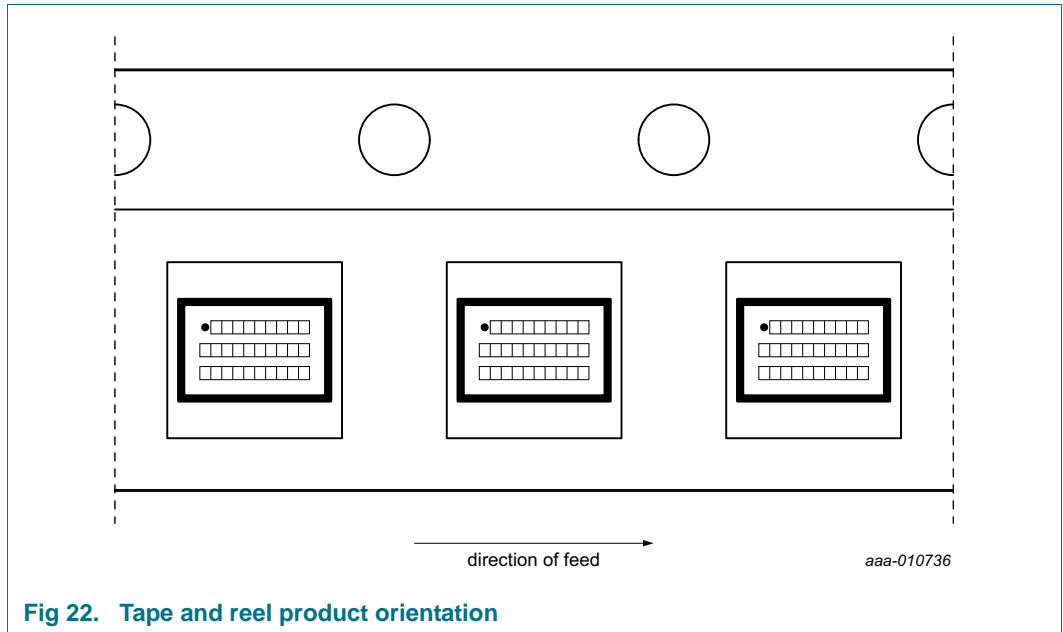


Fig 22. Tape and reel product orientation

Table 39. Die marking

Line	Description	Example
A	Device	NxH5104A1
B	Lot number - Wafer number	P6T659-03
C	Fab - year - week	E TDyyww
D	X-Y coordinates	03 xxx yyyy

11.1 Physical specification

Table 40. Physical specification

Item	Specification	Remark
Solder bump	Material	Plating: SnAg1.8
		Lead-free

12. Package outline

WLCSP13: wafer level chip-scale package; 13 bumps; 2.74 x 2.80 x 0.38 mm

SOT1461-1

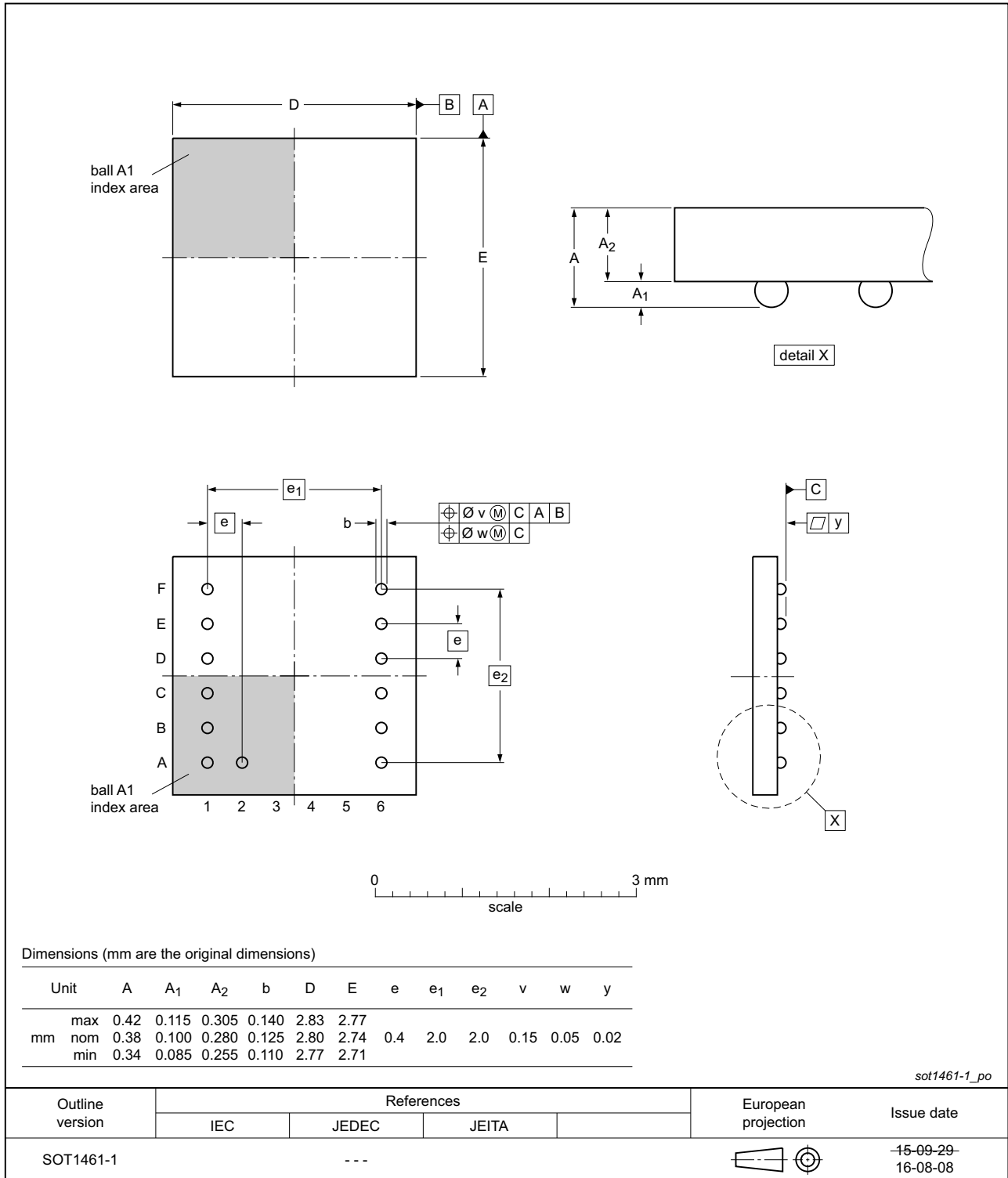


Fig 23. Package outline SOT1461-1 (WLCSP13)

13. Handling information

See [Ref. 1](#) for detailed instructions on handling, soldering and mounting WLCSP packaged devices.

14. Abbreviations

Table 41. Abbreviations

Acronym	Description
EEPROM	Electrically Erasable and Programmable Read Only Memory.
EOC	Extended Operation Command
LDO	Low DropOut regulator.
RoHS	Restriction of Hazardous Substances (Directive 2002/95/EC).
SPI	Serial Peripheral Interface.
SR	Status Register
WLCSP	Wafer Level Chip Scale Package.
WOSR	Wear-Out Status Register
XSR	Extended Status Register

15. References

- [1] **AN11761** — Flip chip
- [2] **AN11660** — V_{AUX} - Auxiliary voltage supply

16. Revision history

Table 42. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXH5104 v.6.1	20170308	Product data sheet	-	NXH5104 v.6
Modifications:	<ul style="list-style-type: none"> • Section 3 “Ordering information” has been updated. • Section 12 “Package outline” has been updated. • Section 15 “References” has been updated. 			
NXH5104 v.6	20170111	Product data sheet	-	NXH5104 v.5
Modifications	<ul style="list-style-type: none"> • Addition to section describing SPI write protection • Data sheet promoted to Product 			
NXH5104 v.5	201609289	Objective data sheet	-	NXH5104 v.4
Modifications	<ul style="list-style-type: none"> • Reference [1] changed • POD updated • Security status changed to Company Public 			
NXH5104 v.4	20160805	Objective data sheet	-	NXH5104 v.3
NXH5104 v.3	20151110	Objective data sheet	-	NXH5104 v.2
NXH5104 v.2	20141211	Objective data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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