

TWR-SMPS-LVFB User's Guide

1 Overview

The Low-Voltage Full-Bridge DC-DC Switch Mode Power Supply Tower board (TWR-SMPS-LVFB) is a peripheral Tower System Module used as a development platform that enables rapid prototyping of various power-control topologies using Freescale MCUs. A variety of power-control topologies such as peak current mode control, average current mode control and voltage mode control can be implemented using the MC56Fx TWR-MC56F8xxx and KVx TWR-KVx MCU Tower System MCU / peripheral board. The dynamic load circuit module is also included in the system to test the performance of power-control topologies and demo software, by connecting a load resistor at the output.

The TWR-SMPS-LVFB module features:

- 20 – 30 VDC power supply voltage input (see [Section 3.2, “Electrical characteristics”](#) for details)
- Output current up to 8 A
- Power supply reverse polarity protection circuitry
- Full-bridge topology
- Synchronous rectification for secondary side

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Overview

- Primary side full-bridge current sensing
- Input DC-bus voltage sensing
- Output voltage sensing
- Low-voltage on-board power supplies
- Two user LEDs, power-on LED and six PWM LED diodes

A block diagram for the TWR-SMPS-LVFB is shown in [Figure 1](#).

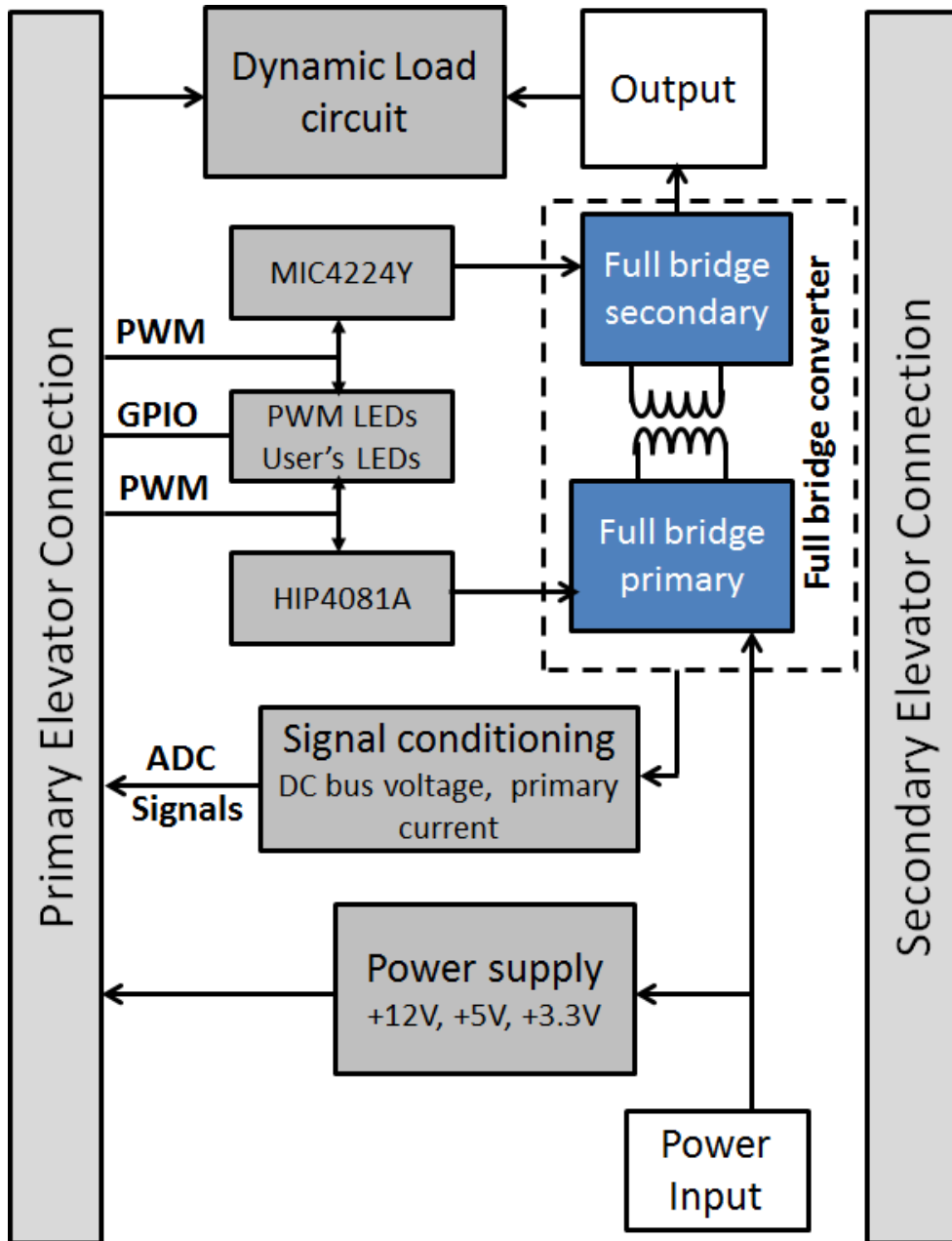


Figure 1. TWR-SMPS-LVFB block diagram

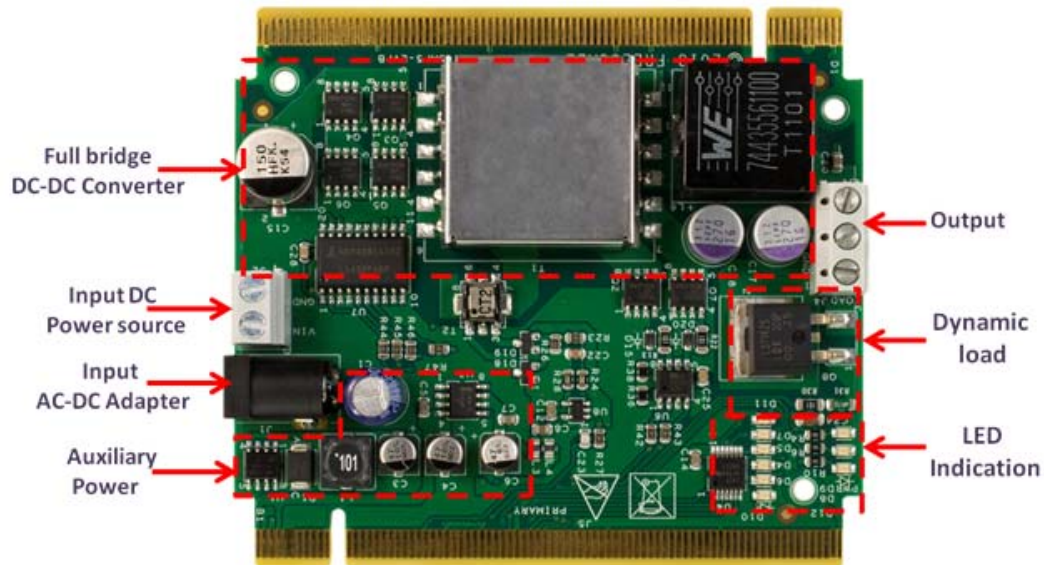


Figure 2. TWR-SMPS-LVFB component placement

2 Reference documents

The documents listed below may be referenced for more information on the Freescale Tower System and the TWR-SMPS- LVFB board:

- *TWR-SMPS-LVFB Schematics*
- *TWR-SMPS-LVFB Quick Start Guide*
- *Controller (56Fxxx/KV4xxx) TWR card Quick Start Guide*
- *Freescale embedded system library FSLESL*

Refer to freescale.com/tower for the latest versions of the Freescale Tower System documentation.

3 Hardware features

This section provides details about the hardware features and functionality of the TWR-SMPS-LVFB board.

3.1 Power supply

Freescale's TWR-SMPS-LVFB Tower board operates on DC input voltages of 20 – 30 V. The TWR-SMPS-LVFB is intended to be powered from an external AC-DC power supply of 24 V, 3 A output or DC power source which can provide 20 – 30 V output. All the needed auxiliary voltages for digital, analog and MOSFET drivers are derived from the input voltage. The module includes 12 V, 5 V and 3.3 V power supplies. The 12 V power supply is used to provide power to the PWM drivers, whereas the 5 V and 3 V power supplies are capable of providing power to the entire Tower System development board platform.

3.1.1 12 V power supply

The 12 V voltage is generated using the LM2594HVM switching step-down regulator. The input to the LM2594 is taken from the input voltage of the TWR-SMPS-LVFB board; it ranges from 20 to 30 V. This regulator can supply up to 500 mA. The 12 V power rail is used to supply power to the MC33269, full-bridge MOSFET driver (HIP4081AIBZ) and synchronous MOSFET driver (MIC4224YM).

3.1.2 5 V power supply

The 5 V voltage is generated from the linear regulator MC33269D, input to the MC33269D is taken from the 12 V supply. This converter can supply up to 800 mA. The linear regulator is used for simplicity of the board design.

3.1.3 3.3 V power supply

The 3.3 V voltage is generated from the MC33269D linear voltage regulator and can supply up to 800 mA. The 3.3 V power rail is important as it is used for both analog and digital circuits. This power rail is also used to lit LEDs. The linear regulator is used for simplicity of the board design.

3.1.4 Analog power supply and grounding

The separated 3.3 V analog voltage and the ground plane are used to sense analog quantities (currents and voltages). This voltage level is generated from the 3.3 V digital power supply using the LC filter. The LC filter is used to derive analog to clean the power rail from digital noise.

3.2 Electrical characteristics

The electrical characteristics listed in [Table 1](#) apply to operation at 25°C with 24 VDC power-supply voltage. The maximal input voltage cannot be higher than 30 V. Only 30 V maximal input voltage is allowed.

CAUTION

If an input voltage higher than 30 V is applied, the plugged-in Tower modules might be damaged.

Table 1. Electrical characteristics

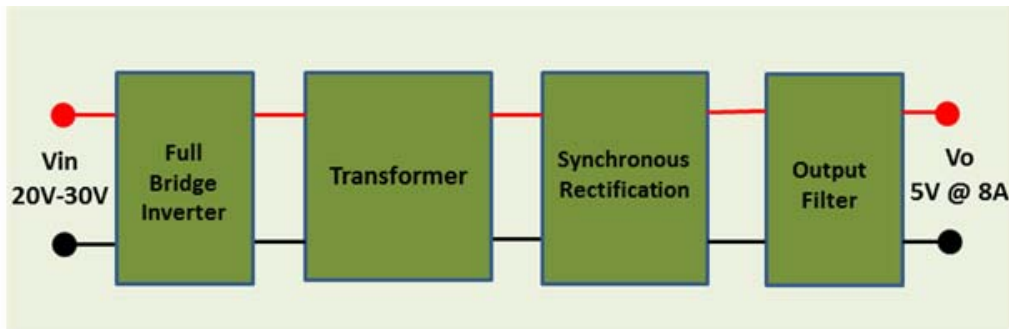
| Characteristics | Symbol | Min. | Typ. | Max. | Units |
|------------------------------|-----------------|------|------|------|--------|
| DC input voltage | V _{in} | 20 | 24 | 30 | V |
| Quiescent current | I _{cc} | – | 220 | – | mA |
| Output voltage range | V _o | – | 5 | – | V |
| Continuous output current | I _o | 0 | – | 8 | A |
| Current sense voltage | I_IN_SENSE | – | 730 | – | mV / A |
| Output voltage sense voltage | VO_SENSE | – | 500 | – | mV / V |
| Output voltage sense voltage | VIN_SENSE | – | 100 | – | mV / V |

Table 1. Electrical characteristics (continued)

| Characteristics | Symbol | Min. | Typ. | Max. | Units |
|--|-----------|------|------|-------|---------|
| Power dissipation per MOSFET | P_{DD} | – | – | 300 | mW |
| Dead time (set by software) | t_{off} | – | – | 0.669 | μ s |
| Dynamic load circuit rise time (2 to 6 A load current) | t_r | – | 600 | – | μ s |
| Dynamic load circuit fall time (6 to 2 A load current) | t_f | – | 600 | – | μ s |

3.3 Full-bridge DC-DC converter

The full-bridge DC-DC converter is a transformer-isolated buck converter. The full-bridge topology contains full-bridge inverter block, transformer, synchronous rectification block, and filter, as shown in Figure 3. The full-bridge inverter block converts the DC input into high frequency AC (frequency used in this design is 150 KHz). The transformer brings the high-frequency AC voltage in level with the output voltage. The secondary side high-frequency AC is rectified to DC through the synchronous rectification. Finally, the LC filter reduces the ripples in the DC voltage to get a final stable DC output. The output voltage is 5 V and it can deliver up to 8 A of load current. Input voltage range is 20 – 30 V DC.


Figure 3. Full-bridge DC-DC converter topology block diagram

3.4 Feedback circuits

The feedback circuits scale down the high voltage / current to a safe low voltage and amplify the low voltage to a voltage permissible for the MCU to sense the power circuit physical quantity. The resistor divider network is used for the voltage feedback and current transformer with the load resistor is used for current feedback.

3.4.1 Output voltage feedback

The output voltage is scaled down by a resistor divider consisting of R33 and R35. The values are chosen in such a way that a 6.6 V output voltage corresponds to 3.3 V at the VO_SENSE output. The VO_SENSE is scaled at 500 mV per volt of the DC output voltage and is terminated on the main primary elevator port.

$$VO_SENSE = V_o \times (R35 / (R33 + R35))$$

where:

- V_o is the output voltage
- VO_SENSE is the corresponding output voltage at the ADC

3.4.2 Input voltage feedback

The input voltage is scaled down by a voltage divider consisting of R32 and R34. The values are chosen in such a way that a 33 V input voltage corresponds to 3.3 V at the VIN_SENSE output. The VIN_SENSE is scaled at 100 mV per volt of the DC input voltage and is terminated on the main primary elevator port.

$$VIN_SENSE = V_{in} \times (R34 / (R32 + R34))$$

where:

- V_{in} is the input voltage
- VIN_SENSE is the corresponding input voltage at the ADC

3.4.3 Full-bridge primary current feedback

The primary current of the full-bridge transformer is converted to scaled voltage by the current transformer (CT) followed by a diode rectifier and a load resistor. The voltage across the load resistor is amplified to get a full resolution of the ADC. The values of the current-sense circuit are chosen in such a way that a 4.5 A instantaneous current corresponds to 3.3 V at the I_IN_SENSE output. The I_IN_SENSE is scaled at 730 mV per 1 A of the primary current and is terminated on the main primary elevator port.

$$I_IN_SENSE = (I_{primary} \times R26 \times (R29 / R28)) / N$$

3.5 Dynamic load circuit

The dynamic load circuit contains a MOSFET and a user control gate driver circuitry to control the external load (resistor). The dynamic load circuit MOSFET connects the external power resistor to the output. The slew rate of the dynamic load and the ON and OFF time is controlled by controlling the gate drive pulse width of the MOSFET. The gate drive of the MOSFET is controlled by the controller (56Fxxx / KVxxxx) using PWM. The PWM of the gate drive is chosen in such a way that the dynamic load MOSFET can have controlled transition from resistive to active region. The slew rate of the output load is controlled by controlling the MOSFET transition time from the resistive to the active region. The ON and OFF time is controlled by keeping the MOSFET in active and inactive regions. The maximum slew rate is limited by the RC (that is $t_c = R30 \times C24$) time constant of the resistor and capacitor used at the gate of dynamic load MOSFET.

3.6 LED indication

This module also contains nine LED indicators. For more details on the LED position and its level please refer to the TWR-SMPS-LVFB schematic.

Table 2. LED indication

| LED | Description |
|-----|---|
| D4 | PWM_HSA indication LED |
| D5 | PWM_LSB indication LED |
| D6 | PWM_LSA indication LED |
| D7 | PWM_SYNCA indication LED |
| D8 | Fault indicator (input under-voltage) |
| D9 | Fault indicator (input over-voltage) |
| D10 | PWM_HSB indication LED |
| D11 | PWM_SYNCB indication LED |
| D12 | Indicates that the +3.3 V level is properly generated |

4 Hardware connection description

This section provides more details about signals of input / output connectors and Tower-elevator connections of the TWR- SMPS-LVFB board.

4.1 Adapter input connector J1

If the AC-DC power supply adapter is used as input source, it is connected to the J1 connector. A 24 V, 3 A, AC-DC adapter is used as the input source.

4.2 Power supply input connector J2

If a DC power supply is used as the input source it is connected to the J2 connector with the positive terminal of the power supply being connected to pin 2 and ground connected to pin 1. The input voltage range is 20 – 30 VDC. The connectors J1 and J2 are both parallel, hence make sure that only one input source is used at a given time.

4.3 Load connector J4

The J4 is a three-pin connector. For application demonstration purposes, two power resistors (2.5 Ω and 1.2 Ω) are used as a load. The power resistor for continuous load is connected across pins 3 and 2, and for dynamic load, it is connected across pins 3 and 1. The value of the power resistor is chosen in such a way that the total current drawn from the 5 V DC output should not be higher than 8 A.

In case an electronic load is used, it should be connected across pins 3 and 2 with positive terminal at pin 3 and ground at pin 2.

4.4 Elevator connections

The TWR-SMPS-LVFB board features two expansion-card edge connectors that interface to the elevator boards in the Tower system: the primary and secondary elevator connectors. [Table 3](#) and [Table 4](#) provide the pinouts for the primary and secondary elevator connectors respectively. An “X” in the “Used” column indicates that there is a connection from the TWR-SMPS-LVFB to that pin on the elevator connector.

Table 3. TWR-SMPS-LVFB primary elevator connector pinout

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|----------------------|----------------------|------|-----|-------------------|-------------|------|
| B1 | 5V | 5 V Power | X | A1 | 5V | 5 V Power | X |
| B2 | GND | Ground | X | A2 | GND | Ground | X |
| B3 | 3.3V | 3.3 V Power | X | A3 | 3.3V | 3.3 V Power | X |
| B4 | ELE_PS_SENSE | Elevator Power Sense | X | A4 | 3.3V | 3.3 V Power | X |
| B5 | GND | Ground | X | A5 | GND | Ground | X |
| B6 | GND | Ground | X | A6 | GND | Ground | X |
| B7 | SDHC_CLK / SPI1_CLK | – | | A7 | SCL0 | – | |
| B8 | SDHC_D3 / SPI1_CS1_b | – | | A8 | SDA0 | – | |
| B9 | SDHC_D3 / SPI1_CS0_b | – | | A9 | GPIO9 / CTS1 | – | |
| B10 | SDHC_CMD / SPI1_MOSI | – | | A10 | GPIO8 / SDHC_D2 | – | |
| B11 | SDHC_D0 / SPI1_MISO | – | | A11 | GPIO7 / SD_WP_DET | – | |
| B12 | ETH_COL | – | | A12 | ETH_CRS | – | |
| B13 | ETH_RXER | – | | A13 | ETH_MDC | – | |
| B14 | ETH_TXCLK | – | | A14 | ETH_MDIO | – | |
| B15 | ETH_TXEN | – | | A15 | ETH_RXCLK | – | |
| B16 | ETH_TXER | – | | A16 | ETH_RXDV | – | |
| B17 | ETH_TXD3 | – | | A17 | ETH_RXD3 | – | |
| B18 | ETH_TXD2 | – | | A18 | ETH_RXD2 | – | |
| B19 | ETH_TXD1 | – | | A19 | ETH_RXD1 | – | |
| B20 | ETH_TXD0 | – | | A20 | ETH_RXD0 | – | |
| B21 | GPIO1 / RTS1 | – | | A21 | SSI_MCLK | – | |
| B22 | GPIO2 / SDHC_D1 | – | | A22 | SSI_BCLK | – | |
| B23 | GPIO3 | – | | A23 | SSI_FS | – | |
| B24 | CLKIN0 | – | | A24 | SSI_RXD | – | |

Table 3. TWR-SMPS-LVFB primary elevator connector pinout (continued)

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|-------------------------|-----------|------|-----|------------------------|-------------|------|
| B25 | CLKOUT1 | – | | A25 | SSI_TXD | – | |
| B26 | GND | Ground | X | A26 | GND | Ground | X |
| B27 | AN7 | – | | A27 | AN3 | – | |
| B28 | AN6 | – | | A28 | AN2 | – | |
| B29 | AN5 | – | | A29 | AN1 | VIN_SENSE | X |
| B30 | AN4 | – | | A30 | AN0 | I_IN_SENSE | X |
| B31 | GND | – | | A31 | GND | Ground | X |
| B32 | DAC1 | – | | A32 | GPIOC5 | OV_MCU | X |
| B33 | TMR3 | – | | A33 | TMR1 | UV_MCU | X |
| B34 | TMR2 | – | | A34 | TMR0 | – | |
| B35 | ANB7 | VO_SENSE | X | A35 | GPIO6 | – | |
| B36 | 3.3V | – | | A36 | 3.3V | 3.3 V Power | X |
| B37 | PWM7 | – | | A37 | PWM3 | PWM_LSB | X |
| B38 | PWM6 | LOAD_CTRL | X | A38 | PWM2 | PWM_LSA | X |
| B39 | PWM5 | PWM_SYNCA | X | A39 | PWM1 | PWM_HSB | X |
| B40 | PWM4 | PWM_SYNCB | X | A40 | PWM0 | PWM_HSA | X |
| B41 | CANRX0 | – | | A41 | RXD0 | – | |
| B42 | CANTX0 | – | | A42 | TXD0 | – | |
| B43 | 1WIRE | – | | A43 | RXD1 | – | |
| B44 | SPI0_MISO (IO1) | – | | A44 | TXD1 | – | |
| B45 | SPI0_MOSI (IO0) | – | | A45 | VSS | AGND | X |
| B46 | SPI0_CS0_b | – | | A46 | VDDA | VDDA_3V3 | X |
| B47 | SPI0_CS1_b | – | | A47 | VREFA1 | – | |
| B48 | SPI0_CLK | – | | A48 | VREFA2 | – | |
| B49 | GND | Ground | X | A49 | GND | Ground | X |
| B50 | SCL1 | – | | A50 | GPIO14 | – | |
| B51 | SDA1 | – | | A51 | GPIO15 | – | |
| B52 | GPIO5 / SPI0_HOLD (IO3) | – | | A52 | GPIO16 / SPI0_WP (IO2) | – | |
| B53 | USB0_DP_PDOWN | – | | A53 | GPIO17 | – | |
| B54 | USB0_DM_PDOWN | – | | A54 | USB0_DM | – | |
| B55 | IRQ_H | – | | A55 | USB0_DP | – | |
| B56 | IRQ_G | – | | A56 | USB0_ID | – | |

Table 3. TWR-SMPS-LVFB primary elevator connector pinout (continued)

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|---------------------|-------------|------|-----|-----------|-------------|------|
| B57 | IRQ_F | – | | A57 | USB0_VBUS | – | |
| B58 | IRQ_E | – | | A58 | TMR7 | – | |
| B59 | IRQ_D | – | | A59 | TMR6 | – | |
| B60 | IRQ_C | – | | A60 | TMR5 | – | |
| B61 | IRQ_B | – | | A61 | TMR4 | – | |
| B62 | IRQ_A | – | | A62 | RSTIN_b | – | |
| B63 | EBI_ALE / EBI_CS1_b | – | | A63 | RSTOUT_b | – | |
| B64 | EBI_CS0_b | – | | A64 | CLKOUT0 | – | |
| B65 | GND | Ground | X | A65 | GND | Ground | X |
| B66 | EBI_AD15 | – | | A66 | EBI_AD14 | – | |
| B67 | EBI_AD16 | – | | A67 | EBI_AD13 | – | |
| B68 | EBI_AD17 | – | | A68 | EBI_AD12 | – | |
| B69 | EBI_AD18 | – | | A69 | EBI_AD11 | – | |
| B70 | EBI_AD19 | – | | A70 | EBI_AD10 | – | |
| B71 | EBI_R/W_b | – | | A71 | EBI_AD9 | – | |
| B72 | EBI_OE_b | – | | A72 | EBI_AD8 | – | |
| B73 | EBI_D7 | – | | A73 | EBI_AD7 | – | |
| B74 | EBI_D6 | – | | A74 | EBI_AD6 | – | |
| B75 | EBI_D5 | – | | A75 | EBI_AD5 | – | |
| B76 | EBI_D4 | – | | A76 | EBI_AD4 | – | |
| B77 | EBI_D3 | – | | A77 | EBI_AD3 | – | |
| B78 | EBI_D2 | – | | A78 | EBI_AD2 | – | |
| B79 | EBI_D1 | – | | A79 | EBI_AD1 | – | |
| B80 | EBI_D0 | – | | A80 | EBI_AD0 | – | |
| B81 | GND | Ground | X | A81 | GND | Ground | X |
| B82 | 3.3V | 3.3 V Power | X | A82 | 3.3V | 3.3 V Power | X |

Table 4. TWR-SMPS-LVFB Secondary Elevator connector pinout

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|-------------------------|--------|------|-----|-------------------------|--------|------|
| D1 | 5V | – | | C1 | 5V | – | |
| D2 | GND | Ground | X | C2 | GND | Ground | |
| D3 | 3.3V | – | | C3 | 3.3V | – | |
| D4 | ELE_PS_SENSE | – | | C4 | 3.3V | – | |
| D5 | GND | Ground | X | C5 | GND | Ground | |
| D6 | GND | Ground | X | C6 | GND | Ground | |
| D7 | SPI2_CLK | – | | C7 | SCL2 | – | |
| D8 | SPI2_CS1_b | – | | C8 | SDA2 | – | |
| D9 | SPI2_CS0_b | – | | C9 | GPIO25 | – | |
| D10 | SPI2_MOSI | – | | C10 | ULPI_STOP | – | |
| D11 | SPI2_MISO | – | | C11 | ULPI_CLK | – | |
| D12 | ETH_COL | – | | C12 | GPIO26 | – | |
| D13 | ETH_RXER | – | | C13 | ETH_MDC | – | |
| D14 | ETH_TXCLK | – | | C14 | ETH_MDIO | – | |
| D15 | ETH_TXEN | – | | C15 | ETH_RXCLK | – | |
| D16 | GPIO18 | – | | C16 | ETH_RXDV | – | |
| D17 | GPIO19 / SDHC_D4 | – | | C17 | GPIO27 / SDHC_D6 | – | |
| D18 | GPIO20 / SDHC_D5 | – | | C18 | GPIO28 / SDHC_D7 | – | |
| D19 | ETH_TXD1 | – | | C19 | ETH_RXD1 | – | |
| D20 | ETH_TXD0 | – | | C20 | ETH_RXD0 | – | |
| D21 | ULPI_NEXT / USB1_DM | – | | C21 | ULPI_DATA0 / USB3_DM | – | |
| D22 | ULPI_DIR / USB1_DP | – | | C22 | ULPI_DATA1 / USB3_DP | – | |
| D23 | ULPI_DATA5 / USB2_DM | – | | C23 | ULPI_DATA2 / USB4_DM | – | |
| D24 | ULPI_DATA6 / USB2_DP | – | | C24 | ULPI_DATA3 / USB4_DP | – | |
| D25 | ULPI_DATA7 | – | | C25 | ULPI_DATA4 | – | |
| D26 | GND | Ground | X | C26 | GND | Ground | |
| D27 | LCD_HSYNC / LCD_P24 | – | | C27 | AN11 | – | |
| D28 | LCD_VSYNC / LCD_P25 | – | | C28 | AN10 | – | |

Table 4. TWR-SMPS-LVFB Secondary Elevator connector pinout (continued)

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|-----------------------|--------|------|-----|-------------------|--------|------|
| D29 | AN3 | – | | C29 | AN9 | – | |
| D30 | AN12 | – | | C30 | AN8 | – | |
| D31 | GND | Ground | X | C31 | GND | Ground | X |
| D32 | LCD_CLK / LCD_P26 | – | | C32 | GPIO29 | – | |
| D33 | TMR11 | – | | C33 | TMR9 | – | |
| D34 | TMR10 | – | | C34 | TMR8 | – | |
| D35 | GPIO21 | – | | C35 | GPIO30 | – | |
| D36 | 3.3V | – | | C36 | 3.3V | – | |
| D37 | PWM15 | – | | C37 | PWM11 | – | |
| D38 | PWM14 | – | | C38 | PWM10 | – | |
| D39 | PWM13 | – | | C39 | PWM9 | – | |
| D40 | PWM12 | – | | C40 | PWM8 | – | |
| D41 | CANRX1 | – | | C41 | RXD2 / TSI0 | – | |
| D42 | CANTX1 | – | | C42 | TXD2 / TSI1 | – | |
| D43 | GPIO22 | – | | C43 | RTS2 / TSI2 | – | |
| D44 | LCD_OE / LCD_P27 | – | | C44 | CTS2 / TSI3 | – | |
| D45 | LCD_D0 / LCD_P0 | – | | C45 | RXD3 / TSI4 | – | |
| D46 | LCD_D1 / LCD_P1 | – | | C46 | TXD3 / TSI5 | – | |
| D47 | LCD_D2 / LCD_P2 | – | | C47 | RTS3 / TSI6 | – | |
| D48 | LCD_D3 / LCD_P3 | – | | C48 | CTS3 / TSI7 | – | |
| D49 | GND | Ground | | C49 | GND | Ground | |
| D50 | GPIO23 | – | | C50 | LCD_D4 / LCD_P4 | – | |
| D51 | GPIO24 | – | | C51 | LCD_D5 / LCD_P5 | – | |
| D52 | LCD_D12 / LCD_P12 | – | | C52 | LCD_D6 / LCD_P6 | – | |
| D53 | LCD_D13 / LCD_P13 | – | | C53 | LCD_D7 / LCD_P7 | – | |
| D54 | LCD_D13 / LCD_P13 | – | | C54 | LCD_D8 / LCD_P8 | – | |
| D55 | IRQ_P / SPI2_CS2_b | – | | C55 | LCD_D9 / LCD_P9 | – | |
| D56 | IRQ_O / SPI2_CS3_b | – | | C56 | LCD_D10 / LCD_P10 | – | |

Table 4. TWR-SMPS-LVFB Secondary Elevator connector pinout (continued)

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|-----------------------|--------|------|-----|--------------------------------|--------|------|
| D57 | IRQ_N | – | | C57 | LCD_D11 / LCD_P11 | – | |
| D58 | IIRQ_M | – | | C58 | TMR16 | – | |
| D59 | IRQ_L | – | | C59 | TMR15 | – | |
| D60 | IRQ_K | – | | C60 | TMR14 | – | |
| D61 | IRQ_J | – | | C61 | TMR13 | – | |
| D62 | IRQ_I | – | | C62 | LCD_D15 / LCD_P15 | – | |
| D63 | LCD_D18 / LCD_P18 | – | | C63 | LCD_D16 / LCD_P16 | – | |
| D64 | LCD_D19 / LCD_P19 | – | | C64 | LCD_D17 / LCD_P17 | – | |
| D65 | GND | Ground | | C65 | GND | Ground | X |
| D66 | EBI_AD20 / LCD_P42 | – | | C66 | EBI_BE_32_24_b / LCD_P28 | – | |
| D67 | EBI_AD21 / LCD_P43 | – | | C67 | EBI_BE_23_16_b / LCD_P29 | – | |
| D68 | EBI_AD22 / LCD_P44 | – | | C68 | EBI_BE_15_8_b / LCD_P30 | – | |
| D69 | EBI_AD23 / LCD_P45 | – | | C69 | EBI_BE_7_0_b / LCD_P31 | – | |
| D70 | EBI_AD24 / LCD_P46 | – | | C70 | EBI_TSIZE0 / LCD_P32 | – | |
| D71 | EBI_AD25 / LCD_P47 | – | | C71 | EBI_TSIZE1 / LCD_P33 | – | |
| D72 | EBI_AD26 / LCD_P48 | – | | C72 | EBI_TS_b / LCD_P34 | – | |
| D73 | EBI_AD27 / LCD_P49 | – | | C73 | EBI_TBST_b / LCD_P35 | – | |
| D74 | EBI_AD28 / LCD_P50 | – | | C74 | EBI_TA_b / LCD_P36 | – | |
| D75 | EBI_AD29 / LCD_P51 | – | | C75 | EBI_CS4_b / LCD_P37 | – | |
| D76 | EBI_AD30 / LCD_P52 | – | | C76 | EBI_CS3_b / LCD_P38 | – | |
| D77 | EBI_AD31 / LCD_P53 | – | | C77 | EBI_CS2_b / LCD_P39 | – | |
| D78 | LCD_D20 / LCD_P20 | – | | C78 | E EBI_CS1_b / LCD_P40BI_AD2 | – | |
| D79 | LCD_D21 / LCD_P21 | – | | C79 | GPIO31 / LCD_P41 | – | |

Table 4. TWR-SMPS-LVFB Secondary Elevator connector pinout (continued)

| Pin | Name | Usage | Used | Pin | Name | Usage | Used |
|-----|-------------------|--------|------|-----|-------------------|--------|------|
| D80 | LCD_D22 / LCD_P22 | – | | C80 | LCD_D23 / LCD_P23 | – | |
| D81 | GND | Ground | X | C81 | GND | Ground | X |
| D82 | 3.3V | – | | C82 | 3.3V | – | |

5 Mechanical form factor

The TWR-SMPS-LVFB board is designed for the Freescale Tower System development board platform as a side-mounting peripheral and complies with the electrical and mechanical specification as described in *Freescale Tower Electromechanical Specification*.

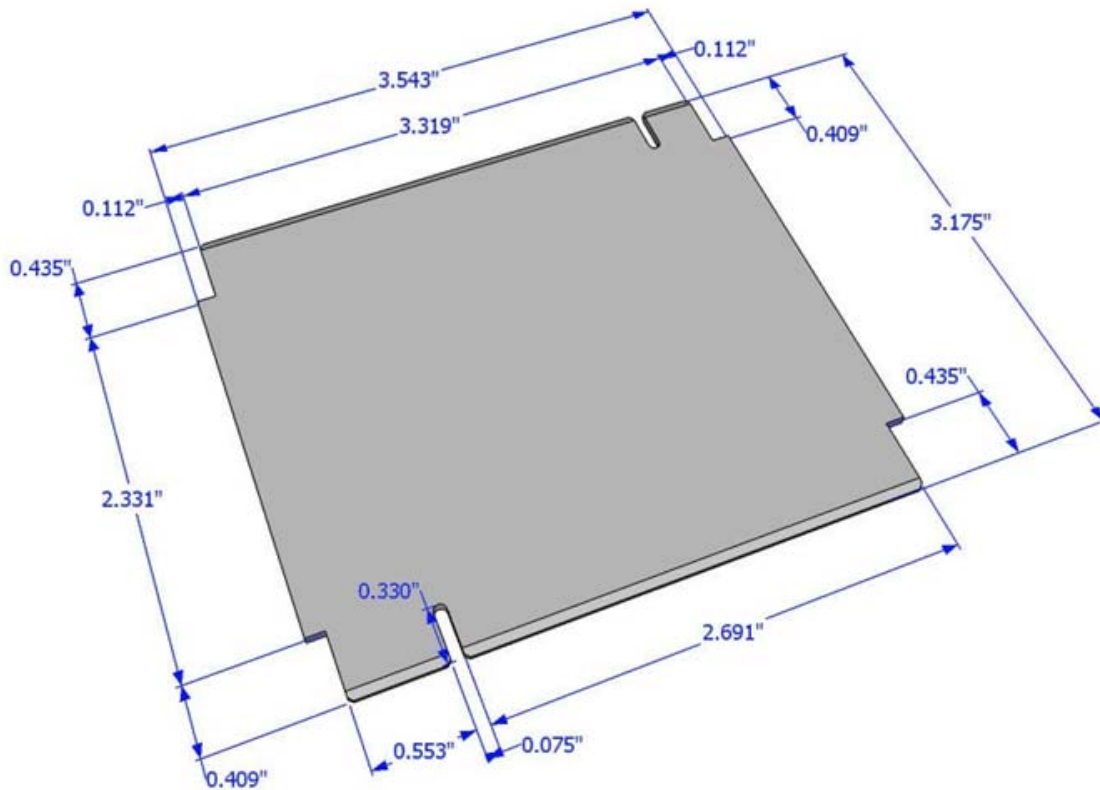


Figure 4. Board dimensions

6 Revision history

Table 5. Revision history

| Revision number | Release date | Description |
|-----------------|--------------|-----------------|
| 0 | 02/2015 | Initial release |

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