



ON Semiconductor®

# FQD4P40

## P-Channel QFET® MOSFET

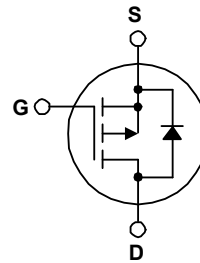
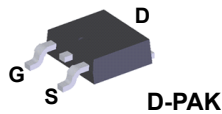
-400 V, -2.7 A, 3.1 Ω

### Description

These P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

### Features

- -2.7 A, -400 V,  $R_{DS(on)} = 3.1 \Omega$  (Max.) @  $V_{GS} = -10 V$ ,  $I_D = -1.35 A$
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 11 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted.

Symbol	Parameter	FQD4P40TM	Unit
$V_{DSS}$	Drain-Source Voltage	-400	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	-2.7	A
	Drain Current - Continuous ( $T_C = 100^\circ C$ )	-1.71	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-10.8	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	260	mJ
$I_{AR}$	Avalanche Current (Note 1)	-2.7	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ C$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ C$ )	50	W
	- Derate above $25^\circ C$	0.4	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ C$

### Thermal Characteristics

Symbol	Parameter	FQD4P40TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.5	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD4P40TM	FQD4P40	DPAK	Tape and Reel	330 mm	16 mm	2500 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.36	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -320\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.35\text{ A}$	--	2.44	3.1	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.35\text{ A}$	--	2.5	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	520	680	pF
$C_{oss}$	Output Capacitance		--	80	105	pF
$C_{rss}$	Reverse Transfer Capacitance		--	11	15	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -200\text{ V}, I_D = -3.5\text{ A},$ $R_G = 25\ \Omega$	--	13	35	ns	
$t_r$	Turn-On Rise Time		--	55	120	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	35	80	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	37	85	ns
$Q_g$	Total Gate Charge	$V_{DS} = -320\text{ V}, I_D = -3.5\text{ A},$ $V_{GS} = -10\text{ V}$	--	18	23	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	3.8	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	9.4	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-2.7	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-10.8	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.7\text{ A}$	--	--	-5.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -3.5\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	260	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	1.4	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 62\text{ mH}, I_{AS} = -2.7\text{ A}, V_{DD} = -50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -3.5\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

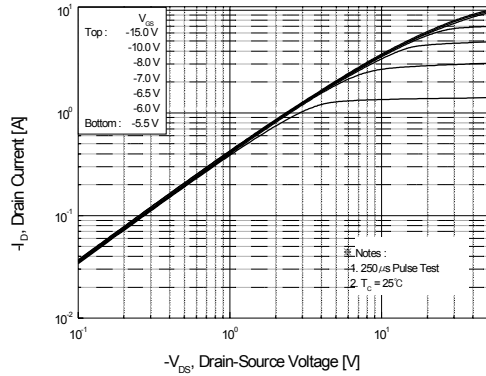


Figure 1. On-Region Characteristics

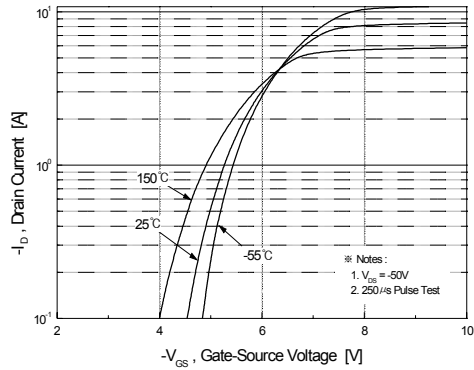


Figure 2. Transfer Characteristics

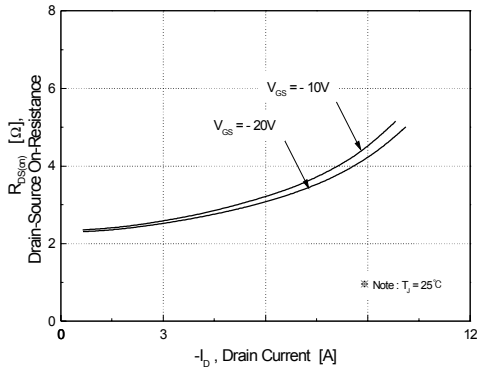


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

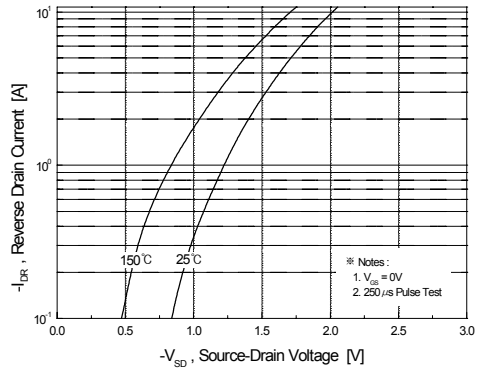


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

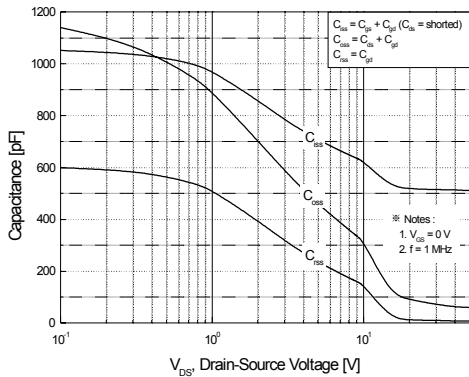


Figure 5. Capacitance Characteristics

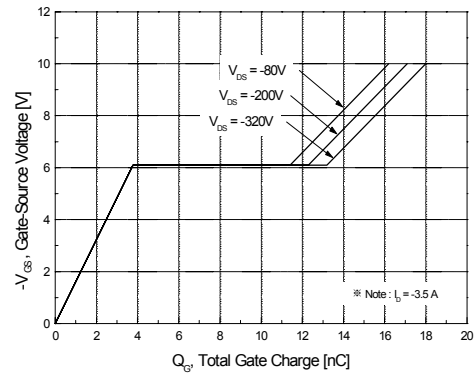
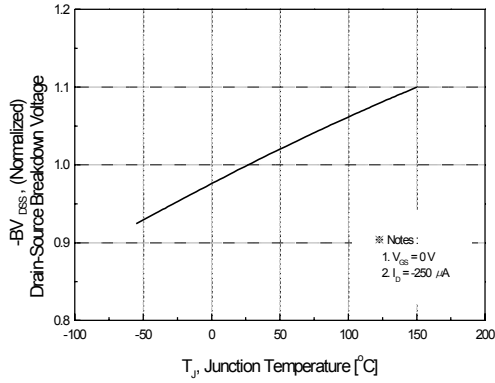
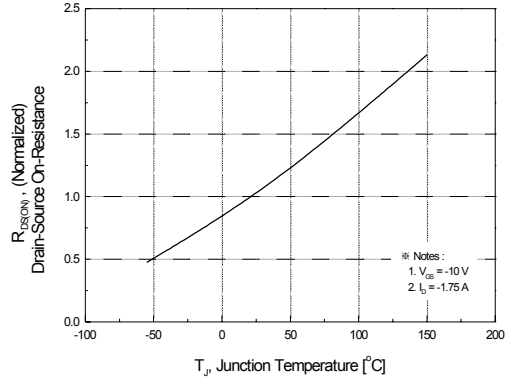


Figure 6. Gate Charge Characteristics

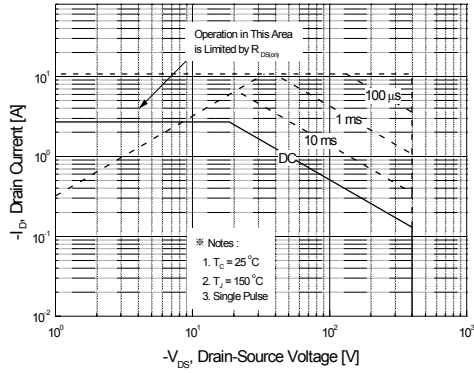
**Typical Characteristics** (Continued)



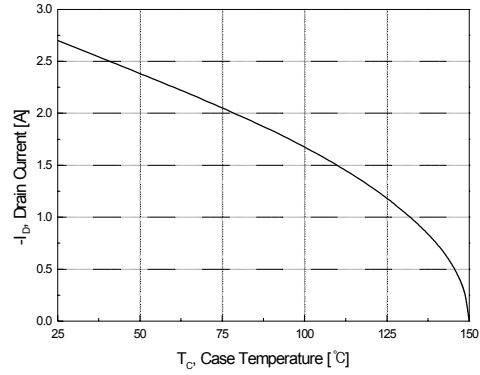
**Figure 7. Breakdown Voltage Variation vs. Temperature**



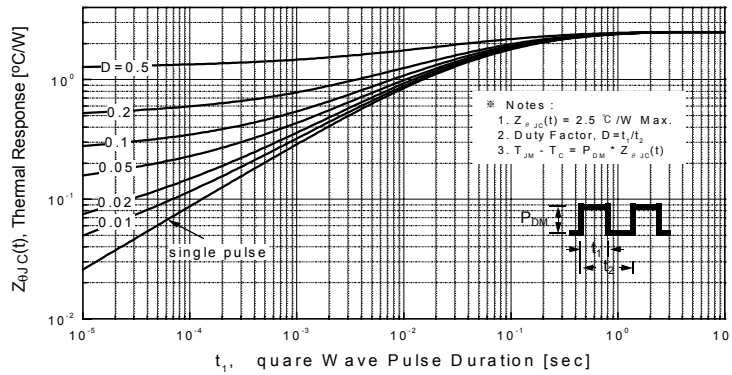
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

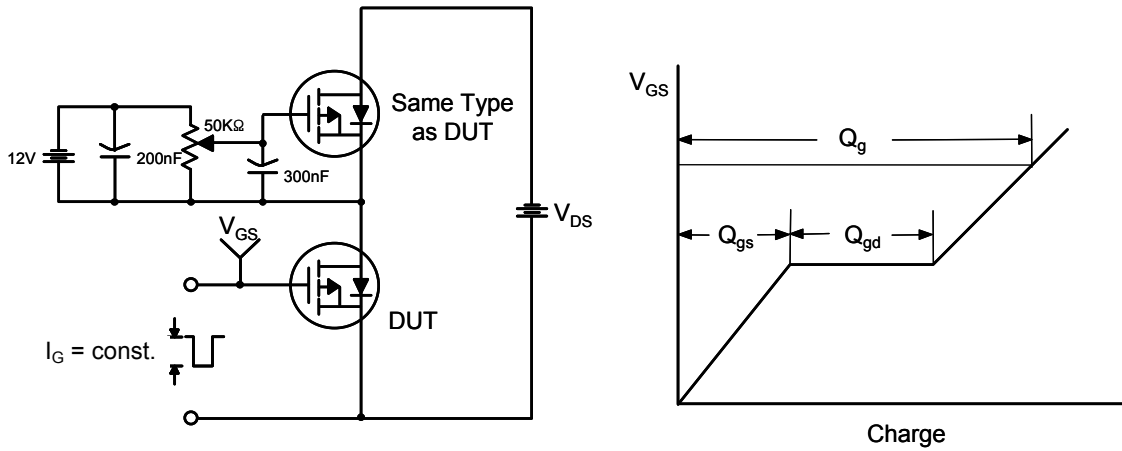


Figure 12. Gate Charge Test Circuit & Waveform

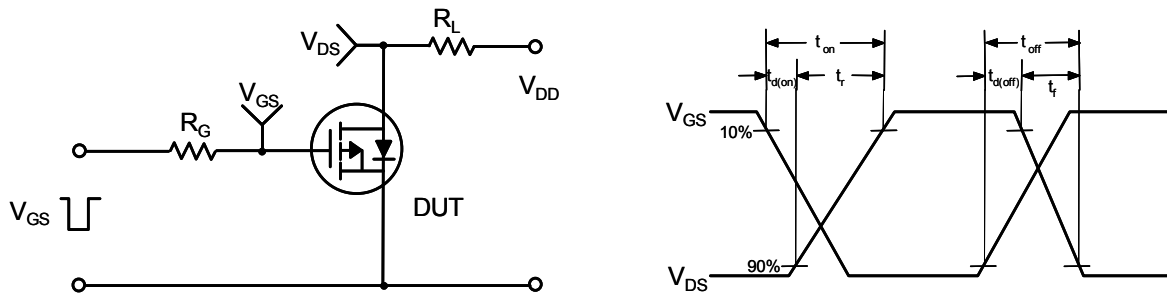


Figure 13. Resistive Switching Test Circuit & Waveforms

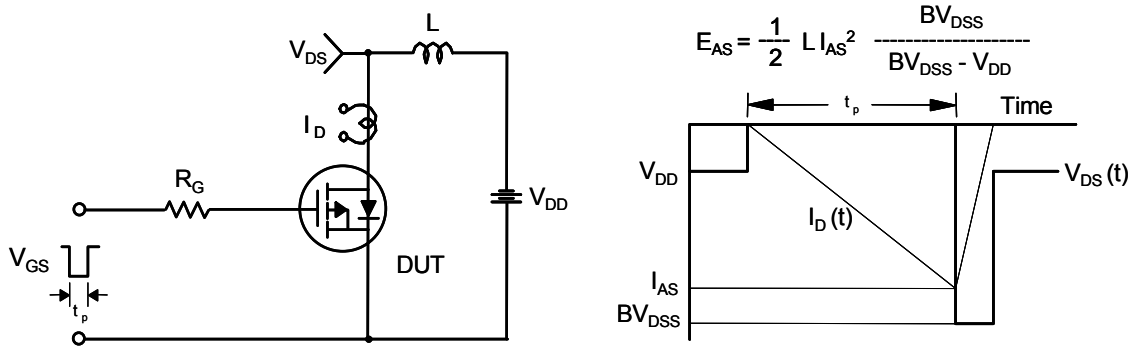


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

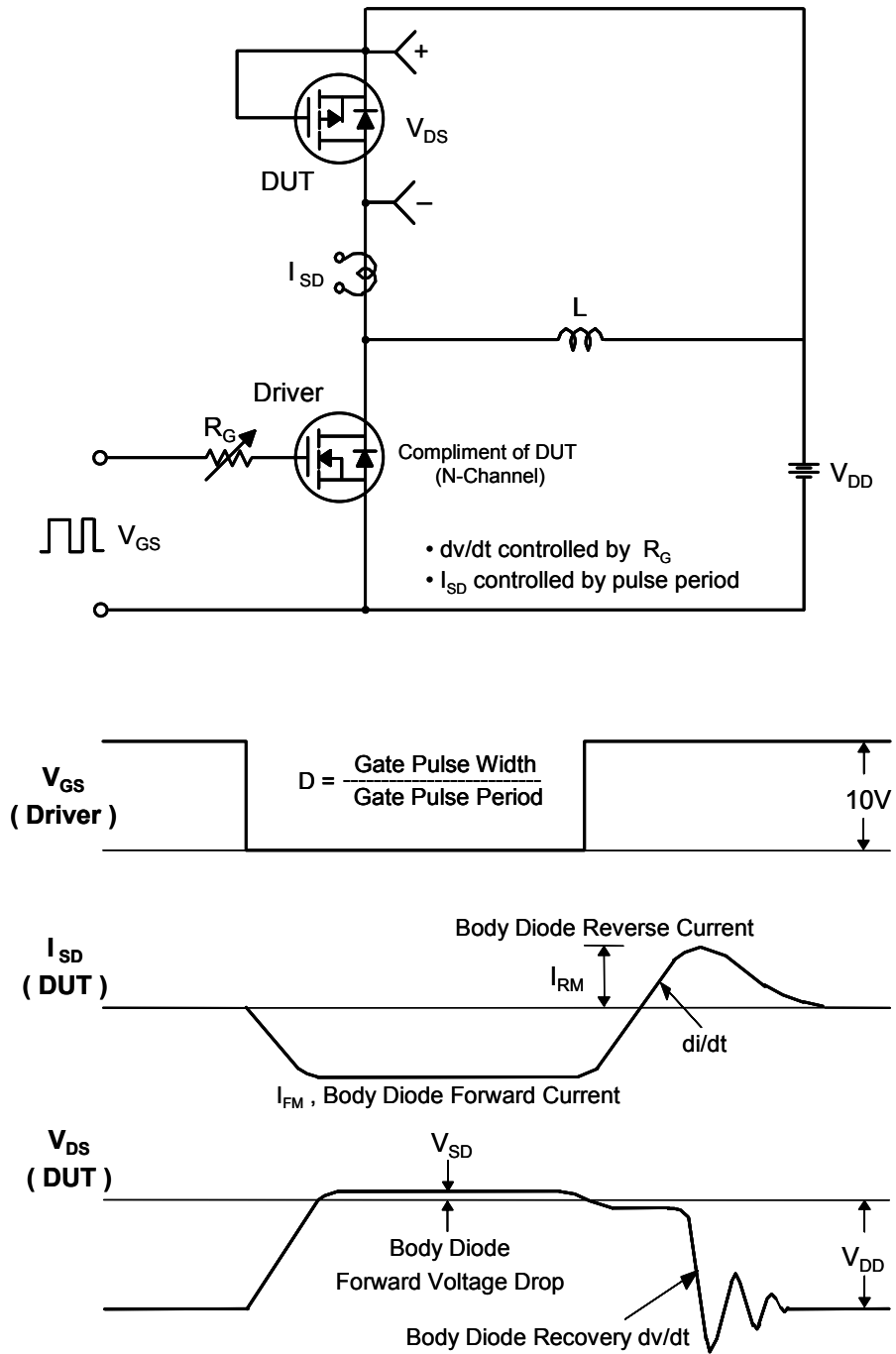
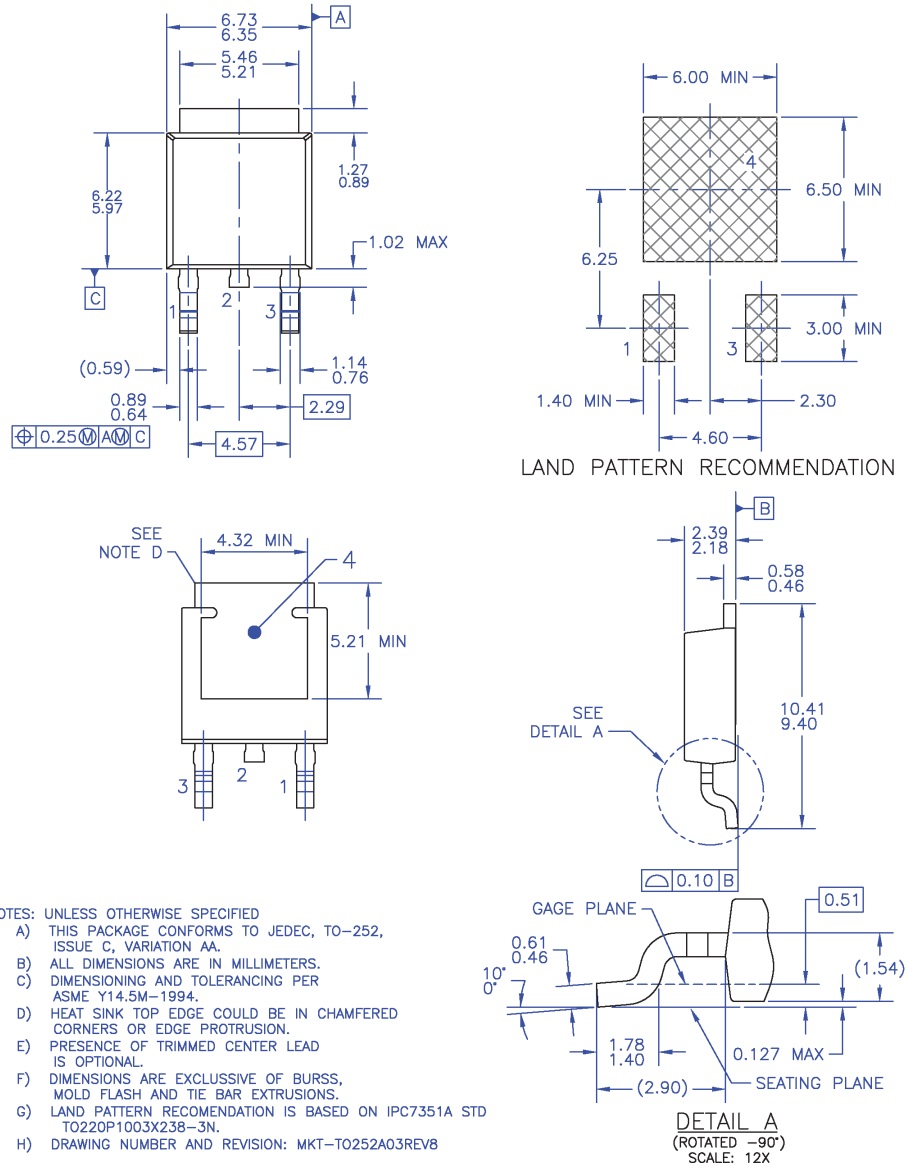



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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